A Series Diode Method of Suppressing Parasitic Oscillation for Boost PFC Converter Operated in Discontinuous Conduction Mode

Qiang Li, Kai Yao, *Member, IEEE*, Junchao Song, Hairui Xu, and Yehua Han

***Abstract*—When a boost power factor correction converter operates in a discontinuous conduction mode, the nonzero characteristic of the average current in oscillation period and the initial value of the inductor current in a switching cycle are the main cause of the influence of the parasitic parameters on input current distortion. The effect of parasitic parameters oscillation is analyzed in detail, and a new method of series diode is proposed, which can effectively decrease the input current distortion and improve the power factor. Selection principles of series diode are given. Experimental results verify the correctness and the feasibility of the theoretical analysis.**

***Index Terms*—Discontinuous conduction mode (DCM), parasitic oscillation suppression, power factor correction (PFC), series diode(SD).**

I. Introduction

POWER FACTOR CORRECTION (PFC) converters have been widely used in power electronic devices because of its significant improvement in input current distortion and input power factor [1]–[15]. Among many topologies, boost circuit has the advantages of small input current ripple, high output voltage, simple structure, and high reliability, which is commonly used in PFC circuits.

The inductor current of the DCM boost PFC converter fully operates in the discontinuous conduction mode [16]–[22]. Furthermore, the inductor current of a boost PFC converter designed for continuous conduction mode (CCM) will operate fully in DCM when the load lightens to a certain degree. At the same time, the input current distortion is serious, and the stability of the system becomes poor [23]–[31].

The causes of this distortion lies in the poor tracking effect of CCM control algorithm operating on DCM, and the serious parasitic oscillation of the boost circuit [23]. In order to solve the influence caused by this inappropriate control algorithm, many improved control strategies have been proposed [24]–[31], which achieve better control effect. However, due to the effect of the parasitic parameters on the distortion, the amount of the harmonic contents in the input current is still high. In order to analyze the influence of the parasitic oscillation on the input current harmonic, it is necessary to model the oscillation process of the converter. The common method is based on the average current model of the inductor [32]–[34], which is unable to get a precise circuit parameters effect on the input current total harmonic distortion(THD). Therefore, in [35], the equivalent model of the converter is established considering the parasitic parameters, and the influence of the parasitic parameters on the input current distortion is analyzed in detail. In [36] and [37], a detailed investigation into the impact of sneak circuits on the performance of the DCM boost converter is achieved, and the design guidelines for eliminating the sneak circuit phenomena are presented. For suppressing the parasitic oscillation, the RC and RCD snubbers have been proposed, while the loss increases as well [23]. In order to reduce the input current harmonics and lower the effect on the efficiency of the converter at light load, the improved control algorithm of an adaptive switching and frequency is provided in [38] and [39]. In [40] and [41], a valley switching method is analyzed and employed to minimize the switching loss and reduce the input current distortion.

The objective of this paper is to clearly show the oscillation process of a boost PFC converter operated in DCM and then propose a method of suppressing the oscillation so as to improve the THD of the input current. The content of this paper is organized as follows. In Section II, the effect of the parasitic oscillation on the input current distortion is analyzed in detail. A series diode (SD) method to reduce the initial value of the inductor current in each switching cycle and the average value of the inductor current in oscillation period is proposed in Section III. The experimental verification is carried out and the results are presented in Section IV. The conclusion is given in Section V.

II. Influence of Parasitic Parameters on the Input Current Distortion

A boost PFC circuit with the parasitic parameters considered is shown in Fig. 1. The MOSFET is equivalent to an ideal one in parallel with a capacitor $C_{\rm oss}$ and a diode $D_{\rm ds}$. The freewheeling diode is considered as an ideal one with a junction capacitance

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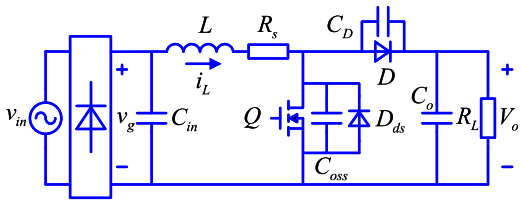


Fig. 1. Boost PFC circuit with the parasitic parameters considered.

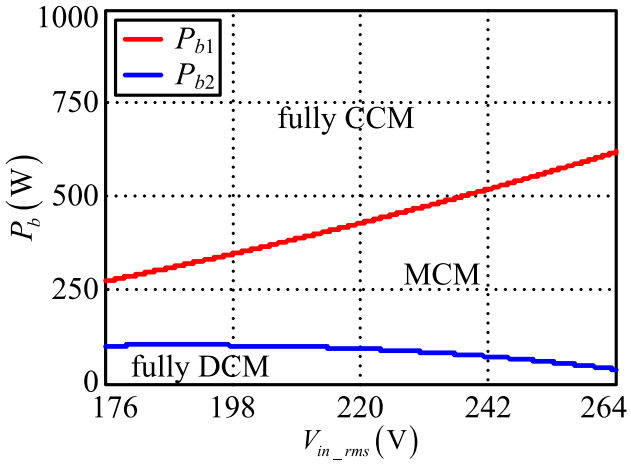


Fig. 2. Curves of the critical load power.

C_D in parallel. The boost inductor L is regarded as an ideal one in series with an equivalent resistance R_s.

In order to facilitate the analysis of the effect of parasitic oscillation on the input current, the hypotheses are made as follows: 1) The switching frequency f_s is far greater than the input voltage frequency f_l and the input voltage is considered constant in a switching cycle; 2) The output voltage ripple is much lower than its dc component V_o.

The input voltage is defined as

$$v_{in}(n) = V_m \sin(\omega n T_s) \tag{1}$$

where V_m and ω are the amplitude and angular frequency of the input voltage, respectively. T_s is the switching cycle, n is the number of T_s, and $1 \le n \le f_s/f_l$.

Then, the rectified input voltage is

$$v_g(n) = V_m \left|\sin(\omega n T_s)\right|. \tag{2}$$

When a CCM boost PFC converter operates at light loads, the critical load power for completely CCM and fully DCM operation is expressed in P_{b1} and P_{b2}, respectively, as follows [26] and [42]:

$$P_{b1} = \frac{V_m^2}{4Lf_s} \tag{3a}$$

$$P_{b2} = \frac{V_m^2 (V_o - V_m)}{4Lf_s V_o}. \tag{3b}$$

Combining with the circuit parameters given in Section IV, Fig. 2 can be plotted from (3a) and (3b), which shows the critical load power corresponding to a certain input voltage, where $V_{\text{in\_rms}}$ is the root mean square (RMS) value of the input voltage. Mixed conduction mode (MCM) means that the converter will operate in CCM around $\pi/2$, and DCM around 0 and π, respectively, during half of an input line cycle.

For DCM operation, when the current drops to zero, the inductor will oscillate with the equivalent parasitic capacitance. At this time, the inductor current i_L does not remain at zero, and the drain source voltage v_{ds} of the switch will not be the output voltage any longer, which presents a nonlinear variation. As the capacitance of C_{in} and C_o is much larger than those of the parasitic capacitor, they can be regarded as a constant voltage source whose influence on the oscillation is ignored. The equivalent boost circuit in the oscillation period is shown in Fig. 3(a). The waveforms of i_L and v_{ds} in a switching cycle are shown in Fig. 4(a).

The KVL and KCL equations for the circuit in Fig. 3(a) are

$$\begin{cases} v_L(t) + R_s i_L(t) + v_{C_D}(t) = v_g(n) - V_o \\ v_{C_{\text{oss}}}(t) - v_{C_D}(t) = V_o \\ i_L(t) = i_{C_D}(t) + i_{C_{\text{oss}}}(t) \end{cases} \tag{4}$$

where

$$\begin{cases} v_L(t) = L\dfrac{di_L(t)}{dt} \\ i_{C_{oss}}(t) = C_{oss}\dfrac{dv_{C_{oss}}(t)}{dt} \\ i_{C_D}(t) = C_D\dfrac{dv_{C_D}(t)}{dt} \\ v_{C_{oss}}(t) = v_{ds}(t). \end{cases} \tag{5}$$

Based on (4) and (5), the differential equation of the inductor current can be obtained as

$$(C_{\text{oss}} + C_D) L \cdot \frac{d}{dt}\left(\frac{di_L(t)}{dt}\right) + (C_{\text{oss}} + C_D) R_s \cdot \frac{di_L(t)}{dt} + i_L(t) = 0. \tag{6}$$

Therefore, the expression of general solution for (6) is

$$i_L(t) = \left\{ \begin{array}{l} k_1 \sin\omega_d [t - (n-1)T_s - T_{\text{on}} - T_{\text{off}}] \\ +k_2 \cos\omega_d [t - (n-1)T_s - T_{\text{on}} - T_{\text{off}}] \end{array} \right\} \times e^{-\frac{R_s}{2L}[t-(n-1)T_s - T_{\text{on}} - T_{\text{off}}]} \tag{7}$$

$$\omega_d = \sqrt{\frac{1}{L(C_{\text{oss}} + C_D)} - \left(\frac{R_s}{2L}\right)^2} = \sqrt{\frac{1}{LC_{\text{eq}}} - \left(\frac{R_s}{2L}\right)^2} \tag{8}$$

where k_1 and k_2 are the coefficients, which will be calculated afterward according to the initial conditions, ω_d is the oscillation angle frequency, C_{eq} is the equivalent parasitic capacitance and $C_{\text{eq}} = C_{\text{oss}} + C_D$.

Two initial conditions can be derived by

$$\begin{cases} i_L\big|_{t=(n-1)T_s + T_{\text{on}} + T_{\text{off}}} = 0 \\ v_L\big|_{t=(n-1)T_s + T_{\text{on}} + T_{\text{off}}} = v_g - V_o. \end{cases} \tag{9}$$

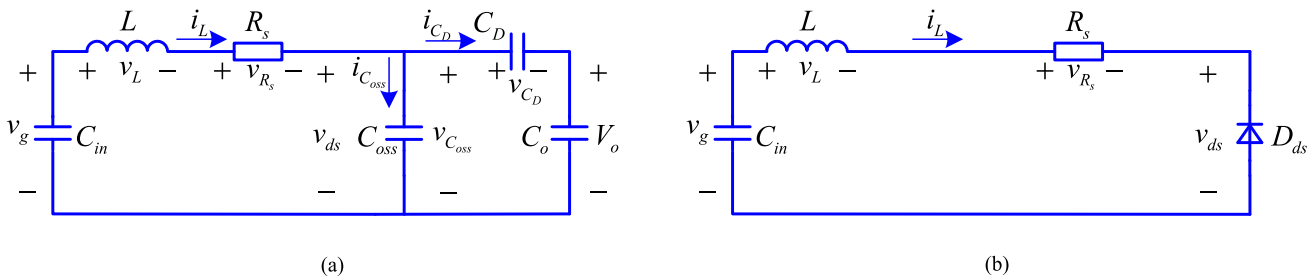


Fig. 3. Equivalent circuits in the oscillation period.

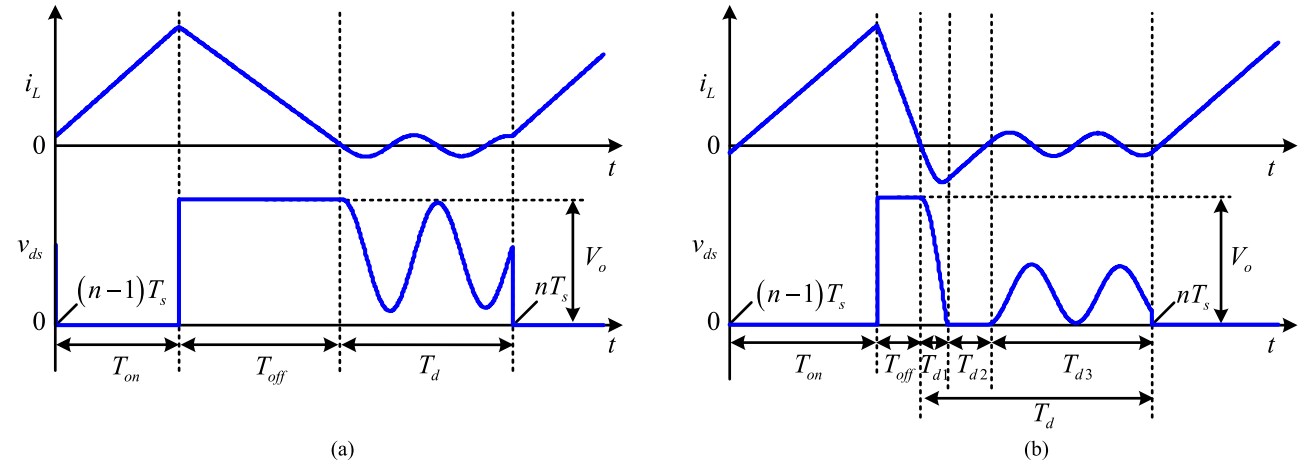


Fig. 4. Waveforms of i_L and v_{ds}. (a) $v_g(n) \geq V_b$. (b) $v_g(n) < V_b$.

Therefore, the undetermined coefficients can be obtained as

$$\begin{cases} k_1 = \dfrac{v_g(n) - V_o}{L\omega_d} \\ k_2 = 0. \end{cases} \tag{10}$$

From (7) and (10), the expression for the inductor current in the oscillation period is

$$i_{L\_T_d}(t) = \frac{v_g(n) - V_o}{L\omega_d} e^{-\frac{R_s}{2L}[t-(n-1)T_s - T_{\rm on} - T_{\rm off}]} \times \sin\left[\omega_d\left(t - (n-1)T_s - T_{\rm on} - T_{\rm off}\right)\right] \tag{11}$$

where $(n-1)T_s + T_{\rm on} + T_{\rm off} \leq t \leq nT_s$.

Substituting (11) into (4) and (5), $v_{\rm ds}$ can be calculated as

$$\begin{aligned} v_{ds\_T_d}(t) &= v_g(n) - L\frac{di_L(t)}{dt} - R_s i_L(t) \\ &= v_g(n) + [V_o - v_g(n)]\, e^{-\frac{R_s}{2L}[t-(n-1)T_s - T_{\rm on} - T_{\rm off}]} \\ &\quad \times \left\{ \begin{array}{l} \cos\left[\omega_d\left(t - (n-1)T_s - T_{\rm on} - T_{\rm off}\right)\right] \\ + \dfrac{R_s}{2L\omega_d} \sin\left[\omega_d\left(t - (n-1)T_s - T_{\rm on} - T_{\rm off}\right)\right] \end{array} \right\} \end{aligned} \tag{12}$$

where $(n-1)T_s + T_{\rm on} + T_{\rm off} \leq t \leq nT_s$.

Due to effect of the parasitic antiparallel diode on the switch, $v_{\rm ds}$ will be clamped to zero by the diode $D_{\rm ds}$ while it oscillates to zero. Depending on whether $v_{\rm ds}$ can oscillate to zero or not, there are two situations about the inductor current and the drain source voltage. The cut-off point is the corresponding instantaneous input voltage which enables the minimum value of $v_{\rm ds}$ to be just zero.

According to (12) and Fig. 4(a), the minimum value $v_{\rm ds}$ can be obtained while $\omega_d[t - (n-1)T_s - T_{\rm on} - T_{\rm off}] = \pi$,

$$v_{\rm ds\_min}(t) = v_g(n) - [V_o - v_g(n)]\, e^{-\frac{R_s \pi}{2L\omega_d}}. \tag{13}$$

Letting $v_{\rm ds_{min}}(t) = 0$, the demarcation point of the input voltage V_b can be solved as

$$V_b = \frac{V_o e^{-\frac{R_s \pi}{2L\omega_d}}}{1 + e^{-\frac{R_s \pi}{2L\omega_d}}}. \tag{14}$$

Formula (14) indicates that V_b is related to $R_s/2L\omega_d$, the greater $R_s/2L\omega_d$ is, the smaller V_b will be, and the greater error between V_b with $R_s = 0$ and that with $R_s > 0$ will be. When $R_s = 0$, the maximum value of V_b equals to $V_o/2$. Generally, in [35], [40], and [42], V_b is considered as $V_o/2$ approximately, due to the reason that the existence of R_s is ignored in the equivalent circuit. Therefore, (14) presents a more accurate expression of V_b.

Fig. 4(a) presents the situation of $v_g(n) \geq V_b$. When $v_g(n) < V_b$, the waveforms of i_L and v_{ds} in a switching period are shown in Fig. 4(b), and the oscillation current can be divided into three stages.

During the first stage T_{d1}, the inductor and the equivalent parasitic capacitor oscillate until $v_{\rm ds}$ drops to zero, and the oscillation process is the same as Fig. 3(a). The expressions of i_{L_Td1}

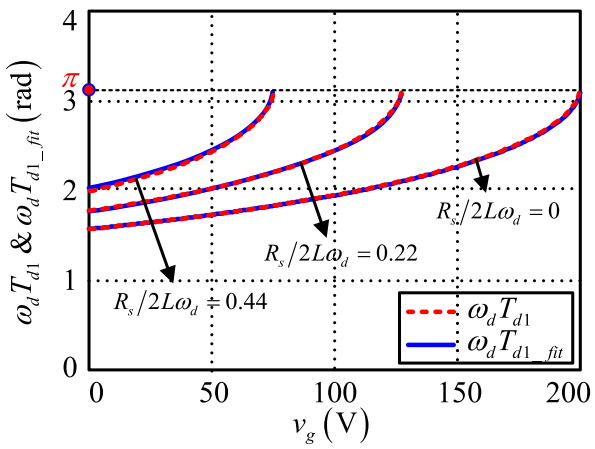


Fig. 5. Values of $\omega_d T_{d1}$ and $\omega_d T_{d1\_\mathrm{fit}}$.

and v_{ds_Td1} are the same as (11) and (12) respectively, where $(n-1)T_s + T_{\mathrm{on}} + T_{\mathrm{off}} \le t \le (n-1)T_s + T_{\mathrm{on}} + T_{\mathrm{off}} + T_{d1}$.

T_{d1} is the solution of the transcendental equation $v_{\mathrm{ds}\_Td1}(t) = 0$, and because of the complexity, it should be noted that there is no analytical expression. Hereafter, the following method is proposed.

For the ideal situation of $R_s = 0$, the solution of $v_{\mathrm{ds}\_Td1}(t) = 0$ is

$$\omega_d T_{d1}\,|_{R_s=0\,\Omega} = \mathrm{acos}\left(\frac{v_g(n)}{v_g(n)-V_o}\right). \tag{15}$$

When R_s>0, the solution of $\omega_d T_{d1}$ with the variation of $R_s/2L\omega_d$ can be drawn by adopting the software of MathCAD, which is shown in Fig. 5 with the red dash line. The ranges of R_s, C_{eq} and L are defined as 0–100 Ω, 0–1000 pF, and 15 μH–3 mH, respectively, so as to be compliant with the vast majority of boost PFC converters. Therefore, the variation range of $R_s/2L\omega_d$ is 0–0.44.

From Fig. 5, it can be seen that $\omega_d T_{d1}$ is related to the values of both $v_g(n)$ and $R_s/2L\omega_d$. For a certain $R_s/2L\omega_d$, the minimum value of $\omega_d T_{d1}$ occurs at $v_g(n) = 0$, which is increasing with $R_s/2L\omega_d$. On the other hand, for different values of $R_s/2L\omega_d$, $\omega_d T_{d1}$ is always able to reach to the same maximum value at $v_g(n) = V_b$. Therefore, the fitted solution of $\omega_d T_{d1}$ may be found out based on the three conditions: 1) The equation of $\omega_d T_{d1\_\mathrm{fit}}$ is the same as (15) while $R_s = 0$. 2) While $v_g(n) = 0$, the value of $\omega_d T_{d1\_\mathrm{fit}}$ increases with the value of $R_s/2L\omega_d$. 3) $\omega_d T_{d1\_fit} = \pi$ while $v_g(n) = V_b$.

Let us change the form of (15) and rewritten it as

$$\omega_d T_{d1}|_{R_s=0\,\Omega} = \mathrm{acos}\left(\frac{v_g(n)+\frac{V_o}{2}-\frac{V_o}{2}}{v_g(n)-\frac{V_o}{2}-\frac{V_o}{2}}\right). \tag{16}$$

It should be noted that the cause of the error between the values of $\omega_d T_{d1}$ shown in Fig. 5 and that expressed in (15) is that $R_s = 0$ is presupposed and (14) is approximately regarded as $V_o/2$. Therefore, replacing "$V_o/2$" in (16) with (14) may be the way out for eliminating the error. Taking the aforementioned three conditions into consideration, the only possible form of replacement is

$$\begin{aligned}\omega_d T_{d1\_\mathrm{fit}} &= \mathrm{acos}\left(\frac{v_g(n)+\frac{V_o}{2}-V_b}{v_g(n)-\frac{V_o}{2}-V_b}\right)\\ &= \mathrm{acos}\left(\frac{v_g(n)+\frac{V_o}{2}-\frac{V_o e^{-\frac{R_s\pi}{2L\omega_d}}}{1+e^{-\frac{R_s\pi}{2L\omega_d}}}}{v_g(n)-\frac{V_o}{2}-\frac{V_o e^{-\frac{R_s\pi}{2L\omega_d}}}{1+e^{-\frac{R_s\pi}{2L\omega_d}}}}\right).\end{aligned} \tag{17}$$

In order to validate the accuracy of the fitted value, (17) is also plotted in Fig. 5 with the blue full line. Obviously, the fitting values of $\omega_d T_{d1\_\mathrm{fit}}$ agree well with those of the actual solution.

In the second stage T_{d2}, the body diode of the switch conducts. The initial value of v_{ds} is zero. The inductor current flows in the opposite direction and decreases until it reaches zero. Fig. 3(b) shows the equivalent oscillation circuit, and the KVL equation is

$$v_L(t) + R_s i_L(t) = v_g(n). \tag{18}$$

Substituting (17) into (11) and (12), two initial conditions can be derived as

$$\begin{cases} i_L\Big|_{t=(n-1)T_s+T_{\mathrm{on}}+T_{\mathrm{off}}+T_{d1}} \\ = \dfrac{v_g(n)-V_o}{L\omega_d} e^{-\frac{R_s}{2L}T_{d1\_\mathrm{fit}}} \sin\omega_d T_{d1\_\mathrm{fit}} \\ v_L\Big|_{t=(n-1)T_s+T_{\mathrm{on}}+T_{\mathrm{off}}+T_{d1}} \\ = \left\{\begin{array}{l} v_g(n) + [V_o - v_g(n)]\, e^{-\frac{R_s}{2L}T_{d1\_\mathrm{fit}}} \\ \times\left(\cos\omega_d T_{d1\_\mathrm{fit}} + \dfrac{R_s}{2L\omega_d}\sin\omega_d T_{d1\_\mathrm{fit}}\right) \end{array}\right\}. \end{cases} \tag{19}$$

Based on (5), (18), and (19), the inductor current i_{L_Td2} and the drain source voltage v_{ds_Td2} can be derived as (20) and (21).The solving process is the same as that of (4)–(12)

$$\begin{aligned} i_{L\_T_{d2}}(t) = {} & \frac{v_g(n)}{R_s} - e^{-\frac{R_s}{L}[t-(n-1)T_s-T_{\mathrm{on}}-T_{\mathrm{off}}-T_{d1}]} \\ & \times\left[\frac{v_g(n)}{R_s} + \frac{V_o - v_g(n)}{L\omega_d} e^{-\frac{R_s}{2L}T_{d1}} \sin\omega_d T_{d1}\right] \end{aligned} \tag{20}$$

$$v_{ds\_T_{d2}}(t) = 0 \tag{21}$$

where $(n-1)T_s + T_{\mathrm{on}} + T_{\mathrm{off}} + T_{d1} \le t \le (n-1)T_s + T_{\mathrm{on}} + T_{\mathrm{off}} + T_{d1} + T_{d2}$. T_{d2} is the solution of $i_{L\_Td2}(t) = 0$, and

$$T_{d2} = -\frac{L}{R_s}\ln\frac{v_g(n)}{v_g(n) + R_s\frac{V_o - v_g(n)}{L\omega_d} e^{-\frac{R_s}{2L}T_{d1}} \sin(\omega_d T_{d1})}. \tag{22}$$

In the third stage T_{d3}, the inductor oscillates with the parasitic capacitance once again until the time when the switch turns ON. The equivalent oscillation circuit is the same as Fig. 3(a) and the solving process is the same as (4)–(12). Similarly, the

expressions of i_{L_Td3} and v_{ds_Td3} are

$$i_{L\_Td3}(t) = \frac{v_g(n)}{L\omega_d} e^{-\frac{R_s}{2L}[t-(n-1)T_s-T_{\rm on}-T_{\rm off}-T_{d1}-T_{d2}]} \times \sin\left[\omega_d\left(t-(n-1)T_s-T_{\rm on}-T_{\rm off}-T_{d1}-T_{d2}\right)\right] \tag{23}$$

$$v_{DS\_Td3}(t) = v_g(n) - v_g(n) e^{-\frac{R_s}{2L}[t-(n-1)T_s-T_{\rm on}-T_{\rm off}-T_{d1}-T_{d2}]} \times \left\{ \begin{array}{l} \cos\left[\omega_d \begin{pmatrix} t-(n-1)T_s-T_{\rm on} \\ -T_{\rm off}-T_{d1}-T_{d2} \end{pmatrix}\right] \\ +\dfrac{R_s}{2L\omega_d}\sin\left[\omega_d \begin{pmatrix} t-(n-1)T_s-T_{\rm on} \\ -T_{\rm off}-T_{d1}-T_{d2} \end{pmatrix}\right] \end{array} \right\} \tag{24}$$

where $(n-1)T_s + T_{\rm on} + T_{\rm off} + T_{d1} + T_{d2} \le t \le nT_s$.

For DCM operation, when the switch turns ON, the inductor current increases linearly

$$i_{L\_T_{\rm on}}(t) = \frac{v_g(n)}{L}\left[t-(n-1)T_s\right] + i_{L\_\rm initial}(nT_s) \tag{25}$$

where $(n-1)T_s \le t \le (n-1)T_s + T_{\rm on}$, $i_{L\_\rm initial}(nT_s)$ is the initial value of the inductor current at the *n*th number of switching cycle, which can be calculated as

$$i_{L\_\rm initial}(nT_s) = \left\{ \begin{array}{l} \dfrac{v_g(n-1)-V_o}{L\omega_d} e^{-\frac{R_s}{2L}T_d}\sin\omega_d T_d, v_g(n-1) \ge V_b \\ \dfrac{v_g(n-1)-V_o}{L\omega_d} e^{-\dfrac{R_s}{2L}T_d}\sin\omega_d T_d,\ v_g(n-1) < V_b \& T_d \le T_{d1} \\ \dfrac{v_g(n-1)}{R_s} - e^{-\dfrac{R_s}{L}(T_d-T_{d1})} \\ \times\left[\dfrac{v_g(n-1)}{R_s} + \dfrac{V_o-v_g(n-1)}{L\omega_d} e^{-\dfrac{R_s}{2L}T_{d1}}\sin\omega_d T_{d1}\right], \\ v_g(n-1) < V_b \&; T_{d1} < T_d \le T_{d1}+T_{d2} \\ \dfrac{v_g(n-1)}{L\omega_d} e^{-\dfrac{R_s}{2L}(T_d-T_{d1}-T_{d2})}\sin\omega_d\left(T_d-T_{d1}-T_{d2}\right), \\ v_g(n-1) < V_b \&; T_d > T_{d1}+T_{d2}. \end{array} \right. \tag{26}$$

When the switch turns OFF, the inductor current decreases linearly

$$i_{L\_T_{\rm off}}(t) = i_{L\_T_{\rm on}}\left((n-1)T_s + T_{\rm on}\right) - \frac{V_o - v_g(n)}{L}\left[t-(n-1)T_s-T_{\rm on}\right] \tag{27}$$

where $(n-1)T_s + T_{\rm on} \le t \le (n-1)T_s + T_{\rm on} + T_{\rm off}$, and

$$T_{\rm off} = \frac{L}{V_o - v_g(n)} i_{L\_T_{\rm on}}\left((n-1)T_s + T_{\rm on}\right). \tag{28}$$

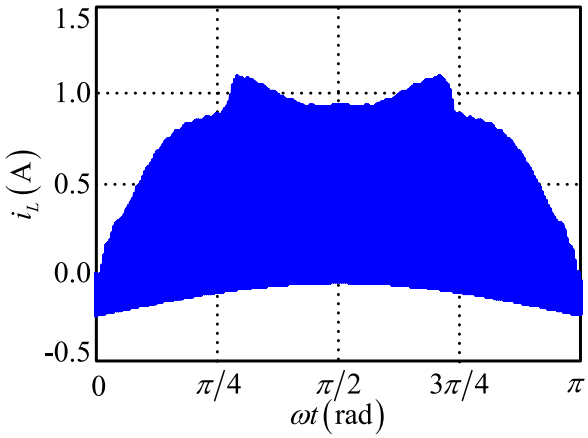


Fig. 6. Theoretical waveform of inductor current.

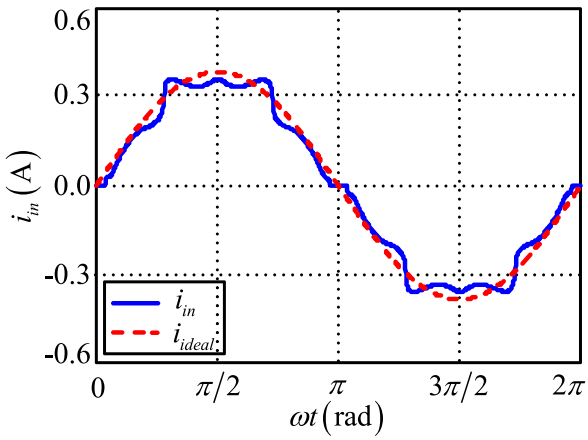


Fig. 7. Theoretical waveforms of input current.

Therefore, the average current in a switching cycle can be expressed as

$$i_{in}(t) = \left\{ \begin{array}{l} \dfrac{1}{T_s}\left[\begin{array}{l} \int_{(n-1)T_s}^{(n-1)T_s+T_{\rm on}} i_{L\_T_{\rm on}}(t)dt \\ +\int_{(n-1)T_s+T_{\rm on}}^{(n-1)T_s+T_{\rm on}+T_{\rm off}} i_{L\_T_{\rm off}}(t)dt \\ +\int_{(n-1)T_s+T_{\rm on}+T_{\rm off}}^{nT_s} i_{L\_T_d}(t)dt \end{array}\right], v_g(n) \ge V_b \\ \dfrac{1}{T_s}\left[\begin{array}{l} \int_{(n-1)T_s}^{(n-1)T_s+T_{\rm on}} i_{L\_T_{\rm on}}(t)dt \\ +\int_{(n-1)T_s+T_{\rm on}}^{(n-1)T_s+T_{\rm on}+T_{\rm off}} i_{L\_T_{\rm off}}(t)dt \\ +\int_{(n-1)T_s+T_{\rm on}+T_{\rm off}}^{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}} i_{L\_T_{d1}}(t)dt \\ +\int_{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}}^{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}+T_{d2}} i_{L\_T_{d2}}(t)dt \\ +\int_{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}+T_{d2}}^{nT_s} i_{L\_T_{d3}}(t)dt \end{array}\right], v_g(n) < V_b. \end{array} \right. \tag{29}$$

Based on the above analysis, the theoretical waveforms of the inductor current and input current in a half line cycle can be drawn in Figs. 6 and 7, where $i_{\rm ideal}$ is the ideal input current.

It can be seen that the input current is distorted seriously due to the oscillation.

Fig. 4 demonstrates that if the average value in oscillation period and the initial value in a switching cycle of the inductor current are equal to zero, the inductor current will not be disturbed, so the distortion of input current can be eliminated. The average current in the oscillation period can be calculated as

$$i_{L\_T_d\_ave}(t) = \begin{cases} \dfrac{1}{T_s}\int_{(n-1)T_s+T_{\rm on}+T_{\rm off}}^{nT_s} i_{L\_T_d}(t)dt, v_g(n) \geq V_b \\ \dfrac{1}{T_s}\begin{bmatrix} \int_{(n-1)T_s+T_{\rm on}+T_{\rm off}}^{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}} i_{L\_T_{d1}}(t)dt \\ +\int_{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}}^{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}+T_{d2}} i_{L\_T_{d2}}(t)dt \\ +\int_{nT_s+T_{\rm on}+T_{\rm off}+T_{d1}+T_{d2}}^{nT_s} i_{L\_T_{d3}}(t)dt \end{bmatrix}, v_g(n) < V_b \end{cases}. \tag{30}$$

Generally, when a converter is designed, the main parameters are determined, and only the parasitic capacitance of the circuit is uncertain, which determines the distortion degree of the input current. Therefore, according to (26) and (30), the waveforms of $i_{L\_\rm initial}(nT_s)$ and $i_{Td\_\rm ave}$ in a half line cycle can be plotted in Figs. 8 and 9. Obviously, the smaller value of $C_{\rm eq}$ results in smaller values of $i_{L\_\rm initial}(nT_s)$ and $i_{L\_Td\_\rm ave}$. Usually, the order of magnitude for oscillation frequency is about megahertz, and the equivalent resistance at such a high frequency is much higher than its dc resistance. The exact value of the resistance is related to the design and fabrication of the inductor, which depends on the power, the input voltage range, required power density, and other specifications of the converter. Here, 10, 50, 100 Ω are taken as examples for the analysis in Figs. 8 and 9.

III. Series Diode Method for Oscillation Suppression

In conclusion, the smaller the parasitic capacitance in oscillation period, the smaller the effect on the input current distortion. Among the commonly used power components, the parasitic capacitance of the diodes is relatively small, and also due to its simplicity, a diode can be introduced into the circuit so as to reduce the equivalent capacitance. From Fig. 3(a), it can be seen that if the diode is connected in series in the oscillating circuit, the equivalent parasitic capacitance can be reduced. Obviously, $C_{\rm eq}$ can be reduced maximally while the diode is connected in series with the inductor.

The boost circuit with SD is shown in Fig. 10(a), and its equivalent oscillation circuit is plotted in Fig. 10(b). $C_{\rm DL}$ is the junction capacitance of the series diode D_L.

In Fig. 10(b), $C'_{\rm eq}$ can be calculated as

$$C'_{\rm eq} = \frac{(C_{\rm oss}+C_D)\,C_{D_L}}{C_{\rm oss}+C_D+C_{D_L}}. \tag{31}$$

Equation (31) indicates that $C'_{\rm eq}$ is less than $C_{\rm DL}$, therefore, if $C_{\rm DL}$ is small enough, $C'_{\rm eq}$ is small enough.

Apparently, D_L is always conductive during the period of $T_{\rm on}$ and $T_{\rm off}$. In the rest time of T_s, the inductor will oscillate with the equivalent parasitic capacitance. The derivation process of the

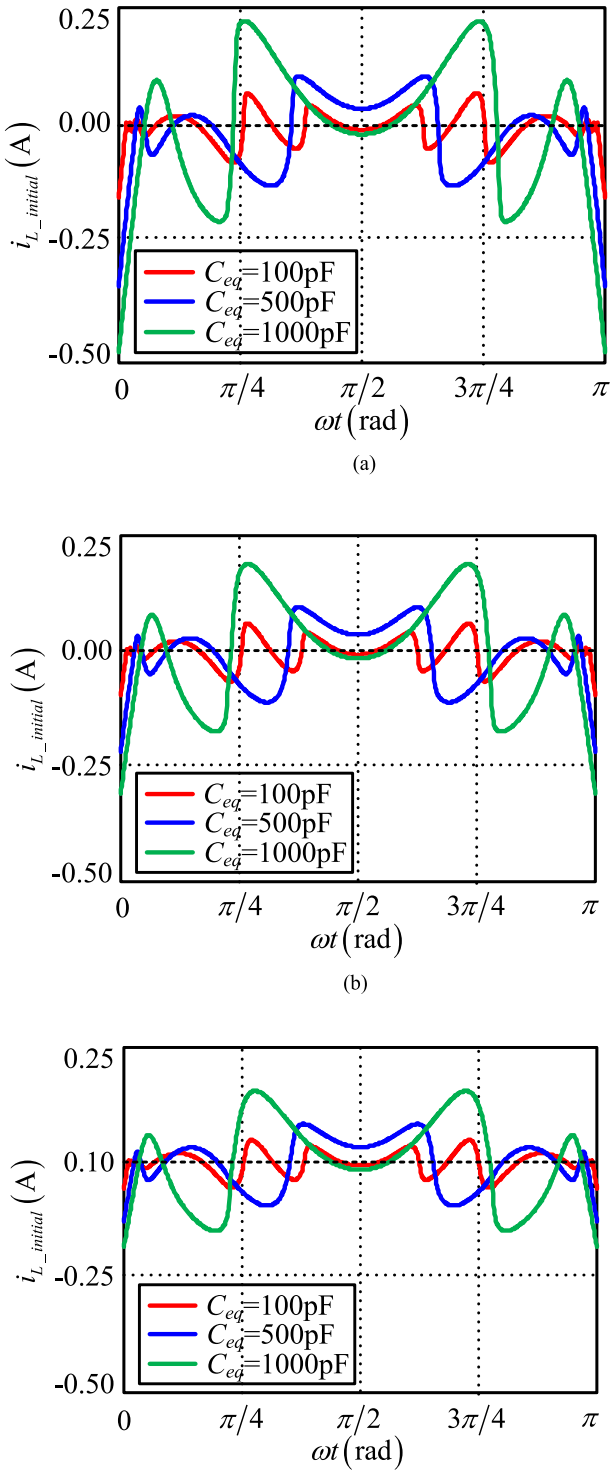
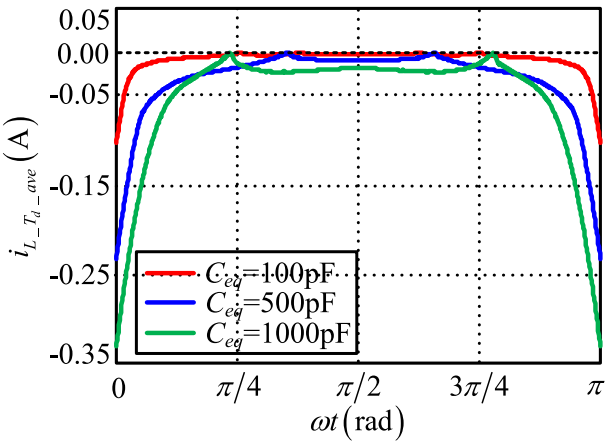


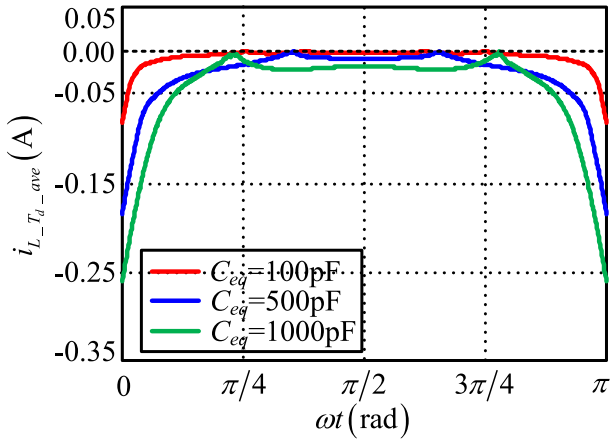
Fig. 8. Values of $i_{L\_\rm initial}(nT_s)$ with different R_s and $C_{\rm eq}$. (a) $R_s = 10\,\Omega$. (b) $R_s = 50\,\Omega$. (c) $R_s = 100\,\Omega$.

inductor current $i'_{L\_T_d}$ is the same as (4)–(12), and the expression is

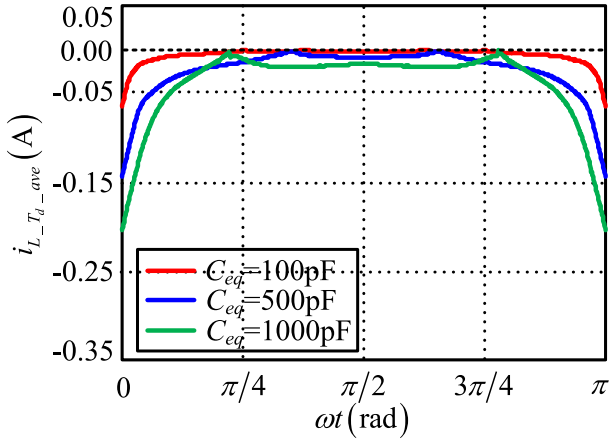
$$i'_{L\_T_d}(t) = \frac{v_g(n)-V_o}{L\omega'_d} e^{-\frac{R_s}{2L}[t-(n-1)T_s-T_{\rm on}-T_{\rm off}]} \times \sin\left[\omega'_d\left(t-(n-1)T_s-T_{\rm on}-T_{\rm off}\right)\right] \tag{32}$$



(a)



(b)



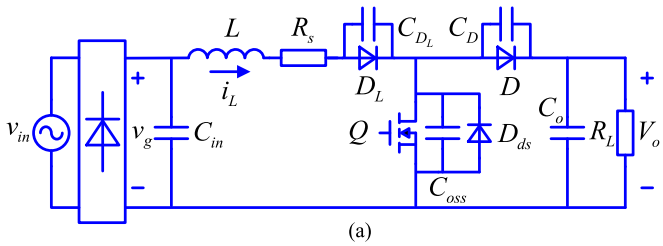
(c)

Fig. 9. Values of $i_{L\_Td\_\mathrm{ave}}$ with different R_s and C_{eq}. (a) $R_s = 10\ \Omega$. (b) $R_s = 50\ \Omega$. (c) $R_s = 100\ \Omega$.

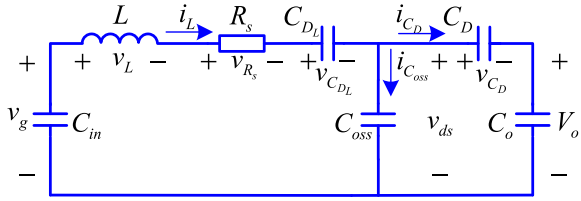
where

$$\omega_d' = \sqrt{\frac{1}{LC'_{\mathrm{eq}}} - \left(\frac{R_s}{2L}\right)^2}. \tag{33}$$

The time instant of $(n-1)T_s + T_{\mathrm{on}} + T_{\mathrm{off}}$ is the initial time of oscillation period, when the diode D_L has just turned OFF, so



(a)



(b)

Fig. 10. Boost circuit with SD and its equivalent oscillation circuit. (a) Boost circuit with SD. (b) Equivalent oscillation circuit with SD.

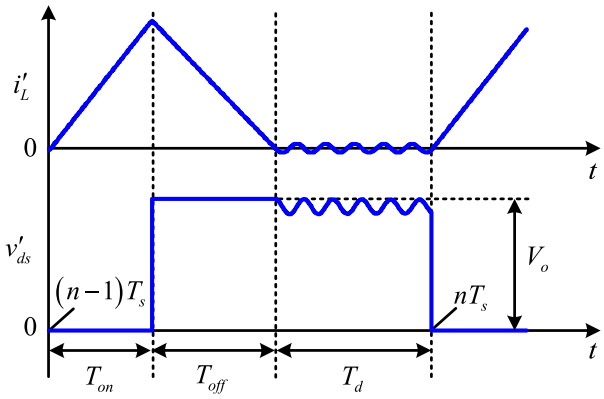


Fig. 11. Theoretical waveforms of $i'_{L\_T_d}$ and $v'_{ds\_T_d}$.

the voltage on C_{DL} equalsto zero. Therefore, the voltage upon C_{DL} in oscillation period can be expressed as

$$\begin{aligned} v_{D_L\_T_d}(t) &= \frac{1}{C_{D_L}} \int_{(n-1)T_s+T_{\mathrm{on}}+T_{\mathrm{off}}}^{nT_s} i'_{L\_T_d}(t)dt \\ &= \frac{[V_o - v_g(n)]\,(C_{\mathrm{oss}} + C_D)}{2L\omega'_d\,(C_{\mathrm{oss}} + C_D + C_{D_L})} \\ &\times \left\{ \begin{array}{l} R_s e^{-\frac{R_s}{2L}[t-(n-1)T_s-T_{\mathrm{on}}-T_{\mathrm{off}}]} \\ \sin\left[\omega'_d \begin{pmatrix} t-(n-1)T_s \\ -T_{\mathrm{on}}-T_{\mathrm{off}} \end{pmatrix}\right] \\ +2L\omega'_d e^{-\frac{R_s}{2L}[t-(n-1)T_s-T_{\mathrm{on}}-T_{\mathrm{off}}]} \\ \cos\left[\omega'_d \begin{pmatrix} t-(n-1)T_s \\ -T_{\mathrm{on}}-T_{\mathrm{off}} \end{pmatrix}\right] \\ -2L\omega'_d \end{array} \right\}. \end{aligned} \tag{34}$$

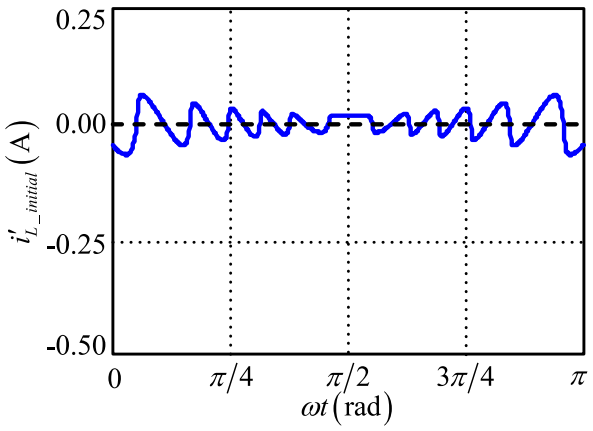


Fig. 12. Waveform of the initial value of the inductor current with SD.

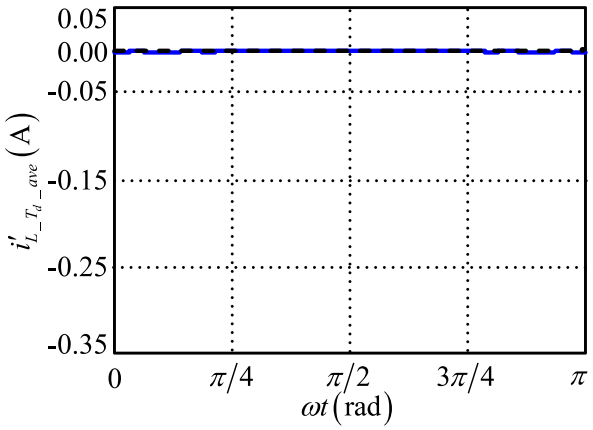


Fig. 13. Waveform of the average value of the inductor current in oscillation period with SD.

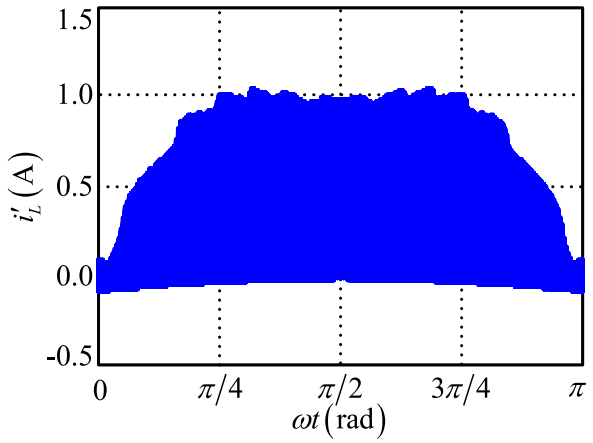


Fig. 14. Theoretical waveform of inductor current with SD.

The drain source voltage can be calculated as

$$v'_{\mathrm{ds}\_T_d}(t) = v_g(n) - L\frac{di'_{L\_T_d}(t)}{dt} - R_s i'_{L\_T_d}(t) - v_{D_L\_T_d}(t)$$
$$= \frac{(C_{\mathrm{oss}} + C_D)\,V_o + C_{D_L}\,v_g(n)}{C_{\mathrm{oss}} + C_D + C_{D_L}} + \frac{V_o - v_g(n)}{\omega'_d}$$

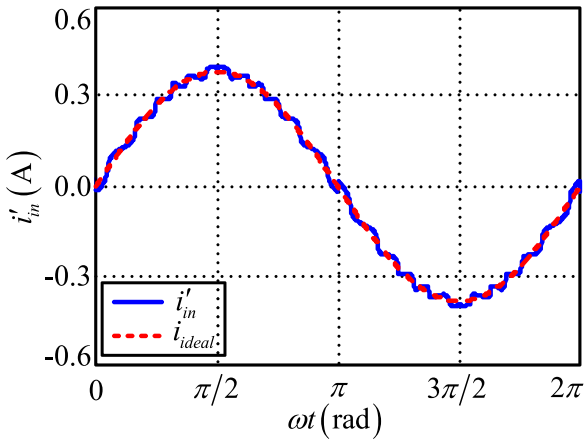


Fig. 15. Theoretical waveforms of input current with SD.

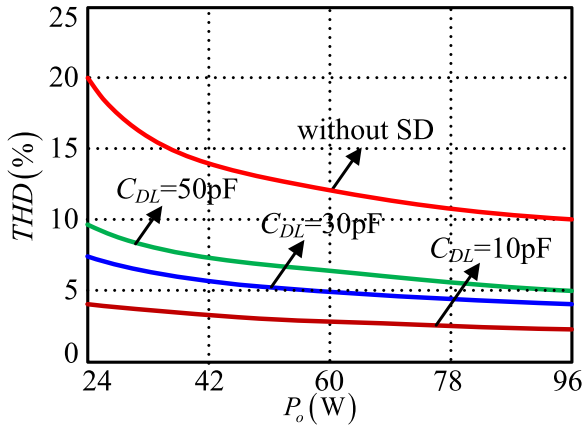


Fig. 16. Theoretical improvements of THD at 220 VAC.

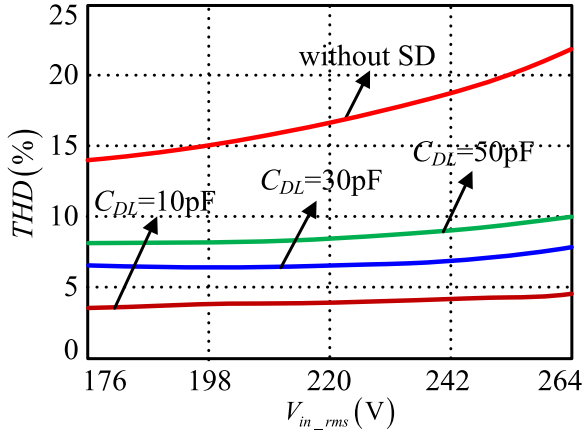


Fig. 17. Theoretical improvements of THD while $P_o = 30$ W.

$$\times \frac{2\,(C_{\mathrm{oss}} + C_D) + C_{D_L}}{C_{\mathrm{oss}} + C_D + C_{D_L}} e^{-\frac{R_s}{2L}[t-(n-1)T_s - T_{\mathrm{on}} - T_{\mathrm{off}}]}$$
$$\times \left\{ \begin{array}{l} \omega'_d \cos\left[\omega'_d\,(t-(n-1)T_s - T_{\mathrm{on}} - T_{\mathrm{off}})\right] \\ +\dfrac{R_s}{2L} \sin\left[\omega'_d\,(t-(n-1)T_s - T_{\mathrm{on}} - T_{\mathrm{off}})\right] \end{array} \right\}. \quad (35)$$

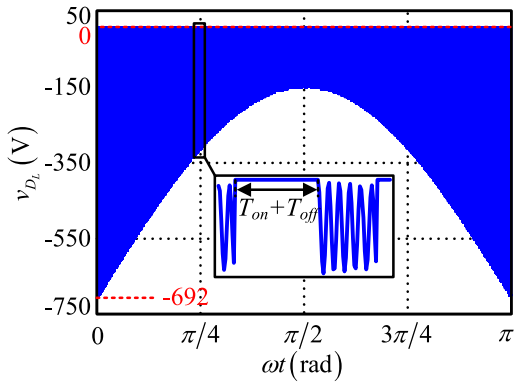


Fig. 18. Theoretical waveform of v_{DL}.

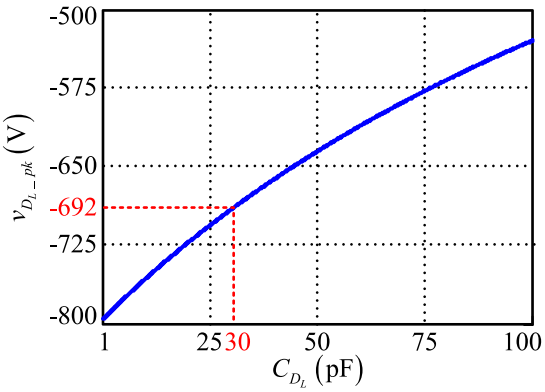


Fig. 19. Relationship between $v_{\mathrm{DL_{pk}}}$ and C_{DL}.

TABLE I
REVERSE PEAK VOLTAGE OF SERIES DIODE

C_{DL}	1 pF	10 pF	20 pF	30 pF
v_{DL_pk}	795 V	759 V	724 V	692 V

Through the differential calculus, the minimum value of (35) in a switching cycle can be obtained while $\omega_d' [t-(n-1)T_s - T_{\mathrm{on}} - T_{\mathrm{off}}] = \pi$, which is

$$v'_{ds\_T_d\_\min\_s}(t) = v_g(n)\left(1+e^{-\frac{R_s\pi}{2L\omega'_d}}\right)\frac{C_{D_L}}{C_{oss}+C_D+C_{D_L}} + V_o\left(\frac{C_{oss}+C_D}{C_{oss}+C_D+C_{D_L}} - \frac{C_{D_L}e^{-\frac{R_s\pi}{2L\omega'_d}}}{C_{oss}+C_D+C_{D_L}}\right). \tag{36}$$

With the variation of $v_g(n)$ during a half line period, the minimum value of (36) can be got at $v_g(n) = 0$,that is

$$v'_{\mathrm{ds}\_T_d\_\min\_l} = V_o\left(\frac{C_{\mathrm{oss}}+C_D}{C_{\mathrm{oss}}+C_D+C_{D_L}} - \frac{C_{D_L}e^{-\frac{R_s\pi}{2L\omega'_d}}}{C_{\mathrm{oss}}+C_D+C_{D_L}}\right). \tag{37}$$

Generally, C_{DL} is much smaller than the sum of C_{oss} and C_D, so $v'_{\mathrm{ds}\_T_d\_\min\_l}$ is always positive in the oscillation period.

According to (32) and (35), the theoretical waveforms of $i'_{L\_T_d}$ and $v'_{\mathrm{ds}\_T_d}$ in a switching cycle are shown in Fig. 11. It can be seen that the oscillation frequency of the inductor current is increased greatly, the oscillation amplitude decreases, and the initial value of inductor current in a switching cycle is nearly zero.

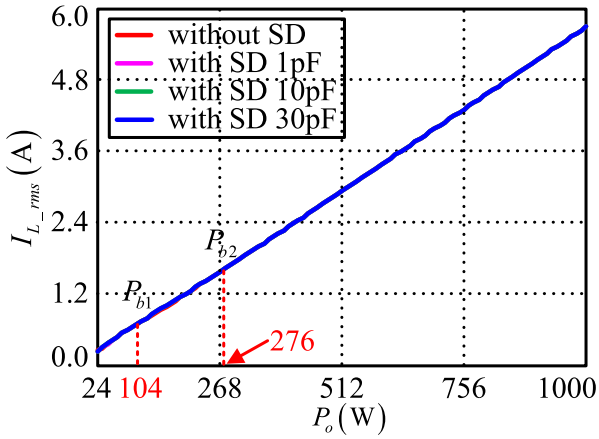


Fig. 20. RMS value of the inductor current.

Similarly, based on (25), (27), and (32), the average current in a switching cycle can be expressed as

$$i'_{\mathrm{in}}(t) = \frac{1}{T_s}\begin{bmatrix}\int_{(n-1)T_s}^{(n-1)T_s+T_{\mathrm{on}}} i'_{L\_T_{\mathrm{on}}}(t)dt \\ +\int_{(n-1)T_s+T_{\mathrm{on}}}^{(n-1)T_s+T_{\mathrm{on}}+T'_{\mathrm{off}}} i'_{L\_T_{\mathrm{off}}}(t)dt \\ +\int_{(n-1)T_s+T_{\mathrm{on}}+T'_{\mathrm{off}}}^{nT_s} i'_{L\_T_d}(t)dt\end{bmatrix}. \tag{38}$$

It should be noted that, the expressions of $i'_{L\_T_{\mathrm{on}}}$,$i'_{L\_T_{\mathrm{off}}}$, and T'_{off} in (38) are nearly the same as (25), (27), and (28) respectively, except for the initial value of inductor current in each switching cycle, which can be written as

$$i'_{L\_\mathrm{initial}}(nT_s) = \frac{v_g(n-1)-V_o}{L\omega'_d}e^{-\frac{R_s}{2L}(T_s-T_{\mathrm{on}}-T'_{\mathrm{off}})} \times \sin\left[\omega'_d\left(T_s-T_{\mathrm{on}}-T'_{\mathrm{off}}\right)\right]. \tag{39}$$

The average current in the oscillation period is calculated as

$$i'_{L\_T_d\_ave}(t) = \frac{1}{T_s}\int_{(n-1)T_s+T_{\mathrm{on}}+T'_{\mathrm{off}}}^{nT_s} i'_{L\_T_d}(t)dt. \tag{40}$$

According to (39) and (40), the waveforms of $i'_{L\_\mathrm{initial}}(nT_s)$ and $i'_{L\_T_d\_ave}$ in a half line cycle are plotted in Figs. 12 and 13, which show that the initial value of the inductor current in each switching cycle and the average value of the inductor current in oscillation period is approximately zero.

Based on (32) and (38), the theoretical waveforms of the inductor current and the input current in a line frequency cycle are shown in Figs. 14 and 15. The distortion of the input current in Fig. 15 is improved effectively compared to that in Fig. 7. The input current with SD is almost sinusoidal.

The THD of the input current can be calculated as

$$\mathrm{THD} = \sqrt{\frac{I^2_{\mathrm{in\_rms}}-I_1^2}{I_1^2}} \times 100\% \tag{41}$$

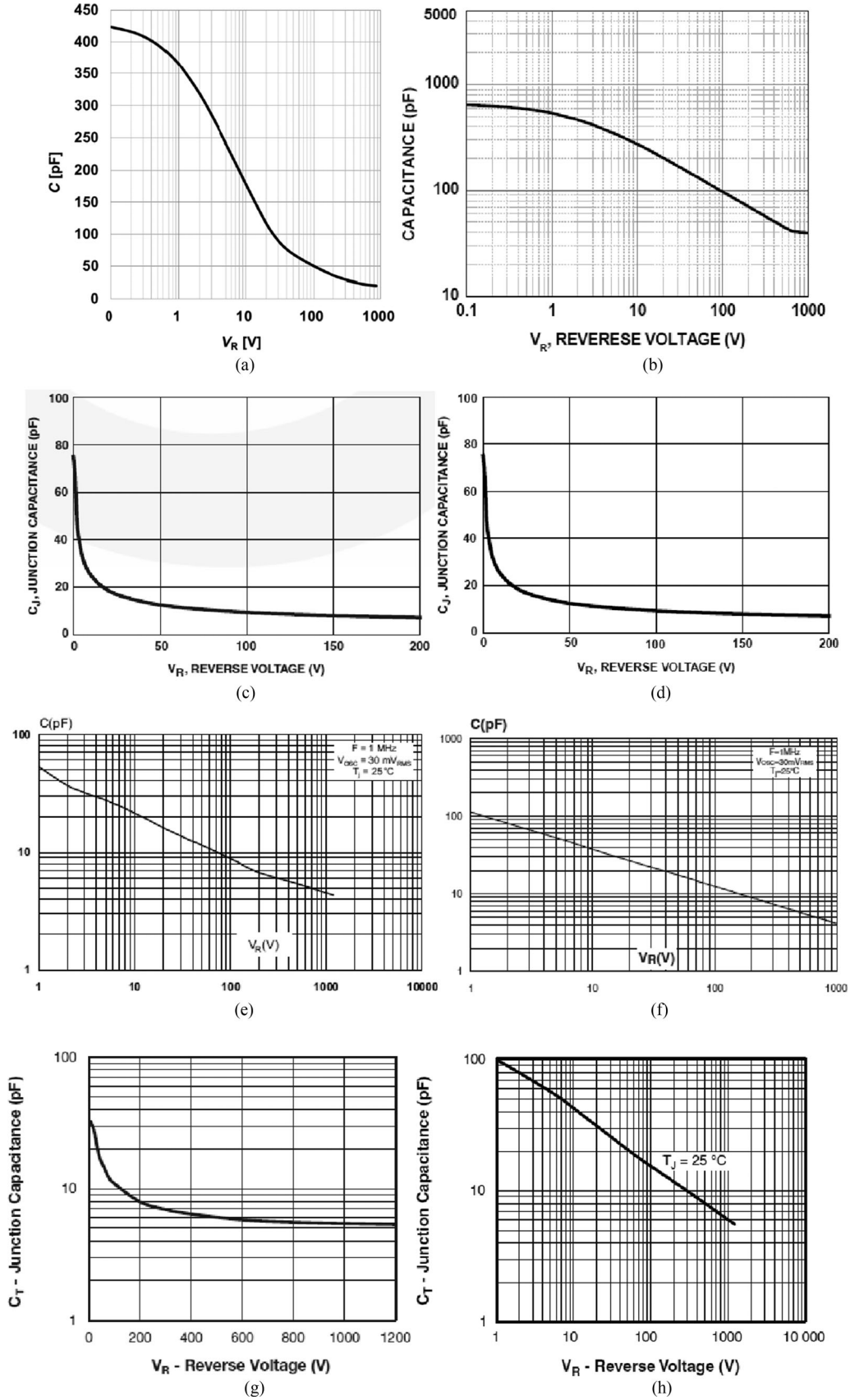


Fig. 21. Junction capacitance versus reverse voltage. (a) Infineon—IDH08G120C5. (b) ON Semiconductor—FFSP08120A. (c) Fairchild—RHRP8120. (d) Intersil—RURP8120. (e) ST—STTH8S12. (f) ST—STTH812. (g) Vishay—VS-8ETU12-N3. (h) Vishay—HFA08PB120PbF.

TABLE II
PROBABLY SUITABLE DIODES

Corporation	Type	V_{RRM}	I_{FAV}	C_j
Infineon	IDH08G120C5	1200 V	8 A	365 pF at V_R = 1V, 50 pF at V_R = 100 V 26 pF at V_R = 400 V, 20 pF at V_R = 800 V
	IDH10G120C5	1200 V	10 A	525 pF at V_R = 1V, 75 pF at V_R = 100 V 37 pF at V_R = 400 V, 29 pF at V_R = 800 V
	IDH16G120C5	1200 V	16 A	730 pF at V_R = 1 V, 100 pF at V_R = 100 V 52 pF at V_R = 400 V, 40 pF at V_R = 800 V
ON Semiconductor	MUR8100E	1000 V	8 A	58 pF at V_R = 100 V
	FFSP08120A	1200 V	8 A	538 pF at V_R = 1 V, 100 pF at V_R = 100 V 50 pF at V_R = 400 V, 40 pF at V_R = 800 V
	FFSP10120A	1200 V	10 A	612 pF at V_R = 1 V, 120 pF at V_R = 100 V 58 pF at V_R = 400 V, 47 pF at V_R = 800 V
Fairchild	RURP8100	1000 V	8 A	30 pF at V_R = 10 V, 12 pF at V_R = 100 V
	RURP15100	1000 V	15 A	60 pF at V_R = 10 V, 21 pF at V_R = 100 V
	RHRP8120	1200 V	8 A	25 pF at V_R = 10 V, 9 pF at V_R = 100 V
	RHRP15120	1200 V	15 A	55 pF at V_R = 10 V, 19 pF at V_R = 100 V
Intersil	RURP8120	1200 V	8 A	25 pF at V_R = 10 V, 9 pF at V_R = 100 V
	RURP15120	1200 V	15 A	56 pF at V_R = 10 V, 23 pF at V_R = 100 V
ST	STTH810	1000 V	8 A	9 pF at V_R = 100 V
	STTH1210	1000 V	12 A	13 pF at V_R = 100 V
	STTH8S12	1200 V	8 A	9 pF at V_R = 100 V
	STTH812	1200 V	8 A	13 pF at V_R = 100 V
	STPSC10H12	1200 V	10 A	725 pF at V_R = 0 V, 100 pF at V_R = 100 V 60 pF at V_R = 300 V
	STTH1212	1200 V	12 A	17 pF at V_R = 100 V
Vishay	VS-8ETU12-N3	1200 V	8 A	12 pF at V_R = 100 V, 8 pF at V_R = 200 V
	VS-HFA08PB120PbF	1200 V	8 A	17 pF at V_R = 100 V, 11 pF at V_R = 200 V
	VS-15ETU12HN3	1200 V	15 A	17 pF at V_R = 100 V, 13 pF at V_R = 200 V
	VS-HFA16PB120PbF	1200 V	16 A	38 pF at V_R = 100 V, 27 pF at V_R = 200 V

where

$$I_{\text{in\_rms}} = \sqrt{\frac{2}{T_l}\int_0^{T_l/2} i_{\text{in}}^2(t)dt} \tag{42}$$

$$I_1 = \frac{\sqrt{2}}{T_l}\int_0^{T_l} i_{\text{in}}(t)\sin\frac{2\pi}{T_l}tdt \tag{43}$$

where $I_{\text{in\_rms}}$ is the RMS value of the input current, I_1 is the RMS value of the fundamental component of the input current, and T_l is the line frequency cycle.

From (29), (38), and (41), the THD of the converter without and with SD are shown in Figs. 16 and 17, respectively. It can be observed that a smaller parasitic capacitance of the series diode leads to a greater improvement of THD.

From (34), the theoretical voltage waveform of v_{DL} in a half line cycle can be plotted, as shown in Fig. 18.

According to (34) and Fig. 18, it can be seen that v_{DL} reaches the peak value $v_{\text{DL}_{\text{p}}\text{k}}$ when $v_g(n)$ equals to zero and $\omega_d'\,[t-(n-1)T_s-T_{\text{on}}-T_{\text{off}}] = \pi$. Therefore

$$v_{D_L\text{-pk}} = -\frac{V_o\,(C_{\text{oss}}+C_D)\left(1+e^{-\frac{R_s\pi}{2L\omega_d'}}\right)}{C_{\text{oss}}+C_D+C_{D_L}}. \tag{44}$$

From (44), it is known that the reverse peak voltage of series diode is only related to the parameters of the circuit and has nothing to do with the input voltage and load power. When the main parameters of the circuit are determined, $v_{\text{DL}_{\text{p}}\text{k}}$ can be calculated by the value of C_{DL}. Fig. 19 is given to show the relationship between $v_{\text{DL}_{\text{p}}\text{k}}$ and C_{DL}. It should be noted that, the required rated voltage of the diode is relatively high, which is independent from the rated power of the system.

Based on (44), the reverse peak voltage of series diode can be calculated for different values of C_{DL}, as shown in Table I.

For different power range, a 1 kW converter will operate in three conduction modes, i.e., fully CCM, MCM, and fully DCM, and the RMS values of the inductor current for these situations can be calculated as (45a), (45b), and (45c), respectively,

$$I_{L\_\text{rms\_CCM}} = \sqrt{\frac{2}{T_l}\sum_{n=1}^{f_s/2f}\begin{bmatrix}\int_{(n-1)T_s}^{(n-1)T_s+T_{\text{on}}} i_{L\_T_{\text{on}}}^2(t)dt \\ +\int_{(n-1)T_s+T_{\text{on}}}^{nT_s} i_{L\_T_{\text{off}}}^2(t)dt\end{bmatrix}} \tag{45a}$$

$$I_{L\_\text{rms\_MCM}} = \sqrt{\frac{2}{T_l}\left\{\begin{array}{l} 2\sum_{n=1}^{N_1}\begin{bmatrix}\int_{(n-1)T_s}^{(n-1)T_s+T_{\text{on}}} i_{L\_T_{\text{on}}}^2(t)dt \\ +\int_{(n-1)T_s+T_{\text{on}}}^{(n-1)T_s+T_{\text{on}}+T_{\text{off}}} i_{L\_T_{\text{off}}}^2(t)dt \\ +\int_{(n-1)T_s+T_{\text{on}}+T_{\text{off}}}^{nT_s} i_{L\_T_d}^2(t)dt\end{bmatrix} \\ +\sum_{n=N_1}^{N_2}\begin{bmatrix}\int_{(n-1)T_s}^{(n-1)T_s+T_{\text{on}}} i_{L\_T_{\text{on}}}^2(t)dt \\ +\int_{(n-1)T_s+T_{\text{on}}}^{nT_s} i_{L\_T_{\text{off}}}^2(t)dt\end{bmatrix}\end{array}\right\}} \tag{45b}$$

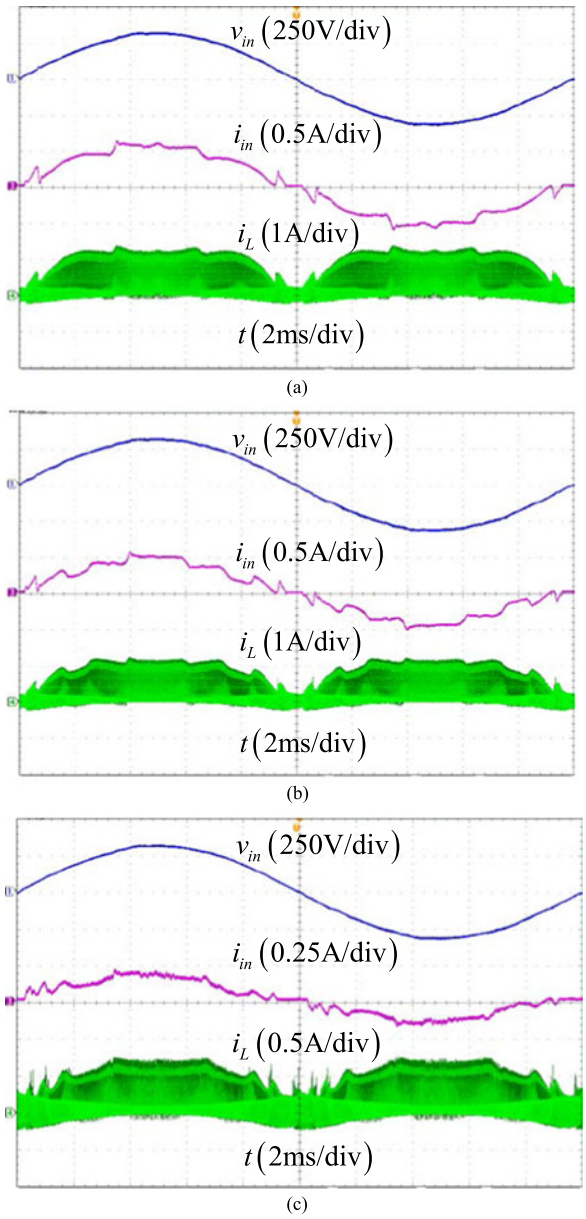


Fig. 22. Experimental waveforms without SD at 220 VAC. (a) $P_o = 88$ W. (b) $P_o = 60$ W. (c) $P_o = 24$ W.

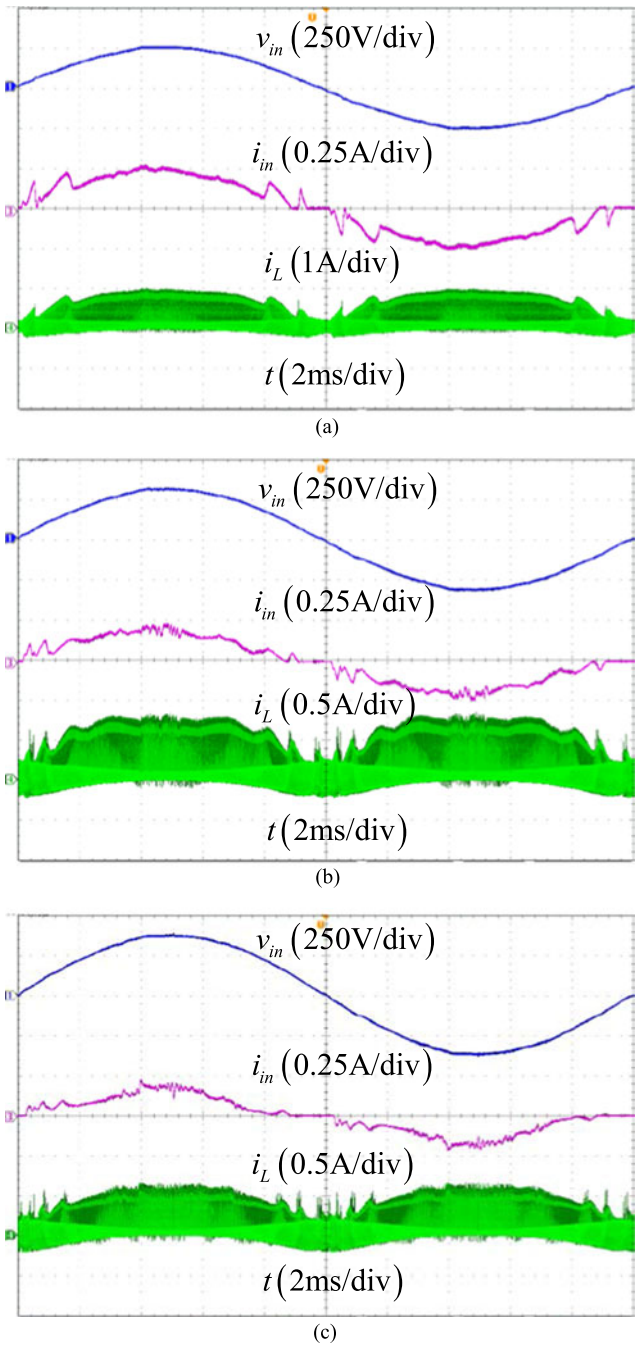


Fig. 23. Experimental waveforms without SD while $P_o = 30$ W. (a) 176 V. (b) 220 V. (c) 264 V.

$$I_{L\_\mathrm{rms\_DCM}} = \sqrt{\frac{2}{T_l}\sum_{n=1}^{f_s/2f}\begin{bmatrix}\int_{(n-1)T_s}^{(n-1)T_s+T_{\mathrm{on}}} i_{L\_T_{\mathrm{on}}}^2(t)dt \\ +\int_{(n-1)T_s+T_{\mathrm{on}}}^{(n-1)T_s+T_{\mathrm{on}}+T_{\mathrm{off}}} i_{L\_T_{\mathrm{off}}}^2(t)dt \\ +\int_{(n-1)T_s+T_{\mathrm{on}}+T_{\mathrm{off}}}^{nT_s} i_{L\_T_d}^2(t)dt\end{bmatrix}} \tag{45c}$$

where

$$\begin{cases} N_1 = \dfrac{\arcsin\left[\frac{V_o}{V_m}\left(1-\frac{4P_oLf_s}{V_m^2}\right)\right]}{\omega T_s} \\ N_2 = \dfrac{f_s}{2f} - \dfrac{\arcsin\left[\frac{V_o}{V_m}\left(1-\frac{4P_oLf_s}{V_m^2}\right)\right]}{\omega T_s} \end{cases}. \tag{46}$$

Obviously, a higher RMS value of the inductor current is corresponding to a lower value of the input voltage.

Combining with the parameters of the converter and substituting $V_m = 176\sqrt{2}$ into (45)–(48), Fig. 20 can be plotted. It is apparent that the maximum RMS value of the inductor current is 5.7 A, which occurs at the full power of 1 kW.

Based on the voltage and current stress, the probably suitable diodes can be searched and found, as shown in Table II. Taking margin into consideration, the diodes with 1200 V of V_{RRM} are more appropriate. From Figs. 16 and 17, it can be known that a

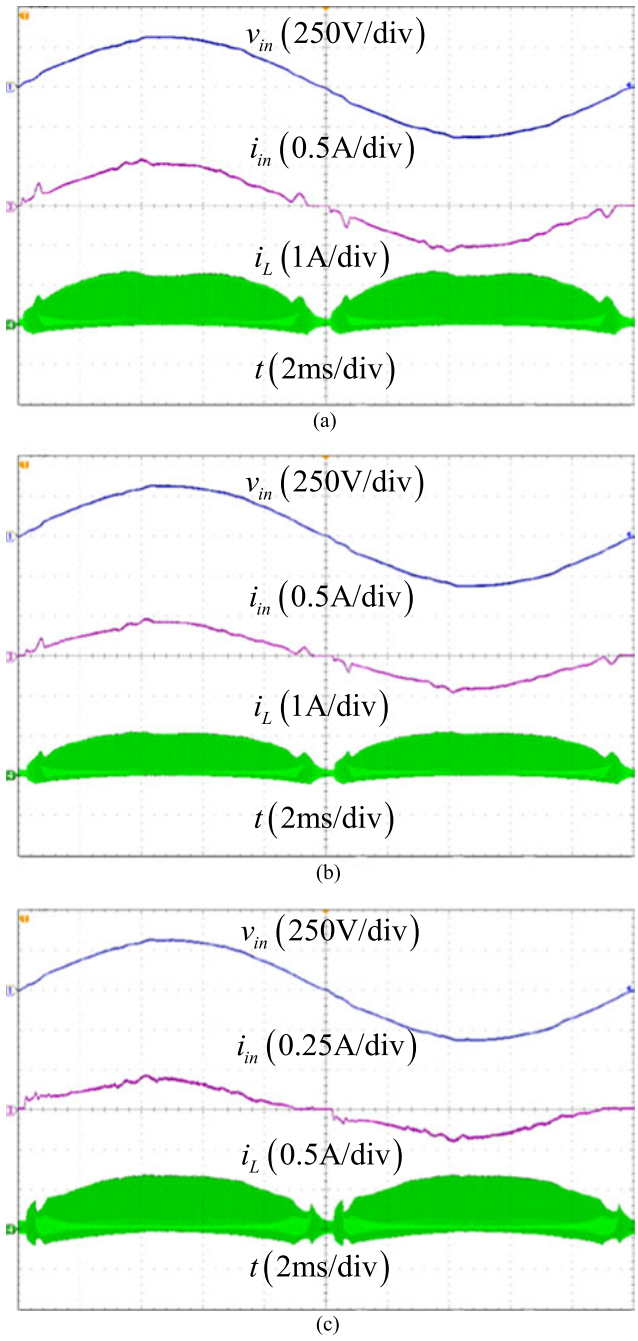


Fig. 24. Experimental waveforms with RCD at 220 VAC. (a) $P_o = 88$ W. (b) $P_o = 60$ W. (c) $P_o = 24$ W.

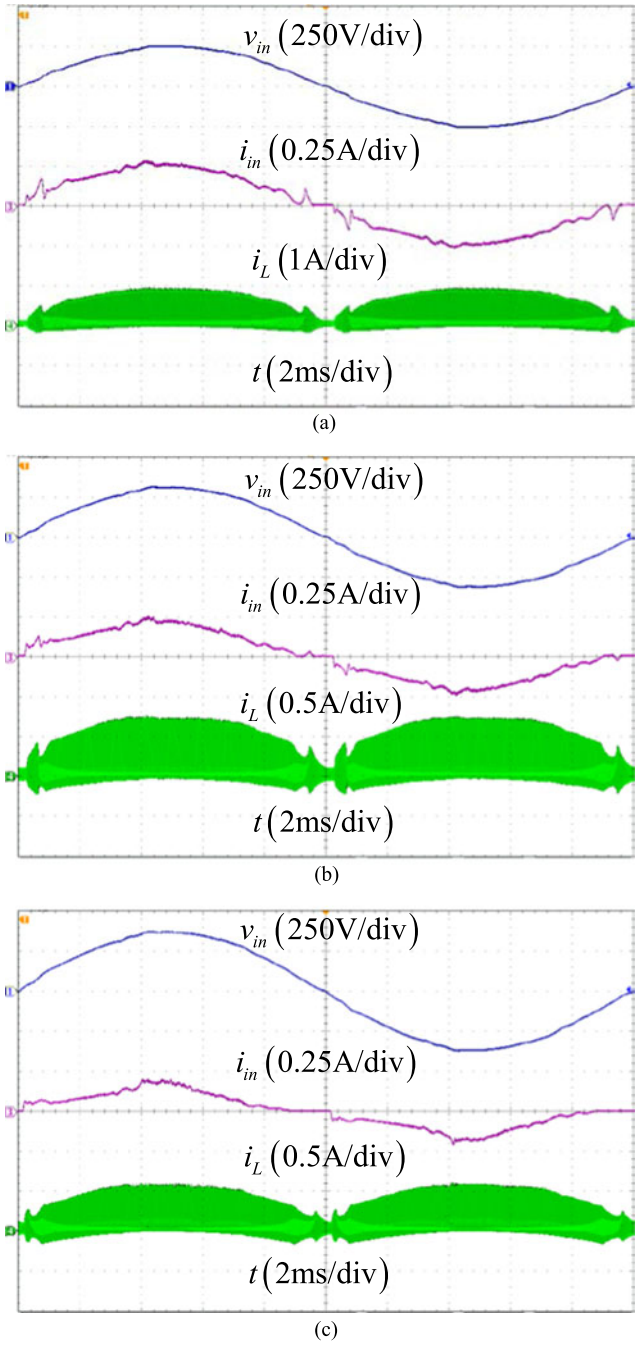


Fig. 25. Experimental waveforms with RCD while $P_o = 30$ W. (a) 176 V. (b) 220 V. (c) 264 V.

smaller C_j of the series diode results in a better improvement of THD. Based on this, RURP8120 from Intersil or RHRP8120 from Fairchild are the most suitable one, for they are characteristic of not only a low but also a comparatively stable value of C_j, which can be observed and compared from the curves of C_j versus the inverse voltage V_R in datasheet, as shown in Fig. 21. In this paper, RURP8120 from Intersil is adopted in the prototype.

For other boost PFC converters with certain parameters, the same method can be used for the analysis and calculation, then the corresponding diode can be searched and selected. In conclusion, the diode should meet the required voltage and current stress, and most importantly, features a low and stable value of the junction capacitance.

IV. Experimental Verification

In order to verify the effectiveness of the proposed method, a 1-kW boost PFC converter based on DSP MC56F8257 has been built and tested in DCM operation. The variable duty cycle

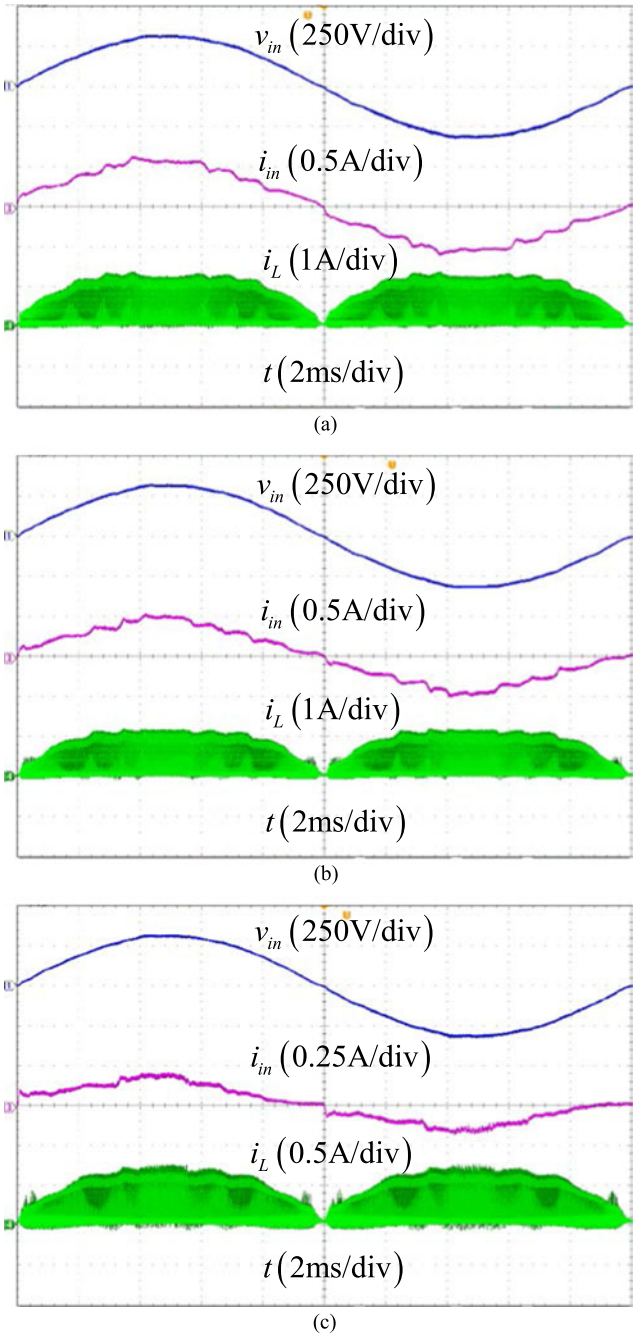


Fig. 26. Experimental waveforms with SD at 220 VAC. (a) $P_o = 88$ W. (b) $P_o = 60$ W. (c) $P_o = 24$ W.

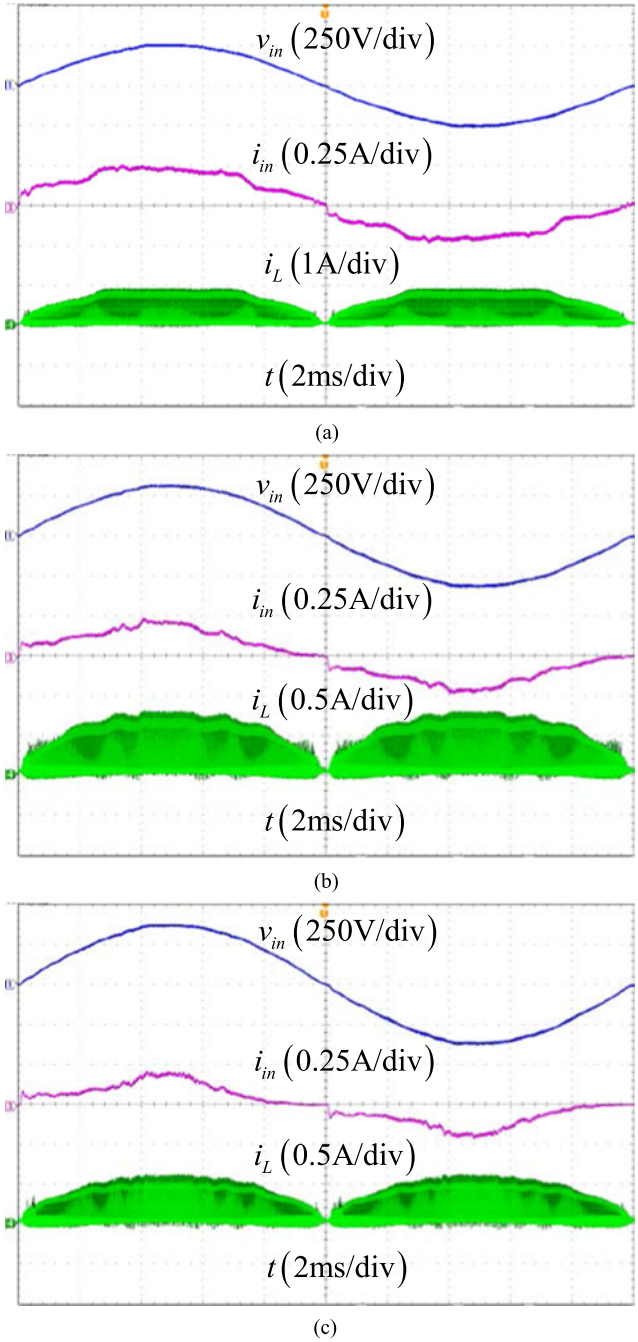
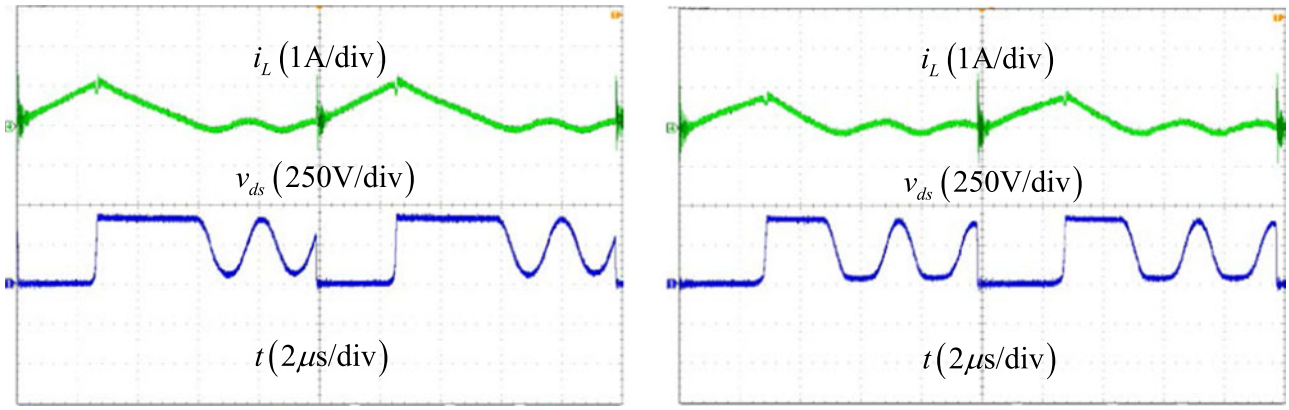


Fig. 27. Experimental waveforms with SD while $P_o = 30$ W. (a) 176 V. (b) 220 V. (c) 264 V.

control strategy proposed in [20] is adopted. The theoretical critical load power of the converter is 96 W at 220 VAC. In the actual experiment, 88 W is employed as the margin is considered. In addition, [23] is studied carefully, which indicates that RCD snubber is a better choice in terms of both the oscillation damping effect and the efficiency, compared to that of RC snubber. Therefore, the RCD snubber is also adopted in the experiment. The specifications and components of the prototype are as follows: $V_{\text{in\_rms}} = 176 - 264$ V, $f_l = 50$ Hz, $f_s = 100$ kHz, $P_o = 24 - 88$ W, $V_o = 400$ V, $L = 560$ μH, $R_s = 32$ Ω, $C_{\text{oss}} = 130$ pF, $C_D = 30$ pF, $C_{\text{DL}} = 30$ pF, $C_{\text{in}} = 0.33$ μF, $C_o = 980$ μF. Power switch: IPP60R099CP, power diode: IDH05S60C, series diode: RURP8120. RCD snubber: $R_r = 2$ kΩ, $C_r = 470$ pF, D_r: BYV28-600. $V_{\text{in\_rms}}$, and P_o are chosen as 220 VAC and 60 W, respectively, for the aforementioned theoretical analysis.

The waveforms of the input voltage, input current, and inductor current are presented in Figs. 22 and 23 without any oscillation suppression circuit, Figs. 24 and 25 with RCD snubber, and Figs. 26 and 27 with SD, respectively. Figs. 22 and 23 show



(a) (b)

Fig. 28. Inductor current and the drain source voltage waveforms without SD. (a) $v_g(n) \geq V_b$. (b) $v_g(n) < V_b$.

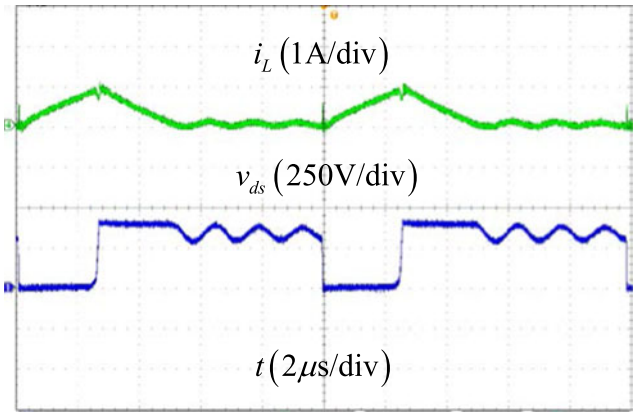


Fig. 29. Inductor current and the drain source voltage waveforms with SD.

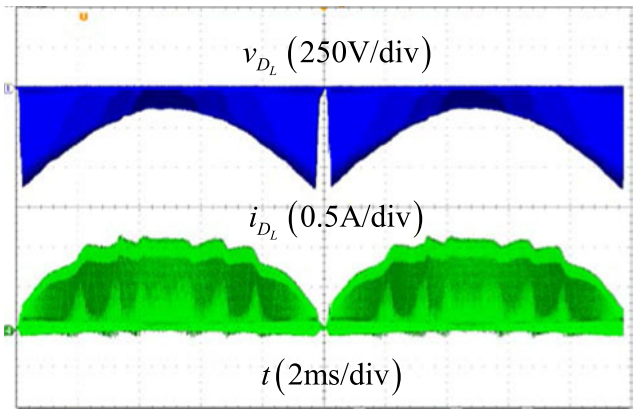
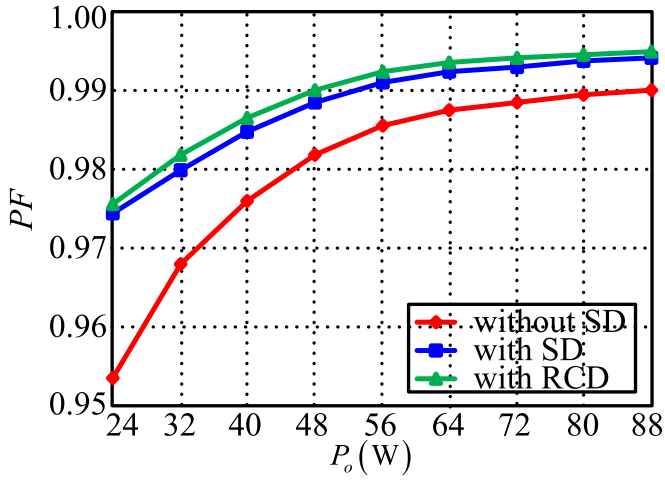
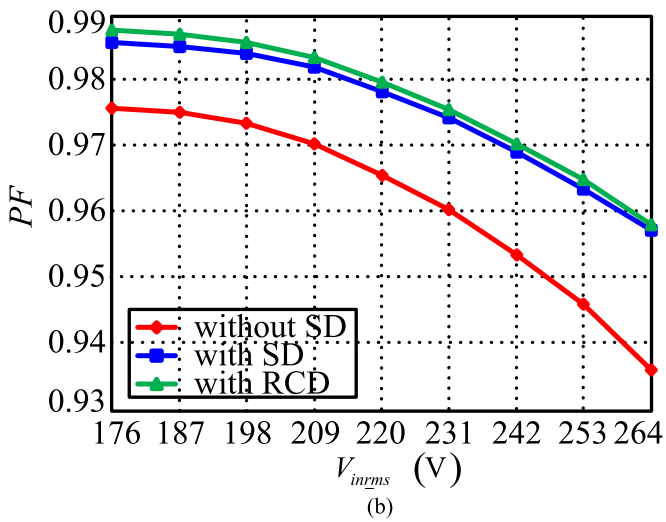


Fig. 30. Voltage and current waveforms of D_L.



(a)



(b)

Fig. 31. Measured PF. (a) PF curves with different P_o at 220 VAC. (b) PF curves with different V_{in_rms} while $P_o = 30$ W.

that when a CCM boost PFC converter operates in DCM, the input current is distorted seriously. It can be seen from Figs. 24 and 27 that the input current is improved effectively, especially at a high power and a low input voltage.

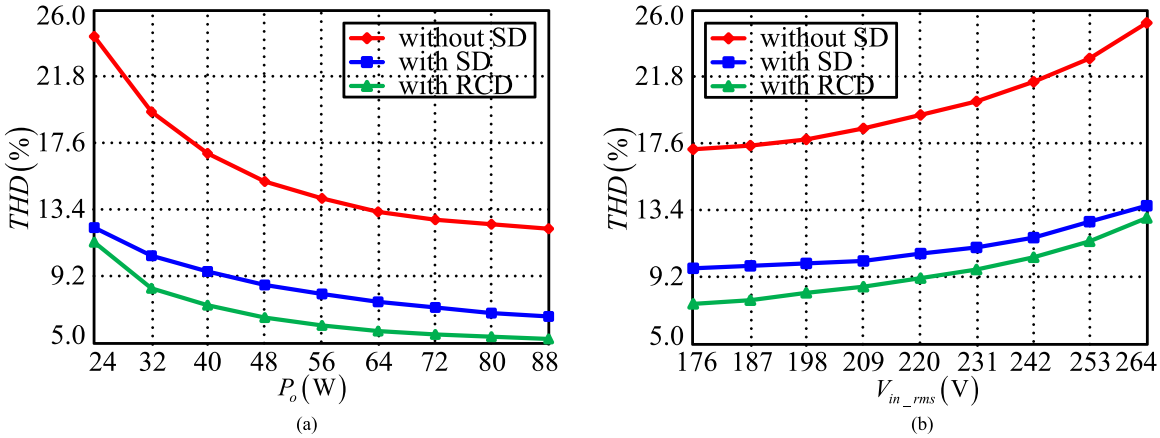


Fig. 32. Measured THD. (a) THD curves with different $P_{\rm o}$ at 220 VAC. (b) THD curves with different $V_{\rm in\_rms}$ while $P_o = 30$ W.

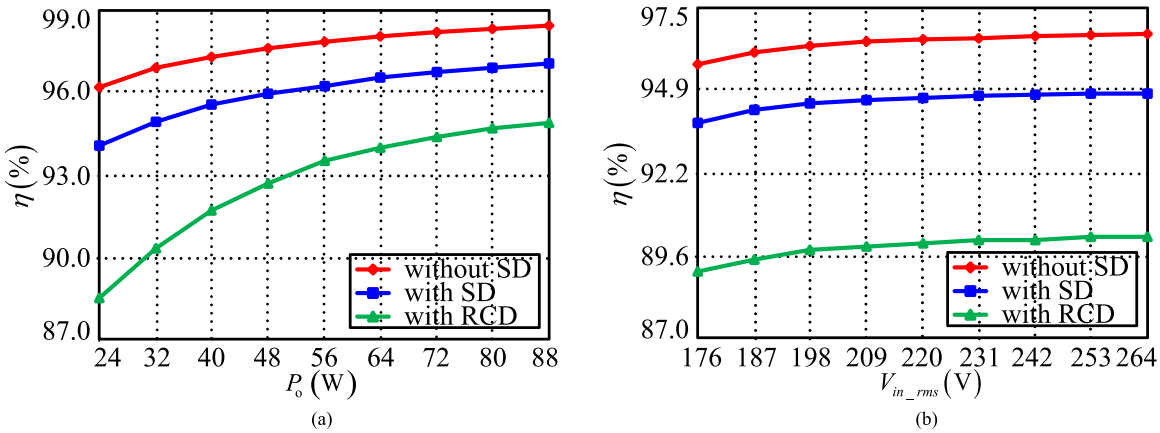


Fig. 33. Measured efficiency. (a) Efficiency curves with different $P_{\rm o}$ at 220 VAC. (b) Efficiency curves with different $V_{\rm in\_rms}$ while $P_o = 30$ W.

The inductor current waveforms in a switching cycle without and with SD are shown in Figs. 28 and 29 while $V_{\rm in\_rms} = 220$ V and $P_o = 60$ W. Figs. 28 and 29 illustrate that the amplitude of the inductor current is decreased with SD, and the inductor current is almost zero at the initial time of the switching period.

Fig. 30 shows the waveforms of the reverse voltage on $D_{\rm L}$ and the current through $D_{\rm L}$. It can be seen that the reverse voltage on $D_{\rm L}$ is basically the same as that of the theoretical analysis.

The PF, THD, and the efficiency curves from experimental results of the converter without SD, with RCD, and with SD at different load power and input voltage are given by Figs. 31, 32, and 33, respectively. From Figs. 31 and 32, it can be seen that the proposed method can effectively decrease the input current distortion and improve the power factor, and the PF is slightly lower than that of RCD snubber. At a certain input voltage, the THD decreases with the increment of the output power, while at a certain output power, the THD increases with the increment of the input voltage, both for the converter without SD, with RCD, and with SD. The contrary is the case for PF.

Fig. 33 indicates that the proposed method brings about some reduction of the efficiency, for the series diode generates the increase of the conduction loss. In the oscillation process, the power consumption of the RCD snubber is higher than that of the SD method; therefore, the efficiency of the converter with SD is higher.

V. Conclusion

The oscillation process of a boost PFC converter operated in DCM is analyzed and the related mathematical expressions are derived and presented in detail. The analysis shows that a smaller equivalent parasitic capacitance results in smaller values of the average current in oscillation period and the initial value of the inductor current in a switching cycle, which, if are equal to zero, the distortion of input current can be eliminated. The series diode method is proposed for reducing the THD and improving the PF. The THD is figured out at different values of parasitic capacitance of the series diode. Also, the voltage and current stress are calculated, and the principle for the selection of the diode is that it should feature a low and stable value of the junction capacitance. In spite of the PF improvement, the SD method brings about an efficiency decrease. Moreover, being independently from the rated power, the required voltage rating of the series diode is high.

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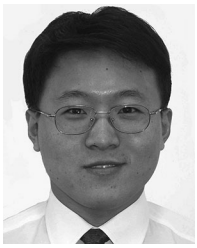

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