A Self-Balanced Step-Up Multilevel Inverter Based on Switched-Capacitor Structure

Amir Taghvaie, Jafar Adabi, and Mohammad Rezanejad

***Abstract*—In this paper, a dc to ac converter with the ability of voltage increasing is presented. This inverter is designed in a way that just one dc source is used. Also, by using power storage technique and with combining charged capacitors and dc source in series form, output voltage levels can be increased. This inverter is in a modular structure and has the ability of capacitor's voltage self-balancing. H-bridge inverter was not used at the end of the proposed converter and all elements tolerate a voltage stress equal to the amount of input dc source. This leads to remarkable decrease of total standing voltage and peak inverse voltage. Other advantage of the proposed inverter is its potentiality of performance in high-frequency applications. The modular form of the proposed inverter provides the potentiality of extension to higher voltage levels and eases the maintenance. Moreover, considering to the fact that the stress of all components of the suggested inverter is equal to the input source, the performance in high voltage is added to the characteristics of the proposed inverter. The nine-level structure of the proposed inverter is simulated and laboratory test is carried out for the verification of its performance.**

***Index Terms*—Bipolar inverter, self-balancing, switched-capacitors, step-up.**

I. Introduction

MULTILEVEL inverters (MLIs) play an important role in energy conversion systems, such as wind, photovoltaic, fuel cells, and electric vehicles [1]. These converters, which consist of dc sources, active switches, and power diodes, can produce staircase voltage waveform with low total harmonic distortion (THD). Power semiconductors in MLIs normally tolerate less voltage stress in comparison with the traditional two-levels counterparts [2]. The other advantages of MLIs are reducing the total losses and the output filter size [3]. On the other hand, the common MLIs such as flying capacitor and neutral point clamped have challenges regarding capacitors voltage balancing especially when the number of levels increases [4], [5]. Cascaded H-bridge MLIs need separate dc sources [6].

Manuscript received September 28, 2016; revised December 26, 2016; accepted February 2, 2017. Date of publication February 15, 2017; date of current version October 6, 2017. Recommended for publication by Associate Editor A. Ioinovici.

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Digital Object Identifier 10.1109/TPEL.2017.2669377

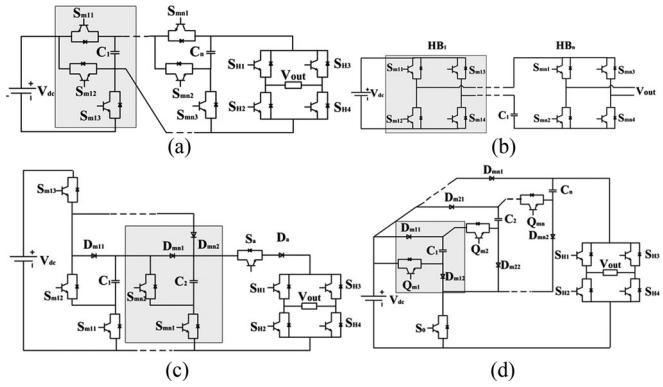

Fig. 1. Different structures of step-up SCMLIs (a) [17], (b) [20], (c) [24], (d) [18].

In many applications with low input dc sources (high or low power, single or multiple dc sources), a high-output ac voltage is required. Transformers or inductors are used in many topologies to boost the voltage in many applications such as grid connected distributed generation (DG) systems [7], electric vehicle [8], and renewable sources [9] in which the input voltage is less than the required output voltage. However, high volume cores in transformers and inductors lead to bulky and heavy converters in mentioned systems [10]. Researchers seek for MLI structures with combination of dc sources and capacitors through different power semiconductors in order to achieve higher output ac voltage in staircase form. Therefore, transformer-less or Inductor-less topologies are introduced. These inverters are required to have minimum possible number of dc sources and low total standing voltage (TSV) for the semiconductors.

Hence, new converters were designed based on switched-capacitors structure [11]–[14] in order to increase the voltage levels but they suffers from high voltage stress on switching components. A generalized MLI is presented in [15] which has the ability of self-balancing and the voltage stress of all elements is equal to input dc source (except the output H-bridge inverter), but a high number of components are used. As shown in Fig. 1(a), Rodriguez and Leeb [16] presented an MLI based on unipolar Marx converter structure for inductively coupled power transfer. This switched-capacitor inverter has been extended to high-frequency applications at [17]. In this inverter, the voltage stress of all elements is equal to the input dc voltage (except the output H-bridge inverter). High switching frequency is used in this structure and multicarrier PWM technique is used as switching method. Proposed structure of [18] reduces the

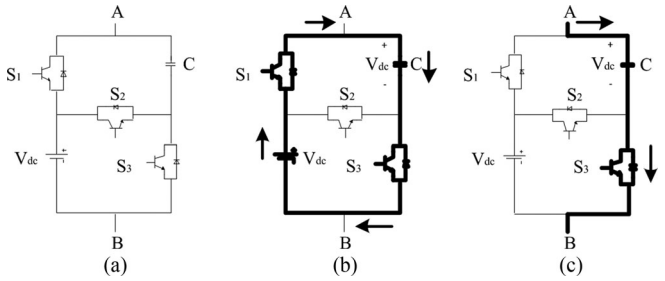

Fig. 2. Presented module in [17].

number of switches to one in each module which leads to reducing drivers and ease the control in comparison with other topologies. However, voltage stress of each switches increase by voltage level increment as well as increasing the number of series diodes. An MLI topology is presented in [19] based on cascaded connection of submultilevel units with reduced switching components. Moreover, MLI based on full-bridge inverter with the ability of self-balancing is presented in [20] but it suffers from high amount of TSV and peak inverse voltage (PIV) in higher levels [see Fig. 1(b)]. In [21], [22], boosting inverter is presented based on switched-capacitors in which an inductor is used in the converter input.

It is essential to consider that all of the above-mentioned structures require an H-bridge inverter at the end of the topology in order to achieve negative and zero voltage levels [23]. Due to application of four power switches, which have to withstand total load voltage, it leads to limitation on selection of semiconductors especially in higher output voltage. Since the requirement for high-voltage ac power supplies increases [24], a self-balanced MLI topology is introduced in this paper to achieve lowest possible TSV and PIV for switches with the capability of staircase multilevel bipolar voltage generation. All components in the proposed structure withstand voltage stress equal to the input dc voltage by eliminating the end-side H-bridge inverter. Four main step-up switched-capacitor multilevel inverters (SCMLIs) topologies are shown in Fig. 1.

In Section II, the general structure and performance of the proposed inverter are presented as well as investigation of different charging and discharging states. Modulation technique is brought in Section III. Section IV calculates capacitors, losses, and efficiency. A comparative study with other existing topologies is conducted in Section V. Laboratory test and simulation are carried out and the results are shown in Section VI to verify the inverter performance. Finally, conclusion of this paper is presented in Section VII.

II. Circuit Topology and Operating Principals

A. Unipolar Module

Fig. 2(a) shows the module of the switched-capacitor presented in [17]. Fig. 2(b) and (c) shows the charging and discharging states of the above module, respectively. However, this module is unipolar and just produces positive voltage.

By cascading mentioned modules, a unipolar MLI is created which needs a full-bridge inverter to create bipolar levels. The number of steps is considered as *n*, the TSV of this inverter is

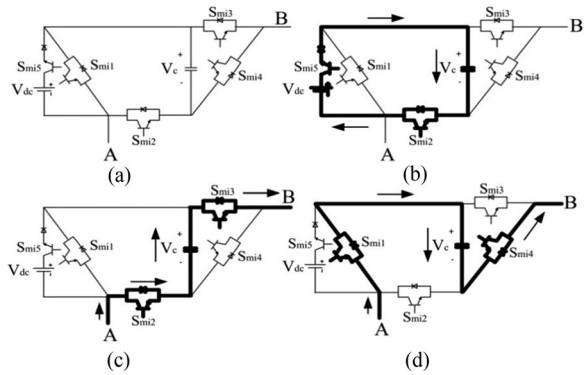

Fig. 3. (a) Proposed module, (b) its charging state, (c) discharging positive state, and (d) discharging negative state.

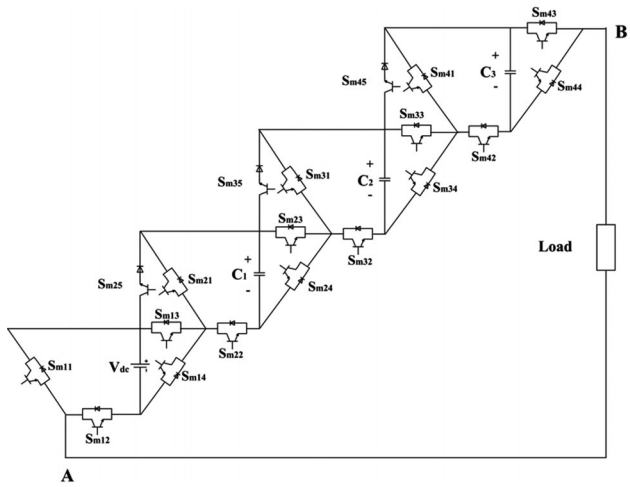

Fig. 4. Proposed switched-capacitor MLI.

obtained as

$$\mathrm{TSV} = (3(n-1) + 4n).V_{\mathrm{dc}} = (7n-3) \times V_{\mathrm{dc}}. \quad (1)$$

Voltage stress of all the components is $1V_{\mathrm{dc}}$ except four full-bridge switches that should tolerate the output ac voltage peak $(n.V_{\mathrm{dc}})$.

B. Proposed Bipolar Module

Fig. 3(a) shows the proposed basic module, which consists of five power switches per one capacitor. The input source in the above module can be fuel cell, PV panel, and batteries. As shown in Fig. 3(b), during charging state, $\mathrm{S_{mi2}}$ and $\mathrm{S_{mi5}}$ are in the ON-state, which connects the input source with the capacitors in parallel. Fig. 3(c) shows the discharging state of the capacitor, where $\mathrm{S_{mi2}}$ and $\mathrm{S_{mi3}}$ are in the ON-state and the output voltage is equal to $+V_{\mathrm{dc}}$. To generate the negative voltage level, as shown in Fig. 3(d), S_{mi1} and S_{mi4} are in the ON-state. It should be mentioned that (S_{mi1} and S_{mi2}) and (S_{mi3} and S_{mi4}) have to be turned ON and OFF complementary.

C. Proposed Switched-Capacitor Topology

Fig. 4 shows the proposed nine-level switched-capacitor structure, which is a cascaded version of bipolar modules of

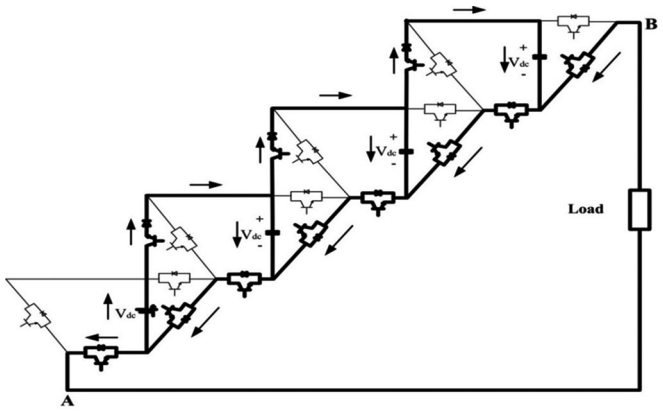

Fig. 5. Charging mode of the proposed SCMLI.

Fig. 3. Since the voltage stress of all the elements is $1V_{\rm dc}$, for a $(2n+1)$ levels output voltage, TSV is obtained as

$$\mathrm{TSV} = (5n-1).V_{\rm dc}. \tag{2}$$

D. Start-Up Mode

In the proposed switched-capacitor inverter, the capacitors are needed to be charged at first. All capacitors are charged in parallel with the dc input source. Fig. 5 shows the switching state for circuit start-up.

In the start-up mode, $S_{\rm mi2}$, $S_{\rm mi4}$, and $S_{\rm mi5}$ switches are in the ON-state and all capacitors are charged equal to $1V_{\rm dc}$, while the output voltage is zero. In the charging state of capacitors, the voltage drop occurs when switches and diodes are in the path. Capacitor's voltage during the charge state is as follows:

$$V_{C_{n\,(\rm charging)}}(t) = V_{{\rm input}_{C_n}} \cdot \left(1 - e^{-\frac{t}{\tau_{C_n}}}\right) \tag{3}$$

where $V_{{\rm input}_{C_n}}$ is the input voltage of capacitors and τ_{C_n} is the time constant of each capacitor. It is worth mentioning that the number of ON state switches or diodes and their ON-state resistant for different paths are not equal. So, capacitor's voltage during the charge state is obtained as following equations:

$$V_{C1\,(\rm charging)}(t) = [V_{\rm dc} - (2\,V_{\rm on,sw} + 2\,V_{{\rm on},D} + (2(R_{\rm on,sw} + R_{{\rm on},D}) + r_{C_1}).i_{C_{av_1}}] .(1 - e^{-\frac{t}{\left(2(R_{\rm on,sw}+R_{{\rm on},D})+r_{C_1}\right).C_1}}) \tag{4}$$

$$V_{C2\,(\rm charging)}(t) = [V_{\rm dc} - (4\,V_{\rm on,sw} + 4\,V_{{\rm on},D} + (4(R_{\rm on,sw} + R_{{\rm on},D}) + r_{C_2})i_{C_{av_2}})] .(1 - e^{-\frac{t}{\left(4(R_{\rm on,sw}+R_{{\rm on},D})+r_{C_2}\right).C_2}}) \tag{5}$$

$$V_{C3\,(\rm charging)}(t) = [V_{\rm dc} - (6\,V_{\rm on,sw} + 6\,V_{{\rm on},D} + (6(R_{\rm on,sw} + R_{{\rm on},D}) + r_{C_3}).i_{C_{av_3}})] .(1 - e^{-\frac{t}{\left(6(R_{\rm on,sw}+R_{{\rm on},D})+r_{C3}\right).C_3}}) \tag{6}$$

where $R_{\rm on,\,sw}$ represents the collector-emitter ON-state resistance, $R_{\rm on\,,D}$ is the antiparallel diode ON-state resistance,

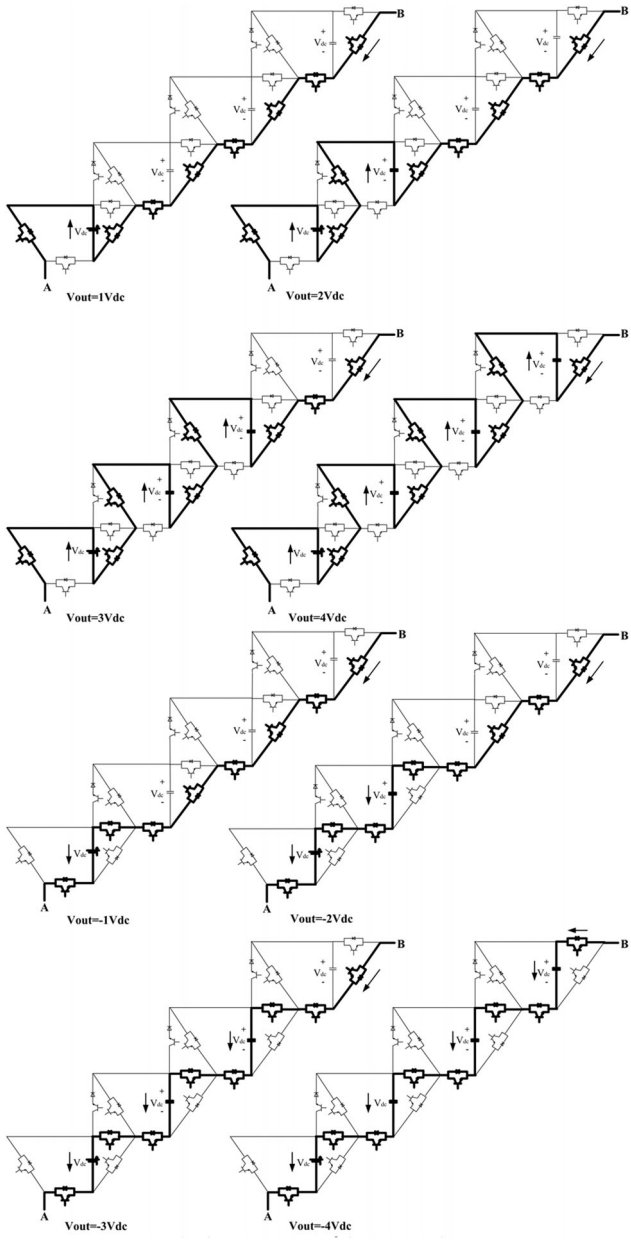

Fig. 6. Discharging states of the proposed inverter.

$V_{\rm on\,,\,sw}$ is the insulated gate bipolar transistor (IGBT) ON-state zero-current collector-emitter forward voltage drop, $V_{\rm on,\,D}$ is representing the ON-state zero-current forward voltage drop of anti-parallel diode, and r_C is ESR of the capacitors and $i_{\rm Cavi}$ is the average current of capacitors.

E. Multilevel Output Voltage Generation Mode

However, for producing the output voltage and creating the staircase waveform with the desired frequency and amplitude, the charged capacitors should be discharged in series in a way that different levels could be created. Because of simplicity and modularity of the proposed switched-capacitors inverter, staircase voltage production is possible by a very simple switching strategy. Fig. 6 shows discharging modes and staircase voltage

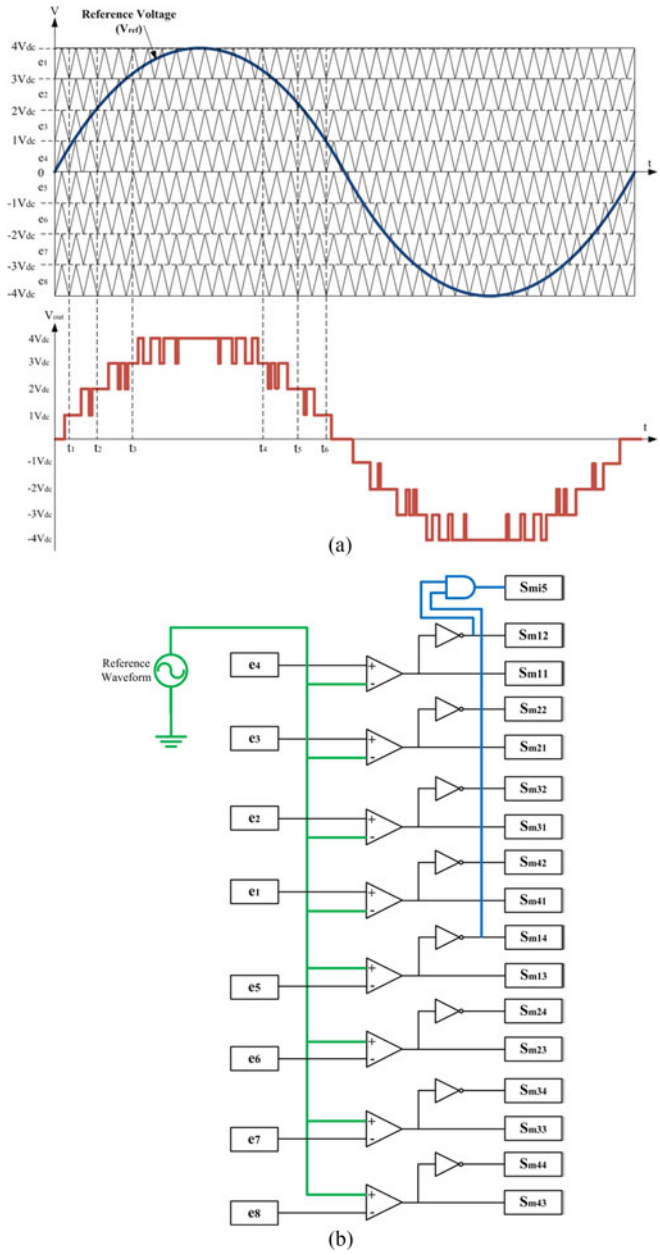

Fig. 7. (a) Carrier-based PWM modulation technique. (b) Logic modulating for the proposed MLI.

production. As it is clear from the figure, S_{mi2} and S_{mi3} (S_{mi1} and S_{mi4}) switches are in the ON-state to produce positive (negative) voltage levels. (S_{mi1} and S_{mi3}) or (S_{mi2} and S_{mi4}) switches would be turned ON for bypassing the capacitor of each module.

III. Modulation Strategy

As shown in Fig. 7, a carrier-based PWM method is used to control the proposed SCMLI in which eight triangular carrier signals are compared with a sinusoidal 50 Hz reference signal to generate required pulses for switches. According to this figure, e_1, e_2, e_3, and e_4 are triangular carriers for positive half-cycle of output voltage which generates the required switching pulses for S_{mi1} and S_{mi2}. Similarly, e_5, e_6, e_7, and e_8 are triangular carriers for negative half-cycle of output voltage which generates the required switching pulses for S_{mi3} and S_{mi4}. Also, S_{mi5} will be turned ON only when both S_{m12} and S_{m14} are in the ON-state. Table I illustrates the ON-state switches in each level.

IV. Calculation of Capacitance, Losses, and Efficiency

A. Determination of Capacitance

The capacitors calculation is one of the most important issues in the switched-capacitors converters to prevent the appearance of high-voltage ripples across capacitors. For a nine-level inverter (see Fig. 7), t_1, $t_2 \ldots t_6$ are calculated as follows [17]:

$$t_1 = \frac{\sin^{-1}\left(\frac{1}{4}\right)}{2\,\pi\,f_{\text{ref}}} \tag{7}$$

$$t_2 = \frac{\sin^{-1}\left(\frac{2}{4}\right)}{2\,\pi\,f_{\text{ref}}} \tag{8}$$

$$t_3 = \frac{\sin^{-1}\left(\frac{3}{4}\right)}{2\,\pi\,f_{\text{ref}}} \tag{9}$$

$$t_4 = \frac{\pi - \sin^{-1}\left(\frac{3}{4}\right)}{2\,\pi\,f_{\text{ref}}} \tag{10}$$

$$t_5 = \frac{\pi - \sin^{-1}\left(\frac{2}{4}\right)}{2\,\pi\,f_{\text{ref}}} \tag{11}$$

$$t_6 = \frac{\pi - \sin^{-1}\left(\frac{1}{4}\right)}{2\,\pi\,f_{\text{ref}}}. \tag{12}$$

The longest discharging times ($t_{x,i}$, t_{yi}) for each capacitor (C_1, C_2, and C_3) are (t_1, t_6), (t_2, t_5), and (t_3, t_4), respectively. Where $t_{x,i}$ and t_{yi} are the beginning and time of the longest discharging period of ith capacitor. Therefore, the maximum discharge amount of capacitors is obtained as

$$Q_{C_i} = \int_{t_{x,i}}^{t_{y,i}} I_{\text{load}}.\,\sin\left(2\pi f_{\text{ref}} t\right) dt. \tag{13}$$

The capacitor's capacity depends on the maximum flowing current and the longest discharging time on load. Considering k as a ripple ratio, the capacitance is calculated as the following equation:

$$C_i > \frac{Q_{C_i}}{k.\,V_{\text{dc}}}. \tag{14}$$

B. Calculation of Losses

Three types of losses are considered for the switched-capacitors converters, which include capacitors charging losses ($P_{\text{loss, cap}}$), switching losses (P_{sw}), and conduction losses (P_{cond}).

1) Capacitor Charging Loss: In the charging state of capacitors, losses of capacitor ripple (P_{cr}) occur due to voltage differences between the dc input and the voltage across capacitors. Capacitors voltage ripple is obtained by following equation

TABLE I
LIST OF ON-STATE SWITCHES IN EACH LEVELS

	ON-state switches	Output voltage
$V_{\rm ref} > e_1$	$S_{m11}, S_{m14}, S_{m21}, S_{m24}, S_{m31}, S_{m34}, S_{m41}, S_{m44}$	$4V_{dc}$
$e_1 \geq V_{\rm ref} > e_2$	$S_{m11}, S_{m14}, S_{m21}, S_{m24}, S_{m31}, S_{m34}, S_{m42}, S_{m44}$	$3V_{dc}$
$e_2 \geq V_{\rm ref} > e_3$	$S_{m11}, S_{m14}, S_{m21}, S_{m24}, S_{m32}, S_{m34}, S_{m42}, S_{m44}$	$2V_{dc}$
$e_3 \geq V_{\rm ref} > e_4$	$S_{m11}, S_{m14}, S_{m22}, S_{m24}, S_{m32}, S_{m34}, S_{m42}, S_{m44}$	$1V_{dc}$
$e_4 \geq V_{\rm ref} > e_5$	$S_{m12}, S_{m14}, S_{m22}, S_{m24}, S_{m25}, S_{m32}, S_{m34}, S_{m35}, S_{m42}, S_{m44}, S_{m45}$	0
$e_5 \geq V_{\rm ref} > e_6$	$S_{m12}, S_{m13}, S_{m22}, S_{m24}, S_{m32}, S_{m34}, S_{m42}, S_{m44}$	$-1V_{dc}$
$e_6 \geq V_{\rm ref} > e_7$	$S_{m12}, S_{m13}, S_{m22}, S_{m23}, S_{m32}, S_{m34}, S_{m42}, S_{m44}$	$-2V_{dc}$
$e_7 \geq V_{\rm ref} > e_8$	$S_{m12}, S_{m13}, S_{m22}, S_{m23}, S_{m32}, S_{m33}, S_{m42}, S_{m44}$	$-3V_{dc}$
$e_8 \geq V_{\rm ref}$	$S_{m12}, S_{m13}, S_{m22}, S_{m23}, S_{m32}, S_{m33}, S_{m42}, S_{m43}$	$-4V_{dc}$

[17]:

$$\Delta V_{Ci} = \frac{1}{C_i}\int_{t_{x,i}}^{t_{y,i}} i_{C_i}(t)\,dt \tag{15}$$

where $i_{\rm Ci}$ is the current passing from ith capacitor and $(t_{\rm x,i},\ t_{\rm y,i})$ are discharging time during series connection of capacitors according to Fig. 6. Therefore, capacitors ripple losses is obtained from the following equation [13]:

$$P_{C_{\rm ripple}} = \frac{f_{\rm ref}}{2}\sum_{i=1}^{3} C_i \Delta {V_{C_i}}^2. \tag{16}$$

Also, the additional losses happen by the internal resistance of capacitors $(r_{\rm C})$. The conduction losses of capacitors $(P_{\rm CC})$ and capacitor's total losses are calculated as

$$P_{\rm CC} = \left(\frac{2\pi f_{\rm ref}}{\pi}\right)\sum_{k=1}^{3}\int_{t_{x,i}}^{t_{y,i}} r_c . {i_{C_k}}^2 . dt \tag{17}$$

$$P_{\rm loss,cap} = P_{C_{\rm ripple}} + P_{\rm CC}. \tag{18}$$

2) Switching Losses: One of the most important sources of the power loss is switching losses which are generated due to switching delays that are intrinsic to the semiconductor devices. As shown in Fig. 8, in turn-ON process, at the end of delay time $(t_{\rm delay,\,on})$, the gate-emitter voltage $(V_{\rm GE})$ reaches to threshold voltage $(V_{\rm T})$ and the collector current $(I_{\rm D})$ starts increasing. In this case, collector-emitter voltage $(V_{\rm CE})$ starts decreasing. The operation in this state finishes when $V_{\rm CE}$ reaches to $V_{\rm on-state}$ which shows the end of turn-ON process. On the other hand, in the turn-OFF process, at the end of delay time $(t_{\rm delay,\,off})$ when $V_{\rm GE}$ reaches to $V_{\rm GE-sat}$, $I_{\rm D}$ starts decreasing and $V_{\rm CE}$ starts increasing. Because in turn-ON and turn-OFF processes, voltage and current do not instantaneously change, both of them can simultaneously have significant values, and their power can reach very high amounts. The loss during turning ON and OFF of the active switches is obtained as following equations [27]:

$$\begin{aligned} P_{{\rm sw},i({\rm ON})} &= f_s\int_0^{t_{\rm on}} V_{{\rm off-state},i}(t).\,i(t)\,dt \\ &= f_s\int_0^{t_{\rm on}}\left(-\frac{V_{{\rm off-state},i}}{t_{\rm on}}(t-t_{\rm on})\right)\left(\frac{I_{{\rm on-state1},i}}{t_{\rm on}}t\right)dt \\ &= \frac{1}{6}f_s\,V_{{\rm off-state},i}\,I_{{\rm on-state1},i}\,t_{\rm on} \end{aligned} \tag{19}$$

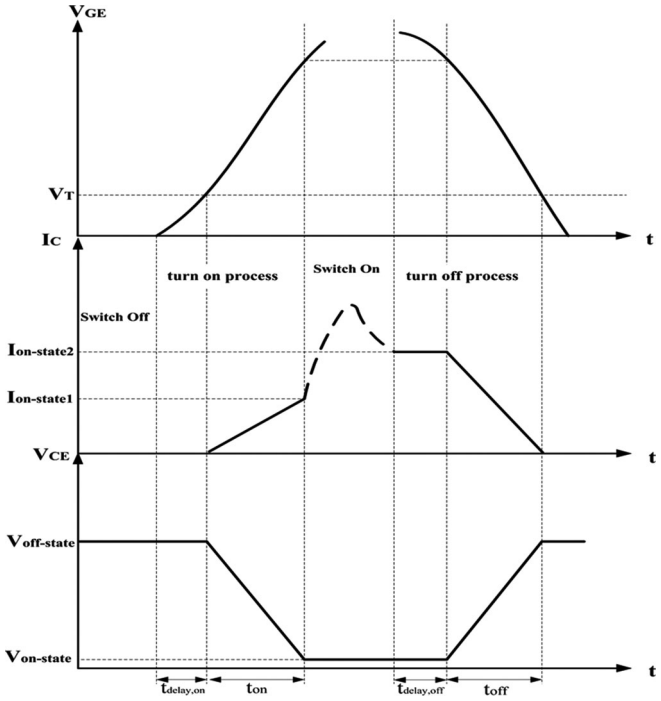

Fig. 8. Transient process of a power switch [27].

$$\begin{aligned} P_{{\rm sw},i({\rm OFF})} &= f_s\int_0^{t_{\rm off}} V_{{\rm off-state},i}(t).\,i(t)\,dt \\ &= f_s\int_0^{t_{\rm off}}\left(\frac{V_{{\rm off-state},i}}{t_{\rm off}}t\right)\left(-\frac{I_{{\rm off-state2},i}}{t_{\rm off}}(t-t_{\rm off})\right)dt \\ &= \frac{1}{6}f_s\,V_{{\rm off-state},i}\,I_{{\rm on-state2},i}\,t_{\rm off} \end{aligned} \tag{20}$$

where $V_{{\rm off-state},i}$ is the OFF-state voltage of the ith switch (equal to $1V_{\rm dc}$ in the proposed structure), $I_{{\rm on-state1},i}$ is the current of the ith switch when the switch becomes completely turned ON, and $I_{{\rm on-state2},i}$ is the current of the ith switch before the turn-OFF of the switch. f_s is the switching frequency that in the proposed structure is obtained as the following equation [17]:

$$f_{s,\,\rm on} = N_{S,\,\rm on}\cdot f_{\rm ref} \tag{21}$$

$$f_{s,\,\rm off} = N_{S,\,\rm off}\cdot f_{\rm ref}. \tag{22}$$

In the above equations, $N_{S,\,\mathrm{on}}$ and $N_{S,\,\mathrm{off}}$ are the number of turn ON and turn OFF of each switch and diode, respectively. $N_{S,\,\mathrm{on}}$ and $N_{S,\,\mathrm{off}}$ for switches of each module is calculated as following equations:

$$N_{S,\,\mathrm{on}} = \frac{t_{\mathrm{on,\,sw}}}{2\pi} \times N_t \times \frac{f_{\mathrm{sw}}}{f_{\mathrm{ref}}} \tag{23}$$

$$N_{S,\,\mathrm{off}} = \frac{t_{\mathrm{off,\,sw}}}{2\pi} \times N_t \times \frac{f_{\mathrm{sw}}}{f_{\mathrm{ref}}}. \tag{24}$$

In the above equations, $t_{\mathrm{on,\,sw}}$ is the time when the switch is ON and $t_{\mathrm{off,\,sw}}$ is the time when the switch is OFF, f_{sw} is the switching frequency and N_{t} is the total number of turn ON or OFF in each switching cycle which is 1 for the proposed structure. Therefore, switching losses is obtained from the relation (27)

$$P_{\mathrm{sw,\,total}} = \sum_{i=1}^{N_{\mathrm{switch}}} \left(\sum_{j=1}^{N_{\mathrm{on}(i)}} P_{\mathrm{sw,\,on}(ij)} + \sum_{i=1}^{N_{\mathrm{off}(i)}} P_{\mathrm{sw,\,off}(ij)} \right) \tag{25}$$

where $N_{\mathrm{on\,(i)}}$ and $N_{\mathrm{off\,(i)}}$ is the number of turn-ON and turn-OFF of the ith switch during one period and N_{switch} is the number of switches. According to the above equations, switching power loss is proportional to the value of the blocked voltage across the semiconductor devices, i.e., OFF-state voltage. Therefore, it is important to reduce this loss because it will be dissipated in the form of heat on the switch. In the proposed structure, all devices are switched when each of them tolerates $1V_{\mathrm{dc}}$. As a result, the switching losses of the proposed structure are very smaller than the conventional structures.

3) Conduction Losses: Conduction losses for the power switch and power diode is obtained from the following equations [25]:

$$P_{\mathrm{cond\,,\,sw}}(t) = V_{\mathrm{on,sw}} . i_{\mathrm{sw,\,avg}} + R_{\mathrm{on,\,sw}} . {i_{\mathrm{sw,rms}}}^2 \tag{26}$$

$$P_{\mathrm{cond\,,}\,D}(t) = V_{\mathrm{on},D} . i_{D,\,\mathrm{avg}} + R_{\mathrm{on,}\,D} . {i_{D,\mathrm{rms}}}^2 \tag{27}$$

where i_{rms} is the RMS current of semiconductors (switches and diodes) and i_{avg} is the average current of semiconductors. As shown in Fig. 6, there are some switches and diodes during discharging paths in each level that cause conduction losses. For steps $\pm(1,\,2,\,3,\,4)$. V_{dc}, the conduction losses are obtained as following equations:

$$P_{\mathrm{con\,,\,(1\,}V_{\mathrm{dc}})} = (5V_{\mathrm{on,sw}} . i_{\mathrm{load,\,avg}} + 5R_{\mathrm{on,sw}} . {i_{\mathrm{load,\,rms}}}^2) + (3V_{\mathrm{on},D} . i_{\mathrm{load,\,avg}} + 3R_{\mathrm{on},D} . {i_{\mathrm{load,\,rms}}}^2) \tag{28}$$

$$P_{\mathrm{con\,,\,(2\,}V_{\mathrm{dc}})} = (6V_{\mathrm{on,sw}} . i_{\mathrm{load,\,avg}} + 6R_{\mathrm{on,sw}} . {i_{\mathrm{load,\,rms}}}^2) + (2V_{\mathrm{on},D} . i_{\mathrm{load,\,avg}} + 2R_{\mathrm{on},D} . {i_{\mathrm{load,\,rms}}}^2) \tag{29}$$

$$P_{\mathrm{con\,,\,(3\,}V_{\mathrm{dc}})} = (7V_{\mathrm{on,sw}} . i_{\mathrm{load,\,avg}} + 7R_{\mathrm{on,sw}} . {i_{\mathrm{load,\,rms}}}^2) + (1V_{\mathrm{on},D} . i_{\mathrm{load,\,avg}} + 1R_{\mathrm{on},D} . {i_{\mathrm{load,\,rms}}}^2) \tag{30}$$

$$P_{\mathrm{con\,,\,(4\,}V_{\mathrm{dc}})} = (8V_{\mathrm{on,sw}} . i_{\mathrm{load,\,avg}} + 8R_{\mathrm{on,sw}} . {i_{\mathrm{load,\,rms}}}^2) \tag{31}$$

TABLE II
COMPARISON OF THE PROPOSED TOPOLOGY WITH SUGGESTED STRUCTURES IN [17], [18], [24], AND [26] FOR A $2n+1$ LEVEL OUTPUT

Comparing items	Fig .1 in [17]	Fig. 1 in [18]	Fig. 2 in [24]	Fig. 2 in [26]	Proposed
Electrolytic Capacitors	n–1	n–1	n–1	n–1	n–1
Number of Active Switches	$3n$+1	n+4	$2n$+4	$3n$+1	$5n$–1
Series diode	0	$2n$–2	$2n$–2	0	0
H-bridge's stress	$n\mathrm{V_{dc}}$	$n\mathrm{V_{dc}}$	$n\mathrm{V_{dc}}$	$n\mathrm{V_{dc}}$	No need
PIV	$n\mathrm{V_{dc}}$	$n\mathrm{V_{dc}}$	$n\mathrm{V_{dc}}$	$n\mathrm{V_{dc}}$	$1\mathrm{V_{dc}}$
TSV ($\times\mathrm{V_{dc}}$)	$7n-3$	n^2+4n	n^2+5n+1	$\frac{n^2}{2}+5n$	$5n-1$
Efficiency	88.36%	87.76%	86.67%	88.25%	91.7%

$$P_{\mathrm{con\,,\,(-1\,}V_{\mathrm{dc}})} = (3V_{\mathrm{on,sw}} . i_{\mathrm{load,\,avg}} + 3R_{\mathrm{on,sw}} . {i_{\mathrm{load,\,rms}}}^2) + (5V_{\mathrm{on},D} . i_{\mathrm{load,\,avg}} + 5R_{\mathrm{on},D} . {i_{\mathrm{load,\,rms}}}^2) \tag{32}$$

$$P_{\mathrm{con\,,\,(-2\,}V_{\mathrm{dc}})} = (2V_{\mathrm{on,sw}} . i_{\mathrm{load,\,avg}} + 2R_{\mathrm{on,sw}} . {i_{\mathrm{load,\,rms}}}^2) + (6V_{\mathrm{on},D} . i_{\mathrm{load,\,avg}} + 6R_{\mathrm{on},D} . {i_{\mathrm{load,\,rms}}}^2) \tag{33}$$

$$P_{\mathrm{con\,,\,(-3\,}V_{\mathrm{dc}})} = (1V_{\mathrm{on,sw}} . i_{\mathrm{load,\,avg}} + 1R_{\mathrm{on,sw}} . {i_{\mathrm{load,\,rms}}}^2) + (7V_{\mathrm{on},D} . i_{\mathrm{load,\,avg}} + 7R_{\mathrm{on},D} . {i_{\mathrm{load,\,rms}}}^2) \tag{34}$$

$$P_{\mathrm{con\,,\,(-4\,}V_{\mathrm{dc}})} = (8V_{\mathrm{on},D} . i_{\mathrm{load,\,avg}} + 8R_{\mathrm{on},D} . {i_{\mathrm{load,\,rms}}}^2). \tag{35}$$

As a result, total conduction loss is the sum of positive and negative steps and calculated as the following equation:

$$P_{\mathrm{con,total}} = P_{\mathrm{con,\,(1}V_{\mathrm{dc}})} + P_{\mathrm{con,\,(2}V_{\mathrm{dc}})} + P_{\mathrm{con,\,(3}V_{\mathrm{dc}})} + P_{\mathrm{con,\,(4}V_{\mathrm{dc}})} + P_{\mathrm{con,\,(-1}V_{\mathrm{dc}})} + P_{\mathrm{con,\,(-2}V_{\mathrm{dc}})} + P_{\mathrm{con,\,(-3}V_{\mathrm{dc}})} + P_{\mathrm{con,\,(-4}V_{\mathrm{dc}})}. \tag{36}$$

Finally, the efficiency can be achieved as

$$\eta = \left(\frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss}}} \right) \times 100 = \left(\frac{\frac{{V_{\mathrm{out(rms)}}}^2}{R_{\mathrm{load}}}}{\frac{{V_{\mathrm{out(rms)}}}^2}{R_{\mathrm{load}}} + (P_{\mathrm{sw}} + P_{\mathrm{cond}})} \right) \times 100. \tag{37}$$

V. COMPARATIVE STUDY

As shown in Table II, the proposed inverter is compared with the four well-known topologies for a $(2n+1)$ level or n steps. Compared with the structures of [17], [18], [24], and [26], the proposed MLI has higher number of switches, but TSV and PIV of the suggested inverter are remarkably lower than other structures (see Fig. 9). Since the proposed inverter does not use H-bridge inverter and provides $1V_{\mathrm{dc}}$ voltage stress on all components has a high chance to perform in medium and high powers and also high frequencies applications.

Moreover, comparison between the proposed SCMLI and others in efficiency point of view is carried out and the results show

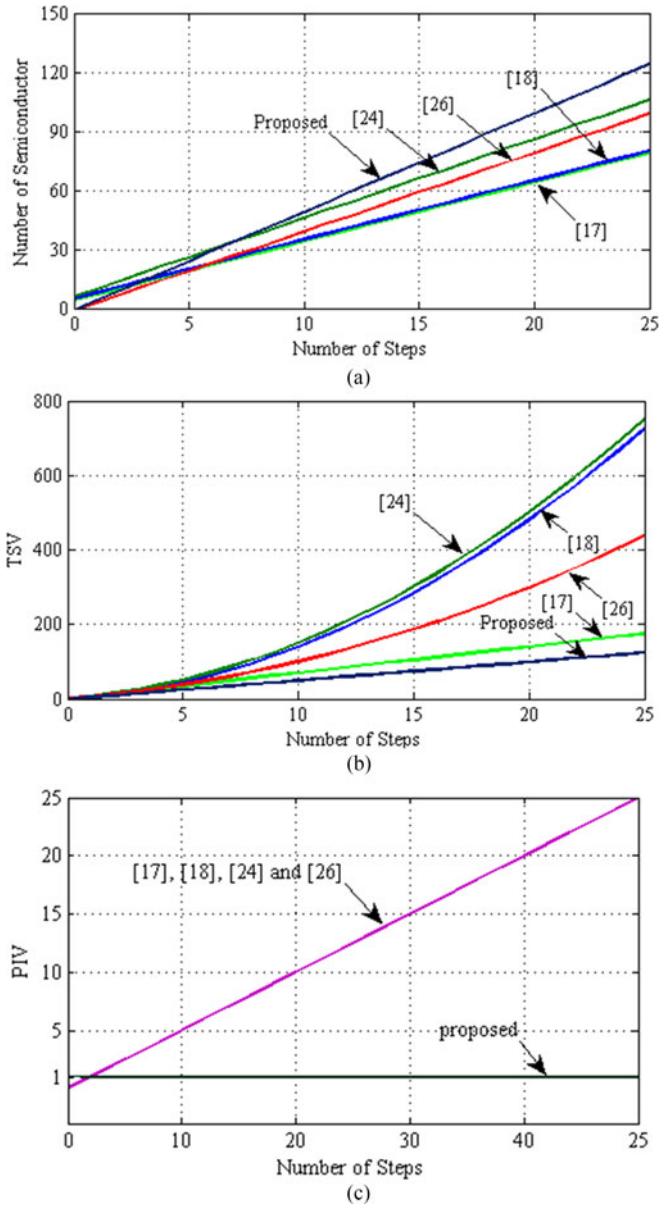

Fig. 9. Comparison diagram of the proposed topology with [17], [18], [24], and [26]. (a) Number of semiconductor, (b) TSV, (c) PIV.

that the proposed topology has better efficiency with the same characteristics. Note that for efficiency comparison, a case study with input voltage of 48 V, switching frequency of 2 KHz, boost ratio of 4 ($n = 4$), and load resistance of 100 Ω is considered for all topologies. Switches from international rectifier (IRF) MOSFET family (IRF520, IRF630, IRF634, and IRF740 for voltage ratings of 100, 200, 250, and 400 V) are used. Note that a 50% voltage rating margin is considered for the selection of switches. Detailed specifications of these switches can be extracted from their datasheets. Series diodes for other topologies are selected among MBR10100, MBR 10200, and APT30D30B. Using precise calculation of losses at previous section, efficiency values for all five topologies are calculated which is shown at Table II. Note that, cases with other parameters are also tried which leads to better performance of the proposed topology in terms of efficiency.

Generation of bipolar voltage levels is one of the advantages of the proposed circuit. As mentioned before, an H-bridge inverter is required at the end side of the traditional converters with the switches with PIV of $n \times V_{\rm dc}$. This adds $4n \times V_{\rm dc}$ to TSV of the circuit. This may be a drawback for the applications with higher dc input voltage. If the output voltage is very large, it will become very difficult to find appropriate power switches for an H-bridge inserted before the load at an acceptable price. In such applications, it will be preferable to have more low voltages rated power switches with their drivers in each switched-capacitor module. According to the analysis of this section, following issues can be concluded.

1) PIV of the proposed topology is $1V_{\rm dc}$ while other topologies need switches with more PIV. This is a benefit especially when the input voltage is high and consequently the rating of switches for H-bridge converter is very high.
2) In addition, selection of a topology depends on the constraints of customers. To explain this, a cost function (CF) is defined as follows to consider the effects of different constraint [19]

$$\begin{aligned} \mathrm{CF} &= N_{\rm semiconductor} + \alpha \,.\, {V_{\rm TSV}}^{pu} + \beta .\, {V_{\rm PIV}}^{pu} \\ &= N_{\rm semiconductor} + \alpha \,\frac{\rm TSV}{V_{\rm dc}} + \beta \frac{\rm PIV}{V_{\rm dc}} \end{aligned} \tag{38}$$

where α is the importance factor of TSV and β is the importance factor of PIV against the number of semiconductors. If TSV and PIV are more important than the number of semiconductors, so α and $\beta > 1$. If TSV and PIV are less important than the number of semiconductors, so α and $\beta < 1$. Fig. 10 shows the comparison between the proposed structure and others in view point of CF. As shown in this figure, the proposed SCMLI has less CF factor than other topologies in different conditions.

VI. Simulation and Experimental Results

A. Simulation Results

Parameters of Table III are used for simulation of the proposed nine-level inverter.

Fig. 11 shows the output voltage and current waveform of the proposed inverter for $R_{\rm load}$ with 50 Hz. Moreover, the proposed inverter has the potentiality of performance in high frequencies; Fig. 12 shows the output voltage waveform in 500 Hz with resistive load.

Also, Figs. 13 and 14 show the output voltage and current waveforms of the proposed inverter with R–L load in 50 and 500 Hz frequencies.

B. Experimental Results

At the implementation stage, features of Table IV are used for the verification of the circuit performance. At this stage, a nine-level is implemented, too. Fig. 15 presented a lab sample of the proposed circuit.

To control IGBTs (12n60a4), pulses are created by processor (DSP TMS320F28335) based on carrier-based PWM

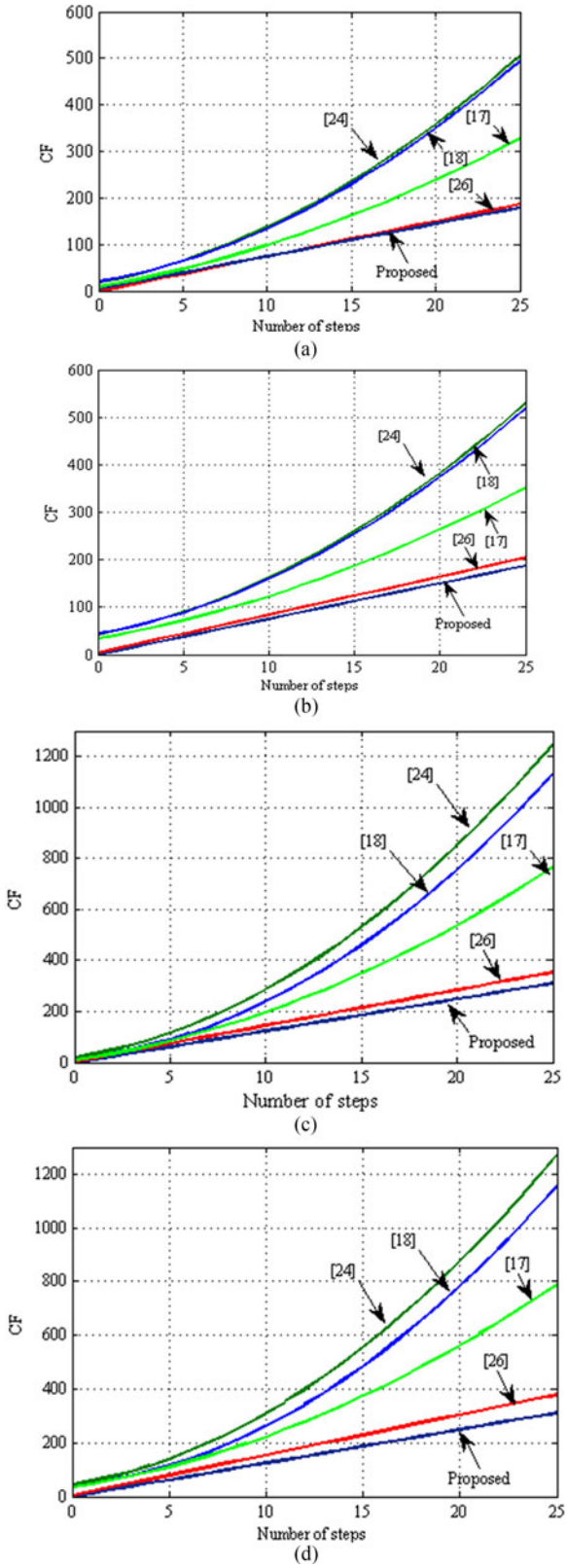

Fig. 10. CF factor versus number of steps for the proposed structure compared with [17], [18], [24], and [26]. (a) $\alpha = 0.5, \beta = 0.5$, (b) $\alpha = 1.5, \beta = 0.5$, (c) $\alpha = 0.5, \beta = 1.5$, (d) $\alpha = 1.5, \beta = 1.5$.

TABLE III
SIMULATION PARAMETERS

Input Voltage(V_{in})	100 V
Number of Output Voltage levels	9
Output Frequency	50 Hz, 500 Hz
Capacitors	4700 µf (refer to calculations of Section IV-A)
Resistive Load (R)	100Ω
Inductive-Resistive Load (R-L)for 50 Hz output	100Ω, 318.5 mH
Inductive-Resistive Load (R-L)for 500 Hz output	100Ω, 31.85 mH

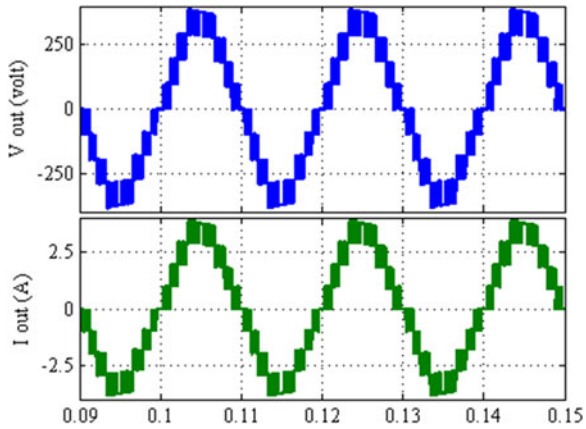

Fig. 11. Output voltage and current waveform in 50Hz frequency with R-load.

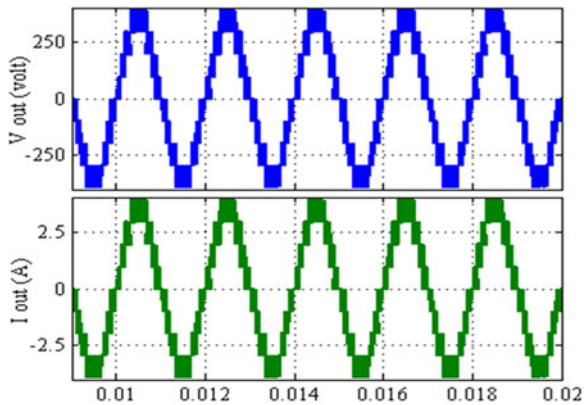

Fig. 12. Output voltage and current waveform in 500Hz frequency with R-load.

modulation technique. As shown in Fig. 16, these pulses (with amplitude of 3.3 V) have to be amplified by buffer IC 74HC244P. Required pulses for turning IGBTs have to be 18 V for ON-state and 0 V for OFF-state. Isolation is also required between power and control circuit which is done by a Driver/Optocoupler IC HCPL3120.

Fig. 17 shows the waveform of the output voltage of the nine-level inverter in 50 Hz. Note that THD for the proposed nine-level inverter is 15.02% and the measured efficiency is 88.93%. It is lower than the calculated values in Section IV. This is due to line impedance and using IGBT12N60 in hardware which

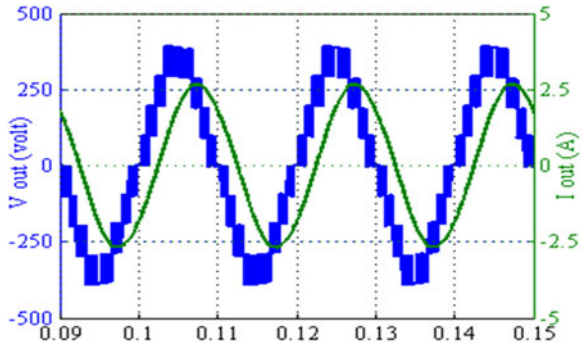

Fig. 13. Output voltage and current waveform in 50Hz frequency with R-L load.

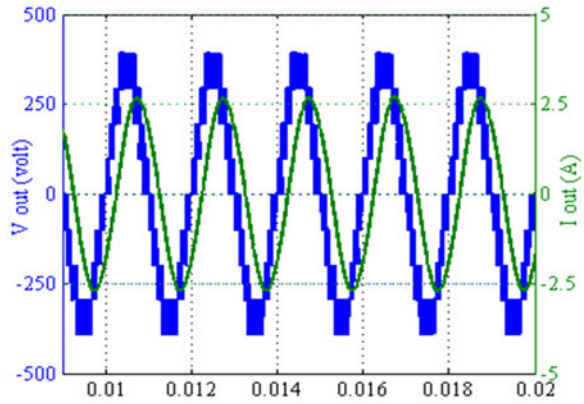

Fig. 14. Output voltage and current waveform in 500Hz frequency with R-L load.

TABLE IV
COMPONENTS OF THE NINE-LEVEL INVERTER

Input Voltage(V_{in})	48 Volts
Number of Output Voltage levels	9
Output Voltage Frequency	50 Hz and 1 KHz
Electrolyte Capacitors	4700 µF
Resistive Load (R)	250Ω
Inductive-Resistive Load (R-L)	100Ω, 100 mH
Diode	MUR860(600 V)
IGBT	12n60a4 (600 V)
Driver/Optocoupler	HCPL 3120
Processor	DSP TMS320F28335
Voltage probe	PINTEK DP- 50
Current probe	FLUKE 80i-110s ac/dc

were available in our laboratory. Note that using 12N60 IGBTs would decrease other topologies as well. Calculated efficiencies are for IRF family MOSFETs which has lower switching time and ON-state voltage. Fig. 18 shows the output voltage waveform at 1 KHz.

Moreover, voltage waveform and current waveform of the output in R–L load is shown in Fig. 19 which confirms the application of the proposed structure and its mentioned control strategy in different operating conditions.

As shown in Fig. 20, the load is changed between $R_{\mathrm{L}} = 100\ \Omega,\ 250\ \Omega$, and 100 KΩ. This result shows that the proposed

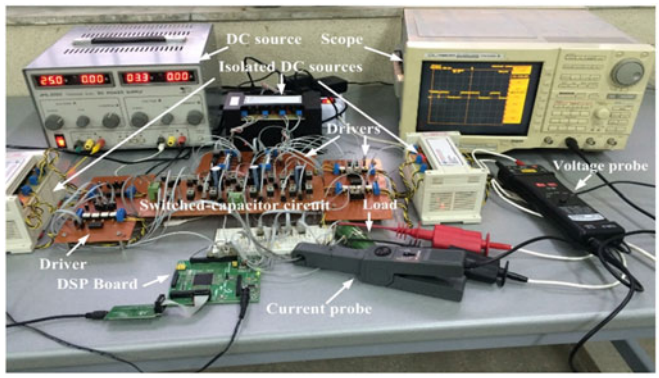

Fig. 15. Experimental test setup.

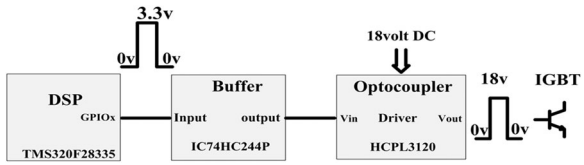

Fig. 16. Switching of an IGBT.

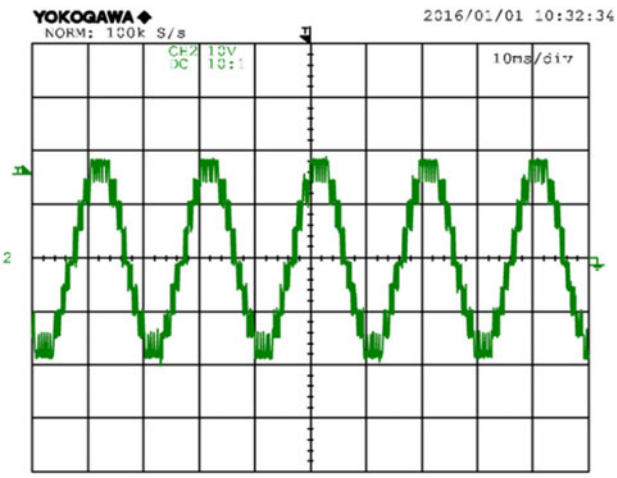

Fig. 17. Output voltage with R-load in 50Hz frequency (probe ×100).

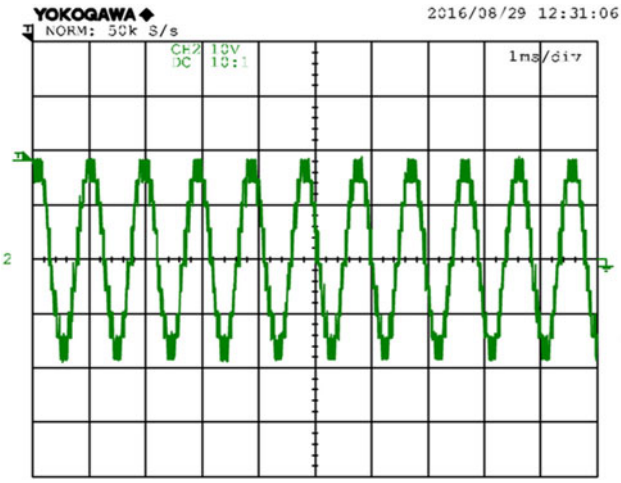

Fig. 18. Output voltage in R-load in 1 KHz frequency (probe ×100).

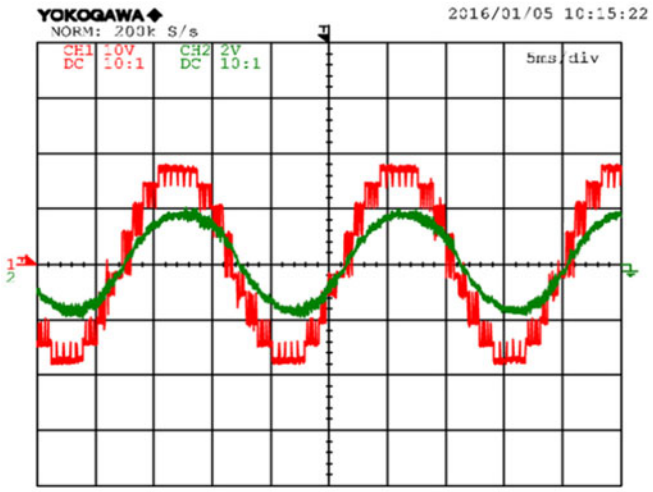

Fig. 19. Waveform of the output voltage and current in R-L load in 50 Hz frequency (voltage probe ×100 and current probe 100 mv/A).

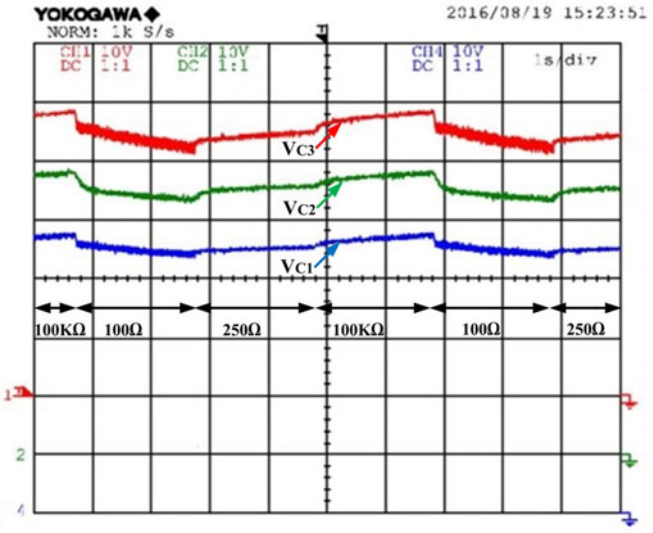

Fig. 20. Dynamic performance of capacitors in changing load.

structure can function in any dynamic condition and keeps its balancing states.

VII. Conclusion

A boost MLI is presented in this paper with the aim of reducing voltage stress on circuit components. A multimodule switched-capacitor network is presented in which by specific connection of the modules, a staircase multilevel voltage is generated. A comprehensive mathematical analysis of the proposed system is conducted to achieve capacitance values, calculation of losses, voltages of each capacitor. Investigation of the proposed nine-level SCMLI topology indicates that charging and discharging states of the proposed SCMLI topology is in a self-balanced manner. Losses calculation of the proposed SCMLI shows that the efficiency of the proposed converter is an acceptable value for this type of converters. A comparison between the proposed inverter and well-known circuits indicates that the proposed inverter has very low amount of TSV and PIV and all components tolerate the same voltage of $1V_{dc}$. Comprehensive simulation study and experimental results are presented to verify the analysis.

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