A Nonreversible 10-kW High Step-Up Converter Using a Multicell Boost Topology

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***Abstract*—The subject of this paper falls under the development of power electronics for more electric aircraft systems. The study concerns the design of a converter whose function is to generate a 300-V dc bus from a standard 28-V dc avionic network. Various systems, such as motor drives, need to be connected to the 28-V dc network. Their design could be simplified significantly, and standardized, by introducing this intermediate 28–300-V stage. The step-up converter in the proposed configuration is integrated as a part of the system. The power specification is 10 kW, which leads to very high-current values on the 28-V side. The choice of the converter topology, therefore, needs to match this central constraint. The proposed converter uses six boost cells, associated to constitute a series–parallel architecture. This arrangement leads to significantly more optimal sizing for high step-up ratios than conventional boost-cell configurations. Cell interconnection is implemented by means of a monolithic InterCell transformer to reduce the weight of the magnetic part. This paper describes the topology, design, and construction of the lab prototype, as well as experimental results obtained during testing.**

***Index Terms*—InterCell transformer, more electric aircraft, multicell boost converter.**

I. Introduction

THE 28-V dc networks installed in numerous types of aircraft for many years have been carried forward in the general specifications concerning future generations of civil aircraft [1]–[3]. Various electrical power systems are connected to this network, and they must be able to operate efficiently under such low voltage. This is very constraining in terms of design, especially for direct connections. This is particularly critical for power chains, such as motor drives [4]–[6]. One solution is to introduce an intermediate stage that performs a dc-to-dc step-up function, easier to optimize than the full chain. The converter described here corresponds to this option. The converter must generate a 300-V dc bus from the 28-V dc network to supply a 300-V power block comprised of an inverter and a permanent magnet synchronous motor, the latter being dedicated to driving a compressor.

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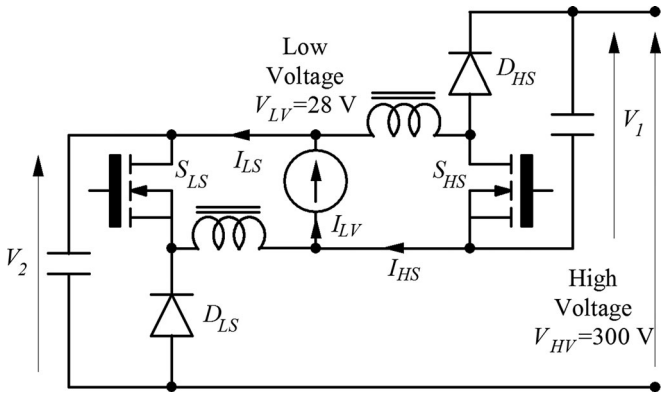


Fig. 1. Double-cell boost association.

This converter is not truly representative of a possible future step-up function embedded in aircraft. Rather, it was developed to conduct exploratory ground tests on a complete power chain. Therefore, galvanic insulation is not required for this lab supply. As such, the initial topology choice was oriented toward the conventional boost cell. The well-known intrinsic limitations of boost cells in cases involving a high step-up ratio (here, close to ten) have been stretched by associating six of these basic cells in a series–parallel assembly using a monolithic InterCell transformer.

The content of this paper focuses on describing the multicell architecture, prototype design, and implementation, followed by a presentation of experimental results.

II. Topology Presentation

A. First Step—Associating Two Boost Cells

The conventional boost cell is very simple, but also well known for its poor efficiency when the voltage step-up ratio is high, due to the combination of high-voltage and high-current stresses on the semiconductor devices. The first step in building the topology is to retain the double-cell association, called "double dual boost" in some publications [7]–[9], as shown in Fig. 1.

If the same duty cycle D is imposed on both cells, the average voltage values across the cells are the following:

$$V_1 = V_2 = \frac{V_{LV}}{1 - D}. \quad (1)$$

From which it can be deduced

$$V_{HV} = V_1 + V_2 - V_{LV} = \frac{1 + D}{1 - D} V_{LV}. \tag{2}$$

The voltage applied to each cell versus V_{HV} is

$$V_1 = V_2 = \frac{V_{HV}}{1 + D}. \tag{3}$$

The relations between the average currents are

$$I_{LV} = \frac{1 + D}{1 - D} I_{HV} \tag{4}$$

$$I_{LS} + I_{HS} = \frac{2}{1 + D} I_{LV}. \tag{5}$$

In case of current balancing on the input, it follows that

$$I_{LS} = I_{HS} = \frac{I_{LV}}{1 + D} \tag{6}$$

where

V_{LV}	input voltage (28-V dc supply);
V_{HV}	output voltage;
V_1 and V_2	floating output voltages of each cell;
I_{LV}	total input current delivered by the 28-V dc supply;
I_{LS} and I_{HS}	input current of each cell.
D	duty cycle.

For high values of the duty cycle D, therefore for high step-up ratios, the cell voltage is close to half of the output voltage value and, likewise, the input current value is close to half of the total input current value supplied by the 28-V source.

The main advantage of this association, compared to the standard series connection of two boost cells, is the symmetrical stress distribution that corresponds to series operation on the high-voltage side and to parallel operation on the low-voltage side.

B. Second Step: Associating 3 × 2 Cells and Interconnecting Using an Intercell Transformer

Despite improvements achieved by using the previous association, some significant limitations remain, such as the high-current value in each cell (close to 200 A for an output power of 10 kW) and the weight of input inductors.

Therefore, a second step in defining the topology was to extend the number of boost cells (3 × 2) to reduce cell current stress [10], which, at the same time, makes it possible to introduce a multiphase monolithic InterCell transformer to minimize the magnetic part. Fig. 2 shows the final topology obtained by associating three double cell described in the previous section. This total cell number was defined by identifying the optimal compromise between the number of power semiconductor devices and the InterCell transformer phase number, considering efficiency and weight (see Section III-A). In the final implementation, each symbolic MOSFET in the diagram above will be comprised of three parallelized MOSFETs (see Section III-A).

In this configuration, for a nominal output power of 10 kW, the theoretical average current value in each cell is 64.4 A, and the voltage value V_1 and V_2 across the cell is 164 V ($D = 0.829$).

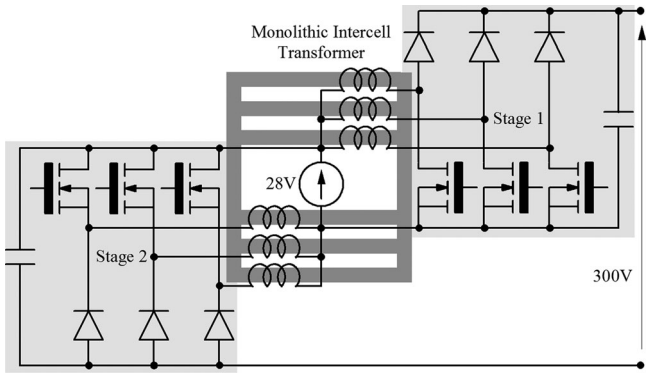


Fig. 2. Multicell topology.

The use of a monolithic InterCell transformer instead of separate inductors is justified by several interesting advantages that are emphasized strongly in [12] and [13]. The following section summarizes the main differences between both options that make the InterCell transformer more efficient.

1) Reduced Weight and Losses: The "InterCell transformer" function in a converter using *k* cells can be achieved by associating *k* separated transformers, with coupling provided by the particular winding arrangement, or by building a specific device with a customized magnetic core [13]. In this second configuration, which we chose in our case, the volume of the magnetic core is lower than the total volume of the *k* cores used in the separated transformer option.

Compared to the inductor solution, the origin of weight savings can be found mainly in the variable influence of the average currents on the magnetic operating conditions in both cases [14]. Fig. 3 and relations 7 to 14 highlight this essential feature.

In the inductor case, there is a direct link between the winding current and the induction created in the core.

The average and alternative components of the current generate, respectively, the average and alternative components of induction with the same relative scale (see relations 9 and 10 and top graph in Fig. 3). If the relative current ripple is weak, the core size depends mainly on the value of B_{DC}, and core losses are low.

Relations of the inductor case

$$\Delta i_{\mathrm{cell}} = \frac{D(1-D)V_{1,2}}{LF_{\mathrm{sw}}} \tag{7}$$

$$\Delta i_{\mathrm{cell}M}(D = 0.5) = \frac{V_{1,2}}{4LF_{\mathrm{sw}}} \tag{8}$$

$$B_{\mathrm{DC}} = \frac{L}{NA_c} I_{\mathrm{cell}} \tag{9}$$

$$\Delta B_M = \frac{L}{2NA_c} \Delta i_{\mathrm{cell}M} \tag{10}$$

where

I_{cell}	current average value per cell;
Δi_{cell}	peak-to-peak inductor current ripple in a boost cell versus the output voltage;
$\Delta i_{\mathrm{cell}M}$	maximal peak-to-peak current ripple per cell ($D = 0.5$);
k	number of cells;

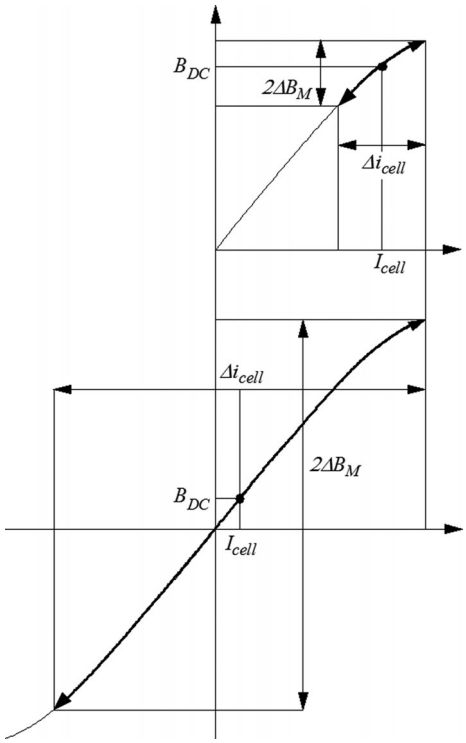


Fig. 3. Magnetic operating conditions.

$F_{\rm sw}$ switching frequency;
ΔB_M peak ac value of induction;
L inductor value in one cell;
A_c magnetic core area;
N number of turns.

In the InterCell transformer case, the average induction in the core also depends on the average current, but in combination with leakage inductors by phase (relation 13). The alternative induction component is imposed by the voltages applied to the windings, such as in a transformer (relation 14).

Relations of the InterCell transformer (ICT) case:

Due to interleaved mode operation combined with ICT behavior [15], the cell current ripple is now

$$\Delta i_{\rm cell} = [kD - q + 1]\,[q\ -\ kD]\,\frac{V_{1,2}}{k^2 L_{\rm ITphase} F_{\rm sw}} \qquad (11)$$

where

$L_{\rm ITphase}$ leakage inductor by phase;
q rank of each variation interval of D, such as $q - 1/k < D < q/k$ and $q = 1, 2, \ldots, k$, on which the periodic evolution of the ripple current versus D is repeated.

This current ripple is maximal periodically for $D = (2q - 1)/2k$

$$\Delta i_{\rm cellM} = \frac{V_{1,2}}{4k^2 L_{\rm ITphase} F_{\rm sw}} \qquad (12)$$

$$B_{\rm DC} = \frac{L_{\rm ITphase}}{N A_c} I_{\rm cell} \qquad (13)$$

$$\Delta B_M = \frac{V_{1,2}}{8 N A_c F_{\rm sw}} = \frac{k^2 L_{\rm ITphase}}{2\ N\ A_c} \Delta i_{\rm cellM}. \qquad (14)$$

By considering a given current ripple in the cells, the InterCell transformer requires a leakage inductor k^2 times lower than the cell inductor in the conventional solution. In addition, the average value of the induction generated in the core legs is $k^2/2$ times lower than the alternating component ΔB_M. Therefore, the InterCell transformer allows using all the magnetic characteristics of the core (see bottom graph in Fig. 3). This induces a significant decrease of the core section, and, therefore, of the core size as well as the winding size. In the end, this global size decrease leads to a total loss decrease.

2) Reducing the Cell Current Ripple: The design constraints mentioned above in the case of inductors generally leads to the choice of high-current ripples that could have a negative impact on the semiconductor device or capacitor sizing. The InterCell transformer is more flexible from this perspective. To provide a qualitative trend, a leakage inductor value of the InterCell transformer *n* times lower than the cell inductor value of the conventional solution leads to a decrease in the ratio *n* of the average induction as well as the cell current ripple.

3) Dynamic Behavior: The dynamic behavior of the boost converter depends directly on the value of the equivalent inductor seen by the low-voltage source. All others parameters being constant, lower is this value, the faster the intrinsic dynamic response of the converter. In the present case, the equivalent inductor is:

1) *L/k* for the inductor solution; and
2) $L_{\rm ITphase}/k$ for the InterCell transformer solution.

The previous sections have showed that the leakage inductor value could be significantly lower than the conventional inductor value; therefore, the equivalent inductor associated with the InterCell transformer could be lower in the same ratio.

III. Power Stage Design and Implementation

A. Choosing the Number of Cells

Generally speaking, determining the optimal choice for the number of cells in a multicell parallel converter is a difficult exercise. Degrees of freedom are limited by technical considerations. First, the choice of the double-cell boost assumes an even number of cells. To take full advantage of the InterCell transformer option regarding the limitation of magnetic fields in the magnetic core [12], the number of cells must be at least six. With these conditions, the number of cells can be $k = 6, 8, 10, 12, \ldots$

Conversely, a very high number of cells drastically increases complexity without significantly increasing performance. It was decided to limit the choice range to six or eight cells.

Before exploring various combinations to determine the best compromise, the switching frequency was imposed to simplify the approach. The justification for this is that the silicon MOSFETs that can be found in the standard 250-V family are the most appropriate devices, considering the cell voltage (164 V). The operating mode of the boost cell induces a high level of switching losses; therefore, the switching frequency $F_{\rm sw}$ must be limited. Some preliminary loss estimations were made on different 250-V MOSFETs by means of a switching loss model deduced from measurements made on a test bench dedicated to characterizing power semiconductor devices [16]. A value of 25 kHz was identified as a satisfying compromise.

TABLE I
ANALYSIS OF DIFFERENT COMBINATIONS OF SEMICONDUCTOR POWER DEVICES

N_{cell}	ND	NMOS	NT	Icell	Rdson at 150 °C	P_{on}	P_{sw_on}	P_{sw_off}	Total losses	Silicon efficiency
4	1	1	16	48.8 A	0.048	102.97 W	21.00 W	1.75 W	1006 W	**90.9%**
4	1	2	24	48.8 A	0.048	55.56 W	21.00 W	1.75 W	626 W	**94.1%**
3	1	3	24	65.1 A	0.048	67.49 W	30.00 W	2.58 W	600 W	**94.3%**

Ncell is the cell number, ND is the diode number per cell, NMOS is the number of parallelized MOSFETs per cell, NT is the total number of power devices, and Icell is the maximal current per cell for 28–300 V and 10-kW operation.

With the scope of analysis delimited by the previous restrictions, different parallel associations of 250-V MOSFETs and six- or eight-phase InterCell transformers were compared. The most powerful MOSFETs available in the 250-V family, and packaged in plastic cases that are easy to parallelize, were chosen (IRFP4768). The positive temperature coefficient of MOSFET R_{DSon}, added to the low characteristic dispersion resulting from the current process quality, enable parallel associations with a good current balance between the devices. To complete the boost cells, an ultrafast 300-V 60-A p-i-n diode was selected (STTH6003CW).

The most significant configurations analyzed (three or four cells per stage) are provided in Table I. Losses are evaluated in each case by using the switching loss model evoked previously. These results show that, in this context, the most appropriate option corresponds to three cells per stage, with three MOSFETs in parallel and one diode, that is, 12 devices per stage and 24 devices for the overall converter.

To complete the previous analysis, different InterCell transformer designs were implemented using a design tool developed specifically for these magnetic components and described in [17]. This tool includes an optimization procedure based on analytic models and verified by the finite-element simulation. For the given specifications, the main characteristics obtained for a six-phase InterCell transformer are the following:

1) ferrite core, aluminum windings;
2) weight, 1300 g;
3) losses close to 65 W;
4) maximal current ripple for kF_{sw} (150 kHz), 5 A;
5) temperature rise, 50 °C.

The other designs concern several variants of six- or eight-phase components and produced very similar results in term of volume, weight, and losses. Indeed, upgrading to eight-phase does not lead to a significant performance improvement. This observation, added to the results obtained on the semiconductor part, confirms the six-cell topology as an efficient option to implement the converter.

B. Thermal Management

The specification of the step-up converter imposed a forced-air cooling system. A specific design tool, based on methods widely described in publications [18], [19], was used to conduct this part of the design. The goal was to optimize an aluminum profile that takes full advantage of the thinnest fins that can be achieved with standard processes, i.e., 800 μm. The first design was made for one boost cell (three MOSFETs and one diode) with an estimated power dissipation of 120 W and a temperature rise on the heatsink of 25 °C. In that case, the junction temperatures are close to 100 °C with room temperature of 50 °C.

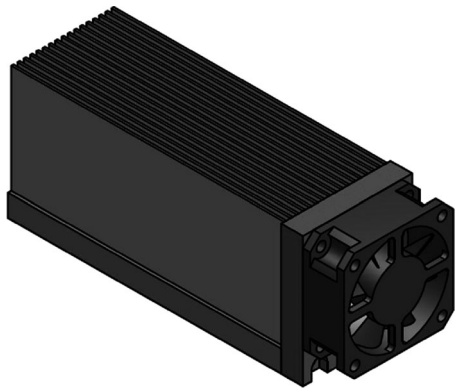


Fig. 4. Cooling profile shape.

The shape of the calculated profile is shown in Fig. 4. The theoretical characteristics are as follows:

1) dimensions: 40 × 40 × 100 mm;
2) thickness of the base plate: 8 mm;
3) number of fins: 17;
4) fin thickness: 800 μm;
5) space between fins: 1.5 mm;
6) weight: 233 g;
7) thermal resistance R_{TH}: 0.23 °C/W for an air speed of 8.5 m/s.

C. Converter Implementation

Implementation is organized around the two main parts that constitute the heatsink profiles and the monolithic InterCell transformer.

The low-voltage -connection boards, through which high-current flows and which support the voltage and current sensors, were also implemented with particular attention. A 3-D printed framework supports the various converter components.

Fig. 5 shows a general view of the converter drawn with a 3-D CAD tool. This implementation is not representative of a possible future converter to be embedded in an aircraft because it does not meet the corresponding strict requirements. Nonetheless, it has been oriented toward obtaining a compact and autonomous system that is easy to integrate in the overall conversion chain to be tested on ground.

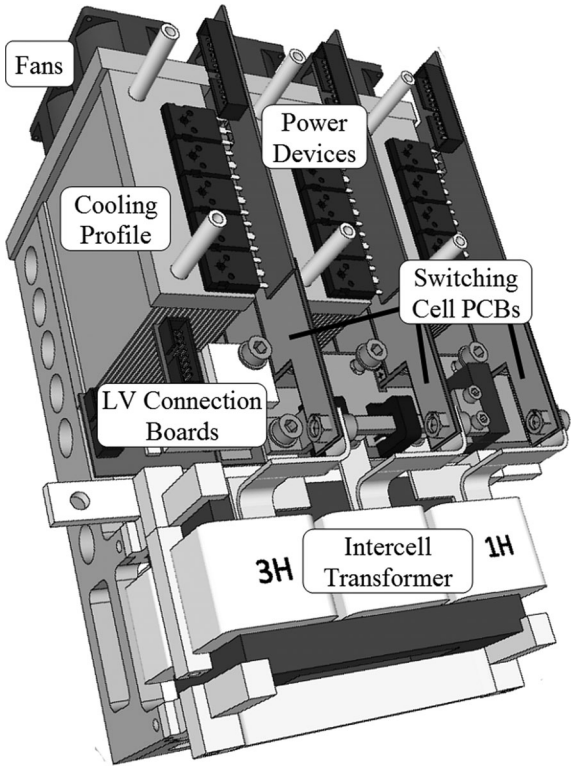


Fig. 5. Three-dimensional CAD image of the prototype.

1) Switching Cells: The switching cells are implemented by pair in accordance with Fig. 1.

The various components, decoupling capacitors, and semiconductor devices are interconnected by a power printed circuit board (PCB) (Cu thickness of 400 μm) and the latter are mounted on the heatsink described in the previous section. The decoupling capacitors are made by associating small-size ceramic capacitors. This option offers two advantages. These components are standard (multiple supply sources) and they offer great flexibility in terms of implementation. Their association allows building an efficient macrocapacitor (here, 64 μF to 250 V per cell with 32 capacitors on the HV side) with an adaptive global shape. Three identical blocks are placed in the framework to constitute the six-cell converter power stage.

2) InterCell Transformer: The monolithic InterCell transformer is made by assembling custom magnetic cores and bobbins [17]. For the magnetic cores, standard U and I ferrite cores were cut, machined, and glued to constitute two pieces. The first piece supports the six columns on which the bobbins are placed; the second piece is the top part closing the core. The windings are made with aluminum ribbon and their output connections are designed to be connected directly to the power PCBs. The various parts are held together by flanges fixed on the framework. Fig. 6 shows these different parts.

3) Low-Voltage Connection Boards: The connection boards correspond to the electrical nodes connected to the two poles of the low-voltage source.

The current flowing through each of these nodes reaches 200 A and the current measurements must be made on this part.

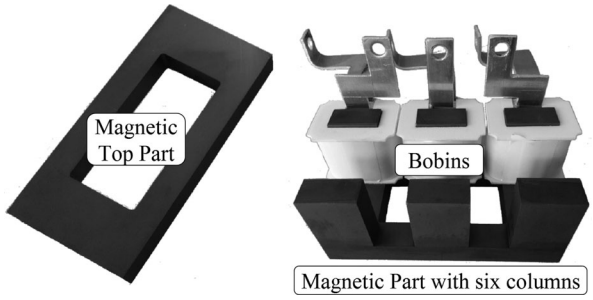


Fig. 6. InterCell transformer implementation.

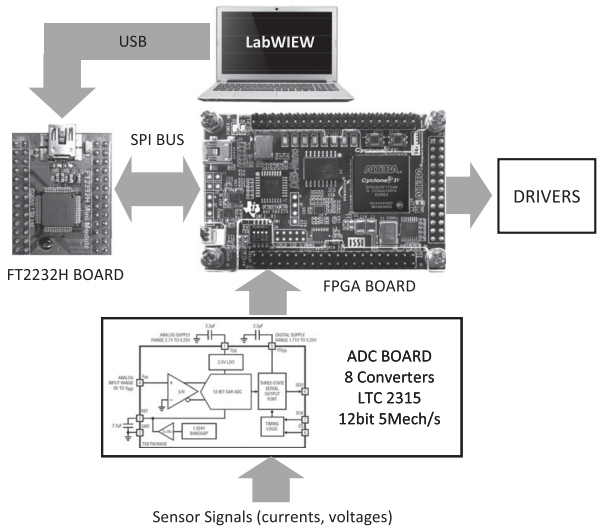


Fig. 7. Organization of the control board.

In addition, the low- and high-voltage terminals are placed on these boards. They are implemented with the same technology as the cell connection board, that is, with power PCBs that are fixed orthogonally to the cell blocks.

IV. Control and Regulation

The heart of the control section is an field-programmable gate array (FPGA) board that performs all functions, from pulse width modulation generation to regulation loops. This FPGA board is supported by a motherboard on which analog-to-digital converters are implemented to acquire the various parameters needed for regulations, plus a USB/SPI BUS interface and all the auxiliary power supplies. The sampling frequency is equal to $k.F_{\rm sw}$, that is, 150 kHz.

The parameters to be adjusted are controlled through a LabView interface that exchanges data with the field-programmable gate array (FPGA) board via the USB/SPI interface. Fig. 7 summarizes this organization.

The schematic in Fig. 8 shows the location of the sensors:

1) four differential current sensors (Hall effect sensor with two wires), two on each stage, are dedicated to regulate cell current balancing;
2) two conventional current sensors, one for each stage, are dedicated to regulate the total input current;
3) three voltage sensors directly provide a measurement of voltages V_{HV} and V_2 and, indirectly, a measurement of

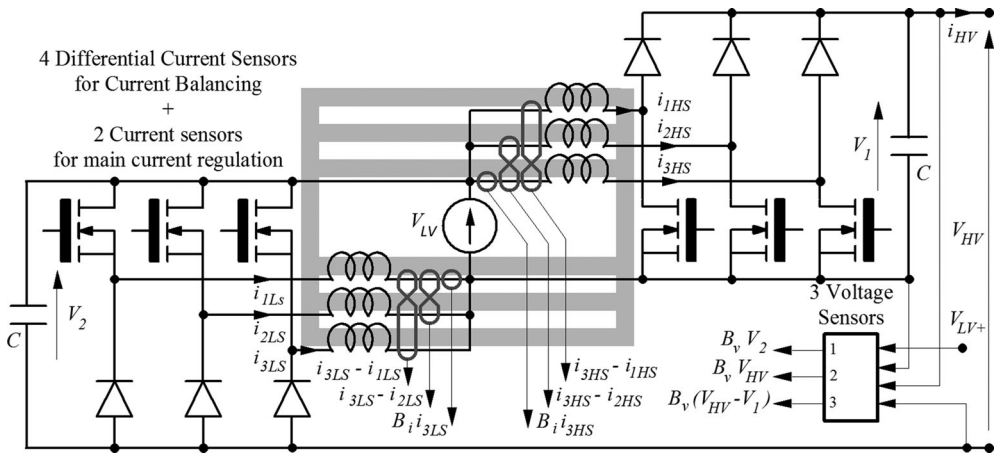
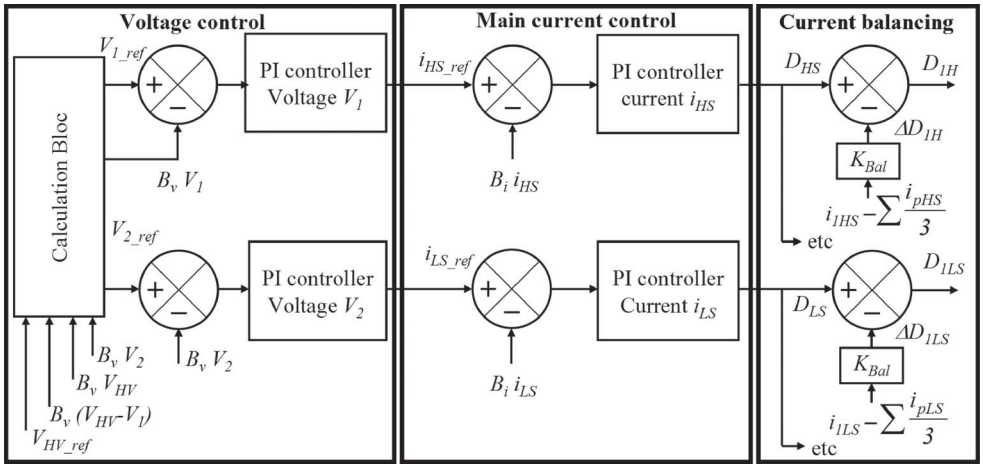
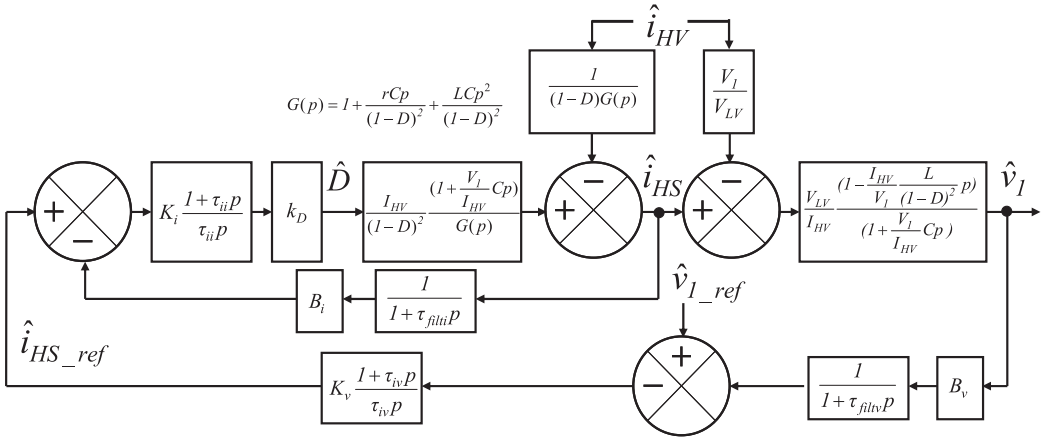


Fig. 8. Sensor location.



(a)



$\hat{x}$, small-signal component of variable x - X, average component of variable x

L, leakage inductance of ICT - C value of output capacitor – r, equivalent internal resistor of one stage

B_i, sensivity of current sensor - τ_{filti}, time constant of current measurement filtering

B_v, sensivity of voltage sensor - τ_{filtv}, time constant of voltage measurement filtering

K_i, proportional coefficient of current PI controller - τ_{ii}, time constant of current PI controller

K_v, proportional coefficient of voltage PI controller, τ_{iv}, time constant of voltage PI controller

(b)

Fig. 9. Current and voltage regulations. (a) Closed-loop arrangement. (b) Small-signal low-frequency model for one stage (example of HS).

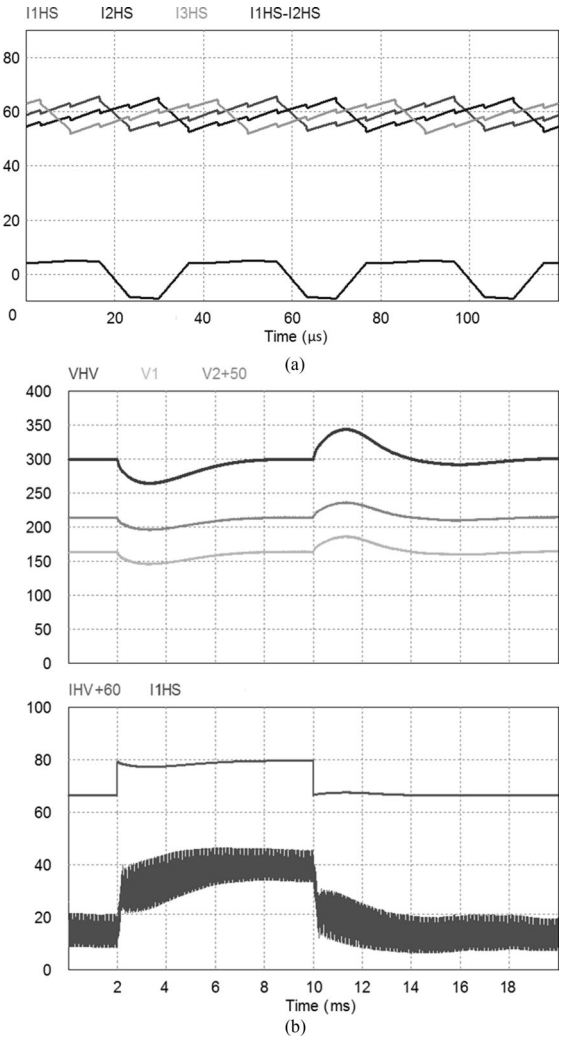


Fig. 10. Electrical simulations. (a) Current waveforms in steady state for 28 to 300 V and 9-kW operation. (b) Voltage and current waveforms for 2- to 6-kW output power step.

voltages V_1 and V_{LV}. This arrangement uses a common reference $(V_{HV}-)$ and was chosen to simplify sensor electronics (based on paired optocouplers).

Three regulation levels are implemented (see Fig. 9(a)). The first level includes four current-balancing loops; the second level, two input current loops; and the third level, two cell voltage loops that provide voltage balancing between the two stages as well regulation of the output voltage. All these closed loops are imbricated and include a PI controller, whose coefficients are adjustable via the LabView interface.

The following values can be calculated from the measurements delivered by the voltage sensors:

$$B_v V_{LV} = B_v V_2 - B_v (V_{HV} - V_1) \,(\text{sensors1 and 3})$$
$$B_v V_1 = B_v V_{HV} - B_v (V_{HV} - V_1) \,(\text{sensors2 and 3}).$$

The references of the floating voltages V_1 and V_2 are then calculated as follows:

$$V_{1\_\text{ref}} = V_{2\_\text{ref}} = (V_{HV\_\text{ref}} + B_v V_{LV})/2.$$

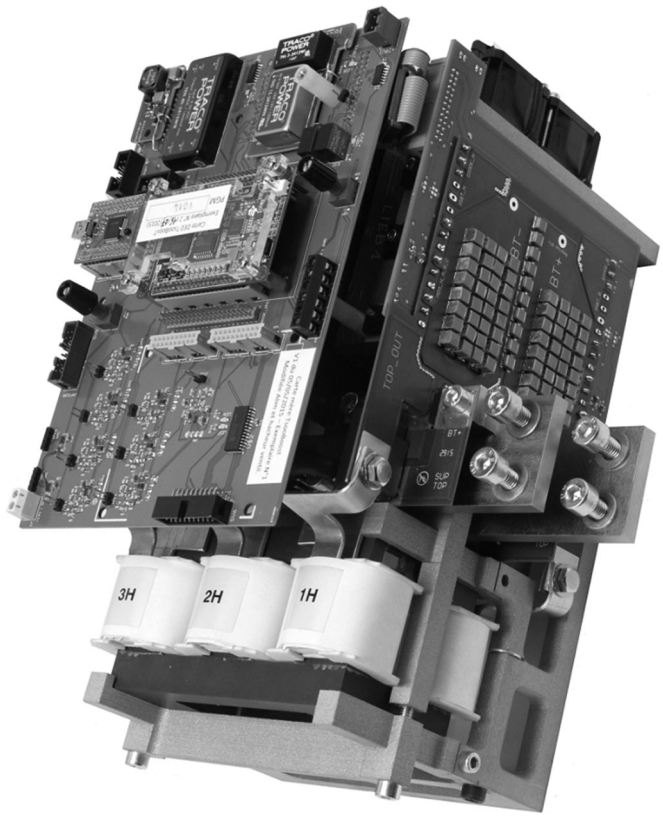


Fig. 11. View of the prototype

The small-signal block diagram in Fig. 9(b), available for one stage, was used to adjust the PI controllers [8], [10], [11]. Electrical simulations of the complete converter confirmed the validity of this block diagram. The current-balancing loops are not represented here because they do not influence the behavior of the other closed loops.

V. Simulations

Different electrical simulations were carried out to verify the electrical behavior of the complete converter (including regulation loops) on a resistive load.

Fig. 10(a) shows the current waveforms in a steady state for 9-kW operation, and shows the typical current ripple at kF_{sw} on the top curves (cell currents). The bottom curve is the differential current between two cells whose average value is maintained at zero by the balance regulation loop.

Fig. 10(b) shows some results on the dynamic behavior of the boost converter. A step load variation is generated by switching the value of the resistive load. This simulation shows the effect of the floating voltage-balance control, which maintains very similar the voltage values V_1 and V_2.

VI. Experimental Results

A prototype was implemented (see Fig. 11) in accordance with the 3-D image in Fig. 5. This prototype is autonomous: the energy needed for control is taken directly on the 28-V dc source, and auxiliary power management as well as programming is designed to permit direct starting under voltage.

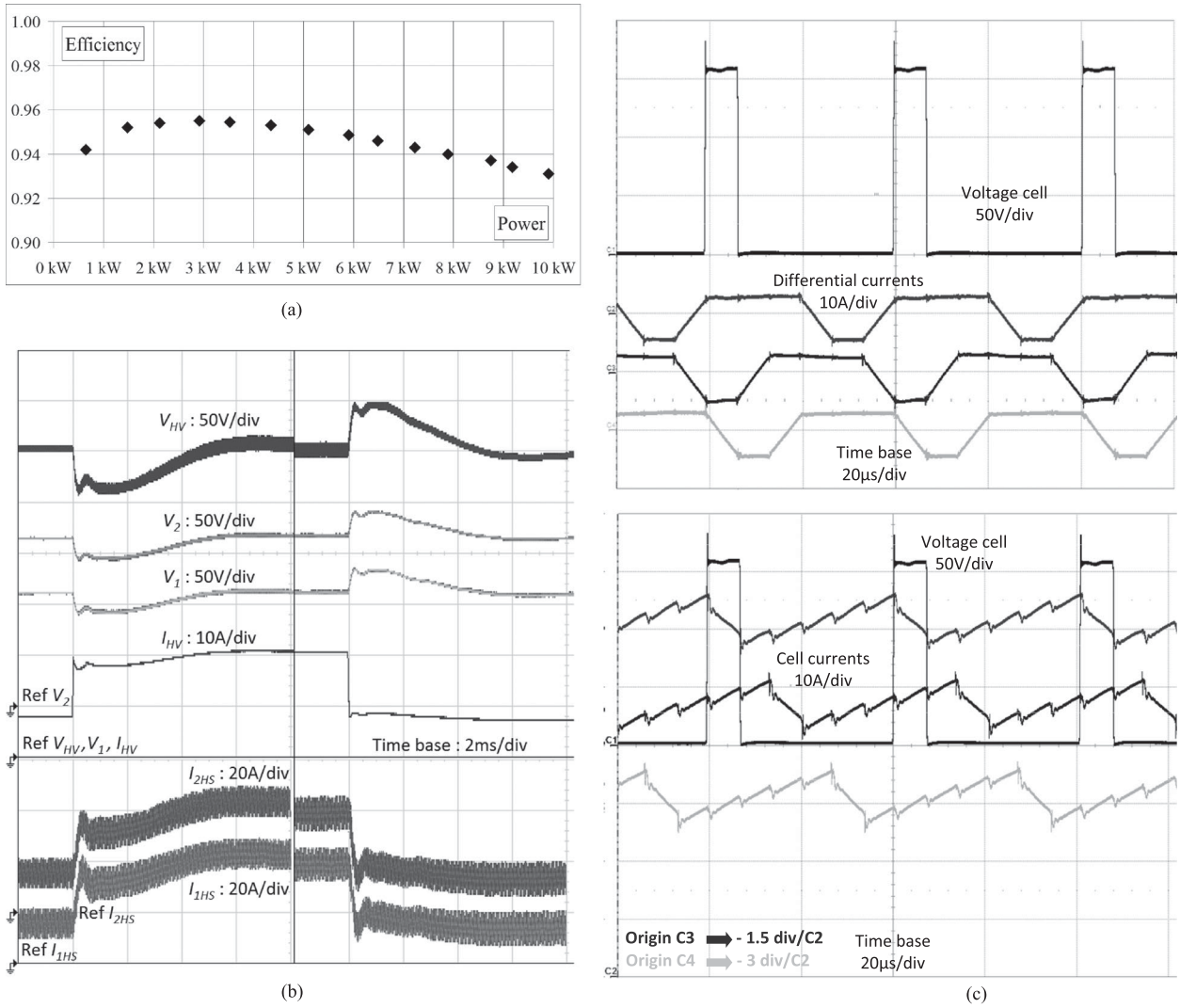


Fig. 12. Experimental results. (a) Efficiency versus output power for 28- to 300-V conversion. (b) Voltage and current waveforms for 2- to 6-kW output power step. (c) Current waveforms in steady state for 28 to 300 V and 9-kW operation.

At this time, the prototype has been tested under resistive load. Efficiency over the complete power range for 28- to 300-V operations is given in Fig. 12(a). The oscillograms in Fig. 12(c) call out some particularities of steady-state electrical operation. The upper oscillogram shows a cell voltage and three differential currents in one of the two stages. This oscillogram demonstrates the good accuracy of the balancing control based on differential current measurements. The imbalance between two cells is lower than 1 A for a nominal current of 65 A.

The lower oscillogram always shows a cell voltage as a reference and, in addition, the three cell currents of one of the two stages. For traces, C3 and C4, the references were shifted under the trace C1 reference (thus off the screen) to better show these cell currents. The shift values are indicated on the figure.

The current waveforms are typical of interleaved converters using InterCell transformers, that is, including a frequency component $F_{\rm sw}$ corresponding to the core magnetization and a frequency component $k.F_{\rm sw}$, due to intercell coupling. On this oscillogram, the component $F_{\rm sw}$ is higher than the component $k.F_{\rm sw}$ because of the air gap that exists between the two parts of the core, inducing a significant magnetizing current, an effect that is combined with a low value of the current ripple at $k.F_{\rm sw}$ due to the chosen operating point.

Finally, transient operation tests were performed by generating step variations of the resistive load between 2 and 6 kW. The results are given in Fig. 12(b). These results are close to simulation results and confirm the efficiency of the balance control concerning the floating voltages as well as the currents.

VII. Conclusion

This paper presents an example of advanced transfer based on technology combining multicell converters and InterCell transformers proposed by the authors. This solution has demonstrated its potential in various applications from around 100 W to 200 kW. The original boost converter described here is in the middle of that range. The topology remains simple and its characteristics are good, despite the use of a low-performance elementary cell.

If necessary, this converter could be improved by replacing the two-level cells by three- or four-level cells to use low-voltage devices much more efficiently. In that case, losses could be reduced, as well as the size of the InterCell transformer, because of the increase in the equivalent switching frequency.

REFERENCES

[1] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Trans. Transp. Electr.*, vol. 1, no. 1, pp. 54–64, Jun. 2015.

[2] X. Zhao, J. M. Guerrero, and X. Wu, "Review of aircraft electric power systems and architectures," in *Proc. 2014 Energy Conf.*, May 2014, pp. 949–953.

[3] S. Njoya Motapon, L.-A. Dessaint, and K. Al-Haddad, "A comparative study of energy management schemes for a fuel-cell hybrid emergency power system of more-electric aircraft," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1320–1334, Mar. 2014.

[4] R. Bojoi, M. G. Neacsu, and A. Tenconi, "Analysis and survey of multiphase power electronic converter topologies for the more electric aircraft applications," in *Proc. Int. Symp. Power Electron., Electr. Drives, Autom. Motion*, 2012, pp. 440–445.

[5] W. Cao, B. C. Mecrow, G. J. Atkinson, J. W. Bennett, and D. J. Atkinson, "Overview of electric motor technologies used for more electric aircraft," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3523–3531, Sep. 2012.

[6] F. Gao, S. Bozhko, G. Asher, P. Wheeler, and C. Patel, "An improved voltage compensation approach in a droop-controlled DC power system for the more electric aircraft," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7369–7383, Oct. 2016.

[7] D. B. Viet, Y. Lembeye, J.-P. Ferrieux, J. Barbaroux, and Y. Avenas, "New high power-high ratio non isolated DC-DC boost converter for fuel cell applications," in *Proc. Power Electron. Spec. Conf.*, 2006, pp. 1–7.

[8] F. S. Garcia, J. A. Pomilio, and G. Spiazzi, "Modeling and control design of the interleaved double dual boost converter" *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3283–3290, Aug. 2013.

[9] H. Hatsuyado and N. Hoshi, "A high boost ratio DC-DC converter for low voltage fuel cell," in *Proc. 3rd Int. Conf. Renew. Energy Res. Appl.*, Oct. 2014, pp. 674–679.

[10] F. S. Garcia, J. A. Pomilio, and G. Spiazzi, "Modeling and control design of the six-phase interleaved double dual boost converter," in *Proc. 9th 2010 IEEE/IAS Int. Conf. Ind. Appl.*, Nov. 2010, pp. 1–6.

[11] A. Amritha and A. Dinesh Pai, "A comparative study of controllers used for interleaved double dual boost converter," in *Proc. 2015 Int. Conf. Control, Commun. Comput.*, Nov. 2015, pp. 101–106.

[12] F. Forest, T. Meynard, E. Labouré, V. Costan, A. Cunière, and T. Martiré, "Optimization of the supply voltage system in interleaved converters using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 934–942, May 2007.

[13] E. Labouré, A. Cuniere, T. Meynard, F. Forest, and E. Sarraute, "A theoretical approach to InterCell transformers, application to interleaved converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 464–474, Jan. 2008.

[14] F. Forest, E. Labouré, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, Mar. 2009.

[15] F. Forest, T. Meynard, E. Labouré, V. Costan, and J.-J. Huselstein, "A multi-cell interleaved flyback using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1662–1671, Sep. 2007.

[16] J. Brandelero, B. Cougo, T. Meynard, and N. Videau, "A non-intrusive method for measuring switching losses of GaN power transistors," in *Proc. 2013 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2013, pp. 246–251.

[17] F. Forest, T. A. Meynard, J.-J. Huselstein, D. Flumian, C. Rizet, and A. Lacarnoy, "Design and characterization of an eight-phase-137-kW intercell transformer dedicated to multicell DC–DC stages in a modular UPS," *IEEE Trans. Power Electron.*, vol. 29, no. 1. pp. 45–55, Jan. 2014.

[18] J. R. Culham and Y. S. Muzychka, "Optimization of plate fin heat sinks using entropy generation minimization," *IEEE Trans. Compon. Packag. Technol.*, vol. 24, no. 2, pp. 159–165, 2001.

[19] U. Drofenik, A. Stupar, and J. W. Kolar, "Analysis of theoretical limits of forced-air cooling using advanced composite materials with high thermal conductivities," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 4, pp. 528–535, Apr. 2011.

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