A Modulation Compensation Scheme to Reduce Input Current Distortion in GaN-Based High Switching Frequency Three-Phase Three-Level Vienna-Type Rectifiers

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***Abstract*—Wide bandgap semiconductors are gradually being adopted in high power-density high efficiency applications, providing faster switching and lower loss, and at the same time imposing new challenges in control and hardware design. In this paper, a gallium nitride-based Vienna-type rectifier with SiC diodes is proposed to serve as the power factor correction stage in a high-density battery charger system targeting for aircraft applications with 800 Hz ac system and 600 V level dc link, where power quality is required according to DO160E standard. To meet the current harmonic requirement, PWM voltage distortion during the turn-off transient, is studied as the main harmonics contributor. The distortion mechanism caused by different junction capacitances of the switching devices is presented. A mitigation scheme considering the nonlinear voltage-dependent characteristics of these capacitances is proposed and then simplified from a pulse-based turn-off compensation method to a general modulation scheme. Simulation and experimental results with a 450 kHz Vienna-type rectifier demonstrate the performance of the proposed approach, showing a THD reduction from 10% to 3% with a relatively low-speed controller.**

***Index Terms*—Gallium nitride (GaN) HEMT, modulation compensation, three-phase rectifier, Power factor correction (PFC), turn-off transition.**

I. Introduction

THE input current distortion caused by transistor turn-off delay can be very problematic for converters with switching frequencies in the hundreds of kHz, especially in the vicinity of the phase current zero-crossing. It has been reported in [1] that this distortion in the Vienna-type rectifier is mainly due to the nonlinear output capacitance $C_{\rm oss}$ of the super-junction MOSFET, because the voltage rise time at turn-off can be quite long within a relatively short switching cycle. This leads to a significant voltage error at the converter ac terminal, as well as corresponding current harmonics through the input boost inductor.

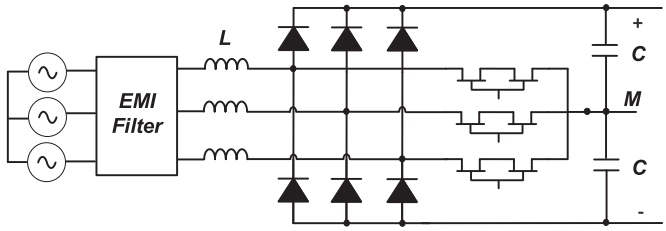

Fig. 1. Schematic of a GaN-based three-phase Vienna-type rectifier as a PFC converter.

The super-junction Si MOSFET has a particularly nonlinear output capacitance, with a steep dropoff of several orders of magnitude at 50–100 V. The turn-off voltage slew rate is initially very low until the drain-source voltage reaches that level. As a result, a significant turn-off delay and relatively short voltage rise time are observed. Hartmann *et al.* [1] proposed compensation for this nonlinear turn-off delay time through curve fitting of experimental data over the whole current range. However, for enhancement-mode (e-mode) gallium nitride (GaN) devices, the turn-off delay time is very short, and the voltage rise time is the dominant component of the turn-off time [2]–[4]. As a result, a new compensation scheme is needed, to avoid severe distortion near zero crossings due to the nonlinear voltage rise time in e-mode GaN. In the case of the Vienna-type rectifier as shown in Fig. 1, the output capacitance of two diodes also participates in the turn-off commutation of each GaN FET. Consequently, it is beneficial to find an analytical model to compensate for this nonlinear distortion, which can be adapted to different combinations of devices using their capacitance characteristic curves.

There have recently been several papers involving the relationship between slow turn-off transients and output capacitance, but their focus is on compensating the dead-time in voltage-fed motor drives [5]–[9] or on the overlap effect in current-fed rectifiers [13]. While most of the past work on dead-time compensation did not consider the nonlinear output capacitance, their basic schemes are still popularly adopted in recent literature. In [6]–[8], the dead-time distortion is treated

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as a voltage loss or voltage error, and this error is compensated to the voltage reference. In [9], the dead-time is modeled as a pulse error and compensated in each PWM period, and the idea is to extend or shrink the diode-clamping edge to cancel the voltage error introduced at the switching edge. Zhang and Xu [5] investigated the excessive compensation issue of the pulse-based method in motor drive applications, when considering the impact from the snubber capacitance of each IGBT module, and then corrected the dead-time compensation by comparing the actual PWM voltage and ideal voltage on both the falling edge and rising edge. In this way, an equivalent volt-second area can be achieved by adjusting the diode-clamping intervals on both edges. Bedetti *et al.* [6] extended the voltage loss compensation scheme by considering a more detailed device model and adding an offline identification of key parameters in motor drive applications. Li *et al.* [10] also adopted the voltage loss compensation scheme but further compensated the dual edges of the critical switching cycle around both zero crossing points of the ripple current. This method requires instantaneous current measurement based on the inductor voltage, introducing extra hardware, and complexity. Though the voltage loss approach avoids adjusting the turning on/off edge in each switching cycle, this paper finds an insufficient compensation on the duty cycle when considering the device output capacitance.

There are also several papers proposing to regulate the dead-time induced harmonics, using feedback controls [11], [12]. However, these methods require high control bandwidth and a sophisticated controller, and are more applicable when the fundamental frequency and switching frequency are relatively low, such as in industrial motor drives. Nevertheless, converters, switching at hundreds of kHz generally require much higher computation speed. With a limited computation capability in a typical DSP controller, feedforward compensation schemes are more appealing.

It is also important to point out the difference between dead-time in the normal half-bridge converters and turn-off delay in Vienna-type rectifiers. For dead-time related voltage distortion, the voltage error only occurs within a fixed dead-time interval, and the distortion can be determined with a voltage error versus phase current curve [6]. However, for the turn-off distortion in Vienna-type converters, the duration is not fixed. Instead, it occupies a varying percentage of the switching cycle, due to the $C_{\rm oss}$ limited commutation of phase current from the main switch to the diode. As a result, the voltage distortion is determined by both the instantaneous current and the instantaneous duty cycle, thus, presenting more challenges.

In this paper, the voltage distortion mechanism is analytically modeled and a compensation method is proposed for Vienna-type rectifiers. The paper is organized as follows. The turn-off timing of GaN devices and the associated voltage distortion mechanism are presented in Section II. The feedforward compensation scheme is presented in Section III, including the basic compensation principle, the instantaneous compensation formula, and the improved generalized modulation compensation formula. The compensation error associated with another scheme is also investigated. Parameter determination and the relations to voltage and current distortion are then covered. Simulation and experimental results are described in Sections IV and V, respectively. Section VI concludes the main findings of the paper.

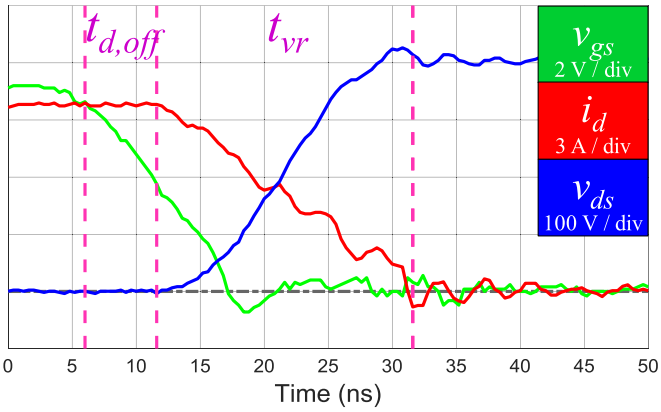


Fig. 2. Turn-off waveforms of a DPT of GaN GS66508P @ 400 V dc.

II. Voltage Distortion Introduced by Output Capacitance During Turn-Off

A. Turn-Off Transient of a GaN Device

The gate driver for a GaN device should be as fast as possible to fully utilize the GaN device's fast switching capability and reduce switching loss. As such, the turn-on transient time is mainly determined by the applied gate voltage, gate resistance, and the gate driver's rising speed and maximum source current.

However, even with a fast gate driver, the turn-off transient is also strongly affected by the load current. The turn-off transient of a GaN device can be divided into three stages. The first stage is turn-off delay, where the gate voltage is falling to the Miller voltage, the channel is still operating in the ohmic region, and the channel resistance is approximately $R_{\rm ds\_on}$. During this time, the drain-source voltage $v_{\rm ds}$ is near zero. The duration $t_{d,\rm off}$ is typically very small, and no switching loss occurs during this time. The second stage is the channel turn-off time, where the gate voltage v_{gs} falls from $V_{\rm Miller}$ to the threshold voltage $V_{\rm th}$. The duration is determined mainly by the gate driver speed. During this time, some of the load currents flows through the device's channel, operating in the lossy saturation region, and the remainder of the load current acts to displace charge in the output capacitances of both complementary devices. The third stage is the $C_{\rm oss}$ charge displacement time, where the device's channel is fully off, and the entire load current is used to displace charge in the $C_{\rm oss}$ of both complementary devices in the circuit. No overlap losses occur during this time, and all apparent energy loss is actually stored in the device's output capacitance until its next turn-on transient occurs. Because this interval is not controlled by the gate driver, it is determined solely by the relationship $dv_{\rm ds}/dt = i/C_{\rm oss}$. Furthermore, since $C_{\rm oss}$ drops nonlinearly as drain-source voltage increases, analysis of the voltage slew rage during this interval can be quite complex.

In order to evaluate the turn-off time distribution for the adopted 30 A//650 V GaN device GS66508P, a sweep of double pulse tests was performed across a range of operating conditions. Fig. 2 shows a typical turn-off transition with 10 A, and

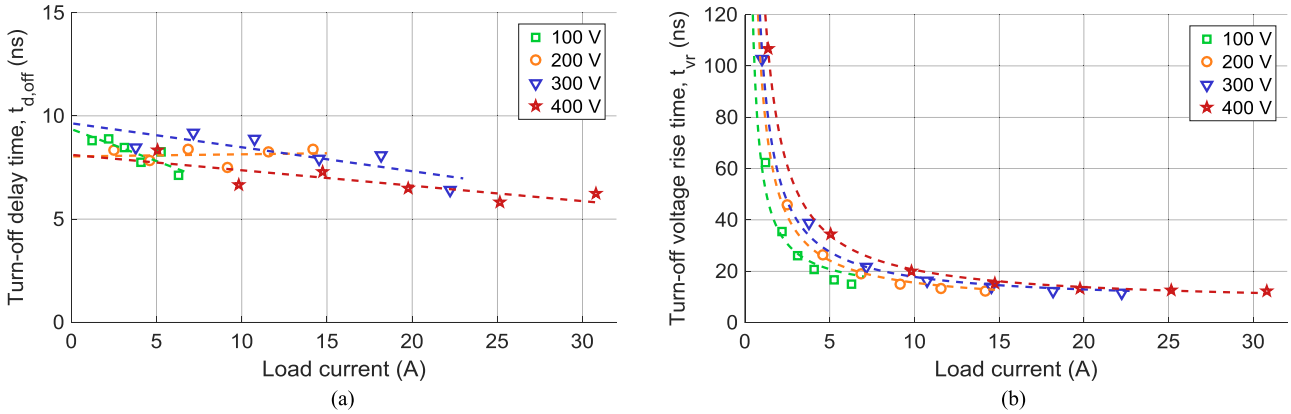


Fig. 3. Turn-off transient duration from DPT results of GaN Systems GS55608P, at different current and voltage conditions. (a) Turn-off delay time and (b) turn-off current voltage rise time.

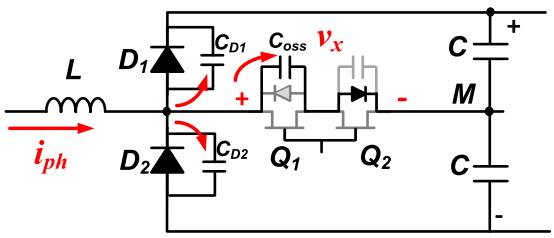


Fig. 4. Charging paths of output capacitances during turn-off for one phase-leg of Vienna-type PWM rectifiers.

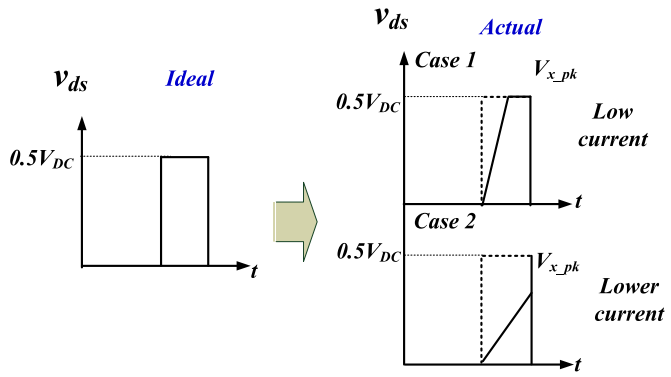


Fig. 5. Ideal and actual PWM voltage shape during turn-off transient.

400 V. As shown, the first interval $t_{d,\mathrm{off}}$ is only about 7 ns, whereas the second interval is not easily distinguished from the third, thus t_{vr} is used to denote this entire voltage rising interval. The duration of these simplified two stages under different load currents and voltages are provided in Fig. 3. Fig. 3(a) shows that the turn-off delay interval is less than 10 ns and is slightly reduced when current increases. Fig. 3(b) indicates a strong inverse relationship between load current and voltage rise time at any blocking voltages.

B. Voltage Distortion During Turn-Off

Fig. 4 shows a phase-leg of a Vienna-type rectifier, consisting of 650 V e-mode GaN devices Q_1, Q_2, and 1200 V SiC diodes D_1 and D_2, with a positive half line cycle illustrated. During the turn-off transient, the Q_1 channel is fully shut off after a short time interval. Then, the input phase current charges the C_{oss} of Q_1 from 0 V to $V_{\mathrm{dc}}/2$, meanwhile the top diode capacitor C_{D1} is discharged from $V_{\mathrm{dc}}/2$ to 0 V. It is worth mentioning that although the bottom diode D_2 does not participate in the current commutation during each half line cycle, its output capacitance is indeed charged up from $V_{\mathrm{dc}}/2$ to V_{dc}. And since all of this charge is supplied by the input current, the voltage rise time can be very long when the current is less than 6 A, especially in the zero crossing regions. Consequently, the terminal voltage of the phase-leg is affected, which causes the input current distortion.

III. Analysis of Proposed Turn-Off Compensation Scheme

A. Basic Compensation Principle

The terminal voltage distortion due to the relatively long turn-off transient cycle can be treated as a voltage loss compared to the ideal PWM voltage. Since the average of the ideal PWM voltage over one switching cycle represents the desired output voltage, a basic compensation scheme would be reshaping the actual PWM voltage so that it has the same average value as the ideal case, (i.e., the same volt-seconds over one switching cycle). This voltage error can be compensated as a pure time delay ($t_{d\_\mathrm{off}} + 0.5\,\mathrm{t_{vr}}$ obtained from a series of experimental data), as in [1], or as the approach to be described in Section III-B. But they become less effective near the zero crossing, when the device does not reach its full blocking voltage during the compensated duty cycle. An analytical approach is, therefore, proposed in this section to accurately and conveniently model and compensate this distortion.

As shown in Fig. 5, the actual PWM voltage patterns during turn-off are divided into two groups based on the relationship between the peak terminal voltage V_{x_pk} and $0.5V_{\mathrm{dc}}$, where the dashed line denotes the desired ideal PWM voltage shape and the solid line represents the actual PWM voltage shape. Clearly, this deviation 'voltage error if the PWM is not compensated. From

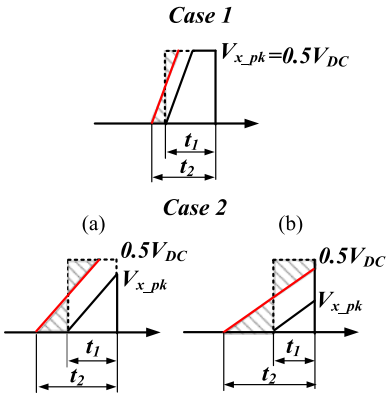


Fig. 6. Two voltage distortion cases associated with different current level and the proposed turn-off compensation scheme considering the voltage shape before and after compensation. The dashed line shows the ideal PWM voltage, the solid black line shows the actual uncompensated turn-off voltage, and the red line shows the compensated voltage based on the shaded volt-second area.

the Power factor correction (PFC) test result and also DPT in Fig. 3, the slew rate of the voltage rise can be approximately considered as a constant. So, the scheme here is to extend the turn-off interval by a certain time, so that the total voltage-second area is still equal to that of the ideal case. Thereby, a compensation scheme is proposed in Fig. 6, considering two cases at different current levels and charging conditions. Here, the black line is the uncompensated voltage pulse, and the red line represents the voltage rising edge of the extended turn-off interval after compensation. In the first case, the capacitance is charged quickly enough to reach 0.5 $V_{\rm dc}$ before the end of the pulse. In Case 2, the current is too low to allow for the voltage to reach 0.5 $V_{\rm dc}$ before the end of the pulse. However, the extended voltage pulse after compensation may in fact be long enough for v_x to reach 0.5 $V_{\rm dc}$, as shown in Fig. 6 Case 2(a). Therefore, it is important for the compensation algorithm to consider which case the pulse will fit into after it is extended, and not just prior to compensation.

The approach of this scheme is to equalize the two shaded volt-second areas as shown in Fig. 6, and thereby compensate for the voltage error. Because the turn-off delay interval $t_{d,\rm off}$ is far shorter than the charging interval in the current range of interest, this interval is neglected for simplicity without affecting the compensation accuracy. As previously mentioned, the slow voltage transition is mainly attributed to the low charging current during the turn-off transient. Though it is reasonable to approximate the charging voltage as a linear rise, the nonlinear capacitances of switching devices do greatly impact the charging time, and must be considered. The three device capacitances can be considered in parallel during the turn-off transient, and are later derived in Section III-E based on the current direction and *dv/dt* polarities shown in Fig. 4. The relationship between phase current and the voltage across these parallel nonlinear capacitances can be described by

$$i_{\rm ph} = C_{\rm total}(v_x)\frac{dv_x}{dt} \tag{1}$$

where $C_{\rm total}(v_x)$ is the sum of the three nonlinear capacitances as a function of the switch-node voltage v_x.

During the short turn-off transient, the phase current $i_{\rm ph}$ can be regarded as a constant, thus

$$t_{\rm charge} = \int_0^{V_{x\_\rm pk}} dt = \frac{\int_0^{V_{x\_\rm pk}} C_{\rm total}(v_x)dv_x}{i_{\rm ph}} = \frac{V_{x\_\rm pk}C_{\rm eq}}{i_{\rm ph}} \tag{2}$$

where $C_{\rm eq}$ is the charge-based equivalent output capacitance over the voltage range $[0,\ V_{x\_\rm pk}]$ for the three T-shape connected devices per phase-leg [14].

Based on (2), it is effective to use this charge-based equivalent capacitance to represent the nonlinear voltage-dependent $C_{\rm total}(v_x)$. Although $C_{\rm eq}$ is also a nonlinear function of $V_{x\_\rm pk}$, it can be approximated as a constant when $V_{x\_\rm pk} = 0.5V_{\rm dc}$. The detailed analysis will be presented in Section III-E.

With the above assumptions, Cases 1, 2a, and 2b from Fig. 6 will be analyzed in detail.

Case 1: Since the volt-second area of the two shaded areas should be equal, one can obtain

$$\frac{1}{2}k(t_2-t_1)^2 = \frac{1}{2}k\left[t_1 - \left(t_2 - \frac{V_{\rm dc}}{2k}\right)\right]^2 \tag{3}$$

where k is defined as the slew rate of $v_{\rm ds}$ in the turn-off transition, given by

$$k = \frac{i_{\rm ph}}{C_{\rm eq}}. \tag{4}$$

Thus, the desired turn-off interval extension can be calculated as

$$\Delta d = \frac{(t_2-t_1)}{T_s} = \frac{V_{\rm dc}C_{\rm eq}}{4T_s}\frac{1}{i_{\rm ph}}. \tag{5}$$

The boundary condition between Case 1 and Case 2 is given in (6) and (7):

$$kt_1 \geq \frac{V_{\rm dc}}{2} \tag{6}$$

$$d > \frac{V_{\rm dc}C_{\rm eq}}{2T_s}\frac{1}{i_{\rm ph}}. \tag{7}$$

Case 2: Here, the peak v_x is below $V_{\rm dc}/2$. So the boundary conditions given in (6) and (7) are not met.

In Case 2a, $kt_2 \geq \frac{V_{\rm dc}}{2}$, which means that the peak voltage after compensation reaches $V_{\rm dc}/2$. The shape of the charge balance for the extended pulse is the same as Case 1, leading to the same equivalence given in (7).

The boundary condition for these cases is

$$\frac{V_{\rm dc}C_{\rm eq}}{4T_s}\frac{1}{i_{\rm ph}} \leq d < \frac{V_{\rm dc}C_{\rm eq}}{2T_s}\frac{1}{i_{\rm ph}}. \tag{8}$$

In Case 2b, $kt_2 < \frac{V_{\rm dc}}{2}$, which means that the peak voltage after compensation is still below $V_{\rm dc}/2$. The area equivalence becomes

$$\frac{1}{2}k(t_2-t_1)^2 = \frac{1}{2}t_1\left(\left(\frac{V_{\rm dc}}{2} - k(t_2-t_1)\right) + \left(\frac{V_{\rm dc}}{2} - kt_2\right)\right). \tag{9}$$

Solving this equation yields

$$t_2 = \sqrt{t_1 \frac{V_{\rm dc}}{k}} \tag{10}$$

$$\Delta d = \frac{(t_2 - t_1)}{T_s} = \sqrt{\frac{C_{\rm eq} V_{\rm dc}}{T_s} \frac{d}{i}} - d. \tag{11}$$

The boundary condition is then given as

$$t_1 < \frac{C_{\rm eq} V_{\rm dc}}{4 i_{\rm ph}} \tag{12}$$

$$d < \frac{V_{\rm dc} C_{\rm eq}}{4 T_s} \frac{1}{i_{\rm ph}}. \tag{13}$$

It is evident that Case 2a can be grouped with Case 1, as the compensation equations give the same result. Therefore, the final compensation model can be described by

$$\Delta d = \frac{(t_2 - t_1)}{T_s} = \frac{V_{\rm dc} C_{\rm eq}}{4 T_s} \frac{1}{i_{\rm ph}}, \qquad \left(d \geq \frac{V_{\rm dc} C_{\rm eq}}{4 T_s} \frac{1}{i_{\rm ph}} \right) \tag{14}$$

$$\Delta d = \frac{(t_2 - t_1)}{T_s} = \sqrt{\frac{C_{\rm eq} V_{\rm dc}}{T_s} \frac{d}{i_{\rm ph}}} - d, \quad \left(d < \frac{V_{\rm dc} C_{\rm eq}}{4 T_s} \frac{1}{i_{\rm ph}} \right). \tag{15}$$

It is also worth noting that at the boundary condition between these two cases, both equations converge to the same result, with $\Delta d = d$, meaning that the duty cycle of turn-off should be doubled at this instant to compensate for the voltage error.

B. Issues With Voltage Error Compensation

The proposed scheme compensates the duty cycle based on the pulse-based adjustments, but it is also possible to directly calculate the duty cycle compensation term based on the average voltage error (16), as in one of the conventional dead-time compensation approaches [10], [11]:

$$\Delta d = \frac{\Delta V}{V_{\rm dc}/2}. \tag{16}$$

However, this assumes the compensated voltage has the ideal shape, which is not realistic still due to the non-negligible $C_{\rm oss}$ charging time. Especially when $V_{x\text{-pk}}$ is below the dc-link voltage (or half of that in three-level converters), this compensation scheme introduces errors. The mechanism is illustrated in Fig. 7, where $S_{\rm bcde}$ is the volt-second area of the uncompensated PWM voltage, time interval a-b is the extended turn-off interval via the proposed method, and interval j-b is the result from the voltage error compensation scheme.

In Case 1, when the peak voltage V_x reaches $0.5V_{\rm dc}$, extending the turn-off duty cycle using (16) effectively compensated for voltage error. The voltage loss area $S_{\rm beg}$ is equal to the rectangle area $S_{\rm jbgh}$ if the pulses are considered as ideal, or the parallelogram area $S_{\rm abef}$ if the actual voltage rise time is considered, and therefore the same performance is achieved as with the proposed method.

However, for either Case 2a or Case 2b, the compensation given in (16) always gives insufficient extension of turn-off

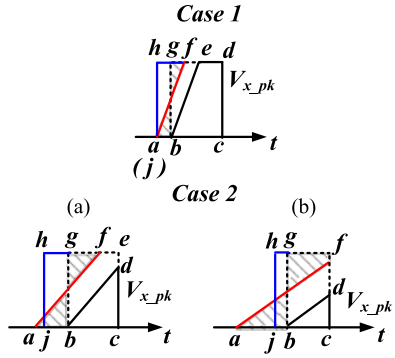


Fig. 7. Insufficient turn-off extension in voltage loss based compensation (blue line: Voltage loss based compensation; red line: Proposed compensation; black line: Uncompensated case; dashed line: Ideal PWM voltage).

interval. This is because the height of $S_{\rm jbgh}$ with that scheme is higher than that of the proposed $S_{\rm abdf}$. As $V_{x\text{-pk}}$ gets smaller, this compensator error grows, as demonstrated in Fig. 7(a) and (b).

C. Modulation Compensation for SPWM and Intuitive Physical Model

As shown in (14) and (15), the desired turn-off compensation term is a function of both instantaneous phase current and instantaneous duty cycle. Additionally, the duty cycle threshold for the boundary condition $d_{\rm th}$ is also a variable, requiring update each control cycle. Relying on the instantaneous d and $i_{\rm ph}$ to judge and update the compensation term is not robust, considering the likely current sampling noise and measurement error. Most importantly, the instantaneous compensation scheme shown in (14) and (15) does not reveal a clear overall picture of the duty cycle compensation over a whole line cycle, nor does it provide an effective way to evaluate the impact of different distortion factors such as switching frequency and dc voltage, or a guideline for control and modulation improvement.

In the following text, the relationship between d and $i_{\rm ph}$ will be exploited, to present an improved compensation scheme only related to d itself, forming the eventual modulation compensation scheme. For the sake of brevity, the case with carrier-based SPWM modulation is first analyzed. As well known, for Vienna-type rectifiers

$$d_{\rm on} = 1 - \frac{V_N \sin(\theta)}{V_{\rm dc}/2}, \ (0 \leq \theta \leq \pi). \tag{17}$$

And considering the unity power factor control as the PFC target

$$i_{\rm ph} = i_N \sin(\theta). \tag{18}$$

From (17) and (18), one obtains

$$d_{\rm on} = 1 - \frac{V_N / I_N}{V_{\rm dc}/2} i_{\rm ph}. \tag{19}$$

Then, an equivalent active resistance is defined

$$R_{\rm target} = \frac{v}{i_{\rm ph}} = V_N / I_N \tag{20}$$

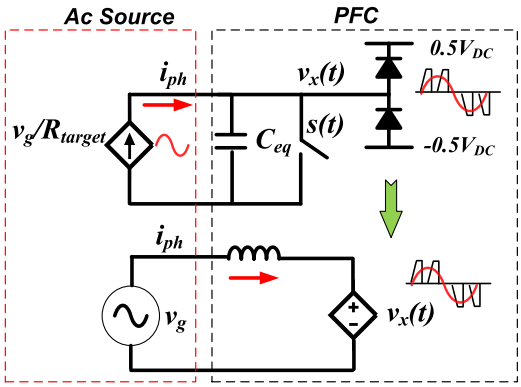


Fig. 8. Intuitive equivalent model of PWM voltage distortion in a unity PFC converter.

where R_{target} represents the unity power factor control for a specific power rating and is sometimes called the loss-free resistance [15]–[16].

Substituting (20) into (19), yields

$$d = 1 - d_{\text{on}} = \frac{R_{\text{target}}}{V_{\text{dc}}/2} i_{\text{ph}}. \tag{21}$$

Substituting (21) into (13), the new boundary d_{th} is derived as

$$d_{\text{th}} = \sqrt{\frac{R_{\text{target}} C_{\text{eq}}}{2T_s}}. \tag{22}$$

Similarly, substituting (21) into (14) and (15), the final compensation equations in the SPWM case becomes

$$\Delta d = \begin{cases} \dfrac{R_{\text{target}} C_{\text{eq}}}{2T_s} \dfrac{1}{d}, & (d \geq d_{\text{th}}) \\ \sqrt{\dfrac{2R_{\text{target}} C_{\text{eq}}}{T_s}} - d, & (d < d_{\text{th}}) \end{cases} \tag{23}$$

which reveals that the distortion is physically determined by the ratio of the time constant $R_{\text{target}} C_{\text{eq}}$ to the turn-off interval.

Since R_{target} represents the equivalent input impedance of the PFC in the line frequency domain, and C_{eq} reflects the device nonideal switching behavior in the high frequency domain, this distortion and its compensation can therefore be interpreted with a circuit model crossing the whole frequency span as illustrated in Fig. 8. As anticipated, since the turn-off charging process is tightly related to $R_{\text{target}} C_{\text{eq}}$, an ideal modulated PWM voltage generated by the PFC on the right side of the circuit will be inevitably distorted, thus the compensation in (23) is needed to achieve the target ac voltage. This intuitive model together with (23) provides a straightforward way to evaluate the input current distortion based on the given power, voltage rating and operation frequency.

Finally, as (23) is only a function of d, the overall compensation for a whole line cycle can be conveniently obtained. The compensation results at 650 V dc, 1.5 kW, and 450 kHz switching frequency are shown in Figs. 9 and 10, indicating the most severe distortion around zero crossing regions.

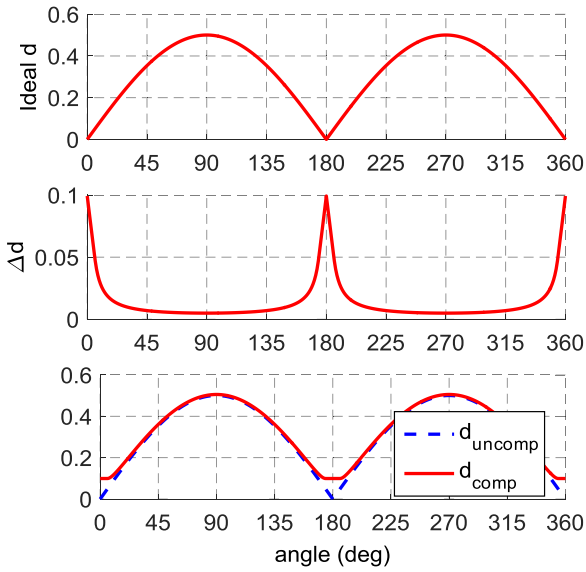


Fig. 9. Duty cycle compensation over a line cycle with SPWM modulation. Top: Ideal (uncompensated) turn-off duty cycle; medium: Compensation term; bottom: Ideal turn-off duty cycle in dashed blue and compensated duty cycle in red.

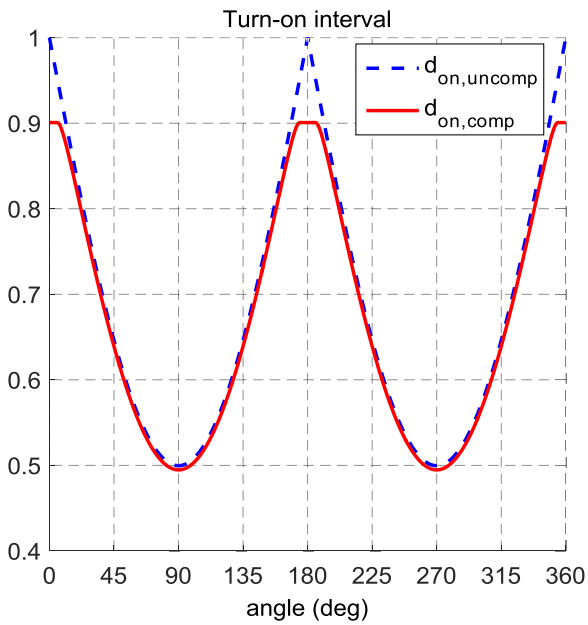


Fig. 10. Corresponding turn-on duty cycle before and after compensation with SPWM modulation. Ideal turn-on duty cycle in dashed blue and compensated result in red.

D. Modulation Compensation for SPWM Plus 3rd Harmonic Injection

To achieve higher dc voltage utilization, space vector modulation (SVM) is preferred. A simple implementation is carrier-based modulation with 3rd harmonic injection. In that case

$$\begin{aligned} d_{\text{on}} &= 1 - \frac{V_N \sin(\theta)}{V_{\text{dc}}/2} - V_{3h} \\ &= 1 - \frac{V_N}{V_{\text{dc}}/2} \left[\sin(\theta) + \frac{1}{4} \sin(3\theta) \right]. \end{aligned} \tag{24}$$

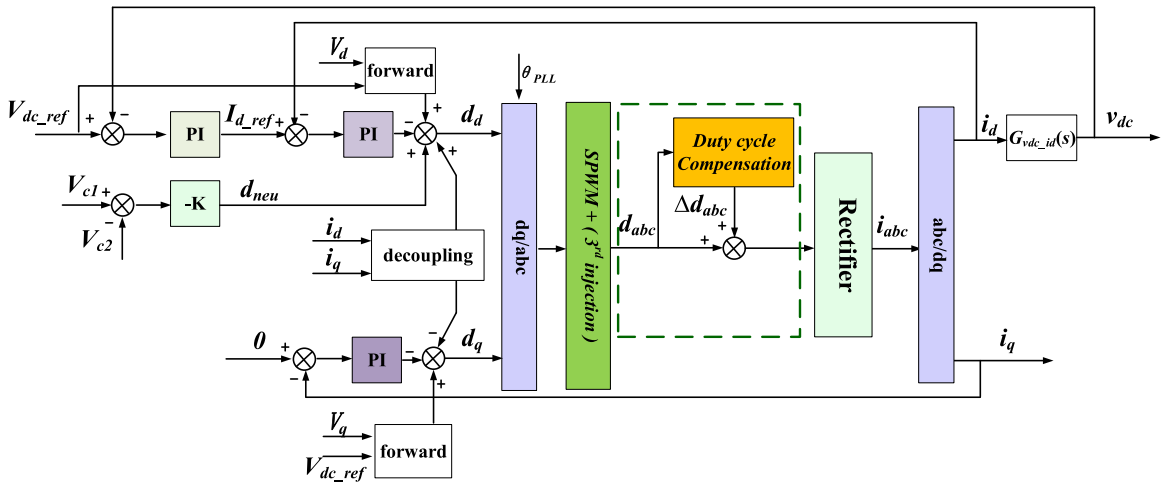


Fig. 11. Control diagram of three-phase PFC with the proposed modulation compensation scheme.

Similar to the SPWM case, with the adoption of the equivalent resistance concept, the duty cycle becomes

$$d = \frac{R_{\text{target}}}{V_{\text{dc}}/2}\left[1 + \frac{1}{4}\frac{\sin(\theta)}{\sin(3\theta)}\right] i_{\text{ph}} = \frac{2R_{\text{target}}\alpha(\theta)}{V_{\text{dc}}} i_{\text{ph}} \quad (25)$$

where α is the only additional term to the SPWM case, and can be simplified as

$$\alpha(\theta) = \left(\frac{7}{4} - \sin(\theta)^2\right) \quad (26)$$

where θ is a known variable from the PLL.

With these revisions, the compensation equations in the SVM case become

$$\Delta d = \begin{cases} \dfrac{R_{\text{target}} C_{\text{eq}}}{2T_s}\dfrac{\alpha(\theta)}{d}, & (d \geq d_{\text{th}}) \\ \sqrt{\dfrac{2R_{\text{target}} C_{\text{eq}}}{T_s}\alpha(\theta)} - d, & (d < d_{\text{th}}) \end{cases} \quad (27)$$

where the boundary duty cycle and angle are constants for a given power target given by

$$d_{\text{th}} = \sqrt{\frac{R_{\text{target}} C_{\text{eq}}}{2T_s}\alpha(\theta_{\text{th}})} \quad (28)$$

$$\theta_{\text{th}} = \sin^{-1}\left(\frac{\frac{7}{4} - \sqrt{\left(\frac{7}{4}\right)^2 - \frac{C_{\text{eq}} R_{\text{target}}}{T_s M^2}}}{2}\right) \quad (29)$$

where M is the modulation index defined as $M = V_N/(V_{\text{dc}}/2)$.

Finally, the control diagram of the three-level converter can be presented as shown in Fig. 11.

The duty cycle before and after compensation at 650 V dc, 1.5 kW, and 450 kHz switching frequency are provided in Figs. 12 and 13, indicating that more compensation is needed around the zero crossing regions.

E. Charge-Equivalent Capacitance Calculation

As mentioned previously, the output capacitance of the GaN FET is not the only one involved in the turn-off charging process, because the capacitances of the two SiC diodes should also be included. However, since the junction capacitance C_{D1} is discharged from $0.5\,V_{\text{dc}}$ to 0 V, and C_{D2} is charged from $0.5\,V_{\text{dc}}$ to V_{dc}, the instantaneous capacitances are different for each device during the transient, because they are nonlinear and voltage-dependent.

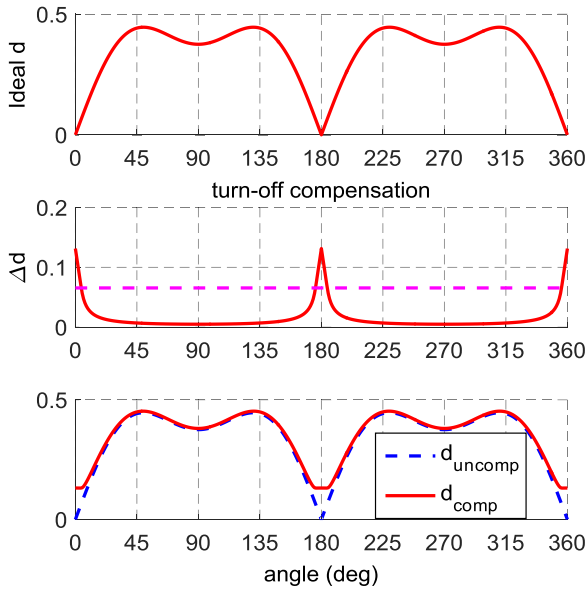


Fig. 12. Duty cycle compensation over a line cycle with 3rd harmonic injection modulation. Top: Ideal (uncompensated) turn-off duty cycle; medium: Compensation term; bottom: Ideal turn-off duty cycle in dashed blue and compensated duty cycle in red.

The charge-based equivalent capacitances for the three nonlinear capacitances are thus derived based on their respective C_{oss} *(V)* curves either from datasheet or measurement

$$C_{\text{eq\_GaN}} = \frac{\int_0^{0.5\text{V}_{\text{dc}}} C_{\text{oss}} dv_{\text{DS}}}{0.5\text{V}_{\text{dc}}} \quad (30)$$

$$C_{\text{eq\_D1}} = \frac{\int_{0.5\text{V}_{\text{dc}}}^{0} C_{\text{D1}} dv_{\text{D1}}}{0.5\text{V}_{\text{dc}}} \quad (31)$$

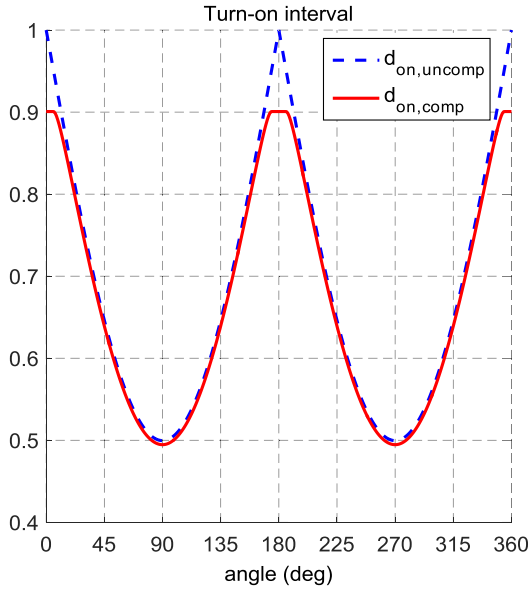


Fig. 13. Corresponding turn-on duty cycle before and after compensation with 3rd harmonic injection modulation. Ideal turn-on duty cycle in dashed blue and compensated result in red.

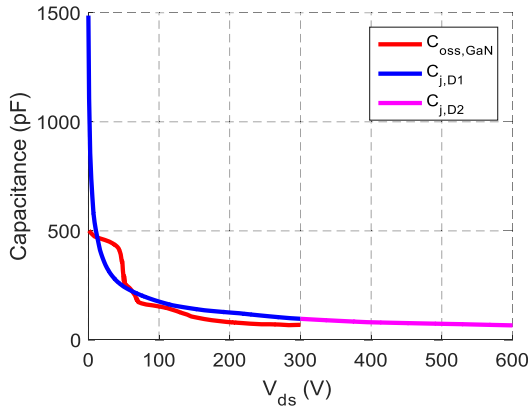


Fig. 14. Nonlinear capacitances of two SiC diodes and one GaN switch.

$$C_{\text{eq\_D2}} = \frac{\int_{0.5\text{V}_{\text{dc}}}^{V_{\text{dc}}} C_{\text{D2}} dv_{\text{D2}}}{0.5\text{V}_{\text{dc}}}. \tag{32}$$

The total charge-equivalent capacitance during the turn-off interval can then be calculated as

$$C_{\text{eq}} = C_{\text{eq\_GaN}} + C_{\text{eq\_D1}} + C_{\text{eq\_D2}} \tag{33}$$

Fig. 14 shows the nonlinear characteristics of the three output capacitances. A total equivalent 434 pF is obtained for 600 V dc bus. Direct measurement results from the slew rate of v_{DS} and current waveforms in Fig. 15 result in an average of 480 pF, which is very close to the calculated number, especially considering the measured error.

The preceding discussion assumes the switch-node voltage v_{ds} eventually reaches 0.5 V_{dc}. However, when the phase current is close to zero, as shown in Fig. 18, the peak voltage V_x might be below 0.5 V_{dc}. Thus, each capacitance shown in (30)–(32) now becomes a function of V_{x_pk}.

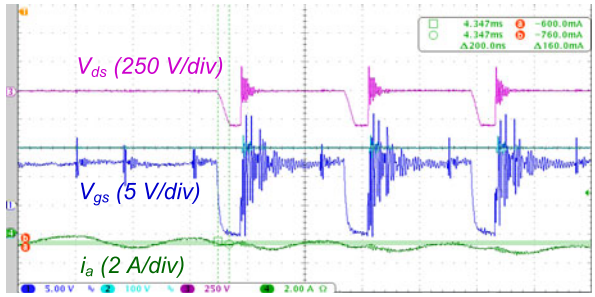


Fig. 15. AC terminal voltage distortion around zero crossing and the voltage slope measurement.

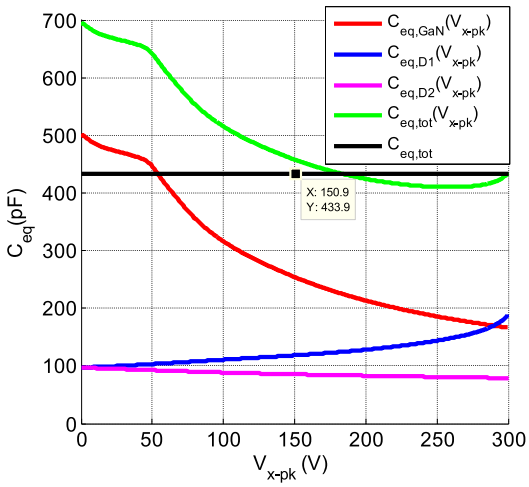


Fig. 16. Charge-equivalent capacitance as a function of V_{x_pk}.

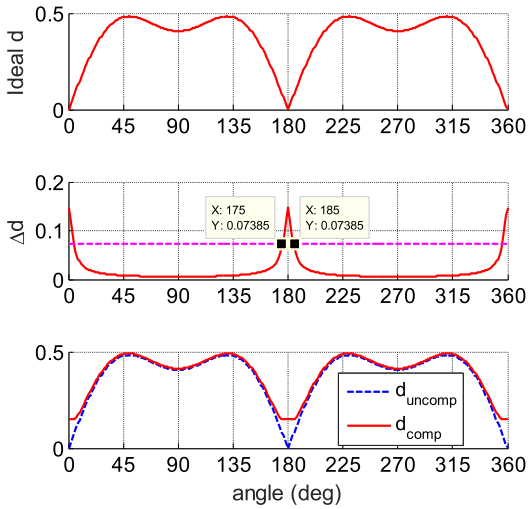
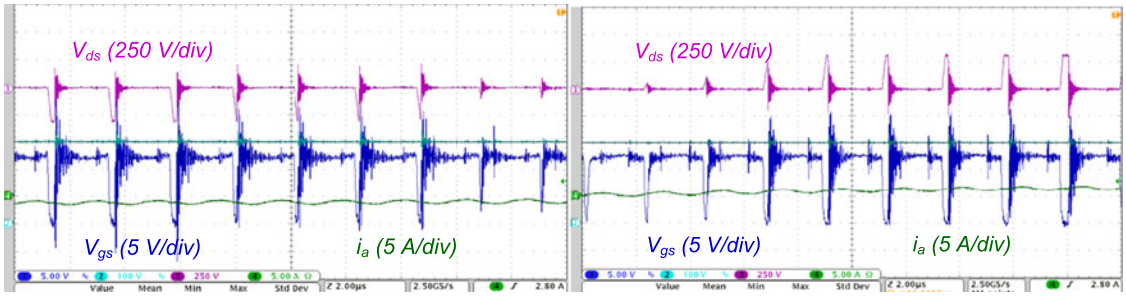


Fig. 17. Duty cycle compensation over a line cycle for SVM.

Therefore, the validity of the constant C_{eq} assumption using (30)–(32) must be examined. First, since the voltage changing directions of these three capacitances are different, their charge-based equivalent capacitances do not increase or decrease in the same way with respect to V_{x_pk}. For instance, as shown in Fig. 16, although $C_{\text{eq, GaN}}$ shows a higher value when V_{x_pk} is lower than $0.5V_{\text{dc}}$, $C_{\text{eq},D1}$ shows the opposite trend. Second, the $V_{x\_\text{pk}} < 0.5V_{\text{dc}}$ case only occurs for 10° around the zero crossing as denoted in Fig. 17, which includes only around ten



(a) (b)

Fig. 18. (a) Experimental waveforms of voltage distortion before zero crossing. (b) Voltage distortion after zero crossing.

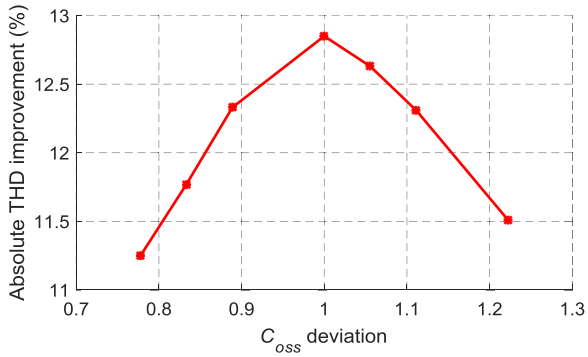


Fig. 19. Absolute THD reduction with the proposed compensation scheme versus the deviation of $C_{\rm oss}$ at 450 kHz switching frequency, 600 $\rm V_{dc}$, 115 $\rm V_{ac}$, and 1.3 kW Load.

switching cycles as shown in Fig. 18 (excluding the fully on cycles). Therefore, in this case, the nonlinear behavior of $C_{\rm eq}$ can be neglected. Consequently, the charge-based equivalent capacitance can be approximately regarded as a constant with $V_{x\_\rm pk} = 0.5V_{\rm dc}$. As shown by the black line in Fig. 16, this approximation results in 434 pF equivalent capacitance for this case.

It has also to be mentioned that the device output capacitance is a pretty stable parameter, based on which engineers estimate the switching loss for hard-switching circuit, dead-time selection for resonant circuit, resonant tank design for quasi-PWM resonant converter, and etc. It has only negligible dependence on the junction temperature, which is true not only for GaN devices [18]–[19] but also for Si MOSFETs [1], [20]. Therefore, the proposed compensation scheme is immune to the operation temperature.

In addition, through the simulation study, it is found that this compensation scheme is not very sensitive to $C_{\rm oss}$ deviation, even considering a certain inconsistency of device output capacitances. This is probably because the majority of the volt-second loss has been compensated by this scheme from the base $C_{\rm oss}$, as long as the deviation of $C_{\rm oss}$ is within a reasonable range. The relationship between THD improvement versus $C_{\rm oss}$ deviation is provided in Fig. 19 through a series of simulations. With 20% $C_{\rm oss}$ deviation, it shows that THD improvement compared to the case without compensation, only varies from 12.8 percentage points to 11.3 percentage points.

If $C_{\rm oss}$ is far away from the datasheet value, the real value can also be obtained through actual testing as already illustrated in Fig. 14.

F. Implementation of Dynamic Compensation

In the above compensation scheme, $R_{\rm target}$ varies as loading condition changes. Thus, the compensation terms (23) and (27) for SPWM and SPWM+3rd injection cases, and their boundary conditions (22) and (28)–(29), respectively, have to been updated online. Seemingly, this adds the computation effort. Especially for the latter case, since there is one trigonometric function and one square root function in (29), one square root function in (28), and an extra variable α, implementation considerations have to been made to simplify the mathematical calculation and reduce the computation burden, if applying this scheme to a relatively lower speed DSP.

Since sin(θ) in (26) is already a known variable from PLL park transformation, α calculation is not a concern. The concern is the boundary duty cycle $d_{\rm th}$ calculation. To simplify it, a quadratic polynomial curving fitting equation is adopted to update $d_{\rm th}$ as a function of $R_{\rm target}$ variation as illustrate in Fig. 20 for different loading conditions. Fig. 21 shows a good match between the fitted equation and (28) in SPWM+3rd injection case

$$d_{\rm th}\left(x\right) = p_1 * x^2 + p_2 * x + p_3 \tag{34}$$

where x is the ratio of $R_{\rm target}$ change with the rated load as the base, indicating different load percentages.

In further, $R_{\rm target}$ can be updated in each control cycle or in a relatively slow rate to save the computation effort, from two known vairaibles voltage V_d and current I_d in the d-q rotated frame

$$R_{\rm target} = \frac{V_d}{I_d}. \tag{35}$$

With that, only the condition when $d < d_{\rm th}$ in (27) needs one square root calculation. For typical DSP controllers such as TI 28x+FPU family, the computation burden of one square root is relatively low.

As one may also notice, the control target in (18) is a steady-state instantaneous current, during the transient, there may be certain compensation inaccuracy since the target resistance will suffer transient change. If the load change is fast, then i_N will also go to the new steady-state load rapidly. The model inaccu-

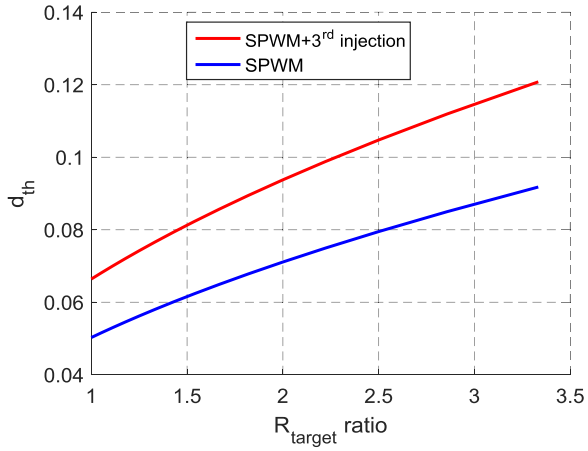


Fig. 20. $d_{\rm th}$ as a function of $R_{\rm target}$ change in two modulation cases.

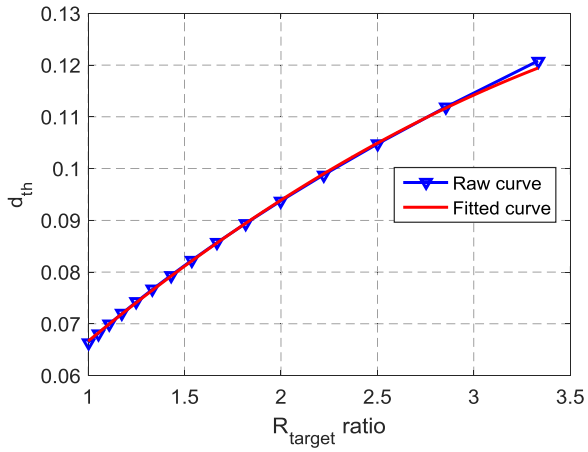


Fig. 21. Fitted $d_{\rm th}$ in SPWM+3rd injection case.

racy in the very short control transient thus can be neglected. If the load change is relatively slow, during this transient, under d-q rotating frame, i_N or i_d will be a linearly changing "dc" variable. Under this condition, the defined $R_{\rm target}$ will be dynamically updated based on measured v_d/i_d under d-q frame as shown in (35). In fact, the link from (17) to (21) is to represent ac input voltage v as $R_{\rm target} * i_{\rm ph}$. As long as $R_{\rm target}$ is updated faster enough, the transient will be taken care of. In further, actually the main drive for the turn-off compensation is to improve the power quality, i.e., to reduce the THD. THD, similar to power factor, is more like a steady-state disturbance index. Now that the compensation can ensure the good steady-state compensation, it helps to reduce current THD.

G. Impact Factors on Current and Voltage Distortion

Since the derived general modulation compensation term reveals the intrinsic relationship between the distortion and circuit parameters, the duty cycle ratio as shown in (36) can be a more effective index to predict the distortion impact from circuit parameters, instead of using the final THD obtained through

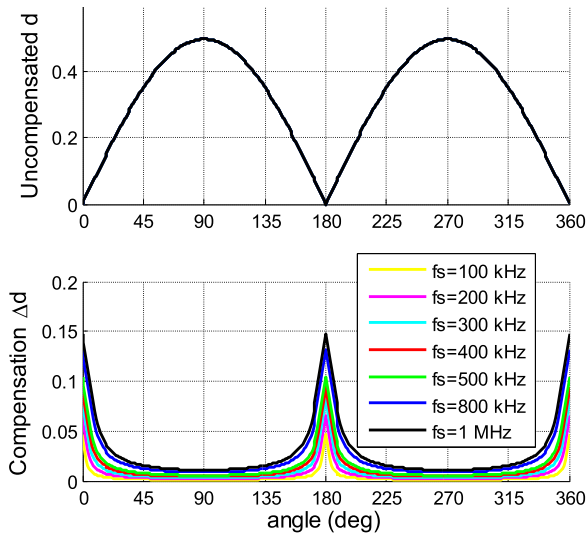


Fig. 22. Duty cycle compensation versus $f_{\rm s}$.

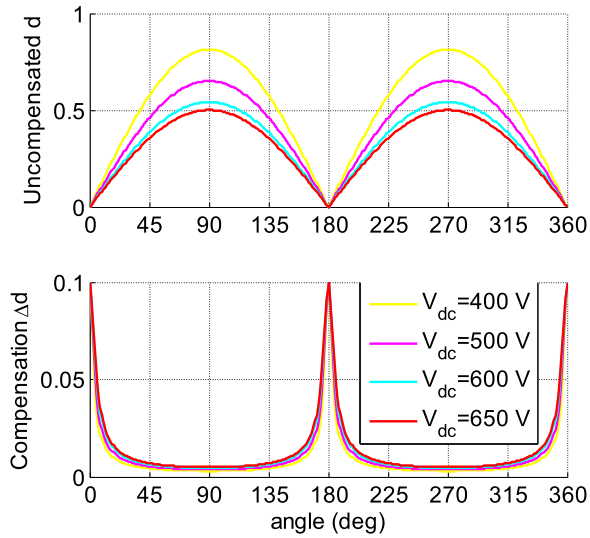


Fig. 23. Duty cycle compensation versus dc-link voltage.

simulations or tests as the indicator

$$\frac{\Delta V}{V_1} = \frac{\Delta d}{d}. \tag{36}$$

From (27) and (36), it is clear that for a given equivalent input resistance, the duty cycle loss is impacted by switching frequency, voltage dependent junction capacitances of diodes and switches, and the instantaneous duty cycle reversely proportional to dc voltage. Therefore, influences from both f_s and dc voltage for the selected devices are studied.

From Fig. 22, it can be inferred that the distortion ratio will rise as f_s increases. With the assumption that the equivalent capacitance is a fixed value, Fig. 23 shows that the absolute distortion stays nearly the same as dc voltage increases, yet the distortion percentage becomes high, due to the reduction of the ideal duty cycle d. Fig. 24 shows that even if the charge-equivalent capacitance is considered for different dc bus

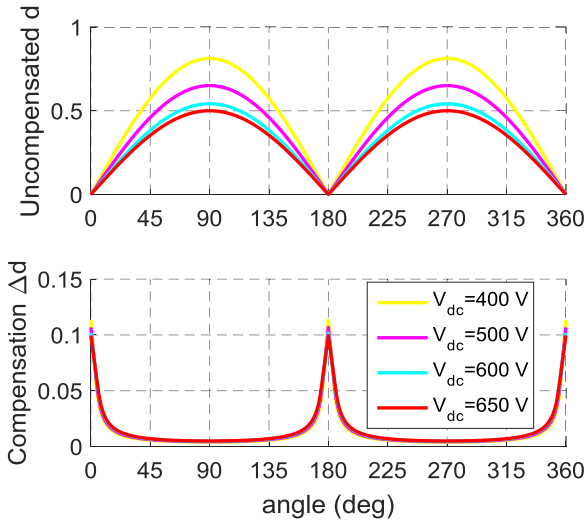


Fig. 24. Duty cycle compensation considering nonlinear $C_{\rm oss}$.

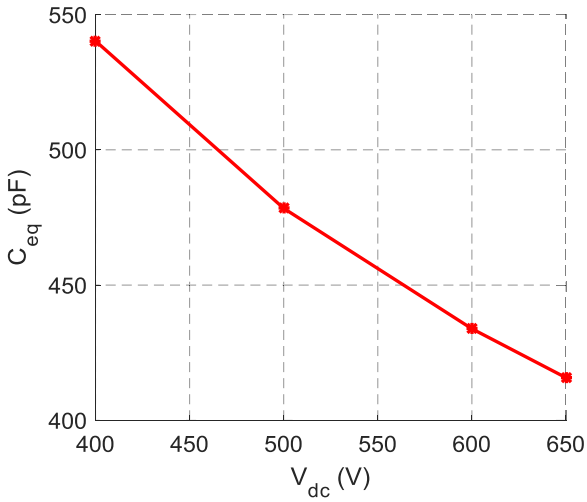


Fig. 25. Charge-equivalent $C_{\rm oss}$ versus dc-link voltage.

voltages, as shown in Fig. 25, the change of the absolute duty cycle loss is still fairly trivial. As a result, the voltage distortion percentage still increases at higher dc voltage.

The phase current's fundamental component is determined by the voltage difference between the ac source and the converter terminal, which is fixed for a given power. However, its harmonics are only determined by voltage distortion at the converter ac terminal assuming a harmonic-free ac source. Therefore, the current distortion is controlled purely by the dc voltage and the duty cycle loss as shown in (37). Based on the above discussion, dc voltage and its associated capacitance dominate the current distortion

$$\Delta i_h = \frac{0.5 V_{\rm dc} \Delta d}{Z_L} \tag{37}$$

Similar conclusions can also be obtained for the case with SPWM + 3rd harmonic injection, as given in Fig. 26 and Fig. 27.

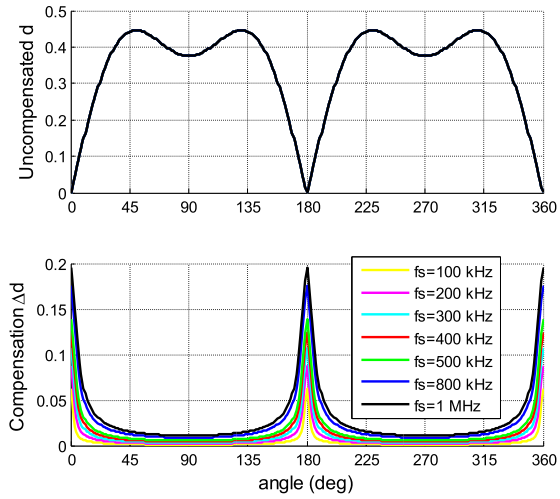


Fig. 26. Duty cycle compensation versus $f_{\rm s}$ for SVM.

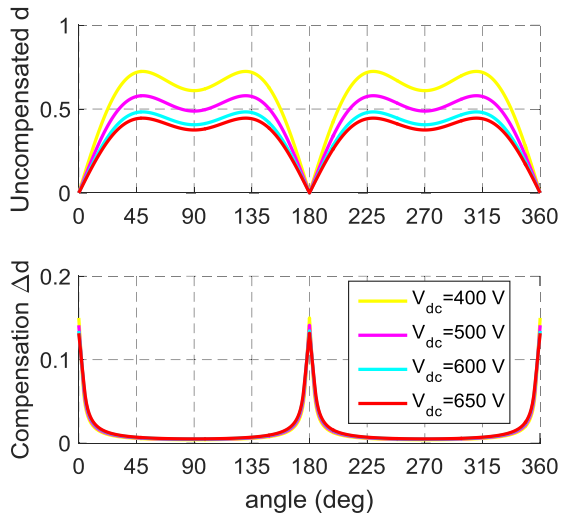


Fig. 27. Duty cycle compensation considering nonlinear $C_{\rm oss}$ for SVM.

IV. Simulation Results

A simulation was constructed to verify this distortion phenomenon and the compensation performance, with ac input phase voltage 115 V rms, dc voltage 600 V, and 1.3 kW load. Constant output capacitances were used to simplify this simulation model. It can be seen from Fig. 28 that the severe current harmonic distortion is effectively suppressed with the proposed compensation scheme under the steady-state operation.

The dynamic performance of this compensation scheme is also verified under the load change condition. A simulation with step-down load change from full load to half load is provided. As shown in Figs. 29 and 30, the proposed control can improve the current quality at both full load and light load, and the transient of load step change is smooth.

V. Experimental Verification

The derived modulation compensation scheme was also verified through a three-phase Vienna-type rectifier prototype operating at 450 kHz with forced cooling, as demonstrated in

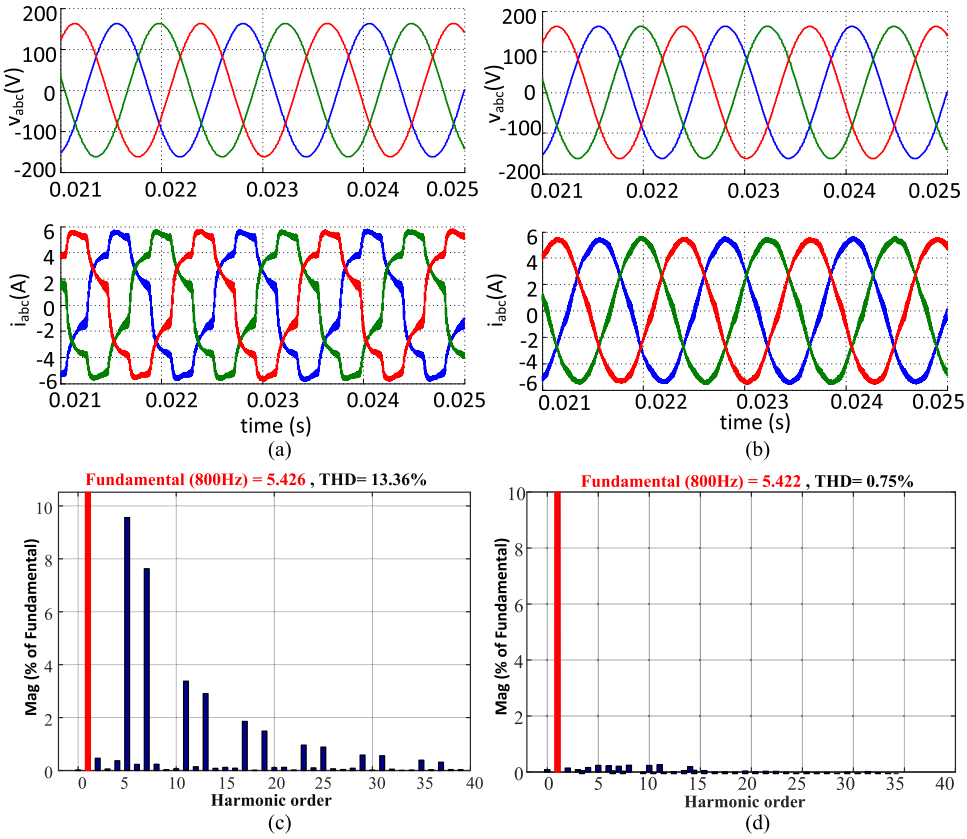


Fig. 28. Simulated phase voltage, current, and harmonic spectra. (a) AC side voltage and current without compensation. (b) AC side voltage and current with compensation. (c) Phase A THD without compensation. (d) Phase A THD with compensation.

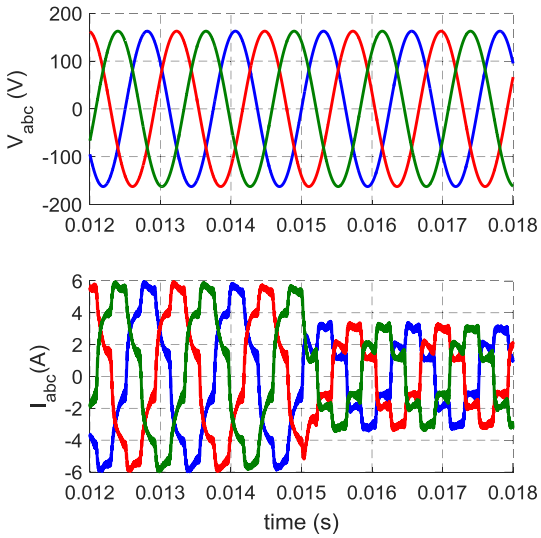


Fig. 29. Simulated ac input current waveforms without compensation under a load step-down change.

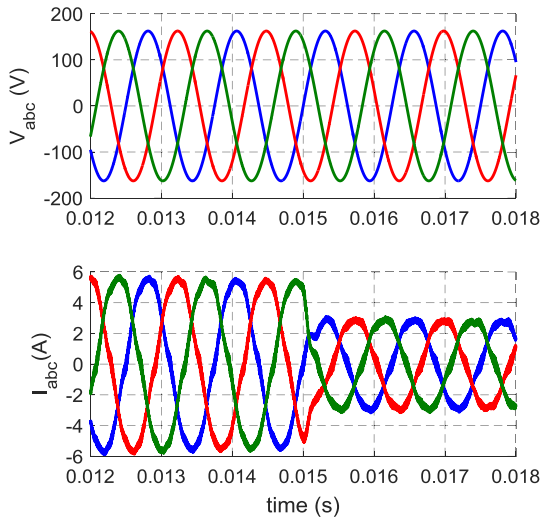


Fig. 30. Simulated ac input current waveforms with the proposed compensation under a load step-down change.

Fig. 31. This rectifier was designed for battery charging in aircraft applications, and is further described in [17]. The controller board, gate driver board, and mainboard were vertically stacked with the heatsink and fan mounted beneath the main board. A TI DSP TMS28377D with four built-in ADCs and enhanced floating-point calculation unit was implemented as the outer dc voltage and inner current loop controller, in which the controller is updated once every four switching cycles due to the computation delays. Therefore, the resulting lower control bandwidth provides very limited harmonic rejection capability for the 800 Hz fundamental ac system adopted in aircraft applications.

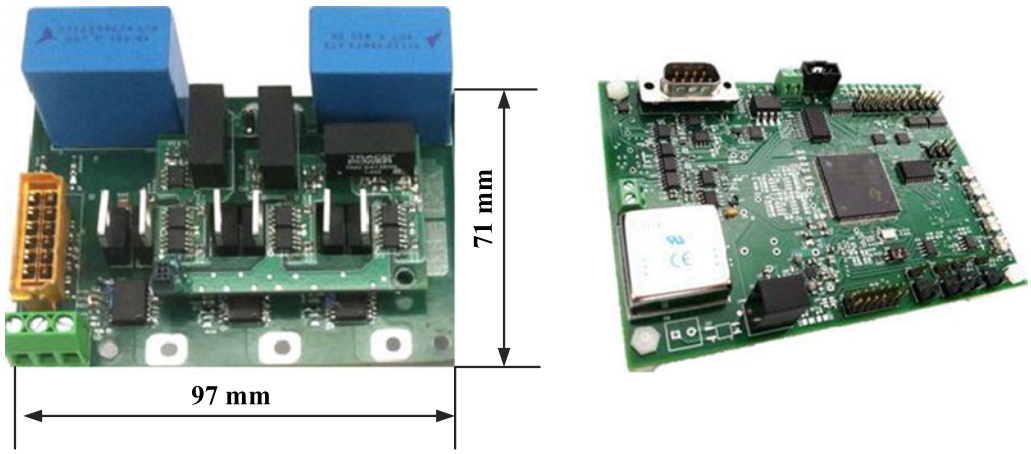


Fig. 31. Prototype of the three-phase three-level Vienna-type rectifier and its controller board.

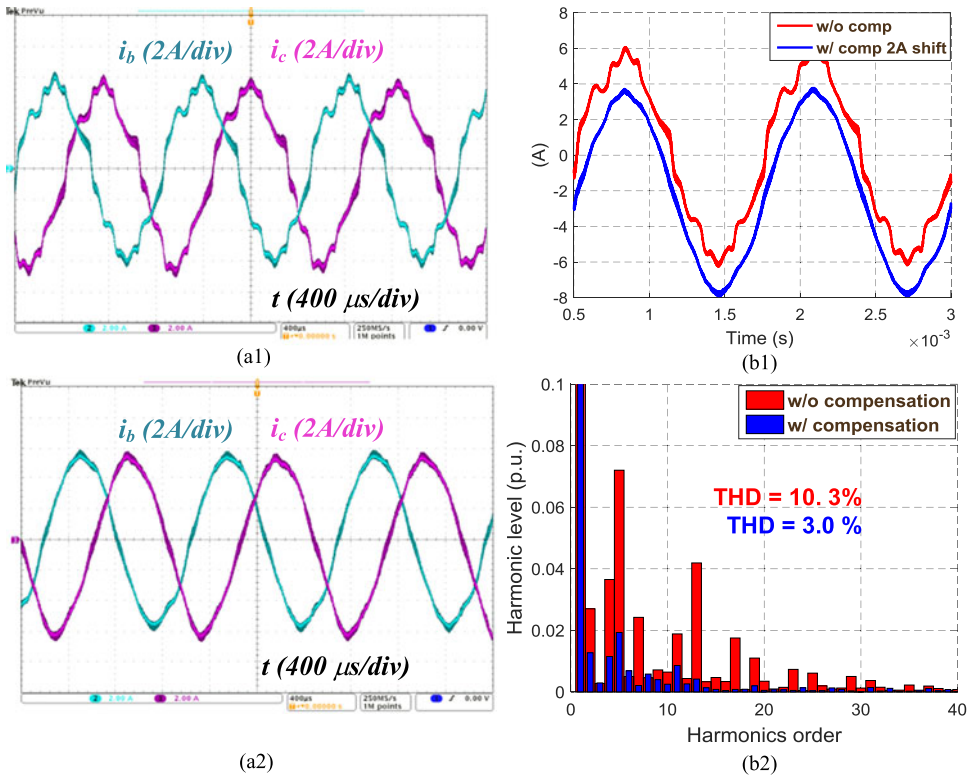


Fig. 32. Experimental comparison of current quality with and without the proposed compensation scheme. (a1-a2) Experimental waveforms of i_b and i_c current without and with compensation. (b1-b2) Comparison of i_b current without and with compensation. (blue curve in (b1) is shifted down by 2 A).

A. Steady-State Compensation Results

Without an accurate voltage error compensation scheme, an obvious distortion was observed in the input currents, mainly consisting of 6k $\pm$ 1 order harmonics due to the six zero crossings of the three phases as shown in Fig. 32. After applying the proposed scheme, those harmonics were significantly suppressed, and the current THD was reduced from 10.3% to 3.0%.

This result also highlights the importance of the feedforward-type compensation, especially for cases with moderate speed DSP controllers. The online implementation of such a modulation compensator for three phases in C code requires less than 800 ns computation time.

To further verify the accuracy of the compensation model, a comparison was made between the effective ac-terminal duty cycle $d_{\text{effective}}$ and the controller output d_{vgs} without the compensation. Here, the actual ac-terminal duty cycle is acquired from the averaged v_{ds} divided by the dc voltage, and d_{vgs} is based on the averaged gate voltage v_{gs} divided by its magnitude. From Fig. 33, it is clearly seen that the distortion from device capacitance causes about 0.1 maximum turn-off duty cycle loss in the zero crossing region excluding the measurement

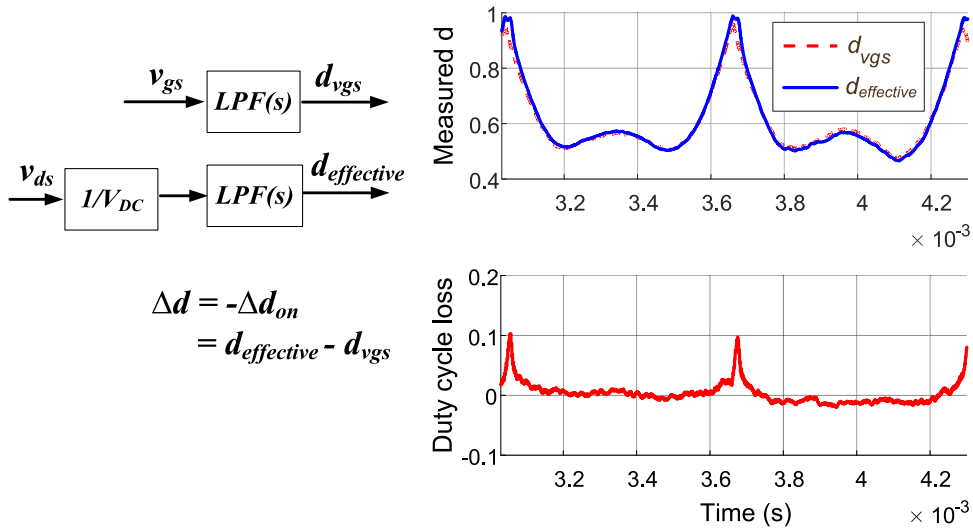


Fig. 33. Turn-off duty cycle loss derived from testing waveforms without compensation.

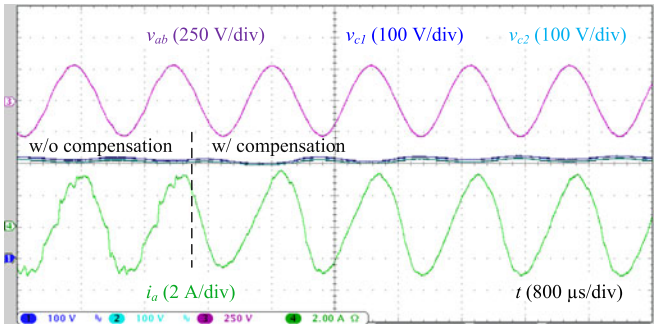


Fig. 34. Input current waveform without and with the proposed compensation under 650 W load condition.

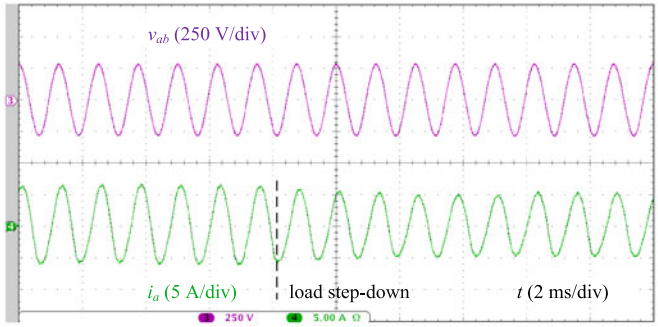


Fig. 35. Experimental ac input current waveforms with proposed compensation under a load step-down change.

error, which matches the desired compensation term calculated in (27) and Fig. 12.

The compensation scheme was also tested at light load. Fig. 34 shows the input current waveform without and with the compensation. Severe distortion is observed when the compensation is not activated. Once it is enabled, the input current quality is effectively improved. A certain 2nd order harmonic is still visible due to the imperfect of dc voltage balance control. This is because the proportional gain of dc voltage balance controller should be enhanced at low load [21], which is out of the scope of this paper.

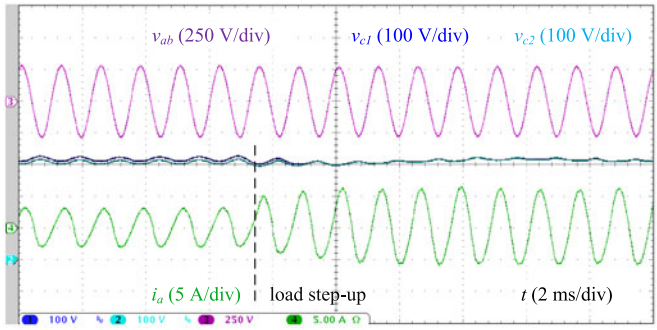


Fig. 36. Experimental ac input current waveforms with proposed compensation under a load step-up change.

B. Dynamic Compensation Results

To verify the effectiveness of the proposed turn-off modulation compensation scheme, both load step-down and step-up tests were conducted. Fig. 35 shows the load step-down result from 1.5 to 1.15 kW under 450 kHz, 115 V_{rms}, and 625 V_{dc}. Fig. 36 provides the load step-up result from 650 W to 1.3 kW. The transitions are smooth with good current quality for the three loading conditions. A certain 2nd order harmonic is observed in the 650 W condition, which is because of the insufficient gain of dc voltage balance controller at light load, as discussed before.

Finally, to demonstrate the impact of switching frequency on current distortion, the switching frequency was intentionally reduced to 112.5 kHz (¼ of 450 kHz). As shown in Fig. 37, even without compensation, the phase A current in the green curve still looks quite sinusoidal with less harmonics in the

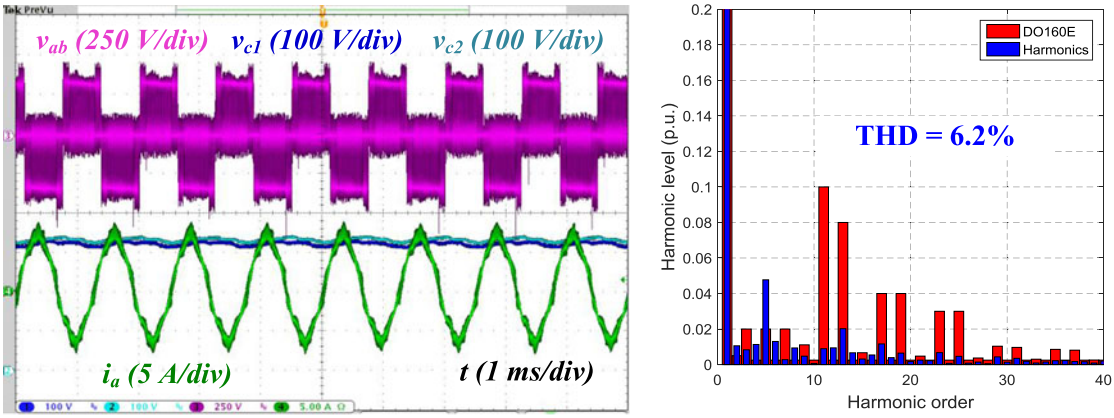


Fig. 37. Experiment waveforms and input current spectra when fs is reduced from 450 kHz to 112.5 kHz, at 115 V_{ac} rms, 650 V_{dc}, and 1.5 kW load.

6k $\pm$ 1 order, and its THD is only 6.2%, much less than the 450 kHz result with no compensation applied. In this case, the higher current ripple on the phase current is because of the intentionally reduced switching frequency.

VI. Conclusion

In this paper, the voltage distortion due to the output capacitances of SiC and GaN devices and their impact on turn-off voltage slew rate was analyzed. A feedforward compensation method was proposed, derived from a pulse-based turn-off voltage error model. With this robust compensation scheme, only the duty cycle is needed to correct the PWM signal, avoiding instantaneous current information and pulse cycle adjustment. The determination of charge-equivalent output capacitance during the turn-off transient was also explained, considering its voltage-dependent nonlinear characteristics. Voltage and current distortions due to these device capacitances can also be conveniently anticipated with the derived compensation and equivalent model, helping determination of circuit parameters early in the design process. Simulation and experimental results for a 450 kHz Vienna-type converter under both steady-state and load change conditions illustrate the performance of the proposed compensation strategy, reducing input current THD from 10% to 3%. The proposed strategy may also be applied to other topologies, providing a solution for mitigating current distortion that is relatively simple to implement in high frequency converters.

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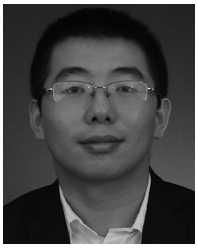

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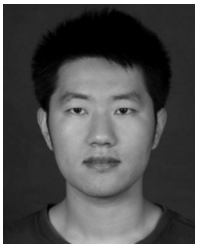

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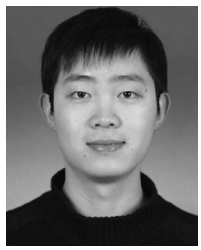

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