A Family of Resonant Two-Switch Boosting Switched-Capacitor Converter With ZVS Operation and a Wide Line Regulation Range

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***Abstract*—In this paper, a family of resonant two-switch boosting switched-capacitor converters (RTBSCs) with ZVS operation and a wide line regulation range is proposed. Based on our previously proposed two-switch boosting switched-capacitor converters (TBSCs), only a small resonant inductor is added, while two bulky capacitor banks are replaced by two much smaller resonant capacitors. Furthermore, by operating RTBSC above the resonant frequency, the transistors are ZVS turned ON and diodes are Zero-current-switching (ZCS) turned ON/OFF. This eliminates the hard-switched phenomenon of TBSC, leading to reduced component size by increasing the operating frequency without sacrificing the overall efficiency. In addition, the voltage-gain range of the RTBSCs is largely expanded and hence the input-voltage range is increased remarkably for regulated output voltage applications. Meantime, the voltage stress on transistors and diodes remains low, equal to the input voltage. A 3X RTBSC prototype with maximum output voltage 150 V, maximum output power 140 W, and a peak efficiency of 98.3% was built. The analysis is verified by simulation and experimental results.**

***Index Terms*—Resonant switched-capacitor converter, two-switch boosting switched-capacitor converter (TBSCs), zero voltage switching (ZVS).**

I. Introduction

SWITCHED-CAPACITOR (SC) converters have the potential to achieve small size, light weight, high efficiency, and high power density for dc–dc power conversion [1]. Over the last few decades, researches in this field flourished and many SC topologies were proposed, such as conventional Ladder SC converter, Dickson SC converter [2], series-parallel SC converter [3], [4], flying capacitor multilevel dc–dc converter [5]–[7], multilevel modular capacitor-clamped dc–dc converter [8], and so forth. The inductor-less property makes SC converter possible to be integrated on chip for milliwatt-power level applications [2],[9], [10]. In addition, applications where power levels are in the range from tens of watts [3], [4],[11] to kilowatt-level [5]–[8],[12], and even tens of kilowatts [13] can be found in previous literatures, demonstrating the widespread utilization of SC converters.

One major limitation for the SC converters is the limited line regulation range, because the voltage gain is almost predetermined by the circuit structure [18]. Several methods were proposed to improve the line and load regulation performances. One method is the on-resistance control [1] to operate the converter at a duty cycle close to 0.5 and a fixed frequency. However, the smaller on-resistance is preferable to achieve higher efficiency, limiting the regulation range. Another method is to change the duty cycle of the transistors, as reported in [3], [4], [11]. But the switching current will be very high if the duty cycle is small, causing high EMI and power losses. One can also use frequency modulation. This method is mainly for chip-level SC converters [9], [10], whose switching frequency range can be adjusted widely in the order of Mega Hertz. A combination of two modulation variables can also be employed to regulate capacitors' charging time and switching frequency so as to achieve the line and load regulation [14]. Moreover, [15]–[17] reported the quasi-switched-capacitor converter, where *p*-type MOSFET being operated as a controllable constant current source to regulate the output. However, the precise control of the current level may be difficult [18] and the cost and circuit complexity will be higher.

To combine the advantages of high-voltage-gain of a SC converter and good output regulation of a switching-mode dc–dc converter, some hybrid converters were proposed. In [19], traditional Fibonacci SC converter and boost/buck–boost converter were coupled to obtain good regulation. In [20], two buck converters were cascaded before and after an n-cell phase-shifted switched-capacitor converter [21]. Aside from the SC converters, SC cells can also be utilized in some traditional inductor-based converters to combine the voltage-lift function and good regulation function. Such voltage-lift technique was employed in Luo converter to increase the output voltage gain in geometric progression [22]. The SC cell—voltage multiplier—was applied in interleaved boost converter [23] and then extended to some other topologies [24]–[27].

Another limitation for SC converters is the hard-switched operation. Some SC converters [2]–[13] suffered from switching loss, hindering the increase of switching frequency.

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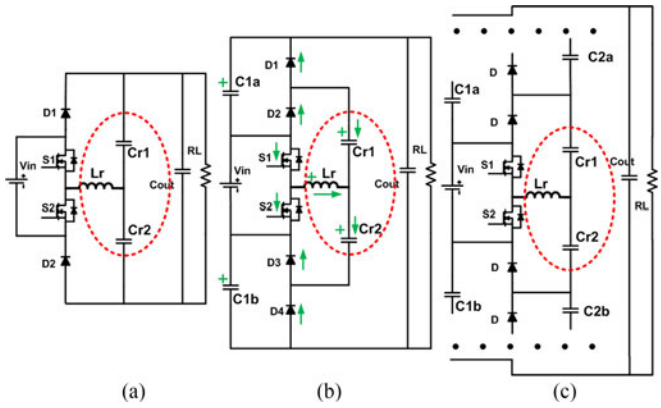

Fig. 1. Topologies of RTBSC. (a) 2X. (b) 3X. (c) NX.

Zero-current-switching (ZCS) SC converters inserting a resonant tank was proposed in [28]–[30]. The switching frequency is lower than the resonant frequency and the resonant current is in DCM. If the resonant frequency is designed to be a much higher value, the added resonant inductor can be integrated on a chip [31]. However, the available control headroom and regulation capability is limited [32]. In theory, the voltage gain is almost fixed. To overcome the voltage regulation issue, a different operating frequency above the resonant frequency was selected in [33]. The resonant current is in CCM and the regulation capability is much better.

In this paper, a family of resonant two-switch boosting switched-capacitor converters (RTBSCs) with ZVS operation and a wide line regulation range is proposed. Compared to our previously proposed TBSCs [34], [35], only a small resonant inductor is added, while two bulky capacitor banks are replaced by two much smaller resonant capacitors. By operating it above the resonant frequency, the transistors are ZVS turned ON and diodes are ZCS turned ON/OFF, reducing the switching loss significantly. In addition, the voltage-gain range is improved significantly, so that it can tolerate large input-voltage-variation if the output voltage is regulated. The different operation modes, voltage-gain curves, soft-switching regions, output characteristics, and current/voltage stresses of the resonant tank for this family are analyzed in details. A 3X RTBSC prototype with maximum output voltage 150 V and maximum output power 140 W was built to verify the analyses.

II. Operation Modes and Voltage-Gain Curves of RTBSCS

The topologies of 2X, 3X, and NX RTBSCs are shown in Fig. 1. In this part, a 3X RTBSC will be analyzed to find different operation modes and the corresponding voltage-gain curves. Then the similar analysis will be extended to N-X RTBSCs.

The topology of 3X RTBSC is shown in Fig. 1(b). $S_{1,2}$ are MOSFETs with internal antiparallel diodes. $D_1 - D_4$ are power diodes. An inductor L_r and two film capacitors $C_{r1,2}$ constitute the resonant tank, which is highlighted in a red circle. Capacitors $C_{1a,1b}$ are charge banks with large capacitance.

The duty cycle of S_1 and S_2 is fixed at 0.5 and their driving signals are complimentary with a short dead-time. The voltage

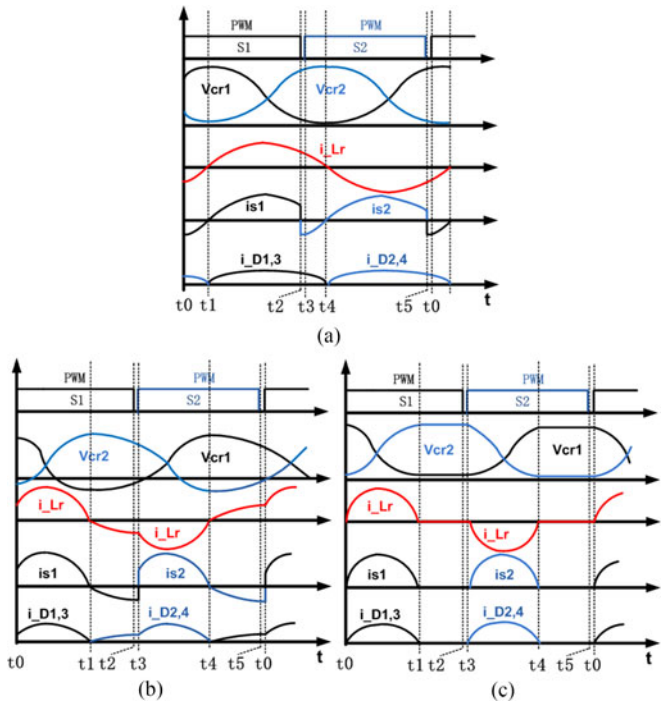

Fig. 2. Operating waveforms (a) $CCM_{1<F<2}$, (b) $CCM_{0.5<F<1}$, and (c) $DCM_{0.5<F<1}$.

across $C_{r1,2}$ is denoted as $V_{cr1,2}(t)$, while the voltages across $C_{1a,1b}$ are defined as $V_{c1a}(t)$ and $V_{c1b}(t)$. The currents flowing through L_r, switches $S_{1,2}$ and diodes $D_1 - D_4$ are represented by $i_{Lr}(t)$, $i_{s1,2}(t)$, and $i_{D1-D4}(t)$ respectively. The switching frequency and resonant frequency are f_s and f_r. The defined positive directions are denoted in green arrows in Fig. 1(b).

For simplicity, several assumptions are made as follows. With the symmetrical structure, the capacitances of C_{r1} and C_{r2} are both equal to C_r, so the maximum (minimum) voltage values across them are both equal to $V_{cr\_max}(V_{cr\_min})$. The capacitances of C_{1a} and C_{1b} are large and equal to each other, so the voltages on C_{1a} and C_{1b} are both considered to maintain at a constant value V_c in one switching cycle. ESRs of all capacitors, on-resistance of switches, and forward voltage of diodes are neglected. Dead-time between the complimentary driving signals is neglected.

A. Operation Modes and Voltage-Gain Curve of 3X RTBSC

1) Frequency Region $f_r < f_s < 2f_r$: When $f_r < f_s < 2f_r$, the transistors are ZVS turned ON and diodes are ZCS turned ON/OFF. In addition, the voltage-gain range is wide by changing f_s within a relatively small range. Moreover, the RMS current stress is lower, which will be discussed in Section IV. Therefore the nominal operating frequency is chosen in this range. The typical operating waveforms and the equivalent circuits in the first half switching cycle are shown in Figs. 2(a) and 3. This operating mode is defined as $CCM_{1<F<2}$. Analyses of converter operation and voltage-gain curve in $CCM_{1<F<2}$ are as follows:

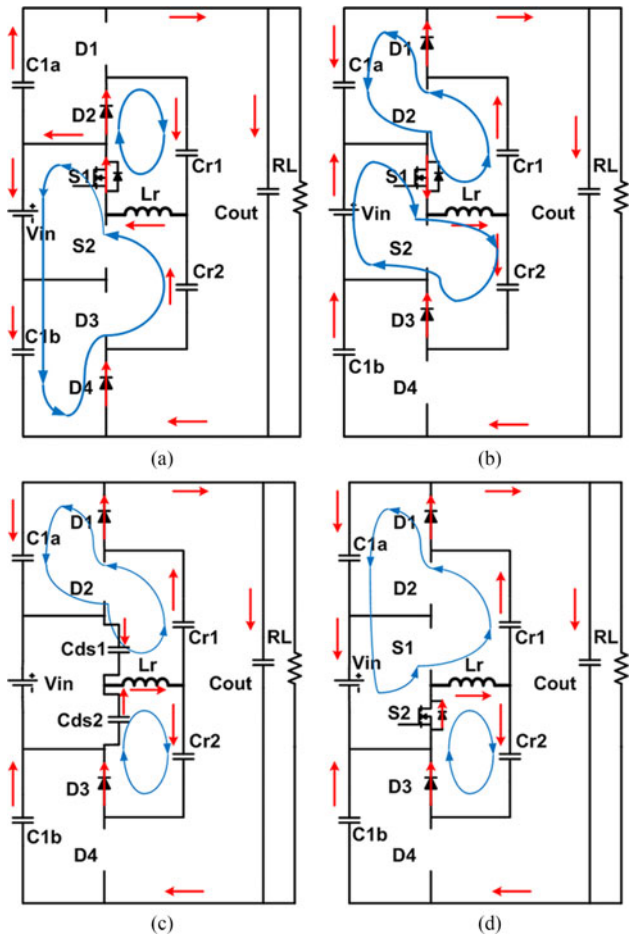

Fig. 3. Operating states (a) $t_0 \sim t_1$, (b) $t_1 \sim t_2$, (c) $t_2 \sim t_2'$, and (d) $t_2' \sim t_3$

First, in every operating state from Fig. 3, the following equation is always held:

$$V_{in} + V_c = V_{cr1}(t) + V_{cr2}(t) = V_{cr\_max} + V_{cr\_min}. \quad (1)$$

As a result, the output voltage is

$$V_o = 2V_c + V_{\rm in} = 2(V_{cr\_max} + V_{cr\_min}) - V_{\rm in}. \quad (2)$$

Second, from Fig. 3, both C_{1a} and the load are charged by C_{r1} during $t_1 - t_4$. Then all the charges stored in C_{1a} will be transferred to the load during $t_0 - t_1$ and $t_4 - t_0$, which means all the charges delivered to the load will be first stored in C_{r1} in each switching cycle. According to the charge balance of C_{r1}

$$C_r(V_{cr\_max} - V_{cr\_min}) = \frac{V_o}{R_L} * \frac{1}{f_s}, R_L \text{ is the load resistance.} \quad (3)$$

Third, the values of V_{cr_max} and V_{cr_min} can be derived according to the KVL and KCL equations in each state.

$[t_1 - t_2]$: In this state, there are two charging loops denoted in blue arrows, as shown in Fig. 3(a). The KVL and KCL equations in this operating state are

$$-L_r\frac{di_{Lr}(t)}{dt} + V_{cr1}(t) - V_c = 0 \quad (4)$$

$$C_r\frac{dV_{cr}(t)}{dt} = -\frac{1}{2}i_{Lr}(t)\,(C_{r1} = C_{r2}). \quad (5)$$

From Fig. 2(a), the boundary conditions are

$$i_{Lr}(t_1) = 0,\ V_{cr1}(t_1) = V_{cr\_max}. \quad (6)$$

Based on (1), (4)–(6), the resonant current and voltage are

$$i_{Lr}(t) = (V_{in} - V_{cr\_min})\sqrt{\frac{2C_r}{L_r}}sin2\pi f_r(t - t_1)$$

$$V_{cr1}(t) = (V_{cr\_max} + V_{cr\_min} - V_{in}) \quad (7)$$

$$+ (V_{in} - V_{cr\_min})\cos 2\pi f_r(t - t_1) \text{ where } f_r = \frac{1}{2\pi\sqrt{2L_rC_r}}. \quad (8)$$

$[t_2 - t_4]$: This interval is composed of three parts—$t_2 - t_3'$, $t_3' - t_3$ and $t_3 - t_4$. At t_2, transistor S_1 is turned OFF and then the loop current will charge the parasitic capacitance C_{ds1} of S_1 and discharge C_{ds2} of S_2 till t_2', shown in Fig. 3(c). The parasitic capacitance is so small and this interval is very short, which is neglected in steady-state calculation. After t_2', the voltage across C_{ds2} is discharged to zero and the internal anti-parallel diode of S_2 starts conducting current, shown in Fig. 3(d). At t_3, transistor S_2 is turned ON with ZVS operation and the charging loop during $t_3 - t_4$ is the same as shown in Fig. 3(d).

During $[t_2 - t_4]$, the KVL and KCL equations are

$$-L_r\frac{di_{Lr}(t)}{dt} + V_{cr1}(t) - (V_{in} + V_c) = 0 \quad (9)$$

$$C_r\frac{dV_{cr}(t)}{dt} = -\frac{1}{2}i_{Lr}(t)\,(C_{r1} = C_{r2}). \quad (10)$$

From Fig. 2(a), the boundary conditions are

$$i_{Lr}(t_4) = 0,\ V_{cr1}(t_4) = V_{cr\_min}. \quad (11)$$

Based on (1), (9)–(11), the resonant current and voltage are

$$i_{Lr}(t) = (-V_{cr\_max})\sqrt{\frac{2C_r}{L_r}}\sin 2\pi f_r(t - t_4) \quad (12)$$

$$V_{cr1}(t) = (V_{cr\_max} + V_{cr\_min}) + (-V_{cr\_max})\cos 2\pi f_r(t - t_4). \quad (13)$$

During $[t_1 - t_4]$, both the resonant current and voltage are composed of two parts of sinusoidal waveforms and the overall frequency is equal to f_s if dead-time is neglected, i.e.,

$$t_2 - t_0 = t_4 - t_1 = \frac{1}{2}\frac{1}{f_s}. \quad (14)$$

According to (7), (12), and (14)

$$(V_{\rm in} - V_{cr\_min})\sin 2\pi f_r\left(\frac{1}{2}\frac{1}{f_s} + t_0t_1\right) + V_{cr\_max}\sin 2\pi f_r(t_0 - t_1) = 0. \quad (15)$$

Similarly, according to (8), (13), and (14)

$$(V_{\rm in} - V_{cr\_min})\cos 2\pi f_r\left(\frac{1}{2}\frac{1}{f_s} + t_0t_1\right) + V_{cr\_max}\cos 2\pi f_r(t_0 - t_1) = V_{\rm in}. \quad (16)$$

By solving (15) and (16), the expression can be obtained as

$$\cos\frac{f_r}{f_s}\pi = \frac{V_{cr\_\min}^2 - 2V_{\rm in}V_{cr\_\min} + V_{cr\_\max}^2}{2V_{cr\_\min}V_{cr\_\max} - 2V_{cr\_\max}V_{\rm in}} < 0\,. \quad (17)$$

Assuming $d = \cos\frac{f_r}{f_s}\pi$, $k = C_r R_L f_s$, and (2), (3), and (17)

$$M_{cr\_\min} = \frac{V_{cr\_\min}}{V_{\rm in}} = \frac{(1-d)\,k^2 + (A-d-3)\,k + 6d + 6 - 2A)}{2\,[(1-d)\,k^2 + 4d + 4]} \quad (18)$$

$$M_{cr\_\max} = \frac{V_{cr\_\max}}{V_{\rm in}} = \frac{(k+2)\,M_{cr\_\min} - 1}{k-2} \quad (19)$$

$$M = \frac{V_o}{V_{\rm in}} = \frac{k\,[(1-d)\,k + 2A - 4d - 4]}{(1-d)\,k^2 + 4d + 4} \quad (20)$$

where $\mathrm{A} = \sqrt{(d^2-2d+1)k^2 + (2d^2-2)k + d^2 + 8d + 7}$.

However, a special scenario should be noted. The minimum voltage gain of the 3X RTBSC is 1, resulting from the structure of the TBSC converter. As a result, the voltage-gain curve maintains at 1 when (20) is smaller than 1. In this condition, equation of charge balance (3) will not be held, while (2) and (17) are still true. This operating mode is defined as $\mathrm{Fixed-Gain}_{1<F<2}$ ($\mathrm{FG}_{1<F<2}$). According to (2) and (17), the following equations are derived:

$$M_{cr\_\max} = \sqrt{\frac{1}{2\,(1+d)}} \quad (21)$$

$$M_{cr\_\min} = 1 - \sqrt{\frac{1}{2\,(1+d)}} \quad (22)$$

$$M = \frac{V_o}{V_{in}} = 1. \quad (23)$$

2) Frequency Region $\frac{1}{2}f_r < f_s < f_r$*:* When $\frac{1}{2}f_r < f_s < f_r$, the transistors are hard-switched and suffer from capacitive turn-on losses and *dv/dt* noise, which is not practical for very high-frequency operation [36]. Typically, the RTBSC does not operate in this region. In order to make the analysis complete, the voltage-gain curve is analyzed as well. The operating waveforms are shown in Fig. 2(b). This operating mode is defined as $\mathrm{CCM}_{0.5<F<1}$.

With the similar method, the equations of resonant current and voltage during $[t_0 - t_1]$ and $[t_1 - t_3]$ can be derived

$$i_{Lr}\,(t) = (V_{\rm in} - V_{cr\_\max})\sqrt{\frac{2C_r}{L_r}}\sin 2\pi f_r\,(t - t_1) \quad (24)$$

$$V_{cr1}\,(t) = (V_{cr\_\max} + V_{cr\_\min} - V_{\rm in}) + (V_{\rm in} - V_{cr\_\max})\cos 2\pi f_r\,(t - t_1) \quad (25)$$

and

$$i_{Lr}\,(t) = (V_{cr\_\min})\sqrt{\frac{2C_r}{L_r}}\sin 2\pi f_r\,(t - t_1) \quad (26)$$

$$V_{cr1}\,(t) = V_{cr\_\min}\cos 2\pi f_r\,(t - t_1)\,. \quad (27)$$

By ignoring the dead-time and charging/discharging time of the parasitic capacitances, the following equations are held:

$$i_{Lr}\,(t_0) = -i_{Lr}\,(t_3) \quad (28)$$

$$V_{cr1}\,(t_0) + V_{cr1}\,(t_3) = V_{cr\_\max} + V_{cr\_\min}. \quad (29)$$

According to (24)–(29), this expression can be obtained

$$\cos\frac{f_r}{f_s}\pi = \frac{V_{cr\_\min}^2 - 2V_{\rm in}V_{cr\_\max} + V_{cr\_\max}^2}{2V_{cr\_\min}V_{cr\_\max} - 2V_{cr\_\min}V_{\rm in}}\,. \quad (30)$$

Moreover, (2) and (3) are still true in this operation region. As a result, the following formulas can be derived according to (2), (3), and (30):

$$M_{cr\_\min} = \frac{V_{cr\_\min}}{V_{\rm in}} = \frac{(1-d)\,k^2 + (B+3d+1)\,k - 2d - 2 - 2B)}{2\,[(1-d)\,k^2 + 4d + 4]} \quad (31)$$

$$M_{cr\_\max} = \frac{V_{cr\_\max}}{V_{\rm in}} = \frac{(k+2)\,M_{cr\_\min} - 1}{k-2} \quad (32)$$

$$M = \frac{V_o}{V_{\rm in}} = \frac{k\,[(1-d)\,k + 2B + 4d + 4]}{(1-d)\,k^2 + 4d + 4} \quad (33)$$

Where $\mathrm{B} = \sqrt{(d^2-2d+1)k^2 - (2d^2-2)k + d^2 + 8d + 7}$.

However, two special conditions should be noted.

First, the minimum voltage gain is 1. As a result, the voltage-gain curve maintains at 1 when (33) is smaller than 1. Equation (3) will not be held, while (2) and (30) are still true. This operating mode is defined as $\mathrm{FG}_{0.5<F<1}$.

According to (2) and (30), the following equations are derived:

$$M_{cr\_\max} = 1 + \sqrt{\frac{1}{2\,(1+d)}} \quad (34)$$

$$M_{cr\_\min} = -\sqrt{\frac{1}{2\,(1+d)}} \quad (35)$$

$$M = \frac{V_o}{V_{in}} = 1. \quad (36)$$

Second, the maximum voltage gain is 3, limited by the TBSC structure. Within a certain frequency range, the gain curve will maintain at 3. In this unregulated region, the resonant current will go to DCM as shown in Fig. 2(c). This operating mode is defined as $\mathrm{DCM}_{0.5<F<1}$. The boundary between $\mathrm{CCM}_{0.5<F<1}$ and $\mathrm{DCM}_{0.5<F<1}$ can be derived as follows:

In $\mathrm{DCM}_{0.5<F<1}$, 3) isn't held. Based on (2) and (30)

$$M_{cr\_\max} = \left(1 + \frac{3}{2k}\right) \quad (37)$$

$$M_{cr\_\min} = \left(1 - \frac{3}{2k}\right) \quad (38)$$

$$M = \frac{V_o}{V_{\rm in}} = 3. \quad (39)$$

TABLE I
IMPORTANT FORMULAS

Freq.	$0.5f_r < f_s < 2f_r$			$f_r < f_s < 2f_r$	
Mode	$FG_{0.5<F<1}$	$CCM_{0.5<F<1}$	$DCM_{0.5<F<1}$	$CCM_{1<F<2}$	$FG_{1<F<2}$
Boundary	(33)<1	(33)>1 $k < 3/2$	(33)>1 $k > 3/2$	(20)>1	(20)<1
M_{cr_min}	(35)	(31)	(38)	(18)	(22)
M_{cr_max}	(34)	(32)	(37)	(19)	(21)
M	1	(33)	3	(20)	1

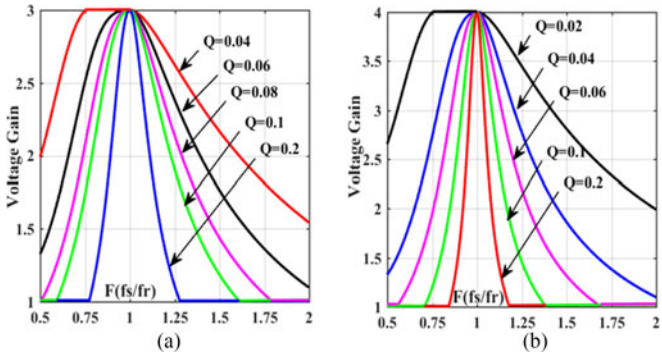

Fig. 4. Voltage gain curve of RTBSC. (a) 3X. (b) 4X.

If $M_{cr\_\min}$ is larger than 0, the resonant tank cannot start resonating in the reverse direction and, thus, the resonant current goes to DCM. As a result, the constraint of $\mathrm{DCM}_{0.5<F<1}$ is $M_{cr\_\min} > 0$, i.e.,

$$k > 3/2. \tag{40}$$

3) Voltage-Gain Curve: The above analyses about operating modes, boundary conditions and voltage-gain formulas are listed in Table I.

In order to plot the voltage-gain curve, two parameters are defined as follows:

$$\text{Frequency ratio} : \mathrm{F} = \frac{f_s}{f_r},\ \text{where } f_r = \frac{1}{2\pi\sqrt{2L_rC_r}} \tag{41}$$

$$\text{Quality factor} : \mathrm{Q} = \frac{Z_r}{R_L},\ Z_r = \sqrt{L_r/2C_r}. \tag{42}$$

As a result, the relationships between d, k and F, Q are

$$d = \cos\frac{f_r}{f_s}\pi = \cos\left(\frac{\pi}{F}\right), k = C_rR_Lf_s = \frac{F}{Q}\frac{1}{4\pi}. \tag{43}$$

Substituting (43) into the formulas in Table I, the voltage-gain curve of 3X RTBSC is plotted in Fig. 4(a).

B. Voltage Gain of N-X RTBSC

The similar analyzing method is used for N-X RTBSC.

When $f_r < f_s < 2f_r$, (17) is always true for all RTBSCs when $f_r < f_s < 2f_r$. The only differences are the equations of output voltage and charge balance

$$V_o = (N-1)\left(V_{cr\_\max} + V_{cr\_\min}\right) - (N-2)\,V_{\text{in}} \tag{44}$$

$$C_r\left(V_{cr\_\max} - V_{cr\_\min}\right) = \frac{N-1}{2} * \frac{V_o}{R_L} * \frac{1}{f_s}. \tag{45}$$

When $0.5f_r < f_s < f_r$, (30) is always true for all RTBSCs. The equations of output voltage and charge balance are exactly the same as (44) and (45).

Considering the above equations and the boundaries between different operating modes, the voltage-gain curve of N-X RTBSC can be obtained. For instance, the voltage-gain curve of 4X RTBSC is plotted in Fig. 4(b).

C. Further Investigation

When $0.5 < \mathrm{F} < 1$, for some small Qs, the gain curve will maintain at the maximum gain (N) over a certain frequency range, in which the RTBSC will lose regulation capability. If the Q is too small, such as when $Q = 0.04$ and $Q = 0.06$ in Fig. 4(b), the RTBSC will lose regulation capability completely in the range $0.5 < \mathrm{F} < 1$. As a result, aside from the hard-switched issue, another restriction preventing the RTBSC from operating in this region is the unregulated region.

When $1 < \mathrm{F} < 2$, the N-X RTBSC has higher "selectivity" than (N-1)-X RTBSC if Q is equal. For instance, when $Q = 0.04$, the voltage-gain range of 3X RTBSC is 1.56–3. However, the voltage-gain range of 4X RTBSC is 1.14–4. If Q is too small, which means very light load condition, the line regulation range is limited. In order to change the voltage gain, switching frequency has to be varied a lot. This phenomenon is pretty similar to the characteristics of series resonant converters [37]. Our future work will focus on this issue.

III. Output Characteristics of RTBSCS

In this section, the output characteristics of RTBSCs will be discussed. As mentioned in Section II, the operation switching frequency is above the resonant frequency, therefore, only modes $\mathrm{FG}_{1<F<2}$ and $\mathrm{CCM}_{1<F<2}$ are applicable. Furthermore, in mode $\mathrm{FG}_{1<F<2}$, the voltage gain is fixed at 1 and the output characteristic can be represented by a straight line. Thus, only the output characteristic in $\mathrm{CCM}_{1<F<2}$ needs to be discussed.

D. Output Characteristic of 3X RTBSC

Several parameters are defined as follows:

$$\text{Current base} : I_b = \frac{V_{\text{in}}}{\sqrt{L_r/2C_r}} \tag{46}$$

$$\text{Normalized output current} : \mathrm{J} = \frac{V_o/R_L}{I_b} = \frac{M}{2\pi f_rC_rR_L} \tag{47}$$

In $\mathrm{CCM}_{1<F<2}$, based on (2), (3), (17), and (47)

$$\mathrm{J} = \frac{F}{4\pi}\left(\sqrt{\frac{-M^2 + 2M + d\left(1 - 2M + M^2\right) + 7}{4\left(d+1\right)}} - 1\right). \tag{48}$$

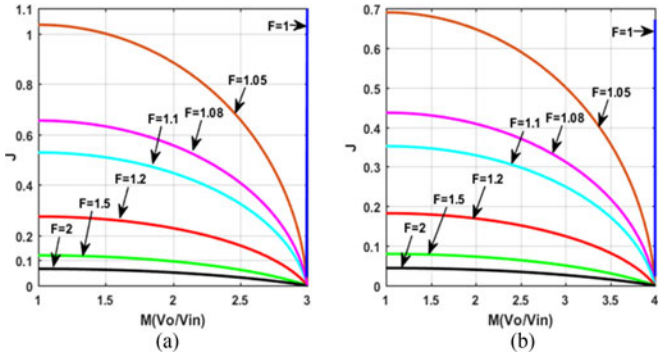

Fig. 5. Output characteristics of RTBSC. (a) 3X. (b) 4X.

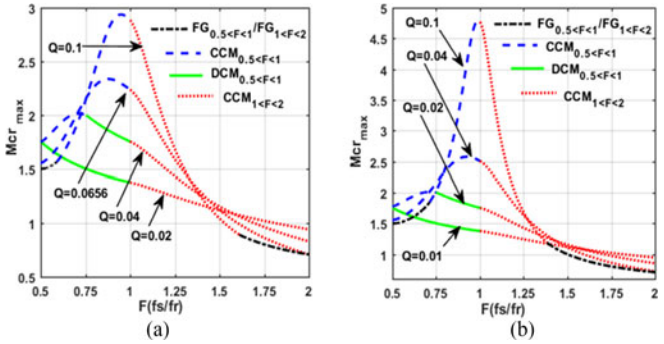

Fig. 6. Voltage stress of the resonant capacitor. (a) 3X. (b) 4X.

Referred to (48), the output characteristic of 3X RTBSC is plotted in Fig. 5(a).

E. Output Characteristic of NX RTBSC

For N-X RTBSC, according to (45) and (47)

$$\mathrm{J} = \frac{F}{2\,(N-1)\,\pi}\,(M_{cr\_\max} - M_{cr\_\min}). \tag{49}$$

When $1 < \mathrm{F} < 2$, the expression of (17) is always the same, while the equation of the output voltage is different, as given in (44). According to (17), (44), and (49), the output characteristic can be derived. For instance, the output characteristic of 4X RTBSC is plotted in Fig. 5(b).

IV. Voltage and Current Stress of the Resonant Tank

A. Voltage Stress of the Resonant Capacitor

In this part, the normalized maximum voltage value $(M_{cr\_\max})$ of the resonant capacitor is analyzed. For 3X RTBSC, the value of $M_{cr\_\max}$ in different operating modes can be obtained from Table I. Considering the boundary constraints, $M_{cr\_\max}$ of the resonant capacitor for 3X RTBSC is plotted in Fig. 6(a). In different operating modes, different patterning is applied.

Similarly, $M_{cr\_\max}$ of the resonant capacitor for 4X Ladder RSC is plotted in Fig. 6(b). The voltage stress for the resonant capacitor under different operating conditions can be easily figured out.

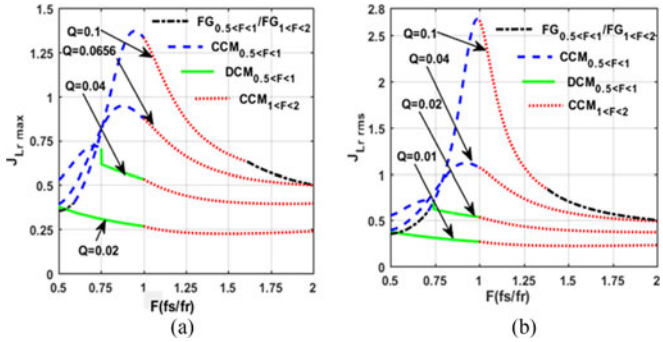

Fig. 7. Current stress of the resonant inductor. (a) 3X. (b) 4X.

B. Current Stress of the Resonant Inductor

In this part, the normalized RMS current stress of the resonant inductor is analyzed.

For 3X RTBSC, from Fig. 2(a) and (b), the current waveform can be approximated to be a sinusoidal wave for simplicity, even though the practical RMS value is smaller. But it will give more design headroom to select the components. As for the $\mathrm{DCM}_{0.5<F<1}$ in Fig. 2(c), the inductor current can be regarded as a periodic waveform composed of sinusoidal piecewise segments.

When $1 < \mathrm{F} < 2$, the equations of the current waveform in $\mathrm{FG}_{1<F<2}$ and $\mathrm{CCM}_{1<F<2}$ are same. The normalized RMS value of the sinusoidal current wave is obtained according to (7) and (46)

$$J_{Lr\_\mathrm{rms}} = \left|\frac{(V_{in} - V_{cr\_\min})\sqrt{\frac{2C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}}\right| = \frac{1}{\sqrt{2}}\,(1 - M_{cr\_\min}). \tag{50}$$

When $0.5 < \mathrm{F} < 1$, the normalized RMS current value of the resonant inductor in $\mathrm{FG}_{0.5<F<1}$ and $\mathrm{CCM}_{0.5<F<1}$ is obtained

$$J_{Lr\_\mathrm{rms}} = \left|\frac{(V_{cr\_\max} - V_{\mathrm{in}})\sqrt{\frac{2C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}}\right| = \frac{1}{\sqrt{2}}\,(M_{cr\_\max} - 1)\,. \tag{51}$$

In $\mathrm{DCM}_{0.5<F<1}$, the normalized RMS current value of the resonant inductor is

$$J_{Lr\_\mathrm{rms}} = \sqrt{F}\left|\frac{(V_{cr\_\max} - V_{\mathrm{in}})\sqrt{\frac{2C_r}{L_r}}}{I_b} \times \frac{1}{\sqrt{2}}\right| = \frac{\sqrt{F}}{\sqrt{2}}\,(M_{cr\_\max} - 1)\,. \tag{52}$$

The corresponding values of $M_{cr\_\min}$ and $M_{cr\_\max}$ can be obtained from Table I. The normalized RMS current value of the resonant inductor for 3X RTBSC is plotted in Fig. 7(a). In different operating modes, different patterning is applied.

Similarly, J_{Lr_rms} of the resonant inductor for 4X RTBSC is plotted in Fig. 7(b). The current stress for the resonant inductor under different operating conditions can be easily figured out.

V. Hardware Design and Experimental Results

A. Hardware Design

In this part, a 3X RTBSC prototype with theoretical maximum output voltage 150 V and maximum power 140 W is designed. Typically, the operating frequency should be in the range of $1 < \mathrm{F} < 2$, but this prototype was designed to operate in the whole frequency range ($0.5 < \mathrm{F} < 2$) for open loop test in order to demonstrate the validity of analyses. While for closed-loop test, the converter will only operate in $1 < \mathrm{F} < 2$.

The highest switching frequency $2f_r$ is designed to be 150 kHz, so the lowest switching frequency $0.5f_r$ and resonant frequency f_r are about 38 KHz and 76 KHz, respectively. The resonant capacitors C_r are chosen to be two 100 nF film capacitors. According to $f_r = \frac{1}{2\pi\sqrt{2L_r C_r}}$, the resonant inductor L_r is about 22 μH.

In order to measure the performance of 3X RTBSC under different load conditions, two resistors —160 Ω and 320 Ω— are chosen and the theoretical values of Q are 0.0328 or 0.0656.

According to Fig. 3, the voltage stress $V_{s\_s1,s2}$ on transistor S_1 and S_2 is equal to the input voltage, i.e., $V_{s\_s1,s2} = V_{\mathrm{in}}$. While for the voltage stress $V_{s\_\mathrm{D1-D4}}$ on diodes $\mathrm{D_1} - \mathrm{D_1}$, it's equal to the voltage across $\mathrm{C_{1a}}$ and $\mathrm{C_{1b}}$, i.e., $V_{s\_\mathrm{D1-D4}} = V_c = V_{cr\_\max} + V_{cr\_\min} - V_{\mathrm{in}} = \frac{V_o - V_{\mathrm{in}}}{2}$. Since the maximum gain of 3X RTBSC is 3, the maximum voltage on the diode is also equal to the input voltage, i.e., $V_{s\_\mathrm{D1-D4}} = \frac{V_o - V_{\mathrm{in}}}{2} = \frac{3V_{\mathrm{in}} - V_{\mathrm{in}}}{2} = V_{\mathrm{in}}$. As shown, the voltage stress on transistors and diodes is low, equal to the input voltage. The voltage stress of the resonant capacitor can be derived from Fig. 6(a), $V_{s\_Cr} \approx 2.4V_{\mathrm{in}}$ when $\mathrm{Q} = 0.0656$.

The RMS current stress of the resonant inductor can be derived from Fig. 7(a), i.e., $I_{\mathrm{rms}\_Lr} \approx 0.95 \times I_b$ when $Q = 0.06256$. From Fig. 2, the RMS current stress of $S_{1,2}$ is $I_{\mathrm{rms}\_S1,S2} = \frac{i_{\mathrm{rms}\_Lr}}{\sqrt{2}}$. In addition, the diode current is only half of the transistor current in every state, so $I_{\mathrm{rms}\_\mathrm{D1-D4}} = \frac{i_{\mathrm{rms}\_Lr}}{2\sqrt{2}}$.

Based on the above analysis, proper components are selected and the parameters of the prototype in open-loop and closed-loop tests are listed in Table II.

B. Simulation and Experimental Results

A family of RTBSCs without parasitic elements is simulated using software PSIM. The parameters of the circuit are selected from Table II, and the voltage-gain curves are shown in Fig. 8.

The solid lines represent the theoretical gain curves, while the black dots/stars/diamonds are simulation results. Seen from the preliminary comparison, the analysis matches the simulation results closely for both 3X and 4X RTBSCs.

A prototype was then built. The experimental waveforms of open-loop test are shown in Figs. 9–12. In open-loop test, the input is fixed at 50 V and then to measure the output voltage with different switching frequencies. Two load resistances are measured to be 163.9 Ω and 322.8 Ω, i.e., $Q = 0.064$ and $Q = 0.0325$ in practice.

TABLE II
Prototype Specifications

Power Level	<140W	C_{1a}, C_{1b}	100uF
Input (V_{in})	OL: 50V	$C_{r1,r2}$	100nF
	CL:40~100V		film capacitors
Output (V_o)	OL: <150V	L_r	22uH
	CL: 120V		
f_s	OL:38~150kHz	f_r	76kHz
	CL:76~150kHz		
C_{in}	100uF	$D_{1\sim4}$	MBR10100G
C_{out}	100uF	$S_{1,2}$	FDPF390N15A

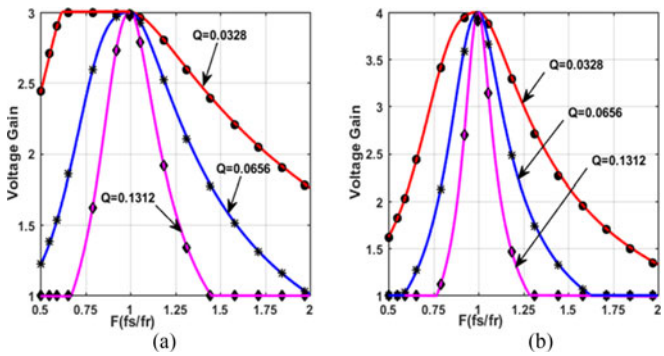

Fig. 8. Simulated voltage-gain curve. (a) 3X. (b) 4X.

In Fig. 9, Q is 0.0325 and f_s is 90 kHz. The experimental waveforms match the waveforms of $\mathrm{CCM}_{1<F<2}$ in Fig. 2(a). From Fig. 9(a), transistor S_1 is ZVS turned ON, because the resonant current is negative when the driving signal of S_1 becomes high. Obviously, the switching noise on the drain-source of MOSFET is reduced a lot due to ZVS operation. Fig. 9(b) shows the resonant voltages on $C_{r1,r2}$. According to Fig. 9(c), $V_{\mathrm{in}} = 50$ V and $V_{\mathrm{out}} = 140$ V, thus, the voltage gain is 2.8.

In Fig. 10, Q is 0.0325 and f_s is 40 kHz. The experimental waveforms match the waveforms of $\mathrm{CCM}_{0.5<F<1}$ in Fig. 2(b). From Fig. 10(a), transistor S_1 is hard-switched turn ON, while the resonant current is in CCM. Fig. 10(b) shows the resonant voltages on C_{r1} and C_{r2}. According to Fig. 10(c), V_{in} is 50 V and V_{out} is 121 V, thus the voltage gain is 2.42.

In Fig. 11, Q is 0.0325 and f_s is 50 kHz. The experimental waveforms match the waveforms of $\mathrm{DCM}_{0.5<F<1}$ in Fig. 2(c). From Fig. 11(a), transistor S_1 is ZCS turned ON, because the resonant current is in DCM. In Fig. 11(b), the resonant voltages on C_{r1} and C_{r2} maintain at constant values when the resonant current goes into DCM. According to Fig. 11(c), V_{in} is 50 V and V_{out} is 137 V, thus, the voltage gain is 2.74.

The boundary between $1 < \mathrm{F} < 2$ and $0.5 < \mathrm{F} < 1$ can be figured out from Fig. 12 approximately. The waveform of resonant current is almost a pure sinusoidal wave at 80 kHz, which is the practical resonant frequency f_r.

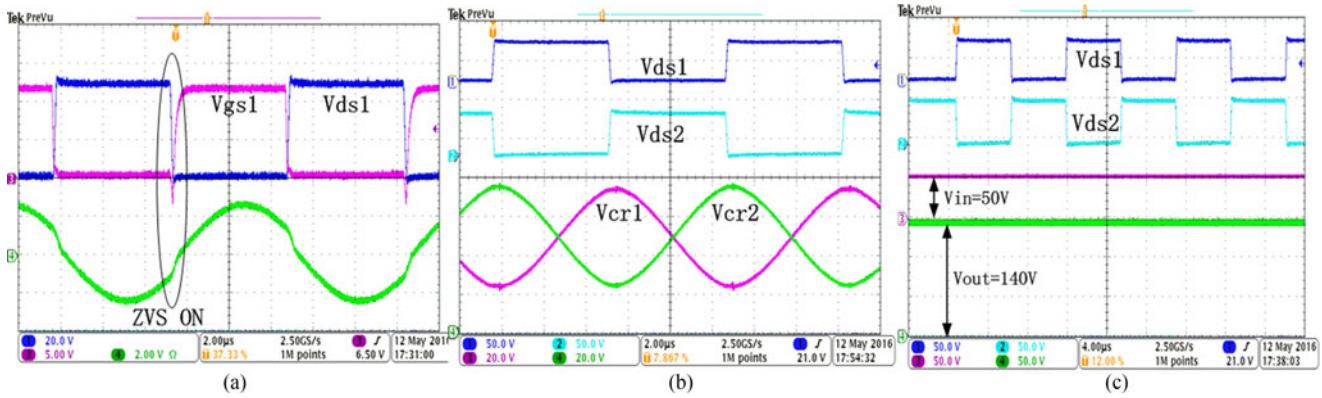

Fig. 9. Operation waveforms in $CCM_{1<F<2}$. (a) V_{gs1}, V_{ds1}, i_{Lr}. (b) V_{ds1}, V_{ds2}, V_{cr1}, V_{cr2}. (c) V_{ds1}, V_{ds2}, $V_{\rm in}$, $V_{\rm out}$.

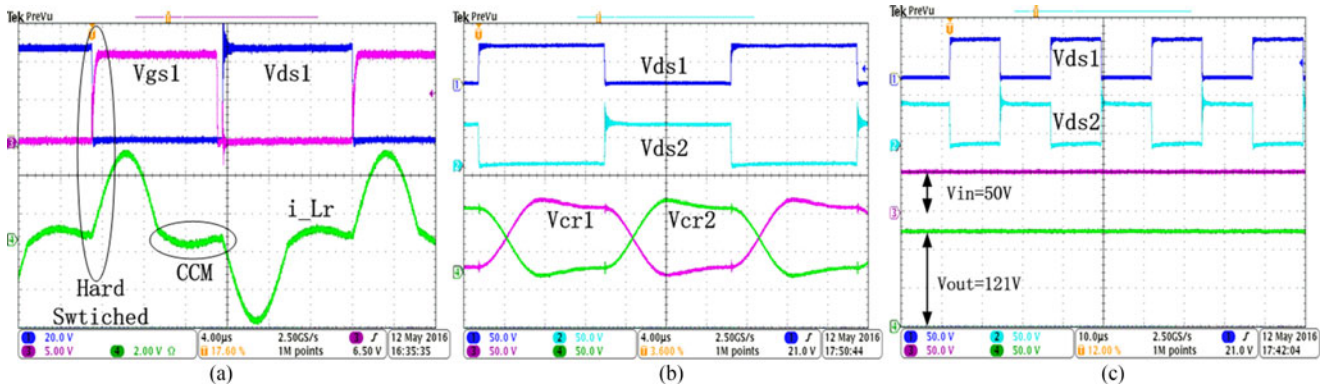

Fig. 10. Operation waveforms in $CCM_{0.5<F<1}$. (a) V_{gs1}, V_{ds1}, i_{Lr}. (b) V_{ds1}, V_{ds2}, V_{cr1}, V_{cr2}. (c) V_{ds1}, V_{ds2}, $V_{\rm in}$, $V_{\rm out}$.

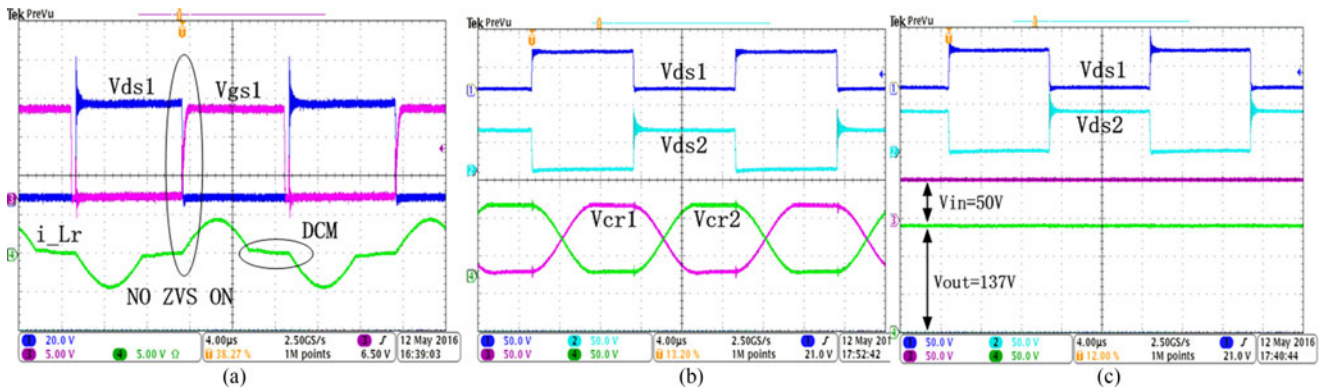

Fig. 11. Operation waveforms in $DCM_{0.5<F<1}$. (a) V_{gs1}, V_{ds1}, i_{Lr}. (b) V_{ds1}, V_{ds2}, V_{cr1}, V_{cr2}. (c) V_{ds1}, V_{ds2}, $V_{\rm in}$, $V_{\rm out}$.

The comparison of experimental and theoretical voltage-gain curve is plotted in Fig. 13(a). The solid lines represent theoretical gain curve, while the dashed lines stand for the experimental results. From the graph, the maximum gain is about 2.84, peaking at round 80 kHz which matches the boundary condition in Fig. 12. The deviations from the theoretical peak gain (3) and resonant frequency (76 kHz) are mainly caused by ESRs, diode forward voltage, parasitic capacitance and the inaccuracy of resonant capacitance and inductance. However, the experimental curve is still close to the analysis and demonstrates the wide voltage-gain range. For $Q = 0.0325$, the voltage gain changes from 2.84 to 1.96 by regulating f_s from 80 to 150 kHz. For $Q = 0.064$, the voltage gain changes from 2.73 to 1.2 by regulating f_s from 80 to 150 kHz. In addition, when $0.5 < \mathrm{F} < 1$, the converter enters $\mathrm{DCM}_{0.5<F<1}$ and the voltage-gain becomes almost a constant over a certain frequency range, seen from the dashed blue line. In practice, this unregulated region will be avoided by operating the RTBSC above the resonant frequency.

In Fig. 13(b), the curve of measured efficiency versus frequency is plotted. When $0.5 < \mathrm{F} < 1$, the transistors are

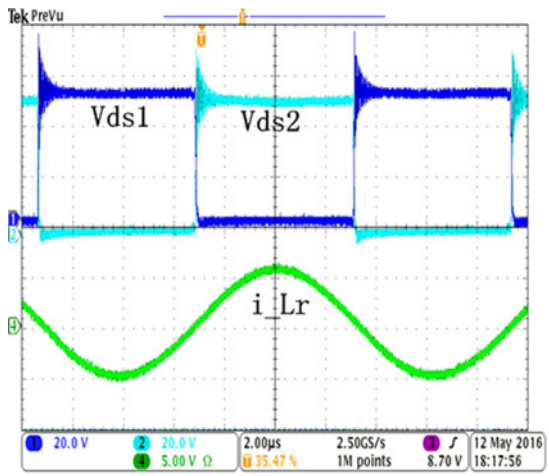

Fig. 12. Boundary condition—$f_s = 80$ KHz.

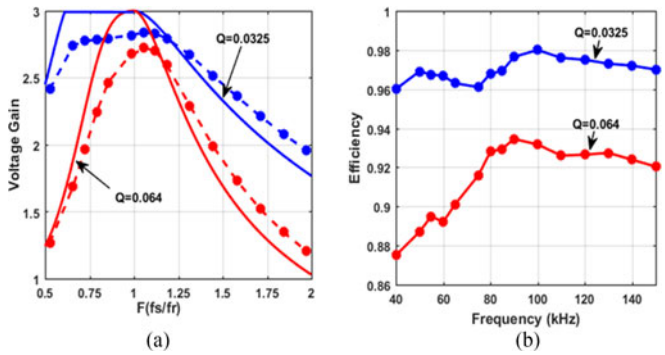

Fig. 13. Open loop results of RTBSC. (a) Voltage-gain. (b) Efficiency.

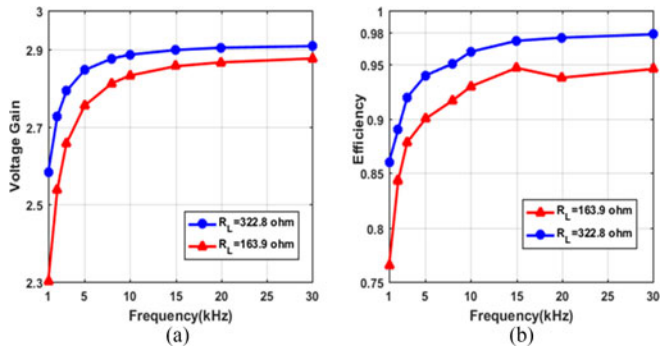

Fig. 14. Experimental results of TBSC. (a) Voltage-gain. (b) Efficiency.

hard-switched, deteriorating the overall efficiency. When $1 <$ F < 2, the transistors and diodes are soft switched, reducing the switching loss largely. In addition, based on the analysis in Section IV, the RMS current stress in $0.5 <$ F < 1 is higher, causing higher conduction loss as well. As a result, the overall efficiency below f_r is lower than that above f_r, which can be seen from Fig. 13(b). Aside from the unregulated issue, this is another reason that the RTBSC will be operating in $1 <$ F < 2.

In comparison, a traditional 3X TBSC converter was built with the same voltage level and power level. In Fig. 14(a), the voltage-gain curves of traditional 3X TBSC converter under

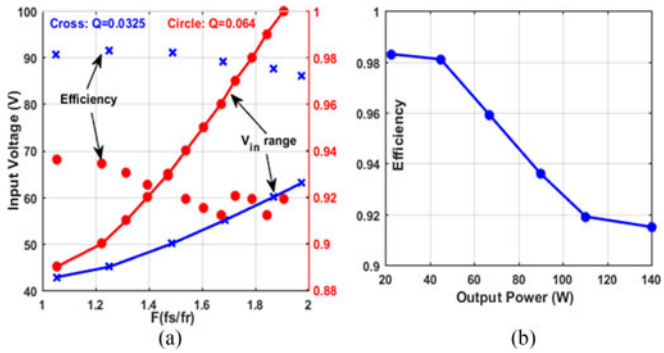

Fig. 15. Closed loop results of RTBSC. (a) Input voltage range. (b) Efficiency versus power.

different load conditions are shown. Only frequency range of 1 k–30 kHz is shown in details, because the capacitors are partially charged and thus the voltage-gain can be regulated in this region. After 30 kHz, the voltage-gain will become almost a constant (30 k–60 kHz) and then start decreasing as the frequency increasing (>60 kHz) due to hard-switched operation. Even in the low-frequency range, the voltage-gain range is much narrower than the proposed RTBSC. More importantly, the efficiency of SC converter is directly proportional to the voltage-gain [18], so the overall efficiency is poor when the voltage-gain is low, as shown in Fig. 14(b). To sum up, the traditional TBSC is more suitable for fixed-voltage-gain, low-frequency-operation and high-power-level (when conduction loss is dominant) applications. In contrast, the proposed RTBSC is more suitable for wide-voltage-gain-range, low-power-level and high-frequency-operation (when switching loss is dominant) applications. Considering the soft-switching operation of RTBSCs, by proper design of the resonant frequency to a much higher value, the component size of the RTBSC can be reduced significantly, while not sacrificing the overall efficiency or regulation range.

A voltage feedback loop is added by TMS320F28335. In the closed loop test, the output voltage is regulated to be 120 V, while the input voltage or load current is varied. The converter is operating in $1 <$ F < 2 by proper selection of upper/lower limit of f_s. The practical lower limit can be obtained from Fig. 12, in which the current waveform is a pure sinusoidal wave, i.e., $f_r = 80$ kHz. Then the upper limit is $2f_r = 160$ kHz.

Fig. 15(a) shows the input-voltage range when $V_{\rm out}$ is regulated to be 120 V. The left y axis represents the input voltage, while the right one stands for the efficiency at this input voltage value. The line with cross is denoted as lighter load ($Q = 0.0325$, $I_{\rm load} = 0.37$A), at which the input-voltage range is 42.8–63 V, but the efficiency is higher due to less conduction loss. The line with circle is denoted as heavier load ($Q = 0.064$, $I_{\rm load} = 0.73$A), at which the input-voltage range is 45–100 V. As noted, the efficiency is well above 91%, even though the input voltage varies widely.

Fig. 15(b) shows the converter efficiency versus output power. $V_{\rm in}$ is 50 V and $V_{\rm out}$ is regulated to be 120 V. As shown, the peak efficiency is 98.3% at 23 W and then the efficiency is decreasing to 90.7% at 140 W. The estimated power loss distribution at 90 W is shown in Table III. In practice, the transistors can be regarded

TABLE III
POWER LOSS ANALYSIS

Device	ESR or V_f	RMS current	Average current	Power loss	Power loss ratio
$S_{1,2}$	31 mΩ	2.4 A	–	0.3 6 W	5.9%
D_{1-4}	0.8 V	–	1.2A	3.84 W	62.5%
$C_{r\,1,2}$	100 mΩ	1.7 A	–	0.58 W	9.4%
L_r	100 mΩ	3.4 A	–	1.2 W	19.5%
$C_{1a,1b}$	100 mΩ	0.9 A		0.16 W	2.7%

TABLE IV
COMPONENT COUNTS COMPARISON

Topology	Gain	Switch	Floatingswitch	Diode	Intermediate Cap. banks
Dickson[2]	3	2	1	4	3
SPC[4]	3	8	4	6	4
TBSC[34]	3	2	1	4	4
[5]	3	6	5	0	2
[6]	3	12	11	0	6
[7]	3	7	5	0	2
[21]	3	12	9	0	5
RTBSC	1–3	2	1	4	2

+2 small resonant Cap. and 1 resonant inductor

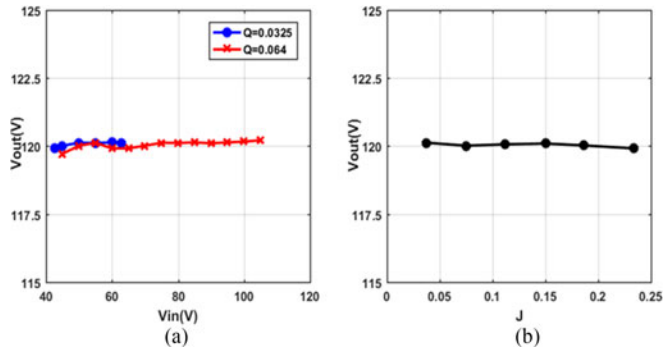

Fig. 16. Regulation curve. (a) Line regulation. (b) Load regulation.

as ZVS turn-OFF due to its parasitic capacitance. Therefore with soft-switching operation of transistors and diodes, switching loss is estimated to be zero and only conduction loss exists. As listed, the loss of the diodes is dominant and the loss of resonant inductor is second highest.

Fig. 16 shows the line regulation curve and load regulation curve under the closed-loop. From Fig. 16(a), the RTBSC can provide line regulation against input voltage changes under different load conditions, and the output voltage can maintain at about 120 V. From Fig. 16(b), the RTBSC can provide load regulation against load changes, and the voltage gain can maintain at about $120\,\mathrm{V}/50\,\mathrm{V} = 2.4$.

Fig. 17 shows the waveforms of load transient response. In Fig. 17(a), V_{in} is set to be 50 V. When the load current is switched from 0.19A to 0.34A with a slew rate of $3.8 \times 10^4\,\mathrm{A/s}$, V_{out} is regulated back to 120 V after about 50 ms. Similarly, when the load current is switched from 0.34 A to 0.19 A, the regulation time is about 70 ms, shown in Fig. 17(b).

Fig. 18 shows the waveforms of line transient response. In Fig. 18(a), the load current is fixed at 0.19 A. When V_{in} is

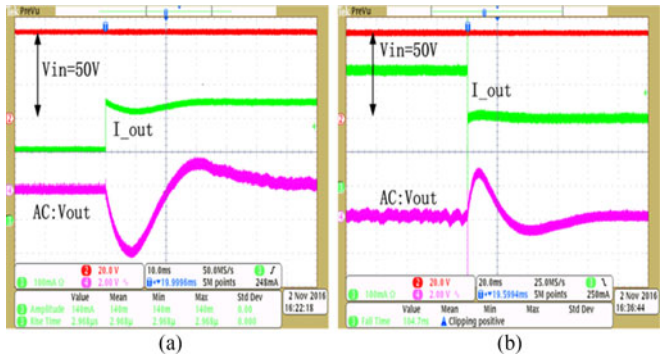

Fig. 17. Load transient response. (a) Uploading current. (b) Downloading current.

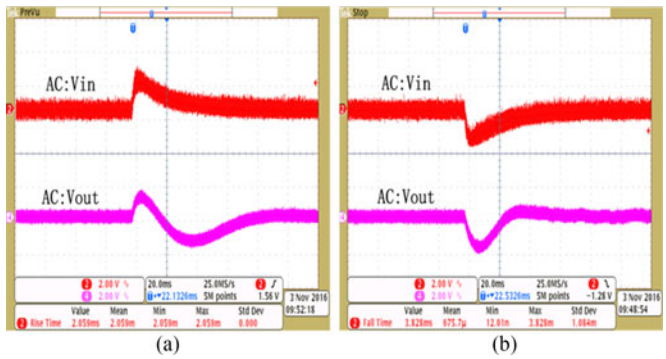

Fig. 18. Line transient response. (a) Up input voltage. (b) Down input voltage.

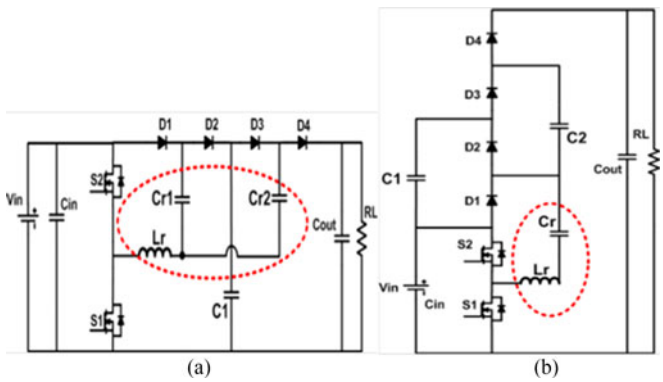

Fig. 19. Topology extension. (a) Dickson SC. (b) Ladder SC.

switched from 50 V to 52 V with a slew rate of $9.71 \times 10^2\,\mathrm{V/s}$, V_{out} is regulated back to 120 V after about 70 ms. Similarly, when V_{in} is switched from 50 V to 48 V with a slew rate of $5.22 \times 10^2\,\mathrm{V/s}$, the regulation time is about 50ms, as shown in Fig. 18(b).

VI. TOPOLOGY EXTENSION AND COMPARISON

A. Topology Extension

The resonant tank and operation principle can be transplanted to some other conventional SC topologies, such as Dickson SC converters and Ladder SC converters as shown in Fig. 19. The resonant tank is highlighted in a red circle. The operation principle is similar to that of the RTBSCs. The continuous resonant

TABLE V
CONVERTER PROPERTY COMPARISON

Topology	Floating output	Power direction	VS on switch	VS on diode	VS on Cap.
Dickson [2]	No	Uni.	Vin	Vin	Vin/2Vm
SPC [4]	No	Uni.	Vin	Vin	Vin
TBSC[34]	Yes	Uni.	Vin	Vin	Vin
[5]	No	Bi.	Vin	N/A	Vin/2Vm
[7]	No	Bi.	Vin	N/A	Vin
[8]	No	Bi.	Vin/2Vin	N/A	Vin/2Vm
[21]	Yes	Bi.	Vin	N/A	Vin
RTBSC	Yes	Uni.	Vin	Vin	Vin

current introduces good regulation capability and ZVS operation. The detailed analysis will be covered in our future work.

B. Topology Comparison

In this part, the component counts, voltage stress (VS) and some properties of the proposed RTBSC are compared with some previous works. All converters have the maximum gain of 3 and the comparison is summarized in Table IV and V.

As shown, the proposed RTBSC has low switch counts and low intermediate capacitor counts, whose costs are typically high. In addition, the VS on all switches, diodes, and capacitors is low, equal to the input voltage $V_{\rm in}$. However, the output of RTBSC is floating, so the control circuit and driving circuit should be designed carefully to reduce the effect of EMI. Furthermore, the diodes of RTBSC could be replaced by active switches to achieve bidirectional power flow, and the semiconductor counts are still lower than those listed bidirectional converters.

VII. CONCLUSION

In this paper, a family of RTBSCs with ZVS operation and a wide regulation range is proposed. The resonant tank is composed of one inductor and two small capacitors for all RTBSCs. Some comprehensive characteristics of this family including operation modes, voltage-gain curves, output characteristics, and voltage/current stresses of resonant tank are analyzed over $0.5 < \mathrm{F} < 2$. When $1 < \mathrm{F} < 2$, the family of RTBSC features ZVS operation and good regulation capability. In practice, the converter is ensured to be operating in this region referred to the derived gain curves and output characteristics. A 3X RTBSC prototype with peak efficiency of 98.3% was designed and built. The analysis is verified by both simulation and experimental results.

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