Thermal Stresses Relief Carrier-Based PWM Strategy for Single-Phase Multilevel Inverters

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***Abstract*—Enhancing power cycling capability of power semiconductor devices is highly demanded in order to increase the long-term reliability of multilevel inverters. Ageing of power switches and their cooling systems leads to their accelerated damage due to excess power losses and junction temperatures. Therefore, thermal stresses relief (TSR) is the most effective solution for lifetime extension of power semiconductor devices. This paper presents a new TSR carrier-based pulse width modulation (TSRPWM) strategy for extending the lifetime of semiconductor switches in single-phase multilevel inverters. The proposed strategy benefits the inherent redundancy among switching states in multilevel inverters to optimally relieve the thermally stressed device. The proposed algorithm maintains the inverter operation without increased stresses on healthy switches and without reduction of the output power ratings. In addition, the proposed algorithm preserves voltage balance of the dc-link capacitors. The proposed strategy is validated on a single-phase five-level T-type inverter system with considering different locations of thermal stresses detection. Experimental prototype of the selected case study is built to verify the results. Moreover, comparisons with the most featured strategies in literature are given in detail.**

***Index Terms*—Lifetime extension, long-term reliability, multilevel inverter, pulse width modulation (PWM), thermal stresses relief (TSR).**

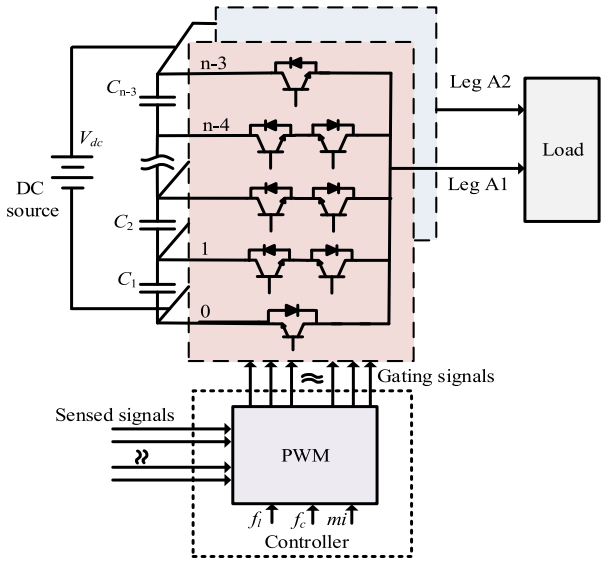

Fig. 1. Schematic diagram of PWM-controlled full bridge *n*-level T-type inverter.

I. Introduction

POWER electronic converters play an important role in several applications for power generation, storage, delivery, and utilization as they acquire higher efficiency and performance. However, power electronics have evinced high failure rates among system components that put their reliability enhancement and lifetime prolongation of major concerns [1]. Power semiconductor devices represent one of the critical elements that define the overall system reliability and robustness [2]. According to [3], thermal stresses including high junction temperature and large junction temperature cycling are the prime root causes of semiconductor failures. In regards, several studies have been performed on reliability of semiconductor devices related to thermal stresses such as failure mechanisms, lifetime models, and thermal management techniques [4].

A generalized diagram of *n*-level full bridge T-type single-phase inverters is shown in Fig. 1. For any *n*-level T-type inverter, there are *n*–3 dc-link capacitors that create different output voltage levels. Then, power semiconductor devices are controlled to output these voltage levels to the load. Power semiconductor devices are usually subjected to continuous dynamic loading that results from power and temperature cycling. These repeated loadings in addition to the large mismatch of coefficients of thermal expansion of power semiconductor layers cause thermo-mechanical fatigue in the form of bond wires lifting off and solder delamination [5]. These ageing effects of power semiconductor devices gradually increase the equivalent thermal resistance of the device, which is reported at failure to be about 20% above its normal value. Then increased thermal stresses are expected that fasten the failure of the device. In addition, ageing of the forced cooling system of power semiconductor devices can lead to the same effects. Therefore, thermal stresses relief (TSR) of semiconductor devices is highly required if increased thermal stresses have been detected in one of the power semiconductor devices.

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Several strategies of thermal stresses management and relief are provided in the literature [6]–[17]. Most of existing conventional strategies rely on derating of the output power [6] or using costly cooling systems [7]. When the operating junction temperature of the semiconductor device exceeds the predefined safety limit, the reference output current of the inverter is reduced and the power losses through the affected device are reduced as a result [6]. A similar strategy for reliability improvement of PV inverters through limiting their maximum feed power is introduced in [8]. However, in this technique, the tested inverter is not operated with its full scale output power and the maximum power point (MPP) cannot be tracked efficiently in renewable energy applications. On another side, the junction temperature of semiconductor devices can be reduced by adding an additional forced cooling device between the thermal grease of the device and the heatsink [7]. However, the added devices increase the system cost and volume. Furthermore, additional power is required to operate the cooling device. Therefore, cost effective thermal stress relief methods for power semiconductor devices are highly needed in order to minimize the wasted energy due to derating of the inverter and the costly added cooling devices.

Another alternative method for TSR of power semiconductor devices is based on optimum design of modulation techniques of inverters. The pulse width of power switches in interleaved converters is controlled to achieve balanced thermal stresses on Insulated-gate bipolar transistor (IGBT) devices through percentage share of different interleaved modules [9]. However, full scale components are needed for each interleaved module that increase dramatically the total system cost in these methods.

The redundancies between the switching states of multilevel inverters represent another cost effective solution for thermal management of IGBT devices [10]. Nevertheless, conventional neutral point clamped (NPC) inverters suffer from unequal loss distribution among devices. Loss redistribution modulation techniques are developed to address this problem [11]. Additionally, the active NPC inverters with modified modulation techniques are developed to achieve losses and stresses reductions [11], [12]. However, the cost and the number of IGBTs in active NPC inverters are high compared to conventional ones. Discontinuous pulse width modulation (DPWM) techniques have been developed in the literature to improve the total efficiency of multilevel inverters by reducing switching transitions of semiconductor devices [13], [14]. A DPWM method for power cycling reliability improvement in NPC inverters is presented in [13]. However, these modulation techniques cannot effectively provide TSR for a particular semiconductor device if increased thermal stresses have been detected. Furthermore, DPWM techniques provide dissimilar thermal stresses on different system components.

The same concept with the same features is applied on space vector PWM (SVPWM) method that is featured with more flexibility [15]. A higher efficiency discontinuous SVPWM method is achieved through avoiding switching the leg with the highest current [15]. Another SVPWM method for lifetime extension of thermally overheated semiconductor devices is developed in [16] and [17]. These methods provide thermal relief for a particular semiconductor device without compromise of the inverter output ratings. However, additional voltage stresses on power components are introduced to achieve voltage balance over the dc-link capacitors. Moreover, the complexity of calculations and implementation of SVPWM techniques increases at higher number of levels in order to define the operating region and to calculate the dwelling times of voltage vectors.

Stimulated by the above-mentioned issues, a new carrier-based TSR PWM (TSRPWM) strategy is proposed in this paper in order to alleviate thermally stressed semiconductor devices in single-phase multilevel inverters. The proposed algorithm provides the benefits of: simple implementation without increased complexity at higher number of levels; no need for output ratings compromise; and cheap solution without extra system cost. In addition, the proposed strategy ensures high performance regarding voltage balance of dc-link capacitors of the multilevel inverter.

The paper is organized as follows: Section II explains the principles of thermal stress relief and lifetime extension of power devices. Section III presents the operation of single-phase five-level inverters. Section IV provides in details the proposed TSRPWM strategy and its generalized implementation. The feasibility and simulation results of the proposed TSRPWM strategy are investigated on a five-level T-type inverter system in Section V. The experimental prototype validation of the proposed strategy is given in Section VI. Section VII provides performance criteria comparison of the proposed TSRPWM strategy with the most featured methods in the literature. The conclusions are summarized in Section VIII.

II. Thermal Stresses and Lifetime Extension

Several modulation techniques can be used to drive multilevel inverters, wherein power semiconductor devices are subjected to different conduction times and switching transitions for each particular modulation technique. Fig. 2(a) shows the relationship between different models of semiconductor devices and modulation techniques. For the sake of accurate modeling for power losses $P_{\rm loss}$ through semiconductor devices, datasheet-based losses calculation methods are mostly preferred and the method in [18] is used in the paper. Then, using thermal models of semiconductor devices, the operating junction temperature T_j and junction temperature cycling ΔT_j can be obtained for the device as [19]

$$T_j = T_h + P_{\rm loss}.\sum_{i=1}^{4} R_{{\rm th}(i)} + P_{\rm loss}.R_{{\rm th}(c-h)} \tag{1}$$

$$\Delta T_j = 2.P_{\rm loss}.\sum_{i=1}^{4} R_{{\rm th}(i)}.\frac{\left(1-e^{-\frac{t_{\rm on}}{\tau_{{\rm th}(i)}}}\right)^2}{1-e^{-\frac{t_e}{\tau_{{\rm th}(i)}}}} \tag{2}$$

where T_h denotes to the operating heatsink temperature in Celsius, and $R_{{\rm th}(i)}$ and $\tau_{{\rm th}(i)}$ represent the thermal resistances and thermal time constant for the ith layer of the thermal model between the junction and case of the semiconductor device. $R_{{\rm th}(c-h)}$ represents the thermal resistance between case and heatsink of the device. Whereas $t_{\rm on}$ is the time of on-state of the power IGBT during the output current fundamental period t_e.

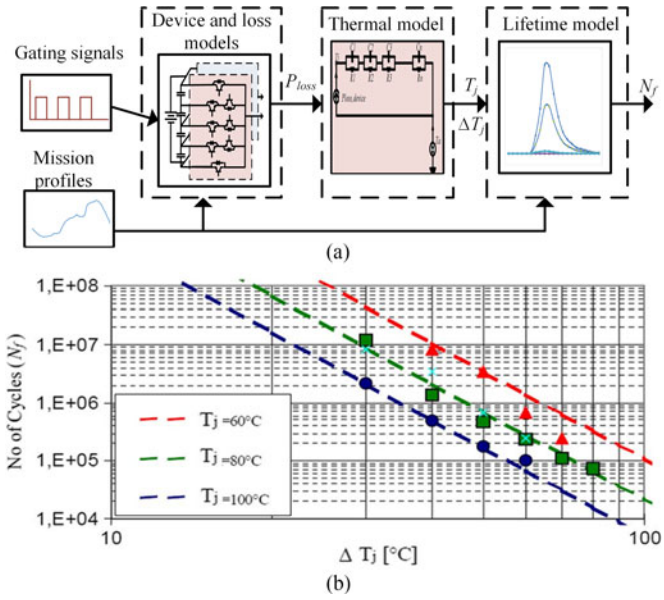

Fig. 2. Various models of power semiconductor device: (a) Relationship between models, and (b) N_f versus T_j and ΔT_j [20].

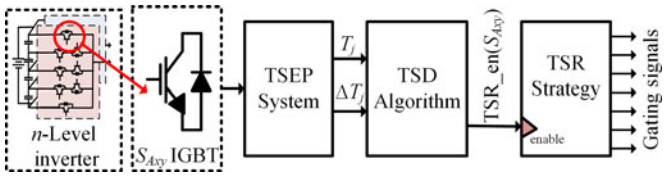

Fig. 3. Schematic diagram of the thermal stresses relief (TSR) system.

The number of cycles to failure N_f represents a good measure for estimating the expected lifetime for semiconductor devices and can be modeled by the well-known Coffin–Manson model as follows [19]:

$$N_f = A.(\Delta T_j)^{\alpha} \cdot \exp\left(\frac{E_a}{K_b T_j}\right) \tag{3}$$

where α and A are constants that can be obtained from power cycling tests, E_a represents activation energy, and K_b represents Boltzmann constant. From (1), the main factors that affect the lifetime of semiconductor devices are the thermal stresses over the device (T_j and ΔT_j), which are mainly affected by the power losses through the device on-state duration of the output current of the inverter. The effect of thermal stress relief on the lifetime of semiconductor devices is shown in Fig. 2(b) [20]. It is found that a small decrease of thermal stresses leads to a great enhancement of the semiconductor device lifetime.

Fig. 3 shows a schematic diagram of a complete thermal relief system for IGBT device S_{Axy} (where *x* denotes to leg number 1, or 2, and *y* denotes the switch location 1, 2, . . . in the leg) in the multilevel inverter. The TSR system for power semiconductor devices has three main steps:

1) estimating thermal stresses using thermo-sensitive electrical parameters (TSEP) [21] for obtaining T_j and ΔT_j of the device;

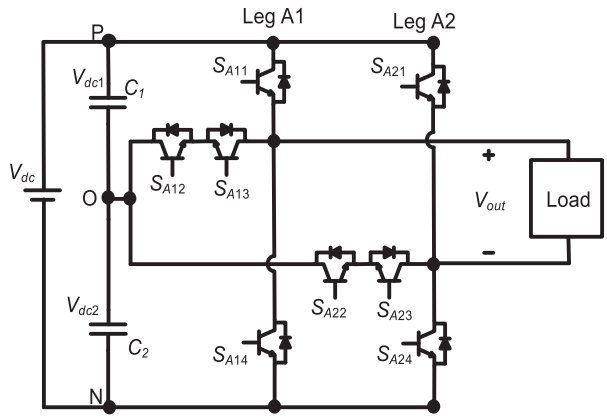

Fig. 4. Single-phase full bridge T-type inverter system.

2) applying thermal stresses detection (TSD) algorithm of the device;
3) activating TSR algorithm.

The recently developed TSEP methods present a good solution to estimate the thermal stresses of semiconductor devices. Then, the estimated T_j and ΔT_j are fed to the TSD system that compares the estimated T_j and ΔT_j with the maximum operating thermal stresses ($T_{j,\mathrm{limit}}$ and $\Delta T_{j,\mathrm{limit}}$), which are provided by devices' manufacturers. Finally, a flag representing TSR enable ($\mathrm{TSR\_en}(S_{\mathrm{Axy}})$) signal is fed to the TSR algorithm to alleviate the thermal stresses of the affected device S_{Axy}, where $\mathrm{TSR\_en}(S_{\mathrm{Axy}})$ equals to 1 if TSR is required and 0 otherwise. In this paper, the problem of the increased TSD has not been tackled. Additionally, it is emulated and implemented by an external ON/OFF switch.

III. Single-Phase Five-Level Inverter Operation

Fig. 4 shows the power stage of a single-phase five-level T-type inverter. Two equal dc-link capacitors are used to generate the voltage levels, which are connected to the load through the IGBT switches. Each leg of the inverter can generate either V_{dc1}, 0, or $-V_{\mathrm{dc2}}$ with respect to neutral point O by connecting the output to the inverter's points P, O, or N, respectively. Therefore, the two legs of the inverter are combined to generate five levels at the output of the inverter that are $+(V_{\mathrm{dc1}} + V_{\mathrm{dc2}})$, $+V_{\mathrm{dc1}}$, 0, $-V_{\mathrm{dc2}}$, and $-(V_{\mathrm{dc1}} + V_{\mathrm{dc2}})$. The controller is required to maintain voltage balance of the two dc-link capacitors ($V_{\mathrm{dc1}} = V_{\mathrm{dc2}} = 0.5V_{\mathrm{dc}}$), and the output levels at this case will be ($+V_{\mathrm{dc}}$, $+0.5V_{\mathrm{dc}}$, 0, $-0.5V_{\mathrm{dc}}$, and $-V_{\mathrm{dc}}$).

The modulation technique is employed to generate various levels of the inverter output voltage. Most common technique is the level-shifted PWM modulation [22], where *n*–1 carriers are needed to generate *n*-levels at the output. The modulating signal and the carrier signals for five-level inverters are shown in Fig. 5. The gating signals for the IGBT switches are generated by continual comparison of the modulating signal V_m with the four carrier signals $V_{\mathrm{cr1}} - V_{\mathrm{cr4}}$. According to the amplitude and polarity of the modulating signal V_m, the line period of V_m is divided into six operating regions R1–R6 as clarified in Fig. 5. Two different voltage levels are generated in each region. Fig. 6

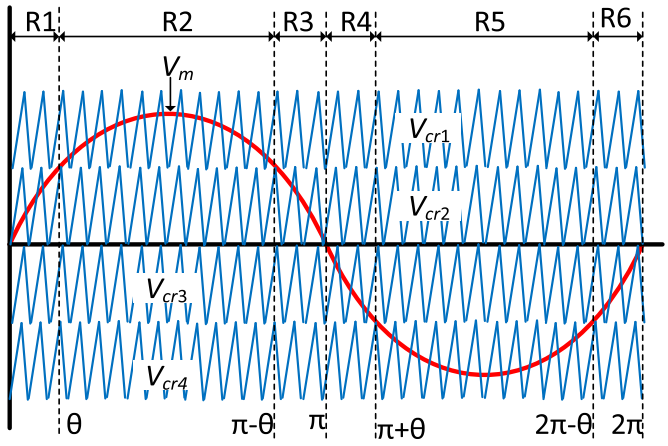

Fig. 5. Carrier-based PWM for single-phase five-level inverters.

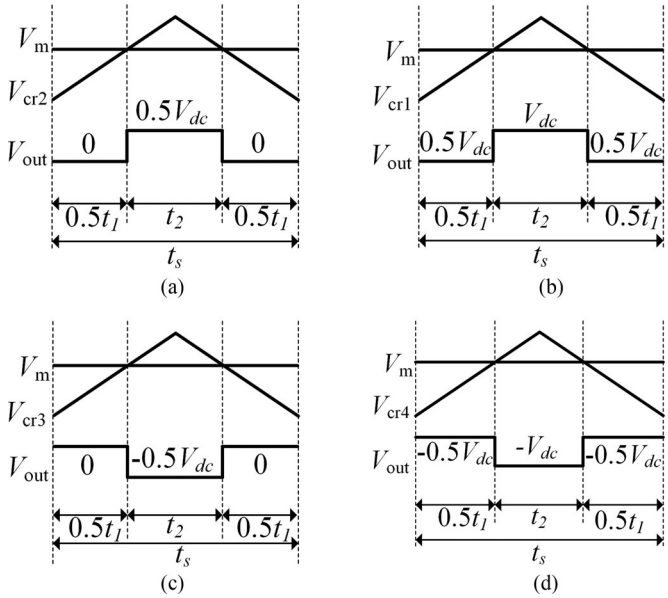

Fig. 6. Output voltages of the inverter at regions: (a) R1 and R3, (b) R2, (c) R4 and R6, and (d) R5.

shows the generated voltage levels at each region R1–R6 of the inverter output. For instance, the voltage levels 0 and $0.5V_{\rm dc}$ are generated in region R1 with dwelling times of t_1 and t_2, respectively.

Table I summarizes inverter switching combinations with their effects on the voltages of dc-link capacitors for generating the output levels of the inverter (where ↑ represents charging mode, ↓ represents discharging mode, and – represents no effects on capacitor voltages). It is clear from Table I that each of $+0.5V_{\rm dc}$ and $-0.5V_{\rm dc}$ voltage levels can be implemented by using two different paths with different switch combinations and different effects on the voltages of dc-link capacitors. Moreover, there are three different paths to implement zero voltage level. Therefore, there are a degree of freedom to select different switches and capacitors combinations to synthesize the output voltage levels, and of course extra freedom can be obtained at higher *n*-levels inverters. This redundancy property can be utilized to enhance the performance of multilevel inverters. The optimum selection of the redundant states is employed

TABLE I
SWITCH COMBINATIONS FOR DIFFERENT LEVELS OF A FIVE-LEVEL INVERTER

Amp.	S_{A11}	S_{A12}	S_{A13}	S_{A14}	S_{A21}	S_{A22}	S_{A23}	S_{A24}	$V_{\rm dc1}$	$V_{\rm dc2}$
$V_{\rm dc}$	1	0	0	0	0	0	0	1	–	–
$0.5V_{\rm dc}$	1	0	0	0	0	1	1	0	↓	↑
	0	1	1	0	0	0	0	1	↑	↓
0	1	0	0	0	1	0	0	0	–	–
	0	0	0	1	0	0	0	1		
	0	1	1	0	0	1	1	0		
$-0.5V_{\rm dc}$	0	1	1	0	1	0	0	0	↓	↑
	0	0	0	1	0	1	1	0	↑	↓
$-V_{\rm dc}$	0	0	0	1	1	0	0	0	–	–

to achieve different objectives such as voltage balance of dc-link capacitors, reduction of Total harmonic distortion (THD) in the outputs, reducing switching power losses, fault tolerant operation, etc.

IV. PROPOSED STRATEGY

The aforementioned analysis of the redundancy property in multilevel inverters shows the following degrees of freedom to optimize their performance: 1) thermal stress relief of IGBT switches can be obtained by redistributing their power losses through proper selection of redundant switching states; and 2) the charge of dc-link capacitors can be balanced by appropriately selecting the charge/discharge switching states. Accordingly, this paper proposes a new lifetime extension method for alleviating thermally stressed semiconductor devices in multilevel inverters. The proposed TSRPWM strategy is based on a carrier-based PWM method.

The proposed TSRPWM method can be explained as follows: taking region R2 as an example and according to the required voltage levels in region R2 as in Fig. 6(b) in addition to their required switch combinations as in Table I, there are two different switching sequences in this region due to the existence of two different paths to generate $0.5\ V_{\rm dc}$ voltage level. Fig. 7 shows the gating pulses for the two allowable switching sequences, called $S_{\rm eq1}$ and $S_{\rm eq2}$ in region R2. It can be observed that different gating pulses are applied in each sequence. For example, S_{A11} is held ON in $S_{\rm eq1}$ for the switching period t_s, and it is subjected to only conduction losses as a result. Whereas in $S_{\rm eq2}$, it is switched ON for period t_2 and turned OFF for period t_1. Consequently, S_{A11} is subjected to conduction losses during period t_2 and switching losses due to ON/OFF transitions. However, the total power losses vary with different locations of the modulating signal V_m in line period and with different modulation indices *mi* as well. The same analysis and observations can be done for other switches and for other operating regions. In region R1, there are six switching sequences that can be obtained for synthesizing V_m, and different switch pulses are applied for each switching sequence.

Therefore, if an increase of the thermal stresses in one of the IGBT devices $S_{\rm Axy}$ has been detected ($\rm TSR\_en(S_{Axy}) = 1$), the proposed TSRPWM strategy is applied. Fig. 8 shows a generalized flowchart for implementing the proposed TSRPWM

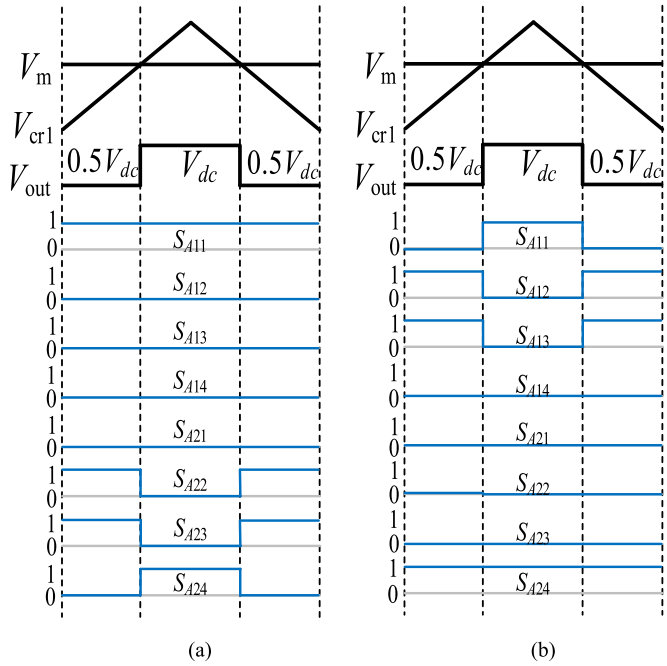

Fig. 7. Gating pulses for IGBT switches in region R2 at: (a) S_{eq1} and (b) S_{eq2}.

strategy for the *n*-level inverter. First, the modulating signal V_m is generated using the required modulation index (*mi*), and line frequency f_l. While, *n*–1 carrier signals V_{cr} are generated using the number of levels *n* and the desired switching carrier frequency f_c of the inverter. Second, the amplitude and sign of V_m define the current operating region R. The desired output voltage levels are performed by comparing the modulating signal V_m with the *n*–1 carriers V_{cr}. Third, the proposed algorithm checks if there are any TSD in the IGBT switches (if $\mathrm{TSR\_en}(S_{\mathrm{Axy}}) = 1$). Finally, the proposed algorithm has to properly select the redundant switching states that achieve the desired performance and the operating mode of the inverter as it is explained in the following parts.

The inverter has two modes of operation under the proposed strategy namely: 1) normal mode (NORM mode) of operation (if $\mathrm{TSR\_en}(S_{\mathrm{Axy}}) = 0$); 2) thermal stress relief mode (TSR mode) of operation (if $\mathrm{TSR\_en}(S_{\mathrm{Axy}}) = 1$). In NORM mode, the redundant switching states are selected so as to achieve voltage balance of dc-link capacitors. If $V_{\mathrm{dc1}} > V_{\mathrm{dc2}}$, the switching states of C_1 discharge are applied. In contrast, if $V_{\mathrm{dc2}} > V_{\mathrm{dc1}}$, the switching states that discharge C_2 are applied. In case of thermal overstress detection TSD in one of the IGBT devices (TSR mode), the proposed algorithm defines the *m* valid switching sequences in the current operating region R in the same way as the aforementioned sequences in region R2. Afterwards, a cost function of the power losses $P_{\mathrm{loss}}(S_{\mathrm{Axy}})$ for the stressed IGBT device is implemented for all valid *m* switching combinations. These calculations of P_{loss} can be implemented in parallel in Field-programmable gate array (FPGA) implementation in order to reduce the required execution time at higher *n*-level inverters due to the increased number of redundant states. Finally, the optimizer selects the optimum switching combination of voltage levels that has the minimum power losses through

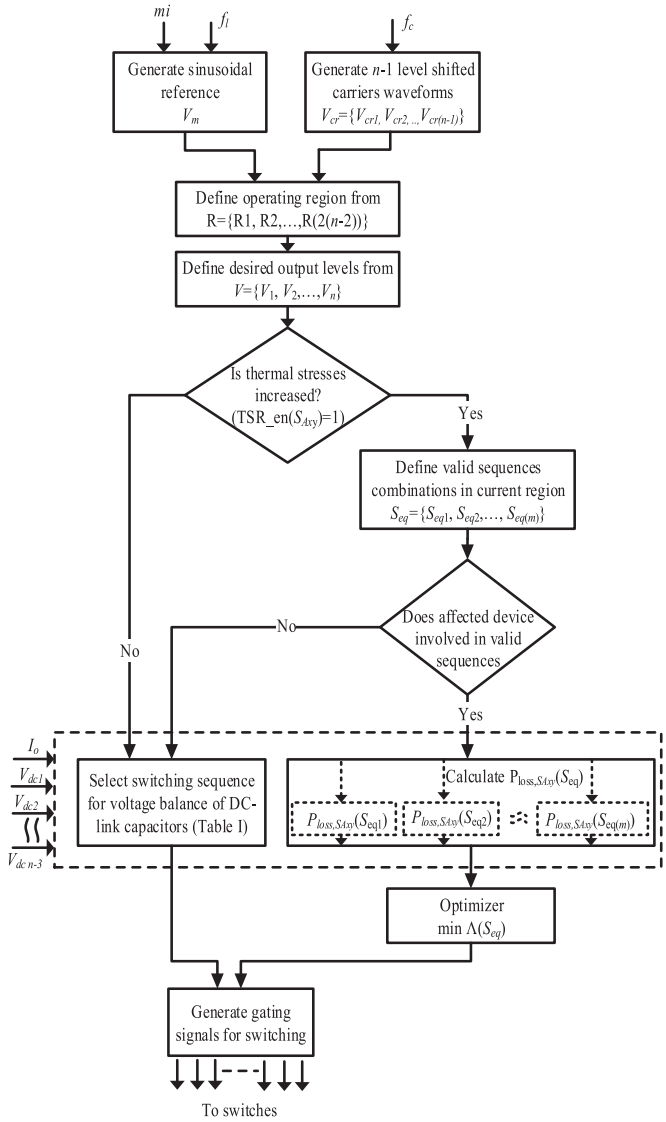

Fig. 8. Generalized implementation of the proposed strategy.

the thermally stressed device. In other regions of the line period that do not utilize the affected device, the optimum switching sequence for achieving voltage balance of dc-link capacitors is selected.

The selected redundant switching states can provide TSR to the thermally stressed IGBT devices and balance the voltages of dc-link capacitors in the same line period. It can be realized from the implementation of the proposed TSRPWM strategy in Fig. 8, its procedures are very easy and simple for hardware implantation compared to the complex calculations in SVPWM techniques in [16] and [17]. Moreover, the proposed TSRPWM can achieve strong alleviation for the affected device by optimally selecting the redundant switching states. The proposed strategy employs the redundant switching states and hence it can preserve the same output ratings, the same number of output levels, and the same output performance. In addition, the proposed strategy maintains the voltage balance over the dc-link capacitors. The proposed TSRPWM method can be applied to different inverter configurations and topologies.

TABLE II
PARAMETERS FOR SIMULATION AND EXPERIMENTAL STUDY

DC-link voltage $V_{\rm dc}$	200 V
DC-link capacitance C_1, C_2	2500 μF
Output frequency f_l	50 Hz
Switching frequency f_s	5 kHz
Output load *R, L*	10 Ω, 3 mH
Heatsink temperature T_h	60 °C
Total thermal resistance between junction and case $\Sigma R_{{\rm th}(i)}$	2.78 °C/W
Thermal resistance between case and heatsink $R_{{\rm th}(c-h)}$	1.4 °C/W

V. SIMULATION RESULTS

To verify the performance and the effectiveness of the proposed TSRPWM strategy, simulation case study has been implemented in PSIM environment. The simulation study demonstrates the ability of the proposed method to extend the lifetime of thermally stressed semiconductor devices, while maintaining voltage balance of dc-link capacitors and preserving the same output ratings. The parameters for the simulation studies are listed in Table II. The performance the proposed PWM strategy has been studied during operation in NORM and TSR modes. Two different case studies of increased TSD are considered in IGBTs S_{A11} and S_{A12} in leg A1 to evaluate the performance of the proposed strategy with different locations of TSD.

In the first case study, it is assumed that there are a TSD in S_{A11} of the inverter (TSR_en$(S_{A11}) = 1$) at time 0.25 s. Fig. 9 shows the performance of the proposed TSRPWM strategy at high modulation index (*mi*) of 0.85. It can be seen that the proposed strategy preserves the same output voltage and current of the inverter at both of NORM and TSR modes of operation. Therefore, the proposed PWM strategy maintains the inverter to continue its operation with the same output ratings of the inverter and the same output levels as well. Moreover, the voltages of dc-link capacitors remain balanced with slight increase in their ripples. However, the capability of the proposed algorithm to extend the lifetime of the thermally overstressed semiconductor device S_{A11} can be proved by the waveforms of its gating pulses. It is clear that the proposed algorithm has a different switching pattern in the affected device at TSR mode than its switching pattern under NORM mode. This can be interpreted as the proposed algorithm optimizes the power losses through the thermally overstressed switch S_{A11}.

The behavior of the proposed TSRPWM strategy with TSD in S_{A11} at low *mi* of 0.45 is shown in Fig. 10. In the operation with *mi* < 0.5, the inverter operates only in four regions of R1, R3, R4, and R6 and the output voltage in this case is synthesized by only three vectors $+0.5V_{\rm dc}$, $-0.5V_{\rm dc}$, and zero voltage levels. According to the switching states in Table I, utilizing $V_{\rm dc1}$ in positive half-cycle of output voltage, utilizing $V_{\rm dc2}$ in negative half-cycle, and utilizing switching sequences of zero voltage level that do not contain S_{A11} will help to reduce the power losses in the affected device S_{A11} to zero. Therefore, the gating pulses of the affected device S_{A11} are switched OFF and the switch is totally relieved. In addition, the voltage balance of dc-link capacitors is naturally performed as the two sources are

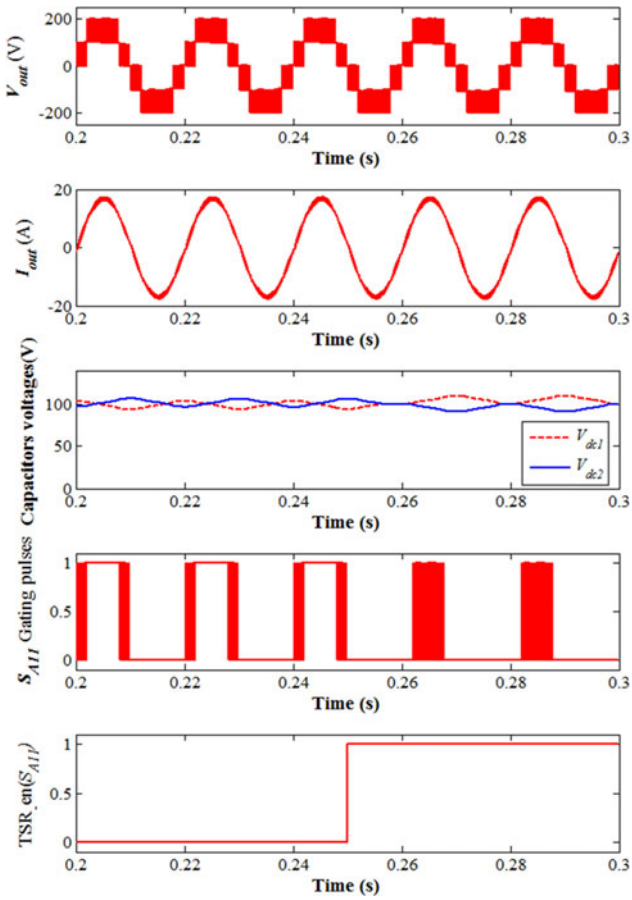

Fig. 9. Simulation results of the proposed strategy at TSD in S_{A11} at $mi = 0.85$.

equally utilized. It can be seen from Fig. 10 that the proposed algorithm preserves the same ratings of $V_{\rm out}$ and $I_{\rm out}$. Moreover, voltages of dc-link capacitors $V_{\rm dc1}$ and $V_{\rm dc2}$ are kept balanced with slight increase in their ripples.

The lifetime of power semiconductor devices is mainly affected by their junction temperature and temperature fluctuation [19]. A comparison of the power losses through the thermally stressed device under both of NORM and TSR modes at different modulation indices is shown in Fig. 11. It can be seen that a significant reduction of the power losses through the affected device S_{A11} can be obtained by the proposed TSRPWM strategy at whole modulation indices range. Thereby, relief of thermal stresses of the affected device is obtained, while maintaining full-rated operation of the inverter. Fig. 12(a) shows the junction temperatures of the affected devices under NORM mode and overstressed mode at different modulation indices using the thermal parameters in Table II. As a direct benefit of reducing the power losses through the affected device S_{A11}, the proposed TSRPWM method provides a lower T_j and ΔT_j for full *mi* range. As a result, the corresponding lifetime of stressed device in multilevel inverters has been extended, which verifies the feasibility of the proposed strategy.

An effective reduction of the thermal stresses of the affected IGBT switch S_{A11} has been fulfilled and the power losses are

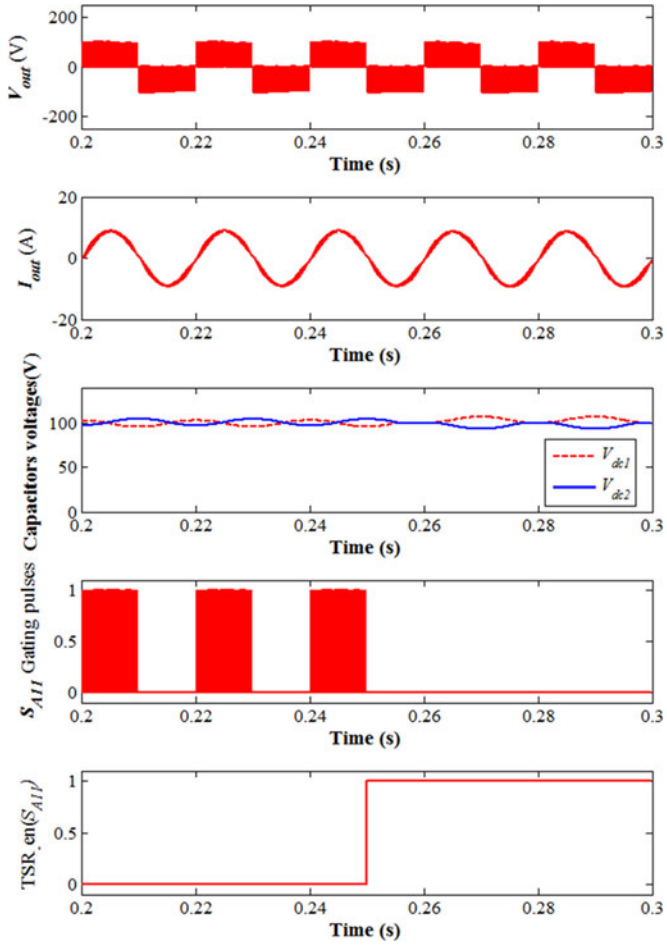

Fig. 10. Simulation results of the proposed strategy at TSD in S_{A11} at $mi = 0.45$.

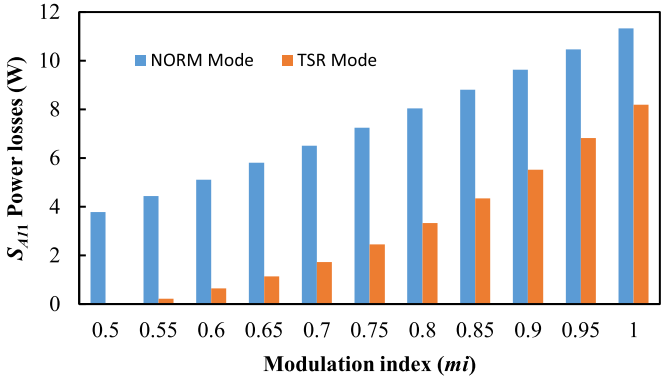

Fig. 11. Comparison of power losses in S_{A11} under NORM and TSR modes at different *mi*.

redistributed and relocated to other less stressed and healthy switches as a result. The estimated junction temperature of all the power switches in the inverter is shown in Fig. 12(b) at *mi* of 0.85. The relocation of power losses is required in TSR mode to preserve the same operation of the inverter without a compromise of its output power ratings and its number of the output levels and without adding extra devices or complex controls.

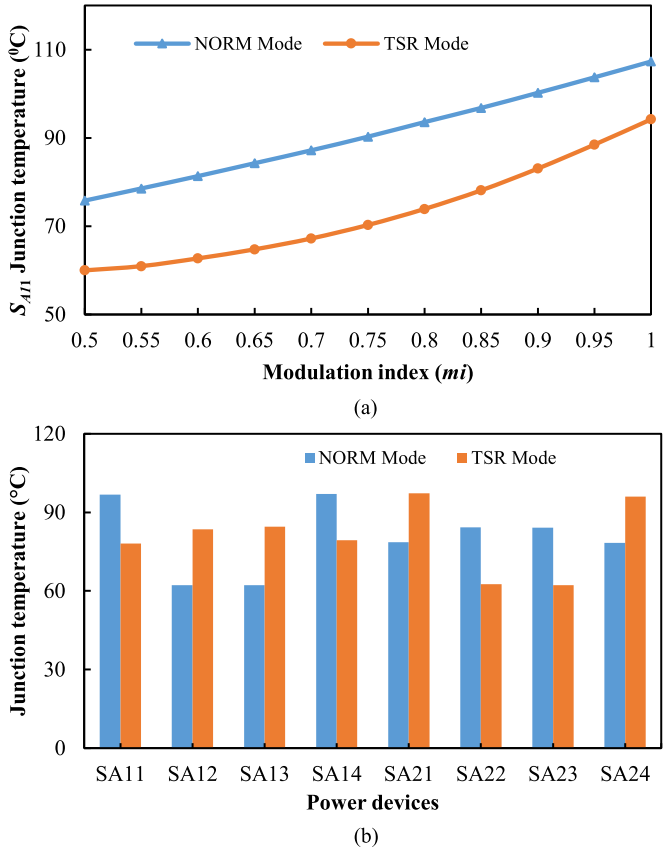

Fig. 12. Estimated junction temperature under NORM and TSR modes of: (a) S_{A11} at different *mi* and (b) Power devices at $mi = 0.85$.

In the second case study, it is assumed that there are a TSD in IGBT S_{A12} in leg A1 of the inverter ($\text{TSR\_en}(S_{A12}) = 1$) at time 0.25 s. Fig. 13 shows the performance of the proposed TSRPWM strategy at high *mi* of 0.85. According to Table I, the output voltage can be generated by using the source V_{dc1} in the positive half-cycle, whereas V_{dc2} is utilized in the negative half-cycle. Therefore, no gating signals are required for the switch S_{A12}, and the switch is effectively relieved.

It is clear from Fig. 13 that the proposed TSRPWM strategy preserves the same V_{out}, the same I_{out} of the inverter, and the same number of output levels. The voltage balance of dc-link capacitors is performed naturally as the two sources V_{dc1} and V_{dc2} are equally utilized during the line period. Moreover, the gating pulses of the device are shown to ensure the effectiveness of the proposed method.

VI. Experimental Results

The feasibility evaluation of the proposed TSRPWM strategy is performed experimentally. The parameters of the selected case study are the same of simulation studies, which are listed in Table II. The experimental setup of the inverter and the controller is shown in Fig. 14. The proposed control algorithm is implemented using a floating point digital signal processing unit (TMS320F28335). The voltages and currents are measured using LV 25-P and LEM LA 50-P transducers, respectively.

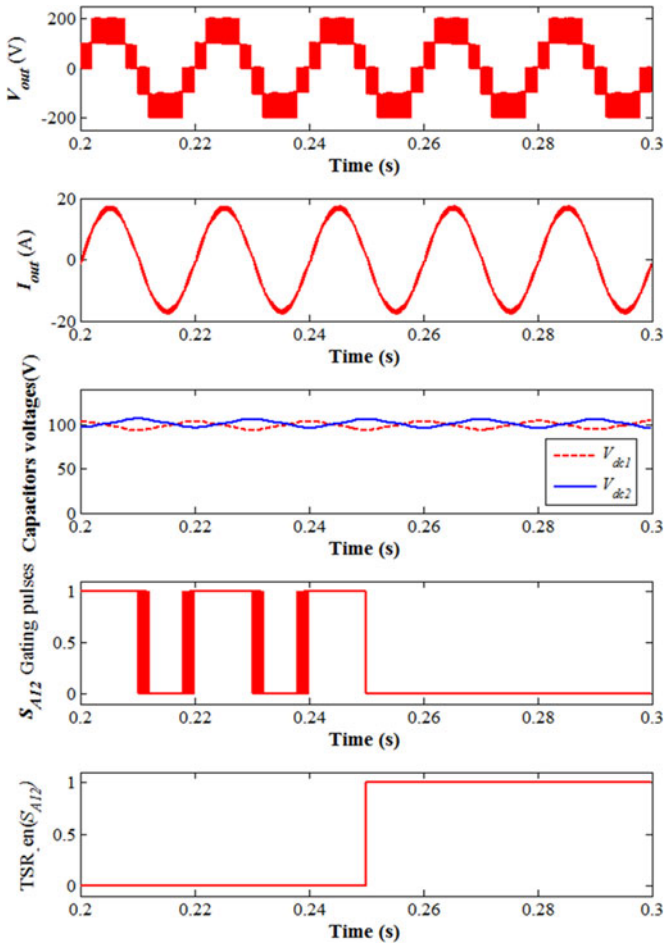

Fig. 13. Simulation results of the proposed TSRPWM strategy at TSD in S_{A12} and $mi = 0.85$.

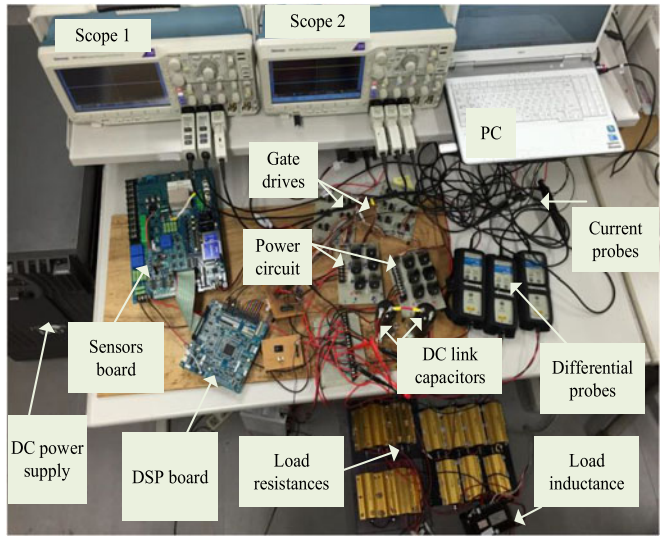

Fig. 14. Experimental setup of the inverter and the controller.

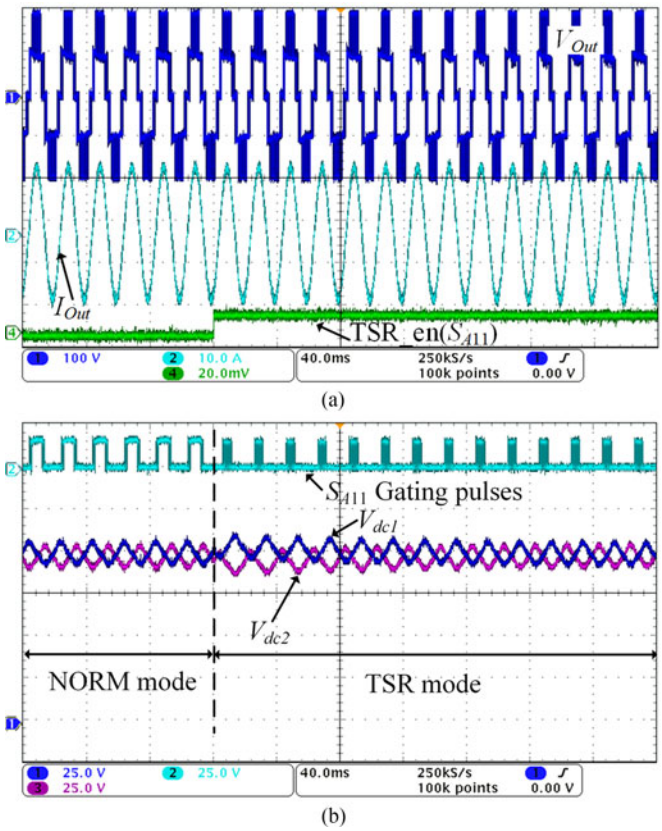

Fig. 15. Experimental results of the proposed strategy at TSD in S_{A11} and $mi = 0.85$: (a) $V_{\rm out}$, $I_{\rm out}$, and TSR_en(S_{A11}), and (b) $V_{\rm dc1}$, $V_{\rm dc2}$, and S_{A11} gating signals.

A digital signal is fed to the controller to emulate the flag of increased thermal stresses TSR_en($S_{\rm Axy}$) in power semiconductor devices.

Fig. 15 shows the experimental results of the proposed TSRPWM at TSD in S_{A11} and high modulation index ($mi = 0.85$). It is evident that the output voltage $V_{\rm out}$, the output current $I_{\rm out}$, and the power rating of the inverter remain the same without derating operation. TSR can be observed from the difference in the switching signals of the affected device S_{A11}. Based on the redundancy among switching states of the multilevel inverter, the proposed strategy operates the inverter with the switching sequence that have minimum power losses through the affected device. Therefore, there are no application limitations of the proposed strategy and it is suitable for several applications with high reliability demands.

In addition, the proposed TSRPWM has maintained voltage balance over dc-link capacitors. However, it can be observed that TSR mode has a little increase in the ripples of dc-link capacitors' voltages compared to NORM mode. This is because that the main objective of the control algorithm in NORM mode is to achieve voltage balance of dc-link capacitors. Whereas the operation of the proposed algorithm in TSR mode is divided to two regions: 1) In the regions that utilize the stressed device, the proposed algorithm selects the optimum switching sequence for achieving TSR; and 2) In the other regions that do not utilize the affected device, the proposed strategy selects the optimum switching sequence for voltage balance of dc-link capacitors. Therefore, voltage balance of dc-link capacitors is achieved in part of the line period in TSR mode, whereas it is performed in whole of the line period in NORM mode.

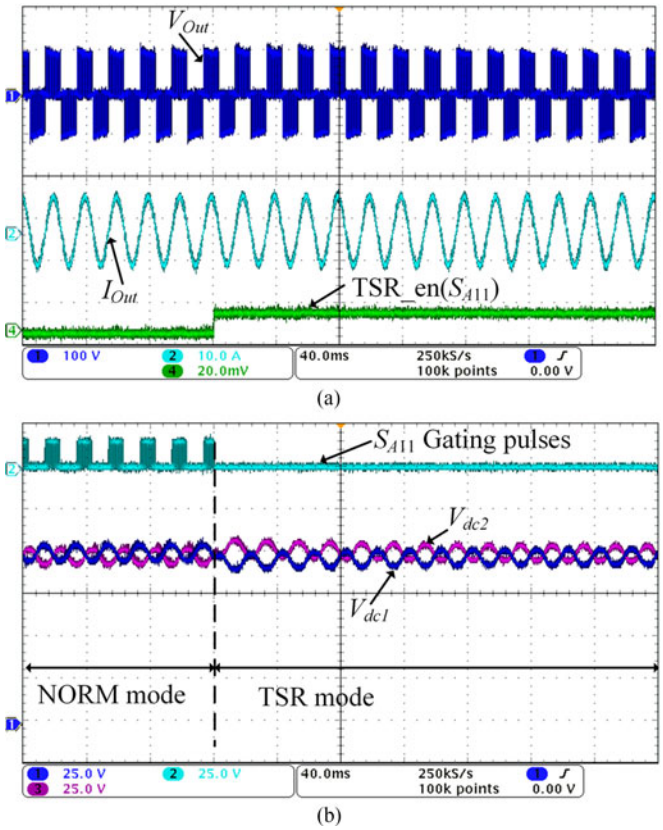

Fig. 16. Experimental results of the proposed strategy at TSD in S_{A11} and $mi = 0.45$: (a) $V_{\rm out}$, $I_{\rm out}$, and TSR_en(S_{A11}), and (b) $V_{\rm dc1}$, $V_{\rm dc2}$, and S_{A11} gating signals.

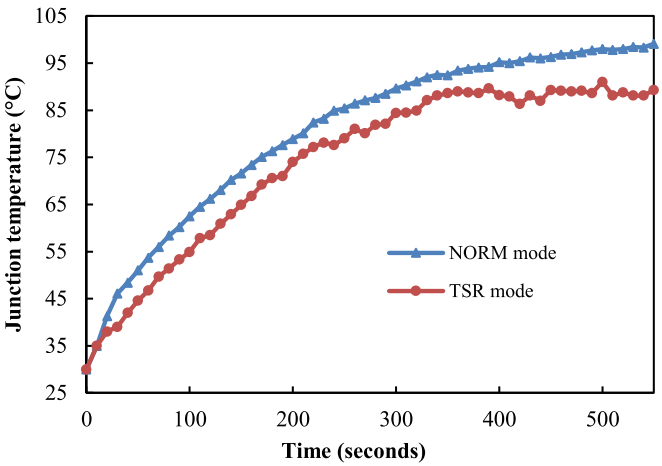

Fig. 17. Experimental junction temperature results at TSD in S_{A11} and $mi = 0.85$.

Moreover, the proposed strategy is tested with TSD in S_{A11} at low modulation index ($mi = 0.45$) and the results are shown in Fig. 16. The output current and voltage remain the same without reduction in both NORM and TSR modes. Besides, voltage balance of dc-link capacitors is preserved in both modes. However, it can be seen that no gating signals are fed to the device after TSD in the device. This emphasizes that the affected device is totally relieved at low *mi* range as there are a full

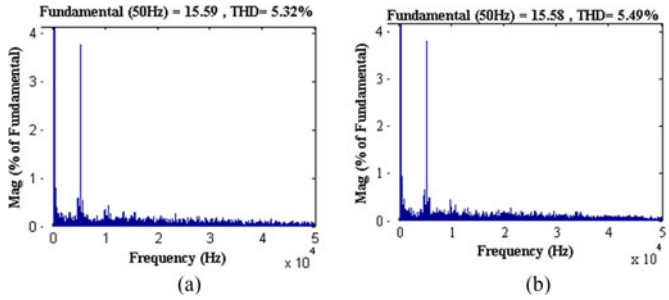

Fig. 18. THD comparison of the proposed algorithm at: (a) NORM mode and (b) TSR mode.

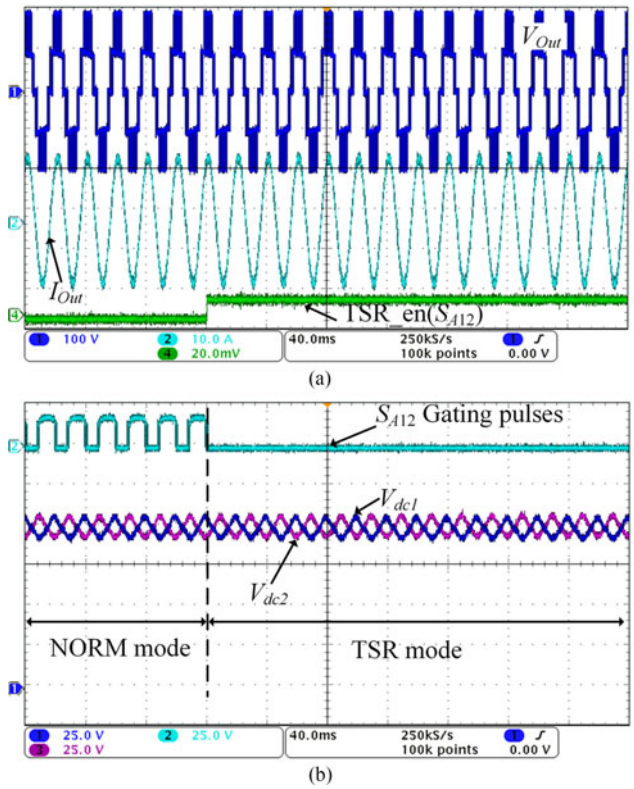

Fig. 19. Experimental results of the proposed strategy at TSD in S_{A12} and $mi = 0.85$: (a) $V_{\rm out}$, $I_{\rm out}$, and TSR_en(S_{A11}), and (b) $V_{\rm dc1}$, $V_{\rm dc2}$, and S_{A11} gating signals.

redundancy of the switching states that utilizes S_{A11} device. The experimental results assure the feasibility of the proposed strategy at whole *mi* range.

The thermal behavior of proposed strategy is tested experimentally using IR camera. Fig. 17 shows the recorded junction temperature of S_{A11} under NORM and TSR modes at $mi = 0.85$. It is clear that TSR mode has lower junction temperature than NORM mode. Relief operation is performed for the stressed device S_{A11} using the proposed TSRPWM and the steady state T_j difference between the two modes is about 10 °C. Hence, operating lifetime and long-term reliability of the multilevel inverter are robustly improved with T_j reduction using the proposed algorithm. Fig. 18 shows comparison of the THD in the output currents in NORM and TSR modes with TSD in S_{A11} and mi = 0.85. A relatively slight increase is seen

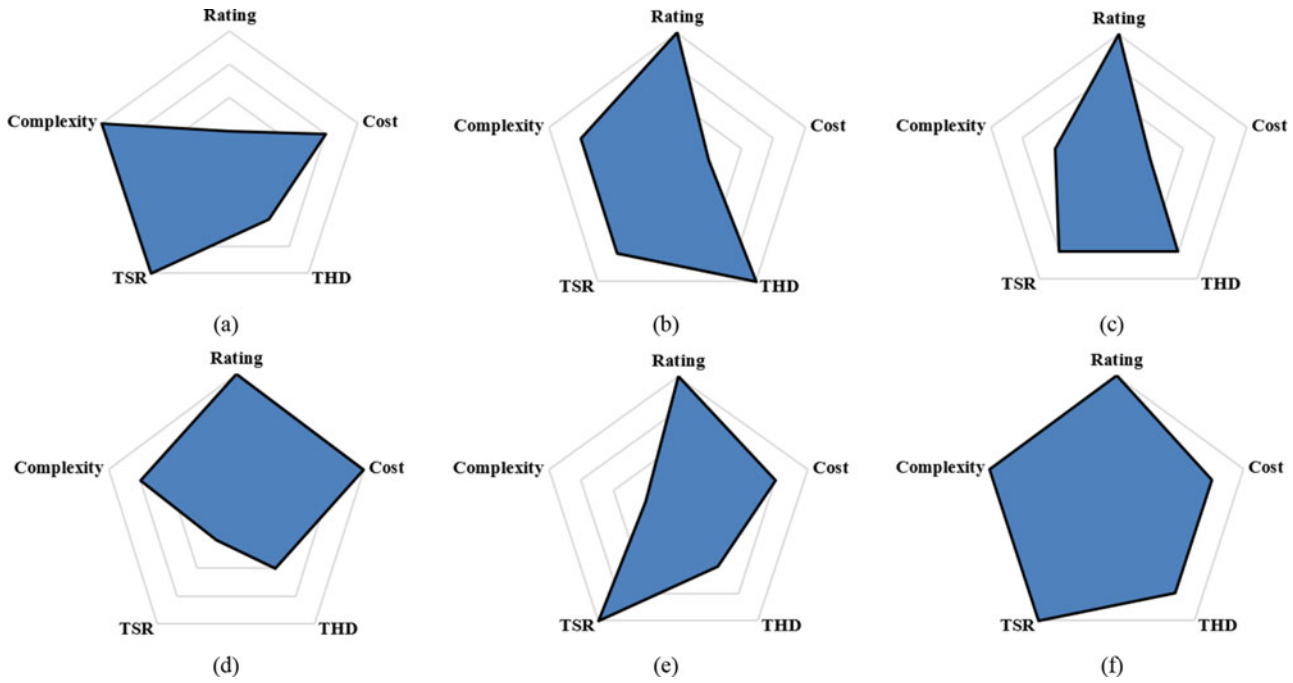

Fig. 20. Comparison of TSR strategies. (a) [6]. (b) [7]. (c) [9]. (d) [13]. (e) [16], and [17]. (f) The proposed TSRPWM method.

in the THD with TSR mode. The NORM mode has THD in the output current of 5.32%, while TSR mode contains THD of 5.49%.

Additional test case study is performed experimentally with TSD in S_{A12} at $mi = 0.85$ and the results are shown in Fig. 19. Preservations of the output ratings including $V_{\rm out}$, $I_{\rm out}$, and voltage balance over dc-link capacitors are guaranteed using the proposed strategy. Regarding TSR, the affected device is totally relieved at whole modulation indices range without interruptions of the output performance. The proposed algorithm is suitable for TSR of IGBT devices at different locations in the inverter. Furthermore, the proposed strategy can be generalized for different multilevel inverters structures.

VII. Comparison of TSR Strategies

Based on the literature review given in Section I and the performance of the proposed algorithm, Fig. 20 proposes a criterion for evaluating and comparing the performance of different TSR methodologies. The overall performance of each methodology is represented by radar view diagram. This radar diagram contains five vertex properties such as complexity, rating, cost, THD, and TSR. Due to the lack of precise evaluation for each criterion, relative comparisons between various TSR methodologies with respect to each other have been carried out. Each vertex property grades the performance of the tested topology from four levels. In this diagram, favorable vertex property of the methodology is located near the periphery of the radar diagram, while unfavorable vertex property is directed toward the origin of the diagram. The main factors for quantifying different performance criteria are shown in Table III. A discussion of each vertex property is provided as follows:

TABLE III
Parameters for Quantifying Different Performance Criteria for TSR Strategies

Criteria	Quantification basis	Score reduction
Complexity	No extra complexity	0
	Control (controlling added device or dc-link capacitors' voltages)	1
	Adjusting TSR controller (percentage share or added CMV voltage)	1
	Complicated arithmetic operations	1
Cost	T_j measurement	1
	Additional devices	1
	Additional driving and powering	1
	Increased ratings of converters	1
Rating	No change	0
	Little reduction	1
	Moderate reduction	2
	High reduction	3
TSR	Highly effective	0
	Moderate effective	1
	Little effective	2
	Not effective	3
THD	No change	0
	Little increase	1
	Moderate increase	2
	Highly increase	3

1) Complexity: The complexity criteria are a measure of the difficulty in implementing the TSR strategy. It represents a key factor in comparing various approaches of the literature with the proposed TSRPWM method. The quantification process of complexity is performed according to the number of complex computations and controls in each strategy. Each added complexity reduces the score of the strategy. For example, in [6], a simple PI controller is

needed to adjust the current reference for achieving TSR. However, driving the added cooling device that requires a precise thermal modeling of the cooling system adds complexity to the strategy in [7]. In [9], the adjustment of the percentage share for the interleaved converters requires precise measurements of the on state resistance of IGBTs in all the interleaved converters. Moreover, different power sharing between the interleaved converters results in circulating currents that require additional control and filters as investigated in [23]. However, in [13], the complexity occurs when adjusting and estimating the injected common mode voltage to relieve different IGBTs locations. In the SVPWM-based method in [16], voltage balance of dc-link capacitors under TSR modes requires complex calculations to replace the space vectors. Based on the evaluation of implementation complexity of SVPWM methods in [24] and [25], SVPWM methods exhibit two additional complexities in defining the region of reference vector in the space vector diagram and in calculating the switching times of the space vectors. From another side, one of the main advantages of the proposed strategy is that it is based on PWM implementation, which does not have the problems of defining the switching times and operating region according to [24] and [25].

2) Rating: The rating criteria represent the ability of the TSR approach to preserve the operation of the inverter with the same output ratings under NORM and TSR modes. It is highly required to operate the inverters at MPP in renewable energy applications. Rating criteria of various strategies are quantified according to the required level of reducing the output rating. TSR strategies are classified into four levels that represent the same rating, little, moderate, or high reduction of output rating level. In [6], derating of the output power is needed to achieve TSR of the affected devices, and results showed that about 50 A reduction of the output current is required to achieve 50% reduction of the power losses in the device. However, in [7] and [9], there are no changes in the output ratings before and after TSD because thermal relief is achieved based on adding cooling devices and interleaving of converters, respectively. Moreover, TSR methods in [13] and [16] and the proposed TSRPWM strategy are based on switching states redundancy in multilevel inverters, and no changes in the output ratings are required as a result.
3) Cost: The cost criteria include the extra charges for the required additional devices, measurement circuits, component ratings, and powering circuits. Each added device is used to quantify and compare different strategies. Excluding the DPWM method, all other approaches require TSEP estimation circuits. Additionally, in [7], additional costs are required for the added cooling device in addition to its powering and driving circuit. The strategy in [13] has the highest cost and requirements among different TSR methodologies. The cost includes using TSEP circuit, full rating converters for all the interleaved modules, and circulating current filters.
4) THD: THD measurements are crucial especially in grid-connected systems. A relative comparison of the changes in THD value between NORM and TSR modes for TSR strategies is carried out because of the different output ratings, output filters, and operating conditions in each strategy. In the analysis, THD changes between NORM and TSR modes are represented by four levels that represent the same THD, little, moderate, or high increase in THD. In [6], a high reduction of the output ratings is required to achieve TSR; however, low output power operation of the inverter increases the THD in the output as investigated in [15]. The same THD is maintained in [7] as there are no changes in the output ratings or the modulation technique. However, in [9], the circulating currents in TSR mode add low- and high-frequency components that make a little increase in the THD in interleaved converters as shown in [26]. Meanwhile, the strategy in [13] is based on the DPWM technique that increases the THD in the outputs [27]. In [16], THD has increased in the outputs in order to achieve voltage balance of dc link capacitors and similarly in [17], THD has increased in TSR mode from 3.4% to 7.3%. The proposed TSRPWM strategy has maintained a little increase in THD from 5.32% to 5.49% that has been verified by simulation and experimental results.
5) TSR: TSR criteria are the measure of the effectiveness of the TSR approach to reduce the junction temperature of the thermally stressed device. The TSR criteria of strategies are divided to four categories that represent high, moderate, little, or no effective for achieving relief. In [6], results showed that about 50 A reduction of the output current can achieve 50% reduction of the power losses in the device, which guarantee a high TSR of the affected device. However, in [7], controlling the added cooling device has effectively maintained the same junction temperature with an output current rise from 6 to 9 A. In [9], a decrease in T_j from 49 °C to 43 °C has been achieved. However, unequal share of the interleaved modules results in circulating currents between modules and additional power losses in switching devices are obtained [23], [26]. Moreover, circulating currents increase at high difference in percentage sharing between modules. From another side, DPWM-based methods represent the worst approach for achieving TSR of thermally stressed devices. This is due to the fact that DPWM strategy is concerned with improving the overall inverter switching power losses, regardless of the individual device power losses or the added conduction power losses. Results of the SVPWM method in [16] have showed an effective TSR of about 10 °C reduction in T_j of the affected device. The feasibility of the proposed TSRPWM to achieve TSR of switching devices has been confirmed with simulation and experimental measurements. A reduction of more than 12 °C has been achieved for the whole operating *mi* range of the inverter.

Fig. 20 illustrates the graphical implementation of the radar diagram shape for the addressed methodologies compared to the proposed TSRPWM strategy. It is clear that the proposed

algorithm achieves the full power rating during NORM and TSR modes, low system complexity, high effective TSR, and little increase in THD and cost compared to the addressed ones. Therefore, the proposed methodology presents its efficacy and effectiveness for motor drives and grid-connected systems.

VIII. Conclusion

This paper has proposed a new carrier-based modulation strategy, called TSRPWM, for single-phase multilevel inverters. It retains the same benefits as the conventional carrier PWM methods, i.e., a simple and easy implementation, but presents a significantly reduced power losses and thermal stresses of the stressed semiconductor devices. The main idea of the new proposed strategy is adaptively selecting the redundant switching states in each switching cycle, in order to optimize power losses through the thermally stressed device. Therefore, both of the junction temperature and temperature cycling of the stressed device are reduced by the proposed strategy compared with NORM mode operation of the device. The results of simulation and experimental prototypes are conformed and verified the new proposed concept. A generalized implementation of the proposed TSRPWM, to provide TSR for any of the components and for any *n*-level inverters, is also presented. Moreover, the proposed strategy maintains the inverter operation with the same output ratings and voltage balance over dc-link capacitors. Finally, the performance of the proposed strategy is compared with the prominent strategies in the literature, and the distinction of the proposed strategy has become clear.

References

[1] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May 2011.

[2] S. E. De Leon-Aldaco, H. Calleja, and J. Aguayo Alquicira, "Reliability and mission profiles of photovoltaic systems: A FIDES approach," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2578–2586, May 2015.

[3] B. Ji, X. Song, E. Sciberras, W. Cao, Y. Hu, and V. Pickert, "Multiobjective design optimization of IGBT power modules considering power cycling and thermal cycling," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2493–2504, May 2015.

[4] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, May 2015.

[5] P. A. Mawby *et al.*, "Study on the lifetime characteristics of power modules under power cycling conditions," *IET Power Electron.*, vol. 9, no. 5, pp. 1045–1052, Apr. 2016.

[6] D. A. Murdock, J. E. R. Torres, J. J. Connors, and R. D. Lorenz, "Active thermal control of power electronic modules," *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 552–558, Mar. 2006.

[7] C. Li, D. Jiao, J. Jia, F. Guo, and J. Wang, "Thermoelectric cooling for power electronics circuits: modeling and active temperature control," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3995–4005, Nov. 2014.

[8] Y. Yang, H. Wang, and F. Blaabjerg, "Improved reliability of single-phase PV inverters by limiting the maximum feed-in power," in *Proc. 2014 IEEE Energy Convers. Congr. Expo.*, 2014, pp. 128–135.

[9] S. Dusmez and B. Akin, "An active life extension strategy for thermally aged power switches based on pulse-width adjustment method in interleaved converters," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5149–5160, Jul. 2016.

[10] K. Ma and F. Blaabjerg, "Modulation methods for neutral-point-clamped wind power converter achieving loss and thermal redistribution under low-voltage ride-through," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 835–845, Feb. 2014.

[11] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2521–2532, Apr. 2017.

[12] Y. Jiao and F. C. Lee, "New modulation scheme for three-level active neutral-point-clamped converter with loss and stress reduction," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5468–5479, Sep. 2015.

[13] J. He, L. Wei, and N. A. O. Demerdash, "Power cycling lifetime improvement of three-level NPC inverters with an improved DPWM method," in *Proc. 2016 IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2826–2832.

[14] J.-S. Lee, S. Yoo, and K.-B. Lee, "Novel discontinuous PWM method of a three-level inverter for neutral-point voltage ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3344–3354, Jun. 2016.

[15] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5579–5591, Oct. 2014.

[16] M. Aly, G. M. Dousoky, and M. Shoyama, "Reliability enhancement of multilevel inverters through SVPWM-based thermal management methodology," in *Proc. 2015 IEEE 2nd Int. Future Energy Electron. Conf.*, 2015, pp. 1–6.

[17] T.-M. Phan, G. J. Riedel, N. Oikonomou, and M. Pacas, "Active thermal protection and lifetime extension in 3L-NPC-inverter in the low modulation range," in *Proc. 2015 IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 2269–2276.

[18] T. Lei, M. Barnes, S. Smith, S. Hur, A. Stock, and W. E. Leithead, "Using improved power electronics modeling and turbine control to improve wind turbine reliability," *IEEE Trans. Energy Convers.*, vol. 30, no. 3, pp. 1043–1051, Sep. 2015.

[19] D. Zhou, F. Blaabjerg, T. Franke, M. Tonnes, and M. Lau, "Comparison of wind power converter reliability with low-speed and medium-speed permanent-magnet synchronous generators," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6575–6584, Oct. 2015.

[20] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power module: A survey," *IEEE Trans. Device Mater. Reliab.*, vol. 16, no. 1, pp. 80–97, Mar. 2016.

[21] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.

[22] A. M. Rao and K. Sivakumar, "A fault-tolerant single-phase five-level inverter for grid-independent PV systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7569–7577, Dec. 2015.

[23] G. Gohil *et al.*, "Modified discontinuous PWM for size reduction of the circulating current filter in parallel interleaved converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3457–3470, Jul. 2015.

[24] O. Dordevic, M. Jones, and E. Levi, "A comparison of carrier-based and space vector PWM techniques for three-level five-phase voltage source inverters," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 609–619, May 2013.

[25] R. Baranwal, K. Basu, and N. Mohan, "Carrier-based implementation of SVPWM for dual two-level VSI and dual matrix converter with zero common-mode voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1471–1487, Mar. 2015.

[26] D. Zhang, F. Wang, R. Burgos, and D. Boroyevich, "Common-mode circulating current control of paralleled interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3925–3935, Dec. 2011.

[27] T. Bruckner and D. G. Holmes, "Optimal pulse-width modulation for three-level inverters," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 82–89, Jan. 2005.

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