Single-Phase PLLs: A Review of Recent Advances

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***Abstract*—Single-phase phase-locked loops (PLLs) are popular for the synchronization and control of single-phase grid-connected converters. They are also widely used for monitoring and diagnostic purposes in the power and energy areas. In recent years, a large number of single-phase PLLs with different structures and properties have been proposed in the literature. The main aim of this paper is to provide a review of these PLLs. To this end, the single-phase PLLs are first classified into two major categories: 1) power-based PLLs and 2) quadrature signal generation-based PLLs. The members of each category are then described and their pros and cons are discussed. This paper provides a deep insight into characteristics of different single-phase PLLs, and therefore, can be considered as a reference for researchers and engineers.**

***Index Terms*—Grid-connected applications, phase-locked loop (PLL), single-phase systems, synchronization.**

I. Introduction

In RECENT years, the single-phase power converters have received a considerable attention because of emerging applications/requirements such as the grid integrating of small-scale renewable energy sources (particularly, rooftop photovoltaic panels), vehicle-to-grid and grid-to-vehicle connections, low-power-rating uninterruptible power supplies, and small-scale power quality conditioners [1]–[5].

A critical part in controlling all single-phase converters is the synchronization unit, which is responsible for the smooth connection of the converter to the utility grid and monitoring the grid condition. The information provided by the synchronization unit (which is often the phase, frequency, and amplitude of the grid voltage fundamental component) is also of vital importance for the converter control strategy during the normal operating condition, particularly for the generation of the reference current for the converter.

Different synchronization techniques have been proposed in the literature. A popular strategy is using a phase-locked loop (PLL). The PLL, in simple words, is a closed-loop control system that locks its output to its input with a constant phase error (ideally zero) [6]. All PLLs, regardless of their differences, have three basic parts [6]. The first one is the phase detector (PD), which generates a phase error signal, i.e., a signal that contains the error between real and estimated phases. The second part is the loop filter (LF), which is mainly responsible for suppressing disturbances inside the PLL control loop. The dynamic response, tracking characteristics, and stability properties of the PLL are also mainly dictated by the LF. In energy and power applications, which are focused on in this paper, the LF is often a proportional-integral (PI) controller. The third part is the voltage-controlled oscillator (VCO), which is responsible for generating the synchronized signal with the PLL input.

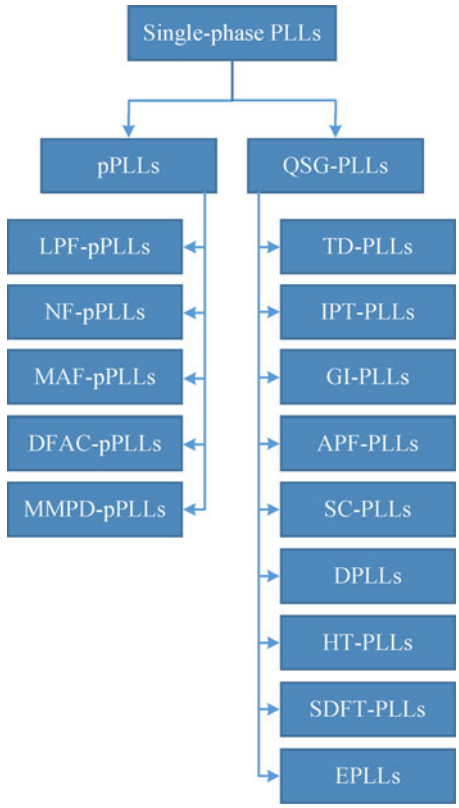

Fig. 1. Classification of single-phase PLLs.

A large number of single-phase PLLs have been developed and proposed in the literature. Here, they are classified into two major categories: power-based PLLs (pPLLs) [7]–[19] and quadrature signal generation-based PLLs (QSG-PLLs) [20]–[54]. Fig. 1 illustrates this classification. This classification is mainly based on the PD of PLLs because the main difference between single-phase PLLs lies in their PD.

The pPLLs are characterized by having a product-type PD [7], [8]. A by-product of such PD is a double-frequency disturbance term, which results in double-frequency oscillatory errors, and

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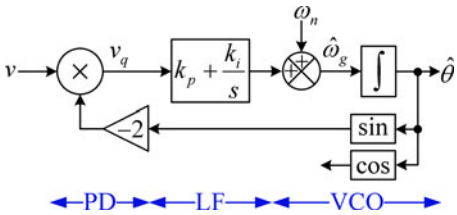

Fig. 2. Schematic diagram of the standard pPLL.

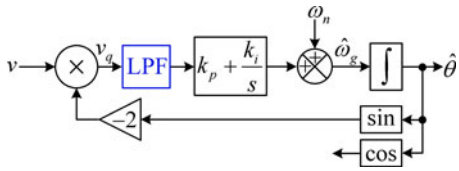

Fig. 3. Schematic diagram of the LPF-pPLL.

therefore, an offset error[1] in the estimated quantities by the standard pPLL. To tackle this issue, several advanced pPLLs have been designed in the recent years [8]–[19]. The main difference between them lies in the filtering strategy they use for rejecting the double-frequency disturbance term.

The QSG-PLLs can be understood as the single-phase version of the conventional synchronous reference frame PLL (SRF-PLL), which is a standard PLL in three-phase applications. What *almost* all QSG-PLLs have in common is a unit for creating a fictitious quadrature signal, which is required for transferring the information into the *dq* frame. This unit can be implemented using different filters/circuits/algorithms [20]–[45]. A member of this class that looks different from others, at least at first glance, is the enhanced PLL (EPLL) [46]–[54]. This PLL, which has been developed based on an optimization perspective, has a close connection with some QSG-PLLs [49]. For this purpose, it has been subsumed under the category of QSG-PLLs.

The main aim of this paper is to provide a review of recent advances in designing single-phase PLLs. To this end, as discussed before, the single-phase PLLs are first classified into two main categories. The members of each category are then described and their advantages and disadvantages are explained. This review provides useful information about the characteristics of different single-phase PLLs, and therefore, can be used as a reference for researchers and engineers working in the field.

II. pPLLs

Fig. 2 shows the schematic diagram of a pPLL, which is a standard PLL in single-phase applications [7], [8]. In this PLL, v is the single-phase input signal, $\hat{\omega}_g$ and $\hat{\theta}$ are the estimated frequency and phase angle, respectively, ω_n is the nominal value of the grid frequency, and k_p and k_i are the proportional and integral gains of the PI controller, which acts as the LF.

To generate the phase error information, this PLL uses a mixer or product-type PD. A by-product of such PD is a double-frequency term, which causes double-frequency oscillatory error, and consequently, offset error in the pPLL estimated quantities. Another shortcoming of the standard pPLL is that it does not provide any knowledge about the grid voltage amplitude. It implies that decoupling the pPLL dynamics from the grid voltage amplitude variations, which requires an estimation of the grid voltage amplitude, may not be carried out. To tackle these shortcomings, several advanced pPLLs have been proposed in recent years. A review of these pPLLs is presented in the following.

[1]The oscillatory errors happen in both the estimated frequency and phase angle. However, the offset error only happens in the estimated phase angle.

A. Low-Pass Filter-Based pPLLs (LPF-pPLLs)

To mitigate the double-frequency disturbance term in the standard pPLL, including a high-order infinite impulse response (IIR) LPF inside the pPLL control loop is suggested in [8]. The schematic diagram of this pPLL, which is briefly referred to as the LPF-pPLL, can be observed in Fig. 3. Notice that the effective removal of the double-frequency disturbance term using the LPF requires a low cutoff frequency for it, which results in a considerably high phase delay in the pPLL control loop, and hence, makes the pPLL transient behavior slow.

Roughly speaking, the LPF-pPLL benefits from a high harmonic filtering capability and noise immunity. Tuning the control parameters of the LPF-pPLL can be carried out by using the trial-and-error procedure presented in [8] or by employing the systematic design approach suggested in [55].

B. Notch Filter-Based pPLLs (NF-pPLLs)

In [9], blocking the double-frequency term by using a non-adaptive IIR NF is recommended. The structure of this PLL, which is briefly called the IIRNF-pPLL, is similar to the LPF-pPLL (see Fig. 3), but the LPF is replaced by the IIR NF. Selecting the notch bandwidth of the IIR NF highly depends on the expected range of variations in the grid frequency. For applications where large frequency drifts are anticipated, a wide bandwidth for the NF should be considered. This selection effectively removes the double-frequency term, but at the expense of causing a large phase delay, and hence, slowing down the pPLL transient response. This problem, of course, can be avoided by using a narrow-bandwidth adaptive NF. It should be pointed out that the harmonic filtering capability of the IIRNF-pPLL can be enhanced by using additional NFs in a serial manner [56] or in a parallel configuration [57]. Tuning the control parameters of the IIRNF-pPLL can also be carried out by using the symmetrical optimum method, as suggested in [58].

In [10], a sort of finite impulse response (FIR) NF for rejecting the double-frequency term in the pPLL is suggested. The schematic diagram of the pPLL with the FIR NF, briefly called the FIRNF-pPLL, can be seen in Fig. 4. The FIR NF, which is implemented using $T/4$ (T is the grid fundamental period) delay units, rather effectively blocks the double-frequency term even when large variations in the grid frequency occur. Moreover, it rejects some specific harmonic components inside the pPLL control loop. These advantages are at the cost of a slow dynamic response for the pPLL because the FIR NF causes large in-loop phase delay. It is worth noting that the

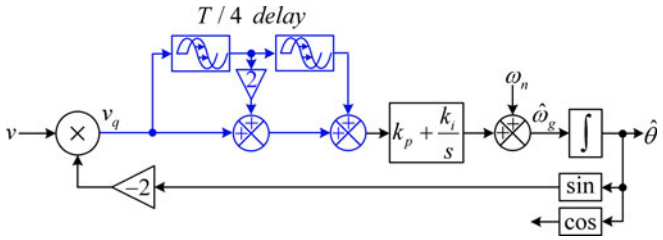

Fig. 4. Schematic diagram of the FIRNF-pPLL.

control parameters of the FIRNF-pPLL may be tuned using the symmetrical optimum method [55]. To this end, the $T/4$ delays in the FIR NF should be replaced by their first-order Pade approximation.

C. Moving Average Filter-Based pPLLs (MAF-pPLLs)

An alternative approach for eliminating the double-frequency term in the pPLL is employing an in-loop MAF [11]–[15]. The MAF, also known as the rectangular window filter, is a linear-phase LPF that is described in the s-domain as

$$\mathrm{MAF}(s) = \frac{1 - e^{-T_w s}}{T_w s} \tag{1}$$

where T_w symbolizes the MAF window length.

To block the double-frequency disturbance component, $T_w = T/2$ is often considered for the window length [13], [14]. Another possible choice is $T_w = T$ [12], which may be useful when rejecting the dc offset (this component appears as a fundamental-frequency component in the pPLL control loop) and all harmonics up to the aliasing frequency are also intended. Notice that the phase delay caused by the MAF is proportional to its window length: the higher the window length, the larger the in-loop phase delay.

The MAF-pPLL (i.e., the pPLL with an in-loop MAF) has a sluggish dynamic behavior. This is particularly true when $T_w = T$ is considered. This problem can be mitigated by replacing the LF (the PI controller) by a proportional-integral-derivative (PID) regulator [13], [14], and preferably, arranging a pole-zero cancellation. Such pole-zero cancellation, nevertheless, considerably reduces the ability of the MAF in rejecting the double-frequency component under off-nominal frequencies. In this condition, a frequency-adaptive MAF is recommended. This adaptability can be provided by using a variable sampling frequency or altering the MAF window length according to the variations of the grid frequency [11], [13], [14].

As a side note, it may be interesting to briefly discuss the MAF implementation. The MAF can be implemented in both recursive and nonrecursive forms. The recursive realization is often preferred as it requires a much lower computation effort. It is also worth mentioning that the amplitude estimation capability can be simply added to the MAF-pPLL by using an extra MAF (see [12, Fig. 5]).

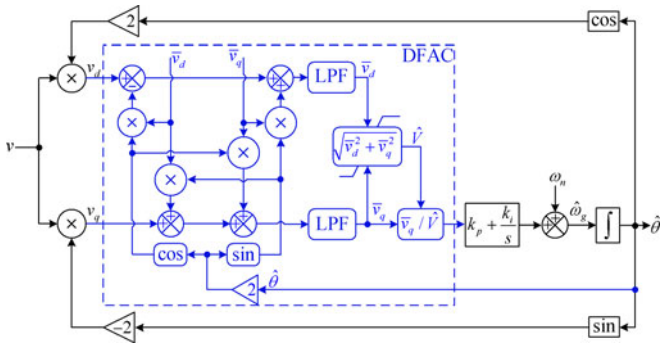

Fig. 5. Schematic diagram of the DFAC-pPLL.

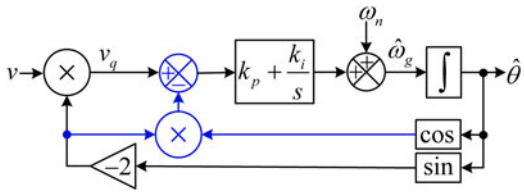

Fig. 6. Schematic diagram of the MMPD-pPLL.

D. Double Frequency and Amplitude Compensation-Based pPLLs (DFAC-pPLLs)

In [16], an amplitude estimation loop (d-axis) is first added to the standard pPLL. The double-frequency terms in both q- and d-axes are then nullified by generating and adding equal but opposite double-frequency components. This technique is called the DFAC method. Incorporating this strategy into the standard pPLL results in the DFAC-pPLL, which its schematic diagram can be seen in Fig. 5. Notice that, contrary to all other pPLLs, the dynamics of the DFAC-pPLL is almost independent of the grid amplitude variations because of the amplitude normalization implemented in this PLL. The LPFs used in the DFAC structure, which are first order, also result in a higher harmonic filtering capability. It is worth mentioning that another version of the DFAC-pPLL with an excellent harmonic filtering capability, but with a bit slower dynamic response can be found in [17].

E. Modified Mixer PD-Based pPLLs (MMPD-pPLLs)

A different strategy to tackle the double-frequency problem in the pPLL is suggested in [19]. This method is called the MMPD. In this technique, as shown in Fig. 6, the double-frequency term is canceled before the PI controller by adding an equal but opposite component, which is constructed using the estimated phase angle. This technique works effectively when the grid voltage amplitude is 1 p.u. Creating this condition, however, is a bit difficult because it requires an effective amplitude estimation/normalization in the MMPD-pPLL input, which its implementation is not a trivial task.

F. Recommendations

Table I provides a performance comparison among some advanced pPLLs. The content of this table is based on extensive numerical results and also the authors' experience. Some of

TABLE I
PERFORMANCE COMPARISON BETWEEN ADVANCED PPLLS

Advanced pPLLs	Features			
	Double-Frequency Disturbance Rejection	Dynamic Response	Harmonic Filtering	Computational Burden
LPF-pPLL [8]	Medium	Very Slow	Good	Low
NF-pPLL [10]	Good[1]	Slow	Medium	Low
MAF-pPLL [13]	Good[2]	Slow[2]	Good	Low
DFAC-pPLL [16]	Perfect	Fast	Medium	Medium
MMPD-pPLL [19]	Poor[3]	Fast	Poor	Low

[1] The NF-pPLL [10] completely reject the double-frequency disturbance term when the grid frequency is at its nominal value. This ability, nevertheless, a bit reduces under large frequency drifts. This problem can be alleviated by adjusting the length of delay units according to the grid frequency variations.

[2] Like the NF-pPLL [10], the MAF-pPLL [12] suffers from the imperfect rejection of the double-frequency disturbance term under large frequency drifts. Of course, this problem in the MAF-pPLL is a bit more serious than that in the NF-pPLL [10]. To tackle this drawback, a variable sampling frequency or a frequency-adaptive MAF can be used [11], [13], [14]. Using a variable sampling frequency, nevertheless, may not be always allowed. The slow dynamic response of the MAF-pPLL [13] can also be solved by using a PID controller as the LF [13], [14].

[3] The MMPD-pPLL suffers from large double-frequency oscillatory ripples under off-nominal grid voltage amplitudes. This problem can be mitigated/removed by adding an amplitude normalization scheme in the MMPD-pPLL input, which is not a very straightforward task [18].

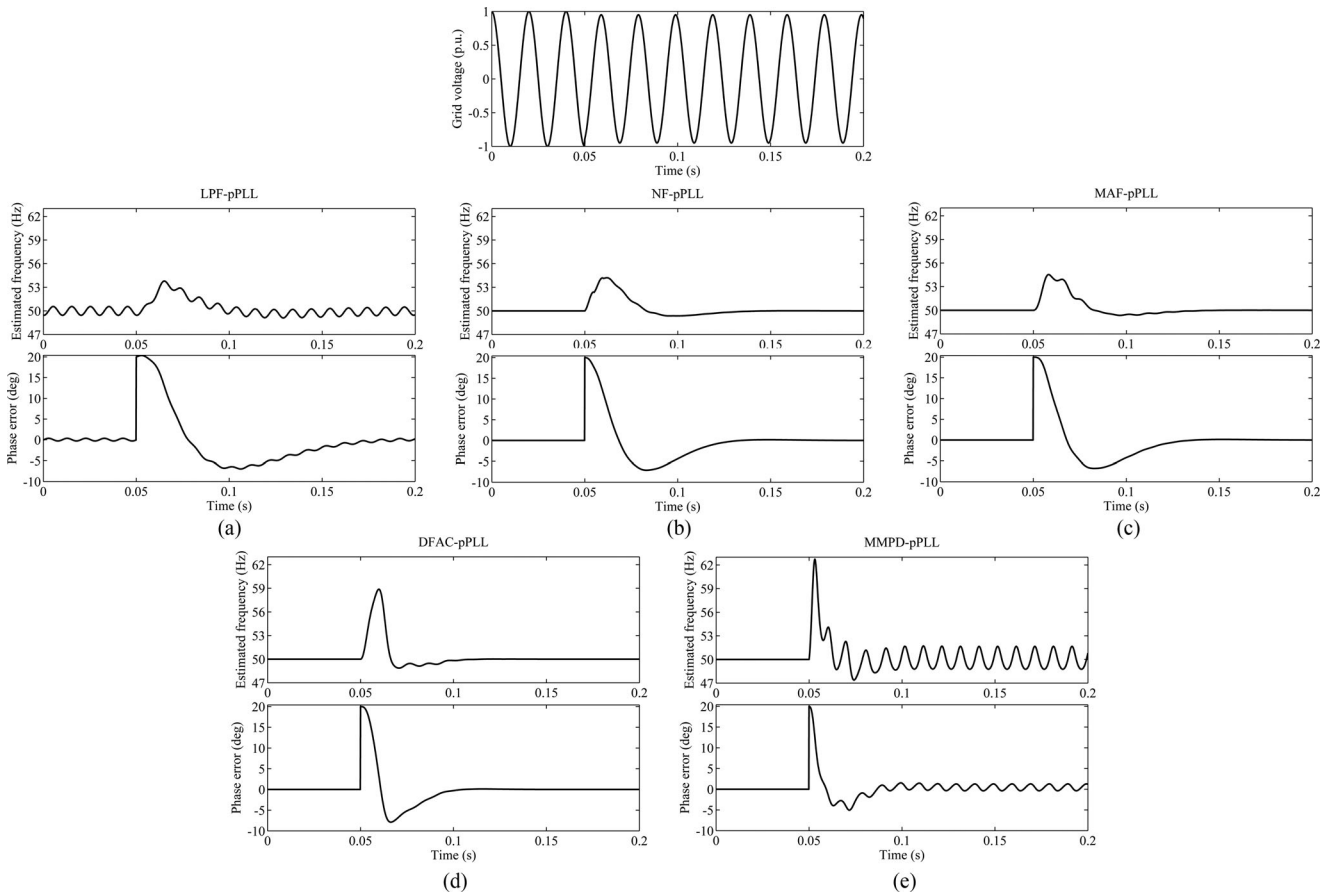

Fig. 7. Performance of (a) LPF-pPLL, (b) NF-pPLL, (c) MAF-pPLL, (d) DFAC-pPLL, and (e) MMPD-pPLL under a phase angle jump of $+20^\circ$ and voltage sag of 0.05 p.u.

these results are shown in Figs. 7–9, which simulate the performance of some advanced pPLLs under a small voltage sag with phase jump, frequency step change, and harmonically distorted grid conditions, respectively. It should be mentioned that the control parameters of all PLLs (except for the MMPD-PLL) are designed using the symmetrical optimum method [16]. The MMPD-PLL control parameters, however, are selected based on the standard tuning approach available for second-order PLLs [7]. All control parameters are summarized in Table II. Notice that the LPF in the LPF-pPLL is a fourth-order Butterworth LPF.

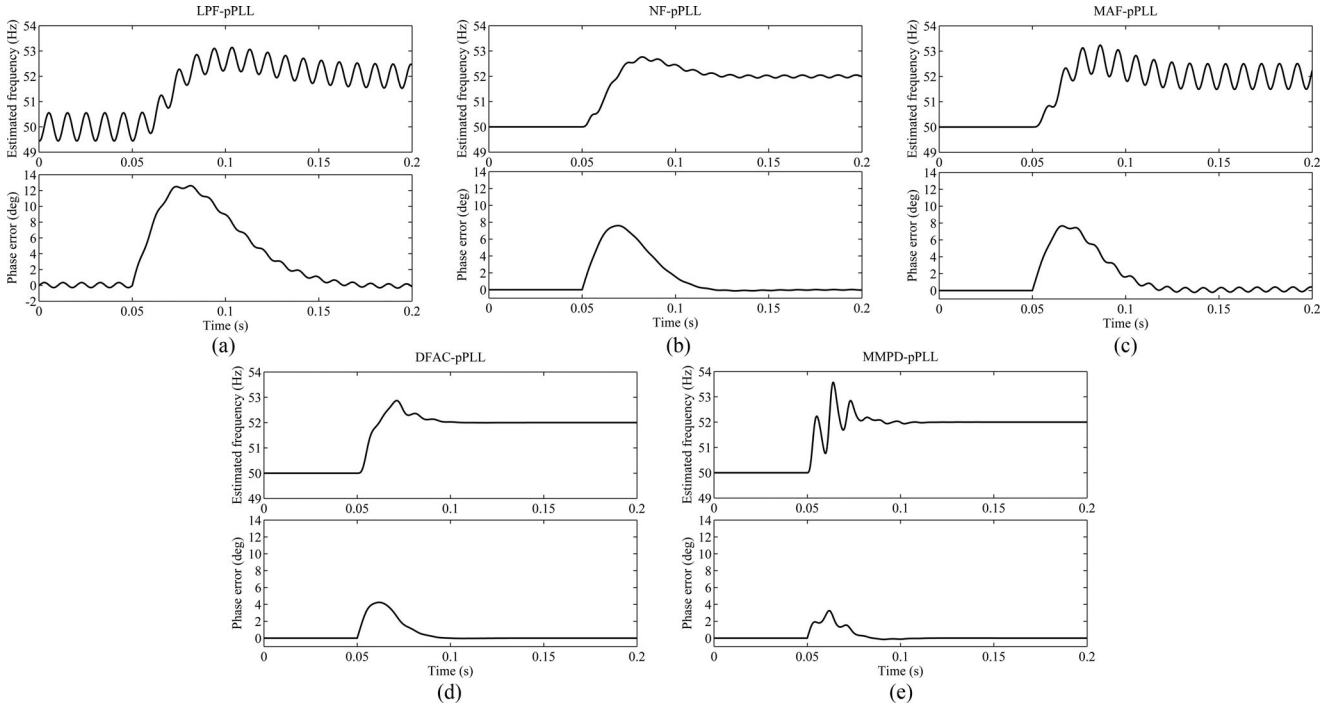

Fig. 8. Performance of (a) LPF-pPLL, (b) NF-pPLL, (c) MAF-pPLL, (d) DFAC-pPLL, and (e) MMPD-pPLL under a $+2$-Hz frequency jump. The grid voltage amplitude is 1 p.u. during this test.

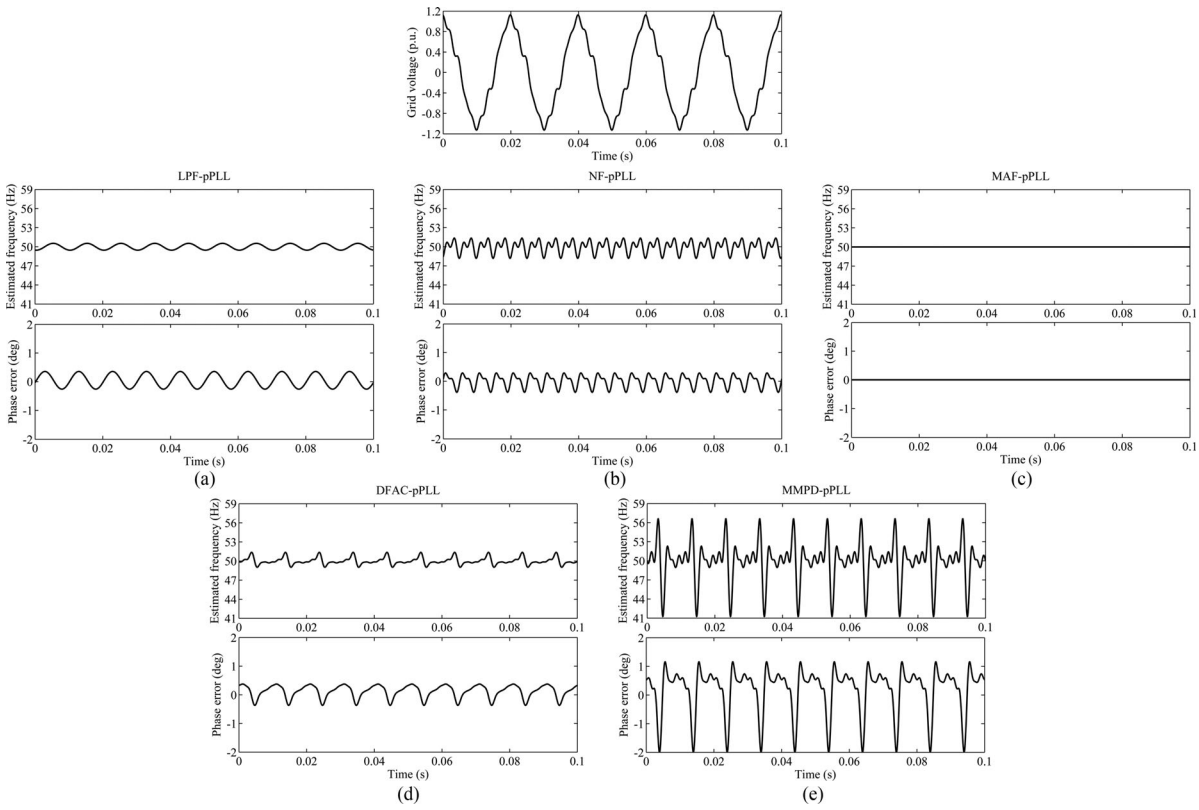

Fig. 9. Performance of (a) LPF-pPLL, (b) NF-pPLL, (c) MAF-pPLL, (d) DFAC-pPLL, and (e) MMPD-pPLL under a harmonically distorted grid condition. The grid frequency is at its nominal value during this test. The grid voltage fundamental component is 1 p.u. and the magnitude of all harmonics (i.e., third, fifth, seventh, and ninth harmonics) is 0.05 p.u.

TABLE II
CONTROL PARAMETERS

PLL	Parameters
LPF-pPLL [8]	$k_p = 51$, $k_i = 1080.7$, $\omega_p = 322$ rad/s
NF-pPLL [10]	$k_p = 20.7$, $k_i = 710.7$
MAF-pPLL [13]	$k_p = 82.8$, $k_i = 2842.8$, $T_w = 0.01$ s
DFAC-pPLL [16]	$k_p = 138.2$, $k_i = 7914.6$, $\omega_p = 333.7$ rad/s
MMPD-pPLL [19]	$k_p = 177.7$, $k_i = 15791$

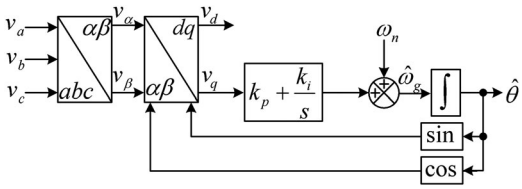

Fig. 10. Schematic diagram of the SRF-PLL.

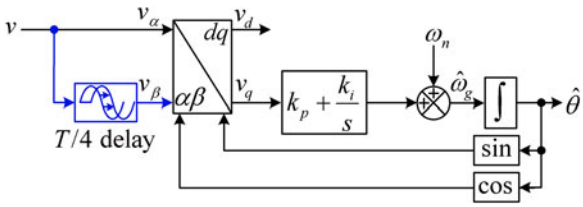

Fig. 11. Standard TD-PLL.

Also, notice that the MMPD-pPLL does not use any amplitude normalization.

Based on the Table I, the DFAC-pPLL is recommended as a good option mainly because it completely removes the double-frequency disturbance component and provides a satisfactory compromise between the dynamic response, filtering capability, and computational burden. The MAF-pPLL (when its LF is a PID controller and its MAF is adapted to the grid frequency variations) can also be an interesting option.

III. QSG-PLLs

The QSG-PLLs are single-phase variants of the conventional SRF-PLL, which is a standard three-phase PLL. The SRF-PLL schematic diagram is shown in Fig. 10. Indeed, the QSG-PLL can be understood as an SRF-PLL with an additional circuit/filter/algorithm that is responsible for generating a fictitious quadrature signal. Such orthogonal signal is needed for transferring the information to the synchronous (*dq*) reference frame.

A. Transfer Delay-Based PLLs (TD-PLLs)

1) Standard TD-PLL: Using the transfer delay (TD) is a typical approach for creating the quadrature signal. In the standard form of this method, the quadrature signal is constructed by delaying the original single-phase signal by $T/4$, where T, as noted before, is the grid fundamental period. The structure of the standard TD-PLL can be seen in Fig. 11. The shortcoming of the standard TD-PLL is that the fictitious signal, i.e., v_β, is not orthogonal to the original single-phase signal under off-nominal grid frequencies. This nonorthogonality causes double-frequency and offset errors in the estimated quantities by the standard TD-PLL. To tackle this issue, some advanced TD-PLLs have been proposed recently.

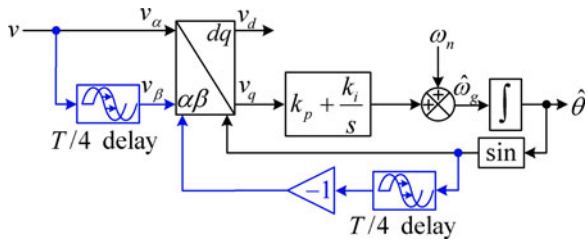

Fig. 12. Schematic structure of the NTD-PLL.

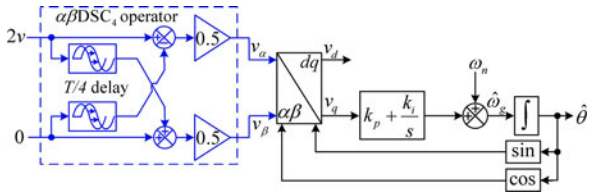

Fig. 13. Alternative mathematically equivalent representation of the standard TD-PLL.

2) Nonfrequency-Dependent TD-PLL (NTD-PLL): To mitigate the aforementioned problems of the standard TD-PLL, the indirect generation of $\cos(\hat{\theta})$ in the Park's transformation matrix by $T/4$ cycle delaying $\sin(\hat{\theta})$ is suggested in [20] and [21]. The resultant PLL, which its structure can be seen in Fig. 12, is called the NTD-PLL. Notice that this technique causes the same nonorthogonality (existing between v_α and v_β under frequency drifts) between sine and cosine terms of the Park's transformation, and consequently, corrects the phase-offset problem of the standard TD-PLL. The NTD-PLL, however, cannot solve the double-frequency problem of the standard TD-PLL. It is worth mentioning that the small-signal modeling, stability analysis, and detailed performance evaluation of the NTD-PLL can be found in [22]. It is also proved in [22] that the NTD-PLL is mathematically equivalent to a pPLL with an in-loop *dq*-frame delayed signal cancellation (*dq*DSC) operator with a delay factor 4. The *dq*DSC operator is an FIR NF, which is rather popular in designing PLLs [59], [60].

3) Enhanced TD-PLL (ETD-PLL): In [22], it is discussed that a single-phase system can be understood as an imbalanced two-phase system, in which the second phase is equal to zero. Based on this fact, it can be concluded that the standard TD-PLL is mathematically equivalent to the PLL structure shown in Fig. 13, in which the $\alpha\beta$-frame delayed signal cancellation operator with the delay factor 4 (or briefly the $\alpha\beta\text{DSC}_4$) is a well-known linear-phase FIR filter for rejecting the grid voltage imbalance in three-phase systems. Based on this equivalence, it is discussed in [22] that the double-frequency error in the standard TD-PLL under frequency drifts can be attributed to the narrow notch bandwidth of the $\alpha\beta\text{DSC}_4$ operator around the fundamental frequency of the negative sequence. Therefore, this problem can be solved by using two cascaded

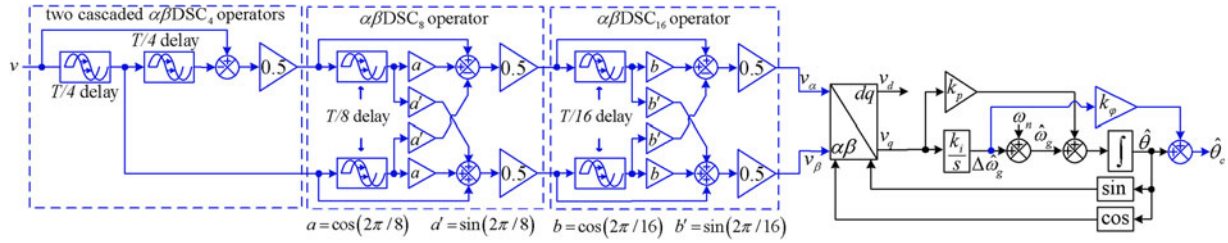

Fig. 14. Schematic structure of the ETD-PLL.

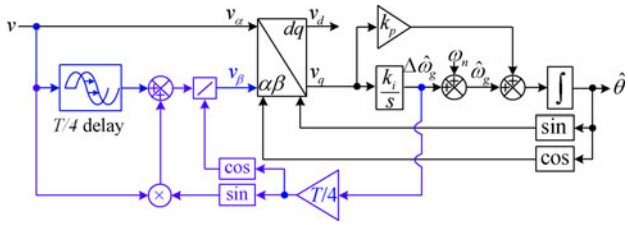

Fig. 15. Schematic structure of the ATD-PLL.

$\alpha\beta\text{DSC}_4$ operators. In a similar manner, it is shown in [22] that the phase-offset problem of the TD-PLL in the presence of frequency drifts is because of the phase shift caused by the $\alpha\beta\text{DSC}_4$ operator. Thanks to the linear-phase property of the $\alpha\beta\text{DSC}$ operators, the phase offset can be corrected by adding a linear phase error compensator (which requires one multiplication and one addition for the implementation) at the TD-PLL output. The harmonic filtering capability of the standard TD-PLL is also enhanced in [22] by using additional $\alpha\beta\text{DSC}$ operators. All these modifications result in the structure depicted in Fig. 14, which is called the ETD-PLL [22].

4) Adaptive TD-PLL: In [23], it is shown that an orthogonal version of the single-phase signal $v(t)$ under frequency drifts can be generated as

$$v_\beta(t) = \frac{v(t - T/4) + v(t)\sin(\Delta\hat{\omega}_g T/4)}{\cos(\Delta\hat{\omega}_g T/4)} \tag{2}$$

where $\Delta\hat{\omega}_g = \hat{\omega}_g - \omega_n$ is an estimation of the grid frequency deviation from its nominal value. Based on this equation, an adaptive TD-PLL (briefly called the ATD-PLL) is then presented, as shown in Fig. 15 [23]. The effectiveness and simplicity are the key features of this strategy because it can accurately generate the fictitious orthogonal signal under frequency-varying environments with a fixed-length delay. It is worth mentioning that the small-signal modeling and stability analysis of the ATD-PLL and its performance comparison with the NTD-PLL can also be found in [23].

5) Variable-Length TD-PLL: To avoid the drawbacks of the standard TD-PLL, adjusting the length of $T/4$ delay according to the grid frequency variations is sometimes recommended. To this end, the number of unit delays required for creating 90° phase shift can first be computed as

$$N = \frac{\hat{T}/4}{T_s} \tag{3}$$

where $\hat{T}$ is an estimation of the grid fundamental period, which can be calculated using the PLL estimated frequency, and T_s is the sampling period. The orthogonal signal can then be calculated by storing N samples in the memory of the processor.

The main difficulty associated with this approach is that N is most often a noninteger number, which implies a fractional delay approximation should be carried out. To deal with this problem, it is recommended in [24] to consider N as

$$N = N_i + N_f \tag{4}$$

where N_i and N_f are the integer and fractional parts of N, respectively. Based on this definition and considering an M-order Lagrange interpolation polynomial for approximating the fractional delay, the N-samples delay can be approximated by

$$z^{-N} = z^{-N_i} z^{-N_f} \approx z^{-N_i} \left(\sum_{l=0}^{M} k_l z^{-l} \right) \tag{5}$$

where

$$k_l = \prod_{\substack{m=0 \\ m \neq l}}^{M} \frac{N_f - m}{l - m}.$$

The accuracy of this approximation depends on the order of the interpolation polynomial and also the sampling frequency. When the sampling frequency is high, using a low-order interpolation polynomial is accurate enough. However, for applications where the sampling frequency is low, a high-order interpolation polynomial should be used, which demands a rather high computational effort. For a sampling frequency of 8 kHz, using a third-order interpolation polynomial is suggested in [24].

For adjusting the length of $T/4$ delay, a different approach is suggested in [25]. In this method, N [which is calculated using (3)] is defined as

$$N = N_n + N_c = N_n \left(1 + \frac{N_c}{N_n} \right) \tag{6}$$

where N_n denotes the number of samples in a quarter fundamental cycle when the grid frequency is at its nominal value and N_c is the difference of N and N_n. Notice that N_n is a positive integer, while N_c is a real number.

Based on the definition (6), the N-samples delay can be expressed as

$$z^{-N} = z^{-N_n\left(1+\frac{N_c}{N_n}\right)} = \left\{ z^{-\left(1+\frac{N_c}{N_n}\right)} \right\}^{N_n} = \left\{ z_v^{-1} \right\}^{N_n} \tag{7}$$

where z_v^{-1} is called the virtual unit delay and is approximated using a Lagrange interpolation polynomial. Therefore, according to (7), the N-samples delay can be realized by cascading N_n virtual unit delays, which implies this technique requires a high

TABLE III
NUMBER OF OPERATIONS REQUIRED FOR THE QUADRATURE SIGNAL GENERATION IN SOME ADVANCED TD-PLLS FOR A SAMPLING FREQUENCY OF 8KHZ

TD-PLLs		Number of Operations			
		S	**T**	$\times/\div$	$+/-$
NTD-PLL [20]–[22]	– – – – – – – – – – – –	80	0[a]	0	0
ETD-PLL [22]	Without harmonic filters	80	0	1	1
	With harmonic filters	140	0	13[b]	9
ATD-PLL [23]	Without trigonometric functions[c]	40	0	7	3
	With trigonometric functions	40	2	3	1
VTD-PLL	Third-order Lagrange interpolation [24]	47[d]	0	16[e]	7
	Virtual unit delay method [25]	80	0	82	42

S = Stored samples and **T** = Trigonometric functions.
[a] The special structure of the NTD-PLL [20]–[22] reduces the number of trigonometric functions required for the PLL implementation.
[b] The number of multiplications in the ETD-PLL [22] can be reduced by applying some optimizations.
[c] In creating the fictitious quadrature signal in the ATD-PLL without using trigonometric functions, the sine and cosine terms are approximated by the first two terms of their Taylor series expansion.
[d] The buffer size depends on the anticipated range of variation in the grid frequency. Here, it has been assumed that the grid frequency will be in the range of $45 - 55$ Hz.
[e] By applying some optimizations, the number of multiplications can be reduced.

computational effort, particularly when the sampling frequency is high.

Here, a TD-PLL with a variable-length delay is briefly referred to as the VTD-PLL. The implementation of the VTD-PLLs sounds to be more complicated than TD-PLLs with a fixed-length delay. Moreover, using variable-length delays makes the small-signal modeling and stability analysis of the VTD-PLLs difficult. To the best of authors' knowledge, no small-signal model for the VTD-PLLs has yet been proposed.

6) Comparison: The performance of all TD-PLLs (except for the standard TD-PLL and NTD-PLL) is more or less satisfactory. Therefore, the determining factor is their computational burden. Table III summarizes the number of operations required for the quadrature signal generation in different TD-PLLs. Based on these results, it seems that the ATD-PLL (when implemented without using the trigonometric functions) and the ETD-PLL (without harmonic filters) are the best choices. Of course, when the sampling frequency is high, the VTD-PLL with a linear interpolation can also be an interesting option as it requires a low computational effort. The NTD-PLL and the VTD-PLL (when implemented using the virtual unit delay method) are not recommended as the former suffers from double-frequency oscillatory ripples under frequency drifts and the latter demands a high computational effort. When a high harmonic filtering capability is required, the ETD-PLL (with harmonic filters) is the only available choice among TD-PLLs. Of course, the harmonic filters of the ETD-PLL may also be applied to other TD-PLLs to enhance their harmonic filtering capability.

B. Inverse Park Transformation-Based PLLs (IPT-PLLs)

The IPT-PLL is a well-known and popular PLL in single-phase applications [8], [26], [42]. In this PLL, as shown in Fig. 16, the fictitious orthogonal signal is generated by applying the IPT to the filtered *dq*-axis voltage components. While any type or order of the LPF can be used in the IPT-PLL, most often (for the sake of simplicity and minimizing the in-loop phase delay) first-order IIR LPFs are employed. The in-loop phase

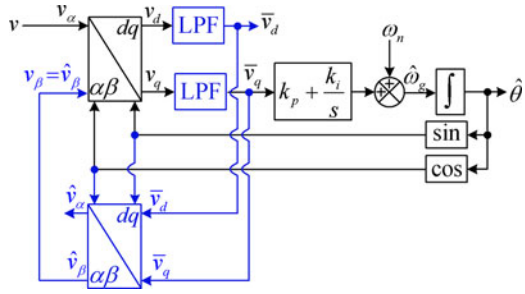

Fig. 16. Schematic diagram of the IPT-PLL.

delay caused by the *q*-axis LPF, of course, can be avoided by considering the signal v_q (instead of the signal $\bar{v}_q$) as the PI controller input. This measure, however, reduces the filtering capability and noise immunity of the IPT-PLL. It is worth mentioning that the control design guidelines and detailed analysis of the IPT-PLL can be found in [8] and [26].

When, in addition to the fundamental component, extracting the dc offset and some harmonic components are needed and/or for applications where a high filtering capability is required, the IPT-PLL can be extended as shown in Fig. 17 [24]. Obviously, selecting the number of filtering modules involves a tradeoff between the detection accuracy and computational burden.

C. Generalized Integrator-Based PLLs (GI-PLLs)

The GI-PLLs are highly popular in single-phase applications because they can be easily and effectively customized for different grid scenarios. A review of these PLLs is presented in what follows.

1) Standard Second-Order Generalized Integrator-Based PLL (SOGI-PLL): Creating the fictitious quadrature signal using an SOGI, also known as the sinusoidal integrator, is highly popular in single-phase applications because, in addition to providing a filtered fictitious orthogonal signal, it also attenuates the harmonic components in the in-phase (α-axis) component.

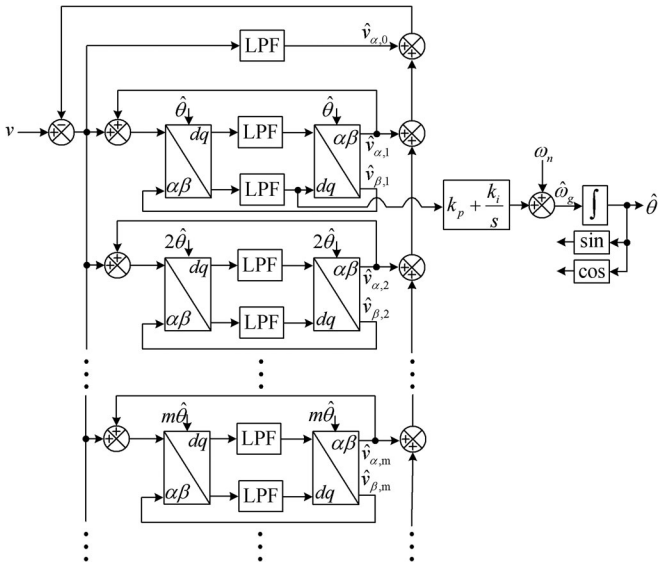

Fig. 17. Extended IPT-PLL for adverse grid conditions.

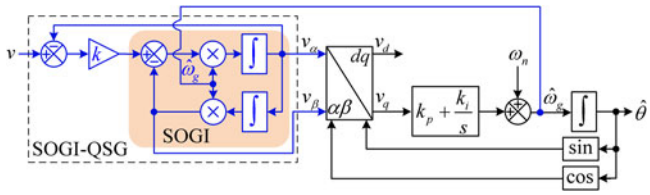

Fig. 18. Schematic structure of the standard SOGI-PLL.

The schematic diagram of the SOGI-PLL can be seen in Fig. 18 [27]. Notice that the frequency estimated by the PLL is fed back to the SOGI for adapting it to the grid frequency variations.

The small-signal modeling and control design guidelines for the SOGI-PLL can be found in [26]. It is also proved in [26] that, under certain conditions, the SOGI-PLL and the IPT-PLL are mathematically equivalent.

2) Frequency-Fixed SOGI-PLLs (FFSOGI-PLLs): As mentioned before, the estimated frequency in the standard SOGI-PLL is fed back to the SOGI-QSG block to make it frequency-adaptive (see Fig. 18). In recent years, however, some attempts for designing FFSOGI-PLLs have been made. In these PLLs, the resonance frequency of SOGI(s) is fixed at the nominal frequency.

Fig. 19(a) [28] illustrates the first method for implementing an FFSOGI-PLL, in which the β-axis output of the nonadaptive QSG-SOGI is multiplied by $\hat{\omega}_g/\omega_n$ to create balanced two-phase signals (two signals whose fundamental components have the same amplitude and 90° phase difference) in the PLL input. The α-axis output v_α, however, is not in-phase with the grid voltage v under frequency drifts. This phase difference results in a phase error in the PLL output, which is corrected by using a phase error compensator.

Fig. 19(b) [29] shows the second approach for implementing an FFSOGI-PLL, in which two nonadaptive SOGI-QSGs are

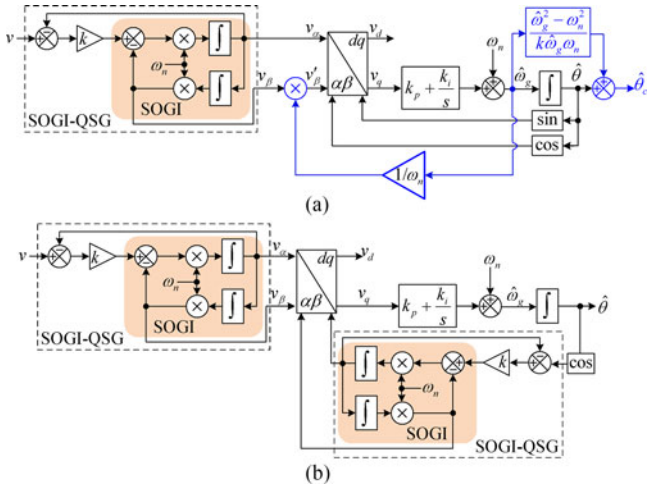

Fig. 19. Schematic structure of two FFSOGI-PLLs.

employed in the PLL structure.[2] The first one is responsible for filtering the disturbance components in the PLL input. It, however, causes phase and amplitude errors under frequency drifts. To correct these errors, a second nonadaptive SOGI-QSG is added in the feedback loop to create the same phase shift and amplitude imbalance in the sine and cosine terms of the Park's transformation. Notice that this idea is similar to that proposed for implementing the NTD-PLL (see Fig. 12).

It is worth mentioning that a critical analysis and accurate modeling of the FFSOGI-PLLs can be found in [71].

3) SOGI-QSG Structures With Enhanced DC Offset and/or Harmonic Rejection Capability: Using Fig. 18 and assuming that $\hat{\omega}_g$ is a constant, the transfer functions relating v_α and v_β to the single-phase signal v in the standard SOGI-QSG can be obtained as

$$G_\alpha(s) = \frac{v_\alpha(s)}{v(s)} = \frac{k\hat{\omega}_g s}{s^2 + k\hat{\omega}_g s + \hat{\omega}_g^2} \tag{8}$$

$$G_\beta(s) = \frac{v_\beta(s)}{v(s)} = \frac{k\hat{\omega}_g^2}{s^2 + k\hat{\omega}_g s + \hat{\omega}_g^2}. \tag{9}$$

It can be observed that the transfer function $G_\alpha(s)$ has a zero at the origin. It means that it provides a zero gain at zero Hertz, and therefore, completely rejects the dc offset. Nevertheless, the gain of $G_\beta(s)$ at zero Hertz is equal to $G_\beta(0) = k$, which means that the orthogonal signal v_β suffers from a dc offset if such component exists in the input signal v. The solid black lines in Fig. 20 clearly show this fact. These results are for $k = \sqrt{2}$. To deal with this problem, several approaches have been proposed in the literature. All these techniques are trying to add one or more origin zeros to (9) [30]–[32], [48], [61]–[64]. Some attempts to enhance the harmonic filtering ability of the SOGI-QSG have also been carried out [32], [63]–[65]. A brief review of these techniques is presented as follows.

[2]The original structure of this PLL is slightly different from what has been shown here. Despite this difference, which is for the sake of consistency with the rest of this paper, the operating principle is the same.

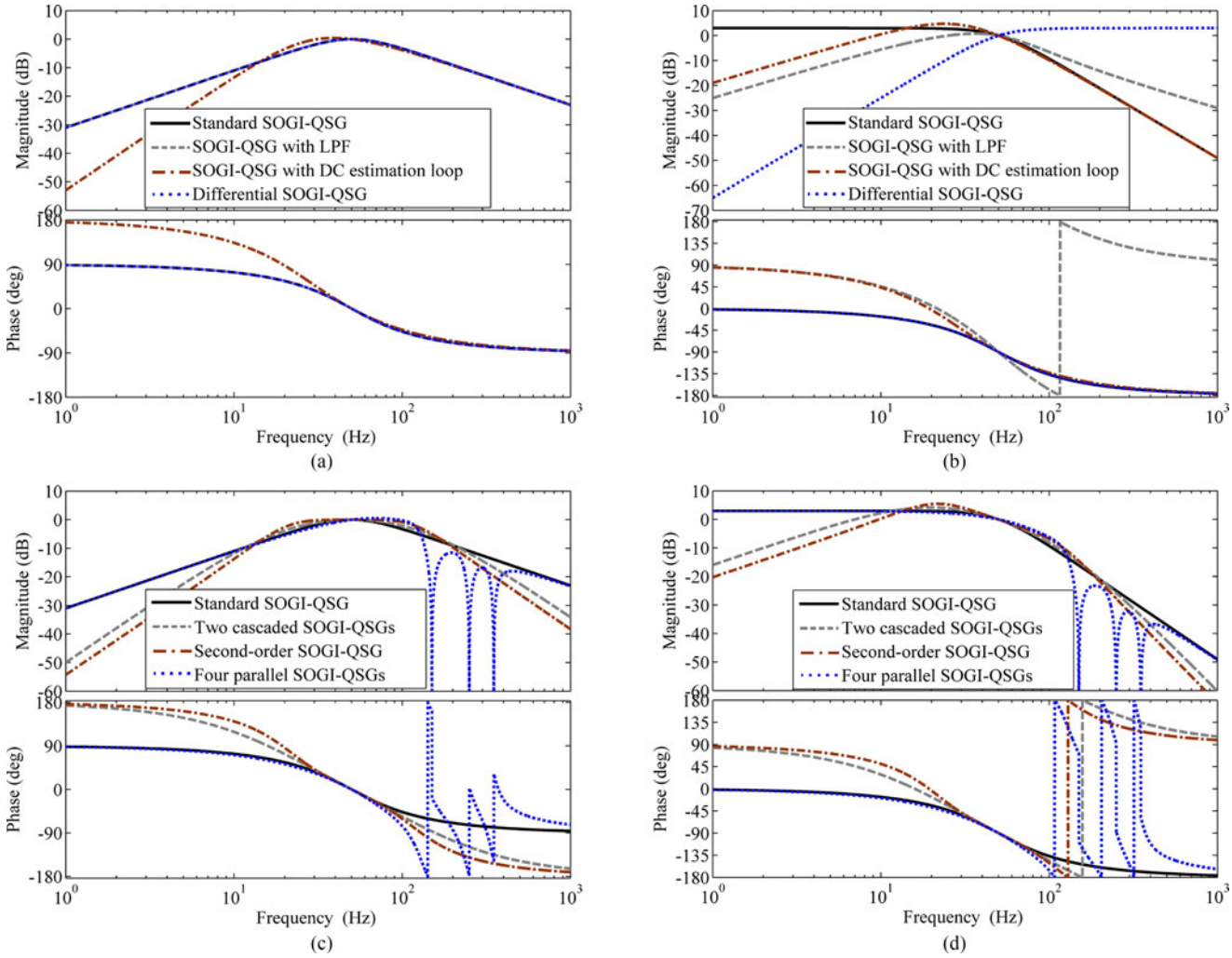

Fig. 20. Upper row: Bode plots for transfer functions relating (a) filtered in-phase output and (b) filtered quadrature-phase output to the input signal in the standard SOGI-QSG, SOGI-QSG with LPF, SOGI-QSG with dc estimation loop, and differential SOGI-QSG. Lower row: Bode plots for transfer functions relating (c) filtered in-phase output and (d) filtered quadrature-phase output to the input signal in the standard SOGI-QSG, two cascaded SOGI-QSGs, second-order SOGI-QSG, and four parallel SOGI-QSGs tuned at the fundamental, third, fifth, and seventh harmonic frequencies.

In [30], including an LPF into the SOGI-QSG, as highlighted in Fig. 21(a), is suggested. Assuming that the LPF is a simple first-order LPF as $\boldsymbol{LPF}(s) = 1/(\tau s + 1)$, where τ is its time constant, the transfer function from the single-phase signal v to the orthogonal signal v_β in this modified structure can be obtained as

$$G_\beta(s) = \frac{v_\beta(s)}{v(s)} = \frac{ks\left(\hat{\omega}_g^2\tau - s\right)}{\left(s^2 + k\hat{\omega}_g s + \hat{\omega}_g^2\right)(\tau s + 1)}. \tag{10}$$

As shown, this technique results in an origin zero, and therefore, completely rejects the dc offset in the orthogonal signal v_β. It, however, results in a reduced high-frequency harmonic and noise filtering capability. The reason is that (10) has a magnitude-frequency response that decays with a rate of -20 dB/dec at high frequencies while the high-frequency decay rate in the magnitude-frequency response of the original transfer function, i.e., (9), is -40 dB/dec. The gray dashed plot in Fig. 20(b) confirm this fact. Notice that the additional LPF has no influence on the α-axis output [see gray dashed plot in Fig. 20(a)]. The obtained results are for $k = \sqrt{2}$ and $\tau = 1/(2\pi 25)$ s.

In [48] and [61], using a dc-offset estimation loop for rejecting the dc component in the orthogonal signal v_β is suggested. Such loop, as highlighted in Fig. 21(b), requires an integrator and few mathematical operations for the implementation, and therefore, can be regarded as a very straightforward approach. Providing an estimation of the dc component and having a negligible influence on filtering of high-frequency harmonics are other characteristics of this technique. The dashed-dotted plots in Fig. 20(a) and (b) corroborates this claim. These results are obtained using $k = \sqrt{2}$ and $k_o = 0.25$.

In [31], the same structure as the standard SOGI-QSG is employed, however, the orthogonal signal v_β is taken from a different point, as shown in Fig. 21(c). This rearrangement, which results in the differential SOGI-QSG, makes the transfer function from the single-phase signal v to the orthogonal signal

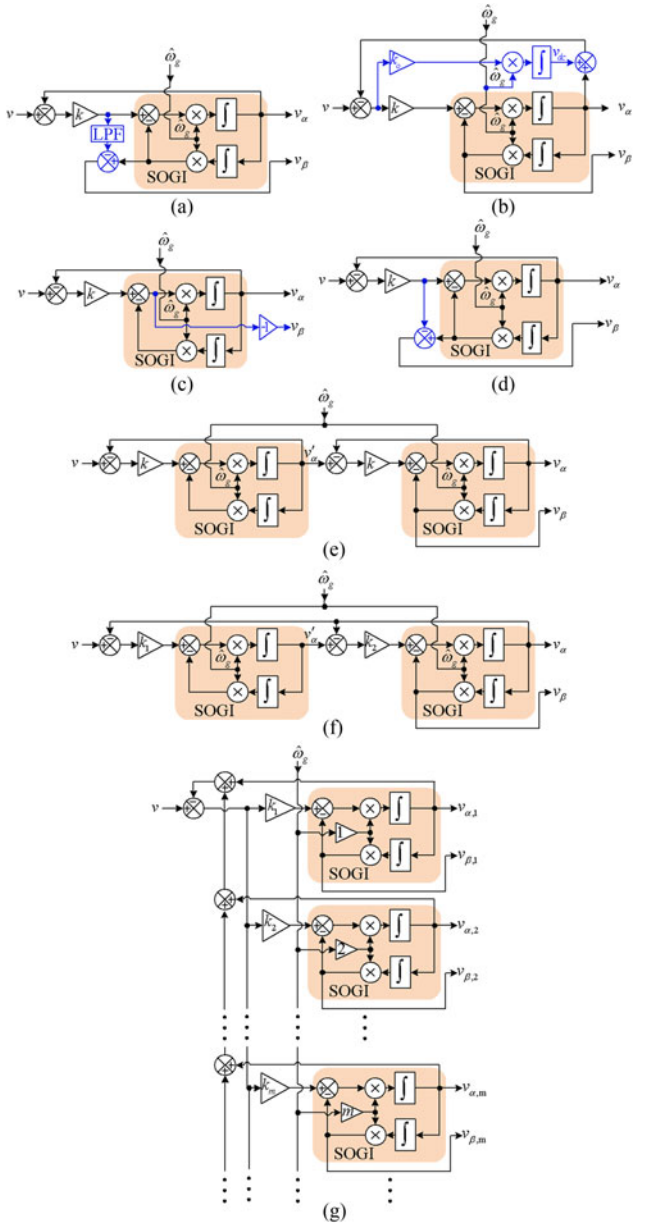

Fig. 21. SOGI-QSG structures with enhanced dc offset and/or harmonic rejection capability.

v_β as

$$G_\beta(s) = \frac{v_\beta(s)}{v(s)} = \frac{-ks^2}{s^2 + k\hat{\omega}_g s + \hat{\omega}_g^2}. \tag{11}$$

This transfer function has two origin zeros, and therefore, completely removes the dc component in the orthogonal signal v_β. However, as its numerator and denominator have the same order, it has a flat magnitude-frequency response at high frequencies, and therefore, a much lower harmonic filtering capability than the standard SOGI-QSG. This fact is clear from the dotted plot in Fig. 20(b). It is worth mentioning that Fig. 21(d) [62] is an alternative mathematically equivalent representation of Fig. 21(c).

In [32] and [63], cascading two standard SOGI-QSGs is recommended. The input of the second SOGI-QSG, as shown in Fig. 21(e), is the filtered in-phase output (v'_α) of the first SOGI-QSG. It implies that the orthogonal signal generated by this technique is completely free from any dc offset. Offering a higher harmonic filtering capability than the standard SOGI-QSG, as shown by gray dashed lines in Fig. 20(c) and (d), is another advantage of this technique. $k = 2\sqrt{2}$ has been considered for obtaining the results.

In [64], it is shown that a standard SOGI-QSG can be seen as a simple first-order LPF in which the integrator is replaced by the SOGI. Therefore, a second-order SOGI-QSG can be implemented by replacing integrators in a second-order LPF by SOGIs. Fig. 21(f) shows the schematic diagram of this second-order SOGI-QSG [64]. The complete rejection of dc component in the orthogonal signal v_β and enhanced high-frequency harmonic filtering capability are the key features of the second-order SOGI-QSG. The dashed-dotted plots in Fig. 20(c) and (d) confirm this fact. $k_1 = 1.56$ and $k_2 = 3.11$ have been considered for the obtained results.

In [65], a parallel combination of SOGI-QSGs tuned at different harmonic frequencies is suggested. These SOGI-QSGs, as shown in Fig. 21(g), are working in a collaborative way each of which is accountable for detecting a particular harmonic component and its quadrature version. In recent years, this structure has received a lot of attention for the signal decomposition purposes. The frequency response of four parallel SOGI-QSGs tuned at the fundamental, third, fifth, and seventh harmonic frequencies can be seen in Fig. 20(c) and (d). It is worth mentioning that the dc-offset estimation loop suggested in [48] and [61] can also be added to this structure.

4) Recommendation: Based on the aforementioned analysis and the Bode plots shown in Fig. 20, the following recommendations are made.

1) When only an enhanced dc-offset rejection capability for the standard SOGI-QSG is intended, the SOGI-QSG structure with the dc-offset estimation loop [see Fig. 21(b)] is recommended.
2) When in addition to rejecting the dc offset, a higher harmonic filtering capability for the standard SOGI-QSG is required, the cascaded SOGI-QSGs [see Fig. 21(e)] or second-order SOGI-QSG [see Fig. 21(f)] are suggested.
3) When a high filtering capability and, at the same time, a signal decomposition strategy are needed, the parallel combination of SOGI-QSGs [see Fig. 21(g)] preferably with the dc-offset estimation loop suggested in [48] and [61] is proposed.

D. All Pass Filter-Based PLLs (APF-PLLs)

Thanks to its ease of implementation, using a first-order APF may be attractive for creating the fictitious orthogonal signal [33]–[35]. Fig. 22 shows the schematic of the standard APF-PLL, which uses a first-order APF of the form $\mathrm{APF}(s) = (\omega_g - s)/(\omega_g + s)$ for the quadrature signal generation. Notice that the estimated frequency $\hat{\omega}_g$ is fed back to the APF for adapting it to the grid frequency changes.

Using APFs for creating the quadrature signal is not limited to the first-order ones. Indeed, high-order APFs may also be used. For example, in [33], a second-order APF is also sug-

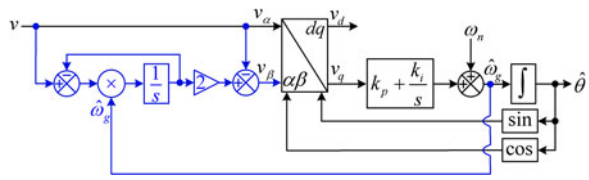

Fig. 22. Schematic diagram of the standard APF-PLL.

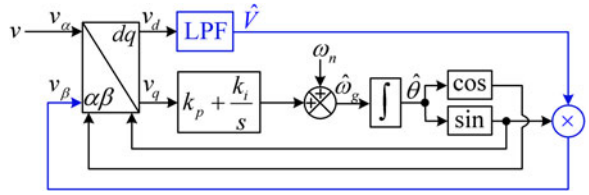

Fig. 23. Schematic diagram of the SC-PLL.

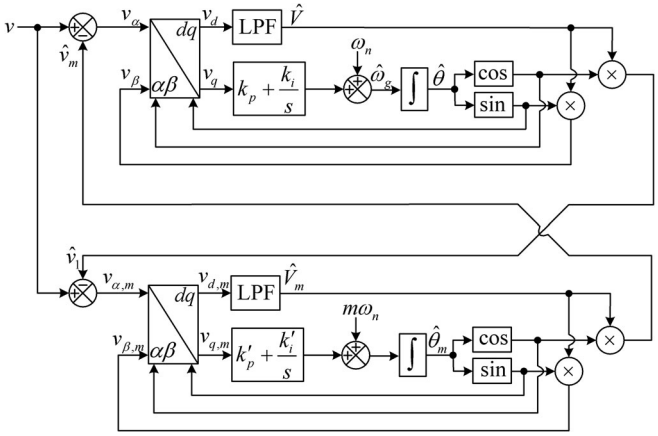

Fig. 24. Extended SC-PLL.

gested. Nevertheless, the reported results indicate no noticeable performance enhancement.

It is worth mentioning that the APF in the PLL input is not necessarily required to be frequency adaptive. Indeed, using a nonfrequency-adaptive APF is also possible. However, to correct the phase error caused by such APF, including a compensator in the PLL output is needed. Another approach is to use the same idea used in the NTD-PLL (see Fig. 12), i.e., employing a second APF for the indirect generation of $\cos(\hat{\theta})$ from $\sin(\hat{\theta})$.

E. Synthesis Circuit PLLs (SC-PLLs)

The SC-PLL [36], which is also called the simplest single-phase SRF-PLL thanks to its ease of implementation [49], constructs the orthogonal signal by using the estimated amplitude and phase angle. The schematic diagram of this PLL can be seen in Fig. 23. It is worth mentioning that the SC-PLL and IP-PLL demonstrate a very similar performance if the PI controller input signal in the IP-PLL is v_q (instead of $\bar{v}_q$).

When in addition to the fundamental component, extracting the phase and amplitude of one or more harmonic components are also needed, or when the presence of harmonics in the SC-PLL input degrades its performance, the SC-PLL structure can be extended (see Fig. 24) to take into account the presence of

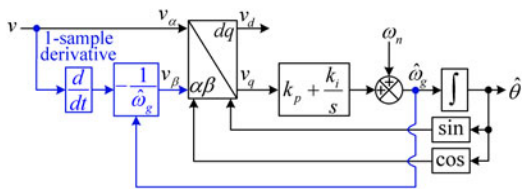

Fig. 25. Schematic diagram of the standard DPLL.

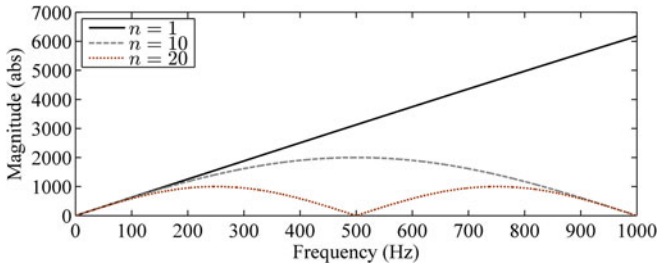

Fig. 26. Magnitude-frequency response of an n-sample differentiator for different values of n. The sampling time in this plot is $T_s = 1e-4$ s.

harmonics [36]. Considering that each extra harmonic requires an additional SC-PLL, therefore, this strategy seems computationally reasonable only when considering very few harmonic components is required.

F. Derivative PLLs (DPLLs)

In the so-called DPLL, which its typical structure can be seen in Fig. 25, the fictitious orthogonal signal is generated by using a differentiator [37]. The problem associated with this technique is that the differentiator, which is often approximated using 1-sample backward difference formula (BDF) as

$$\left.\frac{d(v)}{dt}\right|_{1-\text{sample}} = \frac{v(t) - v(t-T_s)}{T_s} \tag{12}$$

significantly degrades the PLL noise immunity. To deal with this problem, the differentiator can be calculated using the n-sample BDF as [66]

$$\left.\frac{d(v)}{dt}\right|_{n-\text{sample}} = \frac{v(t) - v(t-nT_s)}{nT_s} \tag{13}$$

where n is a positive integer. The higher the value of n, the lower the high-frequency noise amplification is (see Fig. 26). Nevertheless, the n-sample derivative, regardless of causing a longer response time, results in a nonorthogonality between the original signal v_α and the fictitious signal v_β. This problem can be corrected as explained in the following.

Assuming that $v = V\cos(\overbrace{\omega_g t + \varphi}^{\theta})$, where V, θ, and φ are the amplitude, phase angle, and initial phase angle of the single-phase signal, respectively, and substituting it into (13) results

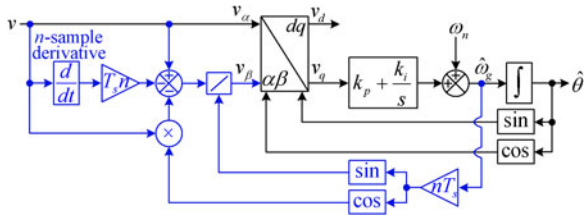

Fig. 27. Schematic diagram of a DPLL with the n-sample differentiator-based fictitious signal generator.

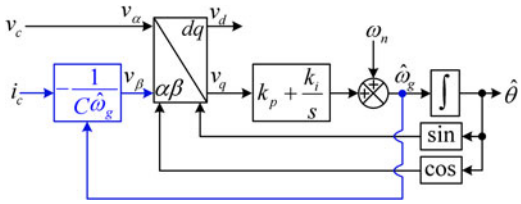

Fig. 28. Fictitious orthogonal signal generation using the inverter capacitor current.

in

$$\left.\frac{d(v)}{dt}\right|_{n-\text{sample}} = \frac{v(t)\left[1-\cos(nT_s\omega_g)\right] - \overbrace{V\sin(\theta)}^{v_\beta}\sin(nT_s\omega_g)}{nT_s}. \quad (14)$$

According to (14), the fictitious orthogonal signal v_β can be calculated as

$$v_\beta(t) = \frac{v(t)\left[1-\cos(nT_s\omega_g)\right] - nT_s\left.\frac{d(v)}{dt}\right|_{n-\text{sample}}}{\sin(nT_s\omega_g)}. \quad (15)$$

Fig. 27 illustrates a DPLL, which uses (15) for generating the fictitious orthogonal signal. For large values of n, this DPLL offers a higher noise immunity than the standard DPLL (see Fig. 25). It should be mentioned that the orthogonal signal generation based on (15) is mathematically the same as that proposed in [66]. However, here, for the sake of consistency with the standard DPLL structure, the derivative function has been kept in the calculation of v_β. It is also worth mentioning that in [38], a two-sample derivative for generating the quadrature signal is suggested. This technique offers a fast dynamic response, but a poor noise immunity. Interesting discussions about the PLL implementation using field-programmable gate array can also be found in [38].

When the PLL is employed for the synchronization and/or control purposes in single-phase inverters with *LC* output filter, the differentiator in the DPLL can be removed and the capacitor current can be used for generating the fictitious orthogonal signal [39], [40]. Notice that there is 90° phase difference between the capacitor voltage and current. Fig. 28 illustrates this idea, in which v_c and i_c denote the capacitor voltage and current, respectively, and C is its capacitance in Farads. As can be seen, the orthogonal signal generation using the capacitor current requires knowledge about the capacitor value. The problem is that the capacitor value may change depends on its aging status and working temperature. It implies that considering a constant value for C may result in an orthogonal signal with a different amplitude than the α-axis component, and consequently, a double-frequency oscillatory error in the PLL estimated quantities.

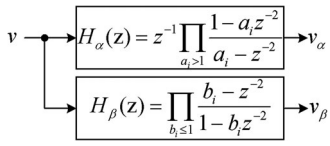

Fig. 29. Creating the fictitious orthogonal signal using an IIR HT.

G. Hilbert Transformer-Based PLLs (HT-PLLs)

The HT in essentially an APF with a particular phase-shifting characteristic, as defined in the discrete-time domain in the following:

$$H(e^{j\omega}) = \begin{cases} -j & 0 \le \omega < \pi \\ +j & -\pi \le \omega < 0. \end{cases} \quad (16)$$

In practice, however, it is very difficult to design a stable filter with such characteristic. Therefore, the HT is often approximated using IIR or FIR filters.

In [41], designing an IIR HT based on the half-band filtering [67] for creating the fictitious orthogonal signal is suggested. The discrete-time realization of this IIR HT can be observed in Fig. 29. The transfer functions $H_\alpha(z)$ and $H_\beta(z)$ in this structure are APFs, which implies their outputs, i.e., v_α and v_β, have the same amplitude as their input signal. These transfer functions also satisfy the Hilbert phase-shifting property in a wide frequency range, which means v_α and v_β are orthogonal to each other even under large frequency drifts. However, the signal v_α may not be exactly in-phase with the input signal v, at least not in the presence of frequency drifts. It means that using this IIR HT does not cause the double-frequency oscillatory error; however, it may result in a phase-offset error in the PLL output, which can be corrected by adding a phase error compensator in its output. It should be mentioned that such phase error compensator may be computationally demanding when a high-order IIR HT is used.

In [42], an FIR HT for generating the fictitious orthogonal signal is proposed. Both type-3 and type-4 FIR filters can be employed for implementing the HT. The type-3 one is often recommended as it requires half the number of multiplications than the type-4 version [38]. The type-3 FIR implementation of the HT can be observed in Fig. 30, in which N (N is an even integer) is the filter order and a_n $(0 \le n \le N)$ are the filter coefficients which are calculated as

$$a_n = \begin{cases} \dfrac{1-\cos\left[\pi(n-N/2)\right]}{\pi(n-N/2)} & n \text{ even} \\ 0 & n \text{ odd}. \end{cases} \quad (17)$$

Notice that $a_n = -a_{N-n}$.

Like the IIR HT, the FIR HT results in two orthogonal signals in its output. However, it suffers from two main shortcomings. First, there is a time delay equal to $NT_s/2$ between v and v_α, which results in a phase-offset error in the PLL output. Notice

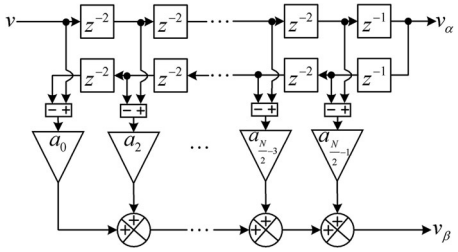

Fig. 30. Creating the fictitious orthogonal signal using a type-3 FIR HT.

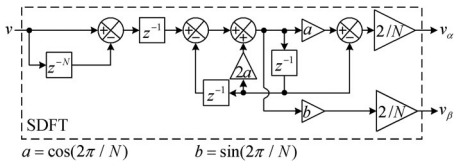

Fig. 31. Creating the quadrature signal using the SDFT.

that the signals v and v_α are supposed to be in-phase. This time delay, when it is small, can be effectively corrected in the PLL output by using a phase error compensator. However, when it is large, using the phase error compensator can significantly degrade the PLL transient behavior. Another issue associated with the FIR HT is that the fundamental component of the signal v_β has a different amplitude than that of the signal v, which demands some sort of amplitude correction. These problems make the FIR HT a complicated and computationally demanding technique for the fictitious orthogonal generation.

H. Sliding Discrete Fourier Transform-Based PLLs (SDFT-PLLs)

Creating the fictitious orthogonal signal using the SDFT, also known as the recursive discrete Fourier transform, has been recommended in [43]–[45]. The SDFT is described as

$$G_{\text{SDFT}}(z) = \frac{\left(1 - z^{-N}\right) z^{-1} e^{j2\pi/N}}{1 - e^{j2\pi/N} z^{-1}} \tag{18}$$

where N is the number of samples within the fundamental period. As shown, the SDFT includes a comb filter, which creates N zeros on the unit circle. These zeros are located at harmonic frequencies up to the aliasing point. There is also a complex pole at the fundamental frequency, which cancels a zero at the same point. Therefore, the SDFT passes the fundamental component and rejects all other harmonics up to the aliasing point. Fig. 31 illustrates the SDFT-based quadrature signal generation, which can be obtained using the real and imaginary parts of the SDFT transfer function.

The main problem associated with the SDFT is an accumulated roundoff error, which may result in the instability in a long run [68]. This problem can be mitigated by including a damping factor into the SDFT transfer function as [43]–[45]

$$G_{\text{SDFT}}(z) = \frac{\left(1 - r^N z^{-N}\right) r z^{-1} e^{j2\pi/N}}{1 - r e^{j2\pi/N} z^{-1}} \tag{19}$$

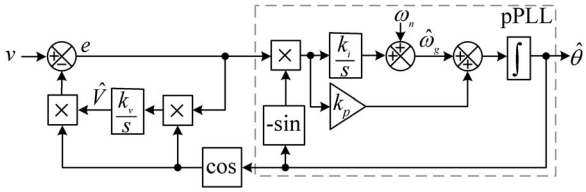

Fig. 32. Schematic diagram of the standard EPLL.

where $r < 1$ is the damping factor. This approach, however, cannot be considered very practical because it involves many manipulations and highly depends on the CPU capability [68].

Another problem is that a fixed sampling frequency with a constant N (the number of samples within the window length of the SDFT) results in offset and oscillatory errors in the SDFT-PLL output and the imperfect rejection of harmonics. To deal with this problem, three approaches can be used. The first one is employing a phase error compensator in the output of the SDFT-PLL and an amplitude compensator between the SDFT and the PLL [45]. These compensators are rather straightforward to implement; however, they do not solve the imperfect harmonic rejection problem of the SDFT under frequency drifts. The second approach is adjusting N through a frequency feedback loop. Notice that the sampling frequency is kept constant in this strategy. This approach is not recommended because changing the SDFT parameters is a sensitive task and may result in instability [69]. The third method is adjusting the sampling frequency according to the fundamental frequency variations so that their ratio remains constant [44]. In this way, aforementioned errors are corrected and the complete rejection of harmonics is achieved. The problem is that using a variable sampling frequency may not be always allowed.

I. EPLLs

The EPLL is highly popular in single-phase applications as in addition to extracting the fundamental component of its input, it estimates the phase, frequency, and amplitude of this component [47]. The schematic diagram of the standard EPLL is shown in Fig. 32. Notice that the EPLL considers the integrator output signal (within the PI regulator) as the estimated frequency. This modification results in a higher filtering capability and a more damped dynamic response in the frequency estimation. It is worth mentioning that the standard EPLL and the SC-PLL (see Fig. 23) are mathematically equivalent [49]. Therefore, the same properties attributed to the SC-PLL can be considered for the standard EPLL.

1) Type-1 and Type-3 EPLLs: The standard EPLL (like all other PLLs discussed so far) is a type-2 system from the control point of view. It implies that the standard EPLL can track phase and frequency jumps with a zero steady-state phase error. Although not as popular as the standard EPLL (the type-2 EPLL), the type-1 and type-3 EPLLs have also been proposed in the literature.

The type-1 EPLL, as shown in Fig. 33 [50], uses a simple gain as the LF. This PLL works effectively when the grid frequency is at its nominal value or very close to it. In the presence of

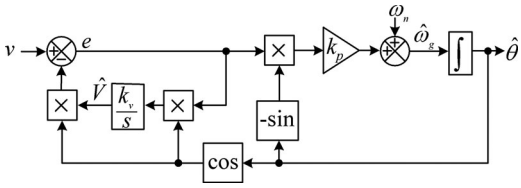

Fig. 33. Schematic diagram of the type-1 EPLL.

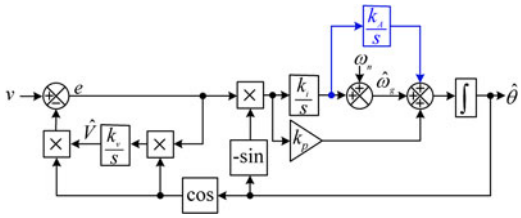

Fig. 34. Schematic diagram of the type-3 EPLL.

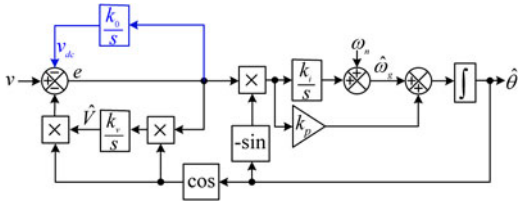

Fig. 35. Standard EPLL with a dc-offset estimation loop.

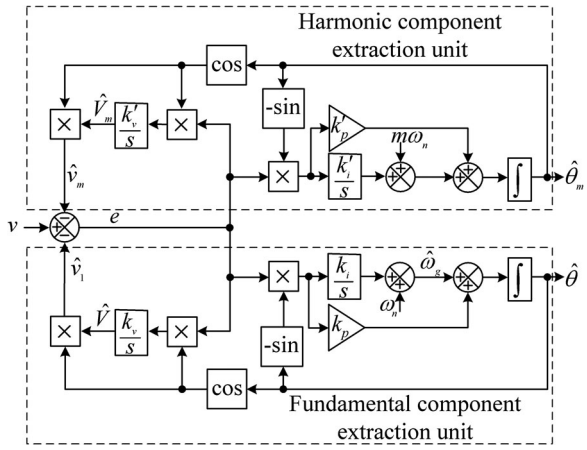

Fig. 36. Parallel EPLLs.

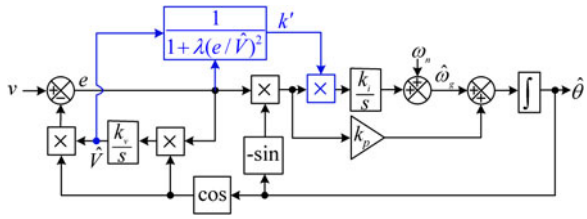

Fig. 37. Adaptive EPLL structure.

frequency drifts, however, a steady-state phase-offset error in the PLL output happens. Therefore, the type-1 EPLL may not be applicable for weak grid conditions and/or microgrids where the grid frequency undergoes large variations.

The type-3 EPLL can be realized by adding an integrator to the standard EPLL as shown in Fig. 34 [51]. This integrator creates an additional open-loop pole at the origin, which ensures a zero steady-state phase error under frequency ramping changes. This can be an interesting feature when the PLL is used for the computation of synchrophasors or for the speed control of electrical motors [70]. This advantage, nevertheless, comes at the cost of degrading the EPLL stability. To be more exact, the type-3 EPLL has a negative gain margin (GM) in decibel, which means it may become unstable under severe voltage sags and faults [70].

It should be mentioned that the type-1 and type-3 versions of other single-phase PLLs can be realized in a similar manner as the type-1 and type-3 EPLLs.

2) EPLLs With Enhanced DC Offset and Harmonic Rejection Capability: The presence of dc offset in the EPLL input, like all single-phase PLLs, results in fundamental-frequency oscillatory errors in its estimated quantities. To deal with this problem, adding a dc-offset estimation loop to the standard EPLL is suggested in [48]. Fig. 35 illustrates the EPLL with the dc-offset estimation loop. The simplicity of implementation, the complete rejection of the dc component steady-state effects on the EPLL estimated quantities, and providing an estimation of the dc component are the key features of this technique. A more detailed analysis of plugging dc-offset estimation loop in the EPLL can be found in [53].

The standard EPLL has a limited harmonic filtering capability. It implies that the presence of harmonics in the EPLL input results in oscillatory errors in the EPLL estimated quantities. To deal with this problem while maintaining a fast dynamic response, a parallel connection of multiple EPLLs can be used [51]. The number of parallel units involves a tradeoff between the detection accuracy and computational effort. For the sake of clarity, Fig. 36 illustrates the parallel connection of two EPLLs, which are responsible for detecting and separating the fundamental component and a harmonic component of order m. Notice that this structure is mathematically equivalent with the extended SC-PLL shown in Fig. 24.

Another approach to enhance the filtering capability of the EPLL (or generally all PLLs) is including window filters inside its control loop [54]. The window filters have been proven to be very effective in the rejection of disturbances inside the EPLL control loop. However, they cause a considerable phase delay inside the EPLL control loop, and consequently, degrades its dynamic response.

3) Adaptive EPLL Structure: In the standard EPLL (or generally all PLLs), there is a coupling between phase and frequency variables. In simple words, the estimated frequency by the EPLL undergoes a large transient when a phase angle jump happens. The same situation may happen during the startup if there is a large difference between the initial phase angle of the EPLL input signal and the initial value of the phase loop integrator. To tackle this problem, an adaptive mechanism is proposed in [52], in which the gain of the frequency estimation loop (k_i) is

TABLE IV
PERFORMANCE COMPARISON BETWEEN SOME ADVANCED QSG-PLLS

QSG-PLLs	Features			
	Double-Frequency Disturbance Rejection	Dynamic Response	Harmonic Filtering	Computational Burden
ATD-PLL [23]	Perfect	Fast	Medium[1]	Medium
IPT-PLL [8], [26]	Perfect	Fast	Medium[2]	Medium
SOGI-PLL [26], [27]	Perfect	Fast	Medium[3]	Medium
APF-PLL [33], [34]	Perfect	Fast	Low	Low
SC-PLL [36]	Perfect	Fast	Low[4]	Low
DPLL [38]	Perfect	Fast	Low	Low
HT-PLL [41]	Perfect	Slow	Good	High
SDFT-PLL [45]	Perfect	Fast	Good	High
Standard EPLL [46]	Perfect	Fast[5]	Low[5]	Low

[1] The harmonic filtering capability of the ATD-PLL can be enhanced by using some $\alpha\beta$DSC operators as discussed in [22].
[2] The harmonic filtering capability of the IPT-PLL can be improved by employing the extended IPT-PLL [24] as shown in Fig. 17.
[3] The ability of SOGI-PLL in rejecting harmonics can be enhanced by using cascaded SOGI-QSGs [63], second-order SOGI-QSG [64], or parallel SOGI-QSGs [65].
[4] An enhanced filtering capability can be obtained for the SC-PLL by using its extended version [36].
[5] The standard EPLL dynamic behavior, particularly during the startup and under phase angle jumps, can be further enhanced by using the adaptive mechanism proposed in [52]. The filtering capability of the standard EPLL can also be improved by the parallel connection of multiple EPLLs [51] or using window filters [54].

multiplied by

$$k' = \frac{1}{1 + \lambda(e/\hat{V})^2} \tag{20}$$

where λ is a positive design constant.

Fig. 37 illustrates this idea. When a phase angle jump happens, the error signal e becomes a large value. It makes k', and consequently, the gain of the frequency estimation loop a small value. As a result, the coupling between phase and frequency variables significantly reduces, which prevents large transients in the estimated frequency after the phase angle jump. In the steady state, when the error signal e converges to zero, the gain of the frequency estimation loop restores to its initial value. It implies that this technique does not influence the steady-state performance of the EPLL and just improves its dynamic response during the phase angle jump and startup. It should be mentioned that this strategy is applicable to other single-phase PLLs.

J. Recommendations

Table IV provides a performance comparison among some advanced QSG-PLLs. Based on these results, using the HT-PLL [41] may not be a wise choice mainly because its implementation involves a high complexity and computational effort. The performance of this PLL is not also very satisfactory. The SDFT-PLL [45] offers interesting features; however, it should be designed and applied very carefully because the roundoff accumulated error may result in instability in a long run [68]. The DPLL [38], APF-PLL [33], [34], SC-PLL [36], and standard EPLL [46] are good options only when the grid voltage is without (or with a little) harmonic pollution because they have a limited harmonic filtering capability. The best possible choices are probably the SOGI-PLL [26], [27], IPT-PLL [8], [26], and ATD-PLL [23] mainly because they provide a satisfactory compromise between the dynamic response, filtering capability and computational complexity. These PLLs can also be effectively customized for adverse grid conditions. This is particularly true for the SOGI-PLL.

IV. CONCLUSION

Providing a review of recent attempts for designing advanced single-phase PLLs was the main aim of this paper. To this end, the available single-phase PLLs were first classified into two categories: pPLLs and QSG-PLLs. The main members of each class were then described, their advantages and disadvantages were explained, and some guidelines to enhance their performances have been presented. Altogether, it seems that the majority of research efforts in the field have been focused on designing advanced QSG-PLLs and this category contains more effective PLLs than the category of pPLLs. The superiority of QSG-PLLs is particularly noticeable in their perfect double-frequency disturbance rejection. The key advantage of pPLLs perhaps lies in their simple structures, which make their analysis and tuning more straightforward than QSG-PLLs. This paper is expected to be a useful reference for new researchers, particularly those who want to make contributions in the field. In addition, it can be a reference guide for those who want to select a single-phase PLL for their particular application.

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