Isolated Bidirectional Grid-Tied Three-Phase AC–DC Power Conversion Using Series-Resonant Converter Modules and a Three-Phase Unfolder

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***Abstract*—Power-bidirectional converters are used to integrate energy storage with both dc and ac distribution grids. A modular bidirectional dc–dc converter system consisting of multiple dual-bridge series resonant converter (DBSRC) modules can be reconfigured to extend the system operating range. This paper proposes a modular three-phase ac–dc converter system by adding a line-frequency unfolder to series-connected outputs of two DBSRC modules. The DBSRC modules are controlled to output time-varying currents, which are then reconstructed into sinusoidal ac currents by the unfolder. Compared with a conventional two-stage system with a dc–dc converter and a two-level voltage-source inverter, the DBSRC–unfolder system has smaller dc-link capacitance, negligible unfolder switching loss, reduced line filter size, and faster dynamic response. The system operation and performance are verified on a 1-kW experimental prototype.**

***Index Terms*—AC–DC power conversion, current control, dc–ac power conversion, power quality, resonant power conversion.**

I. Introduction

GRID-TIED bidirectional ac–dc power converters, also known as regenerative rectifiers, have traditionally been used in industry for motor drive and power generation applications [2]. These converters enable locomotive drives to return braking energy back to the ac grid. They also allow grid connection of wind generators implemented with induction machines. The increasing usage of distributed generation sources, such as photovoltaics, has created stress on the existing ac grid due to their intermittent nature. Grid integration of energy storage such as large battery packs in electric vehicles has been proposed to improve grid stability [3]. Bidirectional ac–dc converters are needed to control power flow between energy storage systems and the ac grid [4]–[6].

International standards such as IEEE 1547 have been established to regulate the connection of distributed resources to the ac grid [7], [8]. Specific limits have been identified for each line-frequency harmonic of the ac current as well as its total harmonic distortion (THD). For low voltages, the two-level voltage-source inverter (VSI) topology is commonly adopted. The low-frequency harmonics can be easily suppressed by using high-frequency pulse width modulation and appropriate control [9]. Switching voltages in VSI contain large harmonics around the switching frequency. A line filter is required to attenuate these high-frequency harmonics in the ac current before it enters the ac grid. The filter structure and component values are chosen for a given switching frequency and the desired amount of attenuation. Keeping the filter structure and attenuation unchanged, increasing the switching frequency generally lowers the component values and, in turn, the filter size [9]. In hard-switched inverters, doing so creates more switching loss and, as a result, degrades efficiency. This design tradeoff limits filter size reduction in a two-level VSI. It can be mitigated by the use of wide-bandgap semiconductor switches or by adding soft switching [10]. Alternatively, the inverter topology can be changed to multilevel [11] or interleaved [12].

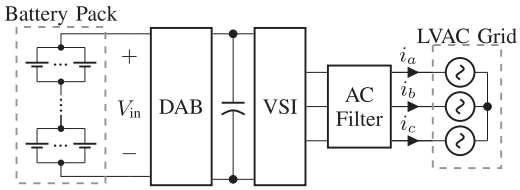

Fig. 1. Conventional bidirectional ac–dc converter system using a DAB converter and a VSI for integrating an electric vehicle battery pack into a three-phase LVAC grid [4]–[6].

The VSI requires a dc voltage higher than the peak line–line voltage. If the dc source voltage is low, a dc–dc converter is required to generate a dc-link voltage high enough for the VSI. For grid-tied battery energy storage applications, a dual-active-bridge (DAB) dc–dc converter can be used between a battery pack and the VSI in Fig. 1 [4]–[6]. In addition to providing bidirectional power flow for charging and discharging the battery, the DAB also builds in high-frequency galvanic isolation to allow easier grounding of the battery for meeting safety regulations [13]. The bulky line-frequency transformer at the VSI output may be eliminated if the dc component of the ac current is kept low enough.

The overall efficiency of a cascaded two-stage inverter system is limited by its individual stages. There has been significant research in reducing the number of power conversion stages

Manuscript received April 26, 2016; revised July 20, 2016 and October 19, 2016; accepted December 28, 2016. Date of publication January 16, 2017; date of current version August 2, 2017. This work was supported in part by the Utah Science Technology and Research Initiative. This paper was presented in part at the *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics* [1]. Recommended for publication by Associate Editor D. Xu.

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Digital Object Identifier 10.1109/TPEL.2017.2652477

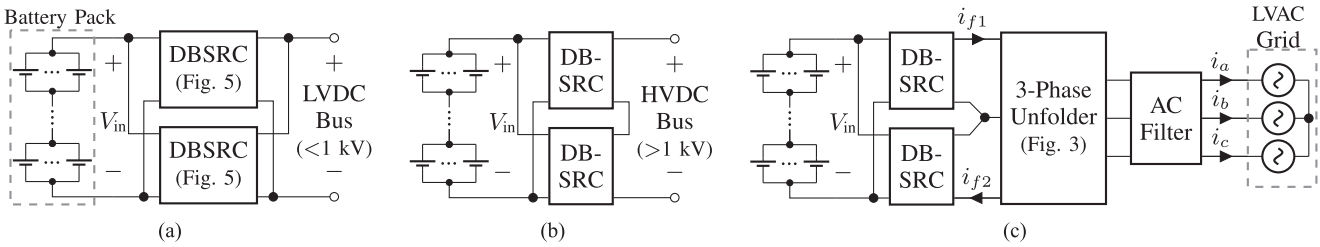


Fig. 2. Modular DBSRC system and its different configurations for dc–dc, ac–dc, and dc–ac conversions. (a) Output-parallel configuration for interfacing battery with an LVDC bus. (b) Output-series configuration for interfacing battery with an HVDC bus. (c) Proposed configuration for interfacing battery with a three-phase LVAC grid based on [19].

while retaining high-frequency isolation. A unidirectional single-stage three-phase ac–dc rectifier based on the Vienna topology is introduced by Kolar *et al.* [14]. A bidirectional single-stage three-phase ac–dc converter is proposed by Gu and Jin [15] and has a grid interface similar to a three-level VSI. The filter design in these cases is subject to the size and switching loss tradeoff that exists in the VSI, where the filter size cannot be easily reduced simply by increasing switching frequency due to increased switching loss.

In addition to the two-stage dc–dc and VSI architecture, there is another class of two-stage systems that use dc–dc followed by a single-phase line-frequency inverter, also known as an unfolder. This architecture is made popular in single-phase ac modules for photovoltaic panels [16]. For single-phase systems, the dc–dc converter is controlled to output a rectified sine wave current. The unfolder switches only at zero crossings of the ac voltage and serves to direct the dc–dc output current to the ac grid. Since the unfolder switches at line frequency and almost zero voltage, its switching loss is negligible. The overall losses are dominated by the dc–dc converter, and the system can be regarded as having only a single power conversion stage. This architecture has been used in a bidirectional electric vehicle battery charger using a DAB converter and a single-phase unfolder [17].

This paper proposes a bidirectional three-phase ac–dc converter system that consists of two high-frequency isolated dual-bridge series-resonant converter (DBSRC) modules and a single line-frequency three-phase unfolder [1]. The proposed system is modular and can be reconfigured to perform dc–dc, ac–dc, or dc–ac conversion depending on application needs. This paper is organized as follows. Motivations and advantages of the proposed system over the conventional two-stage dc–dc and VSI system are described in Section II. This is followed by operation of the three-phase unfolder in Section III. The DBSRC and a complete 1-kW system prototype are designed in Section IV. The filter requirement and control of the proposed system are described in detail in Sections V and VI. Finally, experimental results are provided in Section VII to validate the system performance.

II. System Architecture

A bidirectional dc–dc converter is needed to interface between a battery pack and a dc power distribution bus. The DBSRC can be used for this role. In addition, multiple DBSRC modules can be used for flexibility when connecting to dc buses of different voltages [18]. A system of two DBSRC modules is shown in Fig. 2(a) with inputs parallel connected to the battery. For connection to a low-voltage dc (LVDC) bus, the modules' outputs are parallel connected to increase the system's output current rating. The same system can also be connected to a high-voltage dc (HVDC) bus by series connecting the modules' outputs for increased system output voltage rating, as illustrated in Fig. 2(b).

In cases where the dc bus is unavailable, it becomes beneficial to connect the battery to the ac grid. It is desirable to reuse the DBSRC modules to save cost and meet isolation requirements. A three-phase line-frequency inverter or unfolder is proposed to be added to series-connected DBSRC outputs to provide connectivity to a three-phase low-voltage ac (LVAC) grid. The proposed system in Fig. 2(c) provides flexibility in that the unfolder can be added to perform ac–dc and dc–ac conversions or removed to use the DBSRC modules to perform dc–dc conversion. Modularity of the proposed system enables multipurpose power conversion.

In Fig. 2(c), each DBSRC module internally connects with the unfolder via a three-level dc link. The unfolder provides the system's ac port for grid connection. The input ports of the two DBSRC modules remains parallel connected to the battery. The input voltage V_{in} is largely determined by the battery's state of charge. Similar to the VSI, the proposed system primarily serves to control power flow between the battery and the ac grid. Both the DBSRC and the unfolder support bidirectional power flow.

The proposed DBSRC–unfolder system works by first synchronizing the unfolder switches to the grid voltages. The dc-link currents required to produce the desired sinusoidal ac line currents are then determined from a simple relationship based on the ac angle. Next, each DBSRC module is controlled to track the desired dc-link current profiles. The desired sinusoidal ac currents are then automatically reconstructed from the dc-link currents through the unfolder.

Alternatively, the VSI can be used in place of the unfolder between the DBSRC and the grid [4]–[6]. The advantages of using an unfolder over a VSI are summarized as follows. First, the dc-link capacitance is reduced, as the unfolder dc-link voltages are naturally time varying, and large capacitance is not needed to stiffen the voltages. Second, switching loss in the unfolder is reduced compared to that in the VSI, as the unfolder switches at line frequency. Third, the line filter requirement is relaxed, as results of a line current ripple modulated at twice the DBSRC switching frequency and a higher achievable switching frequency in a soft-switched DBSRC than in a hard-switched

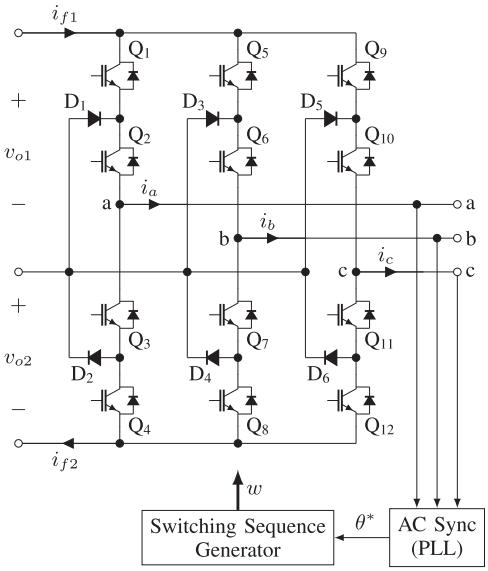


Fig. 3. Three-phase unfolder circuit based on the NPCC and related controls.

VSI. Finally, the reduction in filter component values improves the system's dynamic response. In terms of cost, the unfolder requires more switches but smaller dc-link capacitance and line filter. Therefore, the cost of adding an unfolder versus adding a VSI to the existing DBSRC modules is likely to be similar.

III. Three-Phase Unfolder

As shown in Fig. 3, the three-phase unfolder circuit is derived from the three-level neutral point clamped converter (NPCC) [19], [20]. Unlike the NPCC, the unfolder switches are not modulated at high frequency. Instead, they are programmed to switch at line frequency based on a sequence generated from the ac angle. The switching action directly connects each of the three ac phases to either the top, middle, or bottom dc-link nodes. In grid-tied configuration, the supplied ac voltages are rectified into time-varying positive voltages in the dc link. By generating dc-link currents with the appropriate time-varying wave profile using the upstream DBSRC modules, the desired ac currents are obtained.

A. Switching Sequence

The operation and control of the unfolder can be better understood by first assuming ideal three-phase positive-sequence line–line voltages of amplitude V_m described as

$$\begin{cases} v_{ab}(\theta) &= V_m \sin(\theta) \\ v_{bc}(\theta) &= V_m \sin\left(\theta - \dfrac{2\pi}{3}\right) \\ v_{ca}(\theta) &= V_m \sin\left(\theta + \dfrac{2\pi}{3}\right) \end{cases} \tag{1}$$

where the angle θ is defined as

$$\theta(t) = 2\pi f_{\text{ac}} t. \tag{2}$$

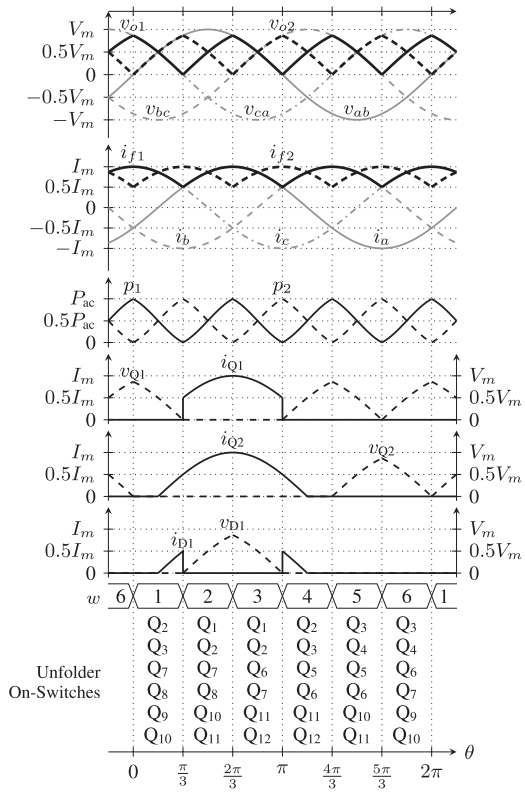


Fig. 4. Unfolder waveforms when operating at unity power factor with power flow from dc to ac, from top to bottom showing supplied line–line voltages (v_{ab}, v_{bc}, and v_{ca}) and produced dc-link voltages (v_{o1} and v_{o2}), dc-link currents (i_{f1} and i_{f2}) and reconstructed ac currents (i_a, i_b, and i_c), instantaneous power processed by DBSRC modules (p_1 and p_2), currents and voltages of selected unfolder devices (v_{Q1} and i_{Q1}, v_{Q2} and i_{Q2}, and v_{D1} and i_{D1}), and switching sequence (w).

The unfolder is controlled using a state variable w that is generated based on the estimated angle θ^*, measured using a phase-locked loop (PLL) on the ac voltages. The estimation error is hereby neglected so that $\theta^* \approx \theta$. For every multiple of 60° in θ, w updates once. This produces a sequence containing six states, in each of which a different set of unfolder switches is activated. This switching action produces a pair of time-varying voltages v_{o1} and v_{o2} in the dc link, as shown in Fig. 4. The dc-link voltages overlap with portions of the line–line voltages and vary between zero and V_{pk}, where

$$V_{\text{pk}} = \frac{\sqrt{3}}{2} V_m \approx 0.9 V_m. \tag{3}$$

The time-varying dc-link voltages reduce dc-link capacitance requirement, as bulk capacitance is not needed to maintain stiff dc voltage.

By regulating the dc-link currents with the upstream DBSRC modules, the desired ac currents of amplitude I_m can be obtained

$$\begin{cases} i_a(\theta) &= I_m \sin\left(\theta - \dfrac{\pi}{6} - \psi\right) \\ i_b(\theta) &= I_m \sin\left(\theta - \dfrac{5\pi}{6} - \psi\right) \\ i_c(\theta) &= I_m \sin\left(\theta + \dfrac{\pi}{2} - \psi\right) \end{cases} \tag{4}$$

TABLE I
UNFOLDER DC-LINK AND AC RELATIONSHIP

w	v_{o1}	v_{o2}	i_{f1}	i_{f2}
1	v_{ca}	v_{ab}	i_c	$-i_b$
2	$-v_{ca}$	$-v_{bc}$	i_a	$-i_b$
3	v_{ab}	v_{bc}	i_a	$-i_c$
4	$-v_{ab}$	$-v_{ca}$	i_b	$-i_c$
5	v_{bc}	v_{ca}	i_b	$-i_a$
6	$-v_{bc}$	$-v_{ab}$	i_c	$-i_a$

where ψ is related to three-phase active power

$$P_{\text{ac}} = \frac{\sqrt{3}}{2} V_m I_m \cos(\psi) \tag{5}$$

and power factor

$$\text{PF} = \cos(\psi), \quad -\pi < \psi \leq \pi. \tag{6}$$

Positive power factors represent forward power flow from dc to ac, and negative values from ac to dc. Operation at different power factors requires dc-link currents to have different wave profiles for producing the desired ac currents. For PF $= 1$, the dc-link and ac currents are shown in Fig. 4. The dc-link currents i_{f1} and i_{f2} vary between $0.5I_m$ and I_m. All dc-link quantities vary at a frequency of $3f_{\text{ac}}$. Reverse power flow from ac to dc is achieved by regulating the dc-link currents to negative values.

B. DC-Link and AC Relationship

The relationship between the dc-link and ac voltages and currents is obtained by analyzing the equivalent circuit of the unfolder in each of the six states. It is summarized in Table I and is valid at any power factor. The current relationship is valid at nonzero dc-link voltages. It is used to sketch dc-link waveforms in Fig. 4 and to establish design requirements on the DBSRC modules.

Each DBSRC output needs to withstand the time-varying dc-link voltage, with peaks up to V_{pk}. At unity power factors (PF $= \pm 1$), the peak dc-link current is I_m and overlaps with the voltage peak. Therefore, the DBSRC output powers p_1 and p_2 will also be time varying and swing between zero and P_{ac}, as shown in Fig. 4. In spite of this, the total power at the dc port is the sum of p_1 and p_2 and is nearly constant, with an average value of P_{ac}. Similarly, assuming a constant dc voltage, the DBSRC input currents will vary, but the total input current will be nearly constant with a small ripple at six times the line frequency. This is beneficial to the battery pack connected to the system, as it is not required to process significant line-frequency energy.

C. Device Stresses

Based on the dc-link and ac waveforms and switching sequence, current and voltage waveforms on unfolder devices Q_1, Q_2, and D_1 are also plotted in Fig. 4. Waveforms on the remaining devices are similar. They are used to derive voltage and current stresses and for device selection.

The peak voltage on all unfolder switches and diodes directly depends on the line–line voltage and is V_{pk}. By comparison, the voltage stress of NPCC switches depends on the supplied dc voltage. For an NPCC with a modulation index of 0.9, the dc voltage of $1.4V_m$ is needed, resulting in a switch voltage stress of $0.7V_m$. In this case, the switch voltage stress in the unfolder is 30% higher than the NPCC.

At unity power factors, current stresses of each outer switch (Q_1, Q_4, Q_5, Q_8, Q_9, and Q_{12}) including its antiparallel diode are

$$\begin{cases} I_{\text{swo,avg}} = \dfrac{\sqrt{3}}{2\pi} I_m \approx 0.3 I_m \\ I_{\text{swo,rms}} = \sqrt{\frac{1}{6}\left(1 + \frac{3\sqrt{3}}{4\pi}\right)} I_m \approx 0.5 I_m . \end{cases} \tag{7}$$

Current stresses of each inner switch (Q_2, Q_3, Q_6, Q_7, Q_{10}, and Q_{11}) including its antiparallel diode are

$$\begin{cases} I_{\text{swi,avg}} = \dfrac{I_m}{\pi} \approx 0.3 I_m \\ I_{\text{swi,rms}} = 0.5 I_m . \end{cases} \tag{8}$$

Each inner or outer switch conducts the corresponding line current for approximately half line period, which leads to very similar stresses for both. Current stresses of each clamping diode (D_1–D_6) are

$$\begin{cases} I_{\text{d,avg}} = \dfrac{2 - \sqrt{3}}{2\pi} I_m \approx 0.04 I_m \\ I_{\text{d,rms}} = \sqrt{\frac{1}{12}(1 - \frac{3\sqrt{3}}{2\pi})} I_m \approx 0.1 I_m . \end{cases} \tag{9}$$

The clamping diodes have very low stresses as they conduct for only one-sixth line period.

At unity power factors, the outer switches switch at near-zero voltage, while the inner switches switch with near-zero current. This in combination with line-frequency switching generates negligible switching loss. High unfolder efficiency can be obtained by using switches and diodes optimized for low conduction loss. In the 1-kW experimental system presented in Section IV, the unfolder switches are implemented with Microsemi APT75GP120JDQ3 insulated-gate bipolar transistors (IGBTs). They are intentionally oversized relative to the system power rating, as the unfolder assembly is designed to be reused in future higher power experiments.

IV. DBSRC–UNFOLDER SYSTEM DESIGN

In addition to supporting bidirectional power flow, DAB dc–dc converters provide galvanic isolation between their primary and secondary circuits. Isolation enables safe operation of multiple dc–dc modules connected input parallel output series, as previously illustrated in Fig. 2(b). With the modules connected to the unfolder and then the ac grid, as in Fig. 2(c), isolation also provides the necessary safety barrier between the battery and the grid.

In addition to isolation and power-bidirectional requirements, dc–dc modules used with an unfolder are subject to wide output voltage variation, as observed in the dc-link voltage waveforms

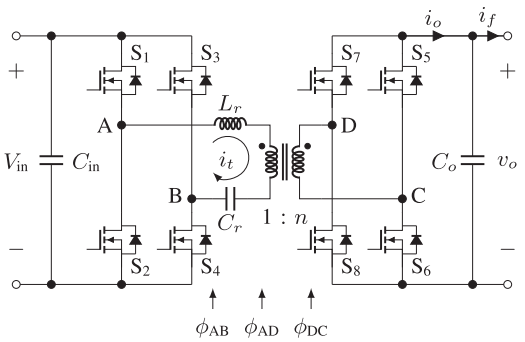


Fig. 5. DBSRC circuit modulated using three phase-shift angles.

of Fig. 4. Various topological variants of the DAB have been compared by Zhao *et al.* [21]. Compared to nonresonant or resonant transition DAB, the DBSRC offers reduced circulating current at nonunity voltage conversion ratios. Compared to other resonant variants, the phase-shift-modulated DBSRC provides faster control response. Therefore, the DBSRC topology is selected for the dc–dc module.

The maximum DBSRC output power is limited by its resonant tank design and varies with input and output voltages. In applications where a constant power characteristic is desired, the DBSRC may be replaced with the bidirectional zero-voltage-switching (ZVS) full-bridge dc–dc converter [22], whose maximum power is not limited by the topology.

A. DBSRC Design and Modulation

A single DBSRC module is shown in Fig. 5. Its experimental prototype is designed for nominal input and output voltages of 500 V each and maximum power of 2 kW. The resonant tank design procedure is based on [23]. The voltage conversion ratio

$$M = \frac{v_o}{nV_{\text{in}}} \tag{10}$$

is set to one at nominal voltages for ZVS of all switches, which results in a transformer turns ratio $n = 1$. The switching frequency is chosen as 100 kHz considering tradeoff between the magnetic component size and the converter switching loss using silicon MOSFET devices. This results in resonant inductor L_r and capacitor C_r values of 200 μH and 34 nF, respectively.

When used with the unfolder, each DBSRC processes a time-varying power of $0.5P_{\text{ac}}$ on average and a peak power of P_{ac}. Thus, although two DBSRCs are used, their maximum powers cannot be utilized simultaneously, and the system's maximum three-phase active power is equal to the maximum power of each DBSRC. Based on this characteristic of the designed unfolder and the DBSRC, the system ratings for ac–dc and dc–ac conversions are summarized in Table II. The ac voltage range is specified according to standard worldwide voltage levels and each DBSRC's output voltage range. Each DBSRC's maximum output power increases with ac voltage.

Voltages of the four switching legs in each DBSRC are phase shift modulated using three control angles ϕ_{AB}, ϕ_{AD}, and ϕ_{DC}. These angles are defined using rising edges of the leg voltages.

TABLE II
DBSRC–UNFOLDER EXPERIMENTAL PROTOTYPE

	Parameter	Value
Ratings	DC Voltage (V_{in})	500 V
	AC Line–Line Voltage	208–380 V rms
	Active Power ($\lvert P_{\text{ac}}\rvert$)	1–2 kW
DBSRC	Switching Frequency (f_s)	100 kHz
	Transformer Turns Ratio (n)	1
	Resonant Inductor (L_r)	200 μH
	Resonant Capacitor (C_r)	34 nF
	Input Capacitor (C_{in})	1 μF
	Output/DC-Link Capacitor (C_o)	1 μF
	MOSFET Switches ($S_{\{1,\ldots,8\}}$)	APT34N80LC3
Unfolder	IGBT Switches ($Q_{\{1,\ldots,12\}}$)	APT75GP120JDQ3
	Grid-Side Filter Inductor (L_g)	15 μH

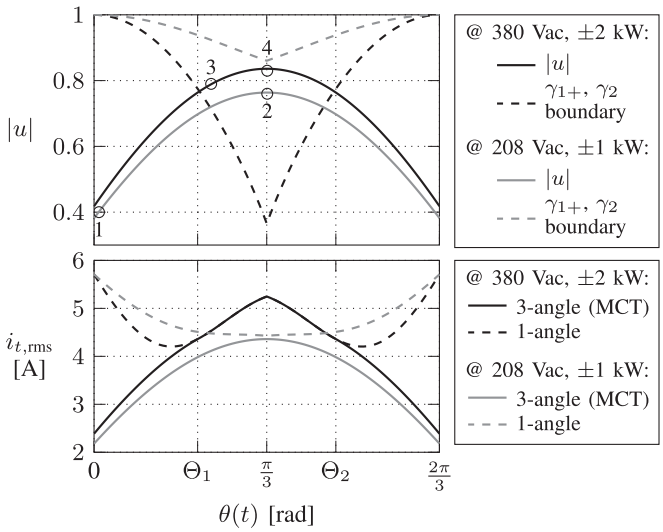


Fig. 6. Top plot shows time-varying normalized power command u and MCT of each DBSRC when used with the unfolder based on ratings in Table II. The bottom time-aligned plot compares tank rms currents in each switching period $i_{t,\text{rms}}$ between using one and three-angle modulation schemes.

They are generated using minimum current trajectories (MCTs) based on M and a normalized power command u defined as

$$u = \frac{\tilde{P}_o}{P_{\text{max}}}, \qquad -1 \le u \le 1 \tag{11}$$

where $\tilde{P}_o$ and P_{max} are the desired and maximum output powers at given input and output voltages, respectively. Introduced by Corradini *et al.*, the MCT is derived by finding angles that minimize the DBSRC resonant tank current at given M and u [23]. For $M < 1$, the generated angles belong to one of two trajectories, γ_{1+} or γ_2. Specifically, if $|u| < \sqrt{1 - M^2}$

$$\gamma_{1+}: \begin{cases} \phi_{\text{DC}} = \pi \\ \phi_{\text{AB}} = 2\pi - 2\arcsin\left(\sqrt{M^2 + u^2}\right) \\ \phi_{\text{AD}} = \dfrac{\phi_{\text{AB}}}{2} + \arctan\left(\dfrac{u}{M}\right) - \dfrac{\pi}{2}. \end{cases} \tag{12}$$

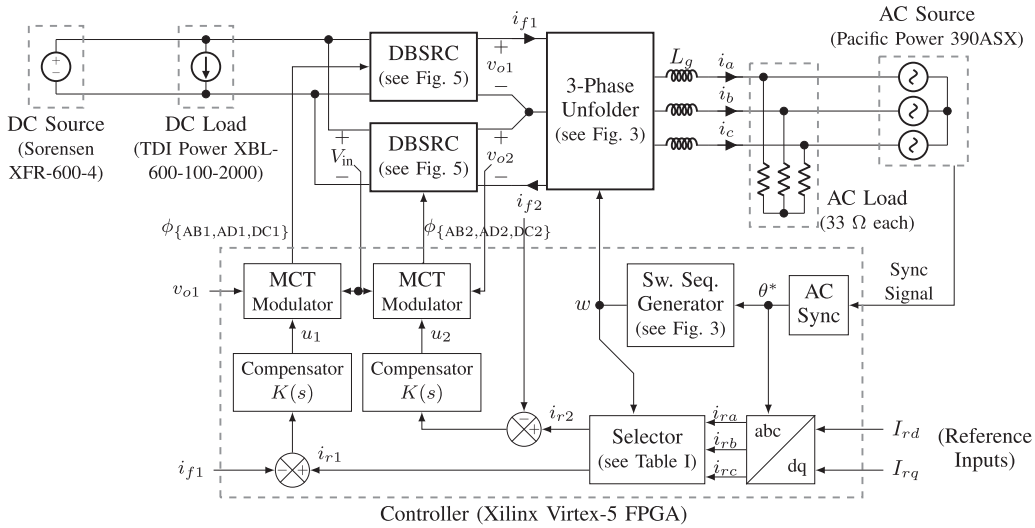


Fig. 7. Experimental setup and controller implementation of the DBSRC–unfolder system.

Otherwise, if $|u| \geq \sqrt{1-M^2}$

$$\gamma_2 : \begin{cases} \phi_{\mathrm{DC}} = \phi_{\mathrm{AB}} = \pi \\ \phi_{\mathrm{AD}} = \arcsin(u). \end{cases} \tag{13}$$

B. Resonant Tank Current in AC–DC and DC–AC Conversions

Three-angle modulation based on the MCT has been shown to provide lower DBSRC resonant tank current in dc–dc conversion especially at nonunity voltage conversion ratios compared to using one-angle modulation [23]. When used with the unfolder, both M and u in each DBSRC are slowly time varying relative to the switching period. Thus, the MCT is expected to provide minimal tank current over the line period.

The time-varying M and u may cause different trajectories being used, leading to different tank current characteristics. To determine the exact trajectories under nominal system ratings, variation in u over one dc-link period or one-third line period is plotted in Fig. 6. Also shown are the trajectory boundaries. The DBSRC operates on γ_{1+} for u less than boundary values or on γ_2 otherwise. For 208 Vrms (line–line) and $\pm$ 1 kW, the DBSRC operates on γ_{1+} at all times. For 380 Vrms (line-line) and $\pm$ 2 kW, γ_{1+} is still used for majority of time, but trajectory switches to γ_2 at around the power peaks between Θ_1 and Θ_2. Also note that this analysis is conducted at nominal input voltage of 500 V. Operating at lower input voltages may lead to $M > 1$ with a different set of trajectories being used [23].

With operating trajectories known, the rms tank currents in each switching period $i_{t,\mathrm{rms}}$ over one dc-link period is also plotted in Fig. 6. Only the fundamental current component is considered. Shown for comparison are the rms currents using one-angle modulation or equivalently operating on γ_2 trajectory at all times. The rms currents are lower or at least equal using MCT, and the difference is especially noticeable at power valleys. Therefore, using MCT yields lower overall rms current over the line period. At 208 Vrms (line–line) for instance, the overall rms tank current is only about 30% higher than the rms line current. The reduced tank current leads to lower conduction and switching losses.

C. Experimental System Construction

The designed DBSRC, line filter, and unfolder parameters are summarized in Table II. They are implemented in hardware and connected to an experimental setup shown in Fig. 7.

The DBSRC inputs are parallel connected to a dc voltage source and an electronic load configured in the constant current mode. The dc source and load together simulate a battery pack. Similarly, the unfolder outputs are connected to both a three-phase ac voltage source and a resistive load, which together represent the ac grid. This setup allows bidirectional power flow and provides well-regulated ac and dc voltages, as the DBSRC–unfolder prototype is primarily tested for ac current regulation and dynamic response.

The DBSRC output currents contain a large ripple at twice switching frequency or 200 kHz in the experimental prototype. The current ripple contributes to grid current harmonics around and beyond the ripple frequency. To attenuate this ripple, inductors L_g are added to unfolder ac port, as shown in Fig. 7, and form a three-phase *LC* filter with the existing DBSRC output capacitors C_o. The inductance used in the experiment is 15 μH to provide $-$37-dB attenuation at 200 kHz with C_o at 1 μF. A detailed filter design procedure is provided in Section V.

A Xilinx Virtex-5 field-programmable gate array (FPGA) is used to control both DBSRC modules and the unfolder. Synchronization with the ac voltages is performed using a digital synchronization signal generated from the ac source. The ac angle is then estimated and used in both unfolder control and DBSRC reference current regeneration. First, three-phase reference currents i_{ra}, i_{rb}, and i_{rc} are generated based on the desired d- and q-axis references I_{rd} and I_{rq}. These reference components are adjusted directly in the experiment to obtain different active and reactive powers delivered to and received from the grid. The references can also come from an outer

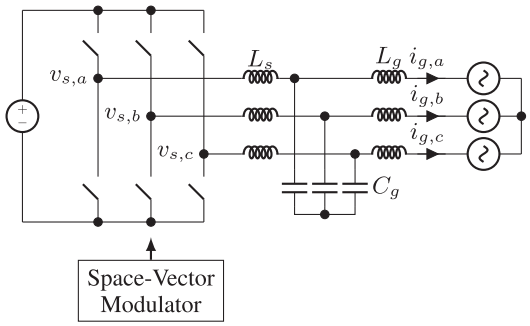


Fig. 8. Two-level VSI with an *LCL* filter.

control loop to achieve ac voltage and frequency regulation in a microgrid [8], using, for instance, the droop method [24]. Next, the DBSRC references i_{r1} and i_{r2} are generated from the three-phase references using the unfolder switching sequence and the relationship outlined in Table I. Each DBSRC module is controlled in closed loop to regulate its output current to track its reference. Regardless of the type and implementation of the outer control loop, these inner current loops shall have fast and accurate reference tracking to produce the desired ac currents. This is achieved through controller optimization, which is detailed in Section VI. Performance of the experimental system is evaluated in Section VII.

V. AC Line Filter Comparison

A quantitative comparison of filter requirements is presented here between the DBSRC–unfolder and the VSI using the IEEE 1547 harmonic limits [7].

A. Two-Level VSI Filter Design

As shown in Fig. 8, a two-level VSI with space-vector modulation is considered [25]. Its *LCL* filter is designed using methods and conditions specified by Beres *et al.* [26]. It operates at 10 kW and 10 kHz, with a dc voltage of 700 V and an ac line–line voltage of 380 V rms and 50 Hz. The magnitude of per-phase inverter switching voltage harmonic is $V_s(h)$, where h is the harmonic order relative to line frequency. The filter admittance $Y(h)$ determines the magnitude of filtered grid current harmonic $I_g(h)$

$$I_g(h) = Y(h) \cdot V_s(h) \tag{14}$$

where $Y(h)$ depends on the impedances of the filter components L_s, L_g, and C_g [26]. The dominant harmonic occurs at $h = m_f - 2$, where the modulation frequency m_f is defined as the ratio between switching and line frequencies. At 10 kHz, the modulation frequency is $m_f = 200$. The filtered grid current is set to the limit I_{lim} imposed by IEEE 1547 as

$$I_g(m_f - 2) = I_{\text{lim}}(m_f - 2) = 0.003 I_m\,. \tag{15}$$

The inverter voltage $V_s(m_f - 2)$ is obtained in simulation. The required filter admittance $Y(m_f - 2)$ of this 10-kW inverter is then obtained as -60 dB. The filter components can then be selected. The filter capacitor C_g is chosen as 10 μF or 5% of base capacitance.

TABLE III
Filter Design Summary

Parameter	10-kHz VSI	10-kHz SRC-UF	100-kHz SRC-UF	Unit
DC Voltage		700		V
AC Line–Line Voltage		380		Vrms
AC Frequency		50		Hz
Active Power		10		kW
Filter Capacitor (C_g)		10		μF
Inductor Window Fill Factor		≈ 40		%
Inductor Temp-Rise		≈ 40		°C
Converter-Side Inductor (L_s)	1.3	–		mH
Core	T400-34D	–		–
Turns	135	–		–
Wire Gauge	9	–		AWG
Copper Loss	14	–		W
Core Loss	13	–		W
Wound Volume	397	–		cm^3
Grid-Side Inductor (L_g)	0.5	1	0.01	mH
Core	T249-34	T400-34	T80-40B	–
Turns	96	180	18	–
Wire Gauge	11	10	14	AWG
Copper Loss	12	20	1.5	W
Wound Volume	126	254	6	cm^3
Total Wound Volume	523	254	6	cm^3

The filter inductances L_s and L_g are selected to obtain the required filter admittance and to minimize the total inductor volume. The Micrometals Inductor Design Software is used to generate complete designs using iron powder toroidal cores [27]. All designs use a set of common constraints that include maximum temperature rise of 40 °C and maximum window fill factor of 40%. Both copper and core losses are considered for the converter-side inductor L_s, while only copper loss is considered for the grid-side inductor L_g as its core loss is insignificant. The minimal volume design results in L_s of 1.3 mH using T400-34D core and L_g of 0.5 mH using T249-34 core. The selected filter component values are comparable to those obtained by Beres *et al.* using the optimal design method to minimize stored filter energy [26]. The designed VSI filter is summarized in Table III.

B. DBSRC–Unfolder Filter Design

The line filter of the DBSRC–unfolder system is now designed and compared with the VSI. To ensure a fair comparison, operating conditions, switching frequency, and filter structure are kept the same. An *LC* filter is used at the unfolder ac terminals. For filter design purposes, the DBSRC modules are modeled as controlled current sources, as shown in Fig. 9(a).

The DBSRC output currents i_{o1} and i_{o2} are modeled as amplitude-modulated rectified sine waves at twice switching frequency. For the line filter design, minimal tracking error between actual and reference DBSRC currents is assumed, so that low-order ($h < 50$) harmonics are negligible. Each of the two

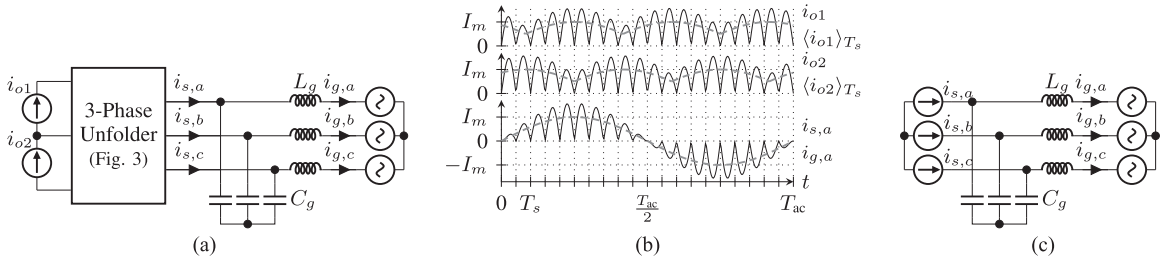


Fig. 9. DBSRC–unfolder with an *LC* filter. (a) System diagram with the DBSRC modeled as controlled current sources. (b) Unfiltered and filtered current waveforms for $f_s = 10 f_{\text{ac}}$. (c) Equivalent circuit model.

DBSRC output currents can then be described as

$$i_o(t) = i_r(t) \cdot \left| \frac{\pi}{2} \sin(2\pi f_s t) \right| \tag{16}$$

where i_r is the reference current. Given a much higher switching frequency than line frequency, the fast-averaged output current $\langle i_o \rangle_{T_s}$ can be considered equal to its reference. Passing i_{o1} and i_{o2} through the unfolder results in modulated three-phase currents $i_{s,a}$, $i_{s,b}$, and $i_{s,c}$, in which phase-a current is

$$i_{s,a}(t) = I_m \sin(2\pi f_{\text{ac}} t) \cdot \left| \frac{\pi}{2} \sin(2\pi f_s t) \right|. \tag{17}$$

It is desired to attenuate switching frequency harmonics in i_s to produce filtered grid current i_g. Exemplary waveforms illustrating i_o and i_s are shown in Fig. 9(b) for the case $f_s = 10 f_{\text{ac}}$.

The modulated three-phase currents can be modeled as current sources, resulting in a simplified equivalent circuit shown in Fig. 9(c). It is suitable for the filter design as linear analysis techniques can be applied. The relationship between magnitudes of source current $I_s(h)$ and filtered grid current $I_g(h)$ is

$$I_g(h) = F(h) \cdot I_s(h) \tag{18}$$

where $F(h)$ is the filter attenuation at harmonic order h, and

$$F = \frac{Z_C}{Z_C + Z_L} \tag{19}$$

where Z_C and Z_L are impedances of filter capacitance C_g and inductance L_g, respectively.

The dominant harmonic order is $h = 2m_f - 1$, as the source current is modulated at twice switching frequency. Using the Fourier analysis, the relationship between magnitudes of the dominant source current harmonic $I_s(2m_f - 1)$ and the fundamental is

$$I_s(2m_f - 1) = \frac{I_m}{3}. \tag{20}$$

In this analysis, the DBSRC switching frequency is set to 10 kHz or same as the VSI, for fair comparison. The filtered grid current is also set to the same IEEE 1547 limit I_{lim} as

$$I_g(2m_f - 1) = I_{\text{lim}}(2m_f - 1) = 0.003 I_m. \tag{21}$$

The required filter attenuation at dominant harmonic $F(2m_f - 1)$ can then be found as -40 dB. Keeping filter capacitance C_g unchanged at 10 μF, the required filter inductance L_g is 1 mH. Using the same inductor design constraints results in T400-34 core for L_g. The designed DBSRC–unfolder filter is summarized in Table III.

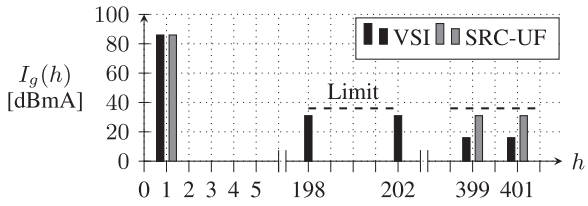


Fig. 10. Harmonic spectra of and IEEE 1547 limit on filtered line currents in the VSI and the DBSRC–unfolder with designed filters in Table III.

Using the designed filters, harmonic spectra of filtered grid currents in both systems are obtained in simulation and plotted in Fig. 10. Both systems have been designed to meet the IEEE 1547 current harmonic requirements. In comparison, the total inductor volume in the DBSRC–unfolder is about 50% smaller than that in the VSI. The size reduction is first due to smaller inductance required to meet filter requirements. This is a result of DBSRC output currents modulated at twice the switching frequency. The absence of the converter-side inductor in the DBSRC–unfolder also contributes to size reduction, as this inductor size in the VSI cannot be easily reduced due to significant core loss.

The filter size in both systems can be further reduced by increase in switching frequency. Burkart and Kolar claim that for a 10-kW two-level VSI implemented with SiC devices, increasing switching frequency beyond 20 kHz provides diminishing return on reduction of inductor volume [28]. The main reasons provided are increased switching loss, which requires more heatsink volume, and high-frequency inductor loss, which complicates the inductor design. In comparison, the DBSRC has been shown to operate at higher switching frequencies at similar power levels. A 15-kW 50-kHz DBSRC with 94% peak efficiency is reported by Du *et al.* [29]. Switching loss in the DBSRC can be more easily managed due to resonance during switching transitions. In addition, the filter inductor L_g in the DBSRC–unfolder is on the grid side and is not subject to high-frequency losses. Considering harmonic requirements alone, the inductor size can be easily reduced with increased DBSRC switching frequency. To demonstrate, the switching frequency in the 10-kW DBSRC–unfolder system is increased to 100 kHz. Keeping all other operating conditions unchanged, including C_g at 10 μF, reduces L_g to only 10 μH. The

filter design with the increased switching frequency will require consideration of conducted emission limits, in addition to grid current harmonic limits. Nevertheless, reduction of the filter size through increased switching frequency can be more easily accomplished in the DBSRC–unfolder compared to the VSI.

VI. DBSRC Module Control

While the high-order ($h > m_f$) harmonics can be effectively attenuated through an appropriate filter design, the low-order ($h < 50$) harmonics are suppressed by control of the DBSRC modules. Referring to Fig. 7, since the dc-link and ac currents are directly related, high-quality ac currents are obtained through accurately regulated dc-link currents. This is achieved through optimizing the DBSRC closed-loop current regulation bandwidth, so that accurate tracking between reference and actual output currents is obtained. A high bandwidth also improves the system's dynamic response to rapidly respond to changes in reference inputs.

A. DBSRC Modeling

Knowledge of the DBSRC control to output current characteristic is necessary for the controller design. The dc or steady-state relationship is first derived, followed by the linearized small-signal relationship. The phasor model developed based on the fundamental approximation is used [30].

In steady state, regardless of whether the MCT is used, the output current I_o can be expressed as

$$I_o = \frac{8}{n\pi^2}\frac{H_0}{Z_0}V_{\text{in}}\sin\left(\frac{\Phi_{\text{AB}}}{2}\right)\sin\left(\frac{\Phi_{\text{DC}}}{2}\right) \cdot \sin\left(\Phi_{\text{AD}} + \frac{\Phi_{\text{DC}} - \Phi_{\text{AB}}}{2}\right) \tag{22}$$

where H_0 and Z_0 are constants dependent only on tank parameters and switching frequency [23]. Notice that I_o only depends on the steady-state input voltage V_{in} and control angles but not on output voltage V_o. Therefore, the DBSRC can be regarded as a near-ideal current source in steady state. This characteristic is desirable, as when used with the unfolder, the DBSRC output voltage is time varying, and a weak dependence of output current on output voltage is preferred, as the output current is to be controlled to track a reference unrelated to the output voltage.

In the dynamic case, for the three-angle modulated DBSRC using the MCT, the small-signal power command to output current transfer function

$$G(s) = \frac{\hat{i}_o(s)}{\hat{u}(s)} \tag{23}$$

can be derived by linearizing the large-signal nonlinear state equations around dc operating points on given trajectory [31]. The Bode magnitude plots of $G(s)$ for selected points in Fig. 6 are shown in Fig. 11. Points 1 and 2 are on the γ_{1+} trajectory, while points 3 and 4 are on the γ_2 trajectory. Closer inspection reveals that points 1 and 2 have identical low-frequency gain, while it varies between points 3 and 4. In fact, it can be shown that the low-frequency gain is invariant for any dc operating point on $\gamma_{1\pm}$ trajectories at constant input voltage but varying output voltage and power. The same does not apply to other trajectories. For the considered DBSRC design, the maximum low-frequency gain variation is only $\pm$ 1 dB under all conditions, as the DBSRC operates primarily on γ_{1+} unless at high ac voltages and powers where it shifts to γ_2.

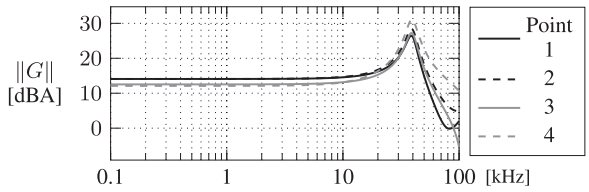


Fig. 11. Bode magnitude plots of DBSRC control to output current response $G(s)$ obtained by linearizing around various operating points in Fig. 6.

In summary, the DBSRC control response in the considered design is quite consistent under varying dc-link voltage and power.

B. Compensator Design

From Fig. 11, $G(s)$ of the considered DBSRC design shows a flat gain for frequencies up to the resonant poles at $f_s - f_0$, where f_s and f_0 are the switching and tank resonant frequencies, respectively. The closed-loop regulation bandwidth is chosen below this frequency to avoid high-frequency unmodeled dynamics. In addition, it is also desired to achieve zero steady-state error as well as attenuation of high-frequency noise. The current loop compensator is, therefore, implemented with an integrator

$$K(s) = \frac{\omega_k}{s}. \tag{24}$$

The integrator gain or unity-gain frequency ω_k is chosen such that the closed-loop response is stable and achieves the desired regulation bandwidth.

Since, for the considered operating conditions, $G(s)$ shows little gain variation, a constant gain compensator will be sufficient to achieve the performance goals and is, therefore, chosen for this design. For cases such as varying input voltage where more variation in control response is to be expected, a gain-scheduled controller with varying gain can be used [31].

C. Compensator Tuning and System Performance

The integrator gain ω_k is selected through both frequency-domain analysis and by evaluating the performance of the complete system with two closed-loop DBSRCs and the unfolder. Computer simulation is carried out using Simulink with each DBSRC and unfolder implemented with full-switching circuit models using the PLECS blockset. The system's dc and ac ports are connected to ideal voltage sources in simulation.

THD of the ac current at unity power factor is measured and recorded in simulation for various closed-loop regulation bandwidth f_c that results from different ω_k values. THD is plotted against f_c in Fig. 12. As expected, an increase in the bandwidth results in better tracking between actual and reference dc-link

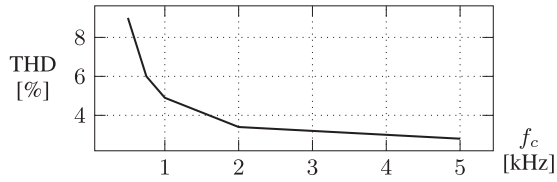


Fig. 12. Simulation ac current THD versus designed DBSRC regulation bandwidth f_c at -0.75 kW, 208-Vrms ac line–line, and 500-V dc voltages.

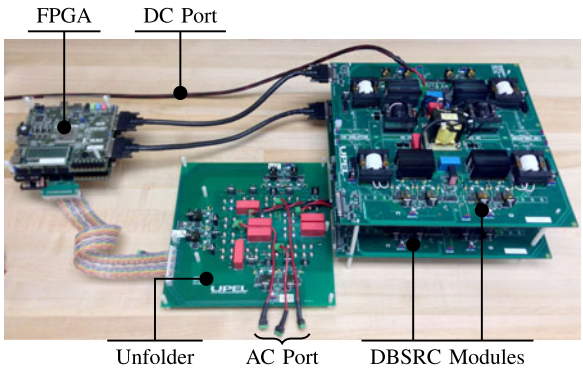


Fig. 13. Photo of the DBSRC–unfolder hardware prototype.

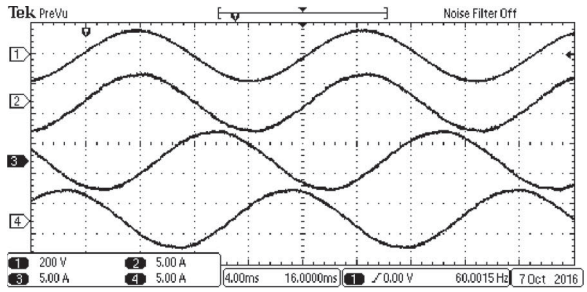
currents and lower ac current THD. The final integrator gain is chosen for a bandwidth of 5 kHz.

A high regulation bandwidth is also necessary to produce reactive ac currents at nonunity power factors. In such cases, the reference currents (i_{r1} and i_{r2} in Fig. 7) can contain large steps around unfolder state transitions. A high bandwidth reduces rise and settling times of actual output currents and reproduces these reference steps. The result is high-quality ac currents at any power factor.

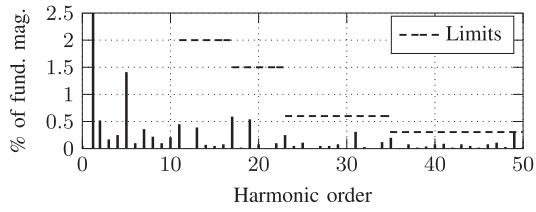
VII. Experimental Verification

An experimental system of the DBSRC–unfolder has been constructed with parameters in Table II and connected, as shown in Fig. 7, with controller optimizations from Section VI to evaluate its ac current regulation and dynamic response. A photo of the system prototype is shown in Fig. 13. In addition to the power circuits of Figs. 3 and 5, the unfolder and DBSRC modules contain all associated gate-drive circuits, while each DBSRC additionally contains voltage and current sensors and analog-to-digital converters. Grid-side filter inductance of 15 μH, as selected in Section IV, is used in all experiments. All experimental results are obtained at a dc voltage of 500 V and an ac line–line voltage of 208 Vrms.

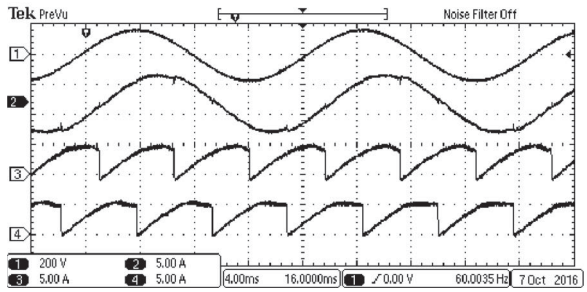
The steady-state ac current waveforms at unity power factor are shown in Fig. 14(a). The experiment is conducted for positive power flow or delivering 1.2 kW to grid. The three ac currents are measured following reference directions shown in Fig. 3. The line-neutral voltage of phase a is also displayed to show the phase relationship. The oscilloscope data for current i_a are used to obtain the harmonic spectrum in Fig. 14(b). All harmonics are within the IEEE 1547 limits. The corresponding THD is 2.5% and matches with simulation results in Fig. 12.



(a)



(b)



(c)

Fig. 14. Experimental steady-state waveforms at 1.2 kVA and different power factors. (a) At PF $= 1$ and delivering 1.2 kW to grid, displaying Channels 1 through 4 as line-neutral voltage v_{an}, ac currents i_a, i_b, and i_c, respectively. (b) Harmonic spectrum of and IEEE 1547 limits on i_a at PF $= 1$. (c) At PF $= 0.8$ and delivering 1 kW and 0.7 kvar to grid, displaying Channels 1 through 4 as v_{an}, i_a and dc-link currents i_{f1} and i_{f2}, respectively.

Operation at the power factor of 0.8 is verified in Fig. 14(c). The displayed dc-link currents show expected profile as required at this power factor. The measured THD of 4% is slightly higher than at unity power factor. Further controller optimization is expected to reduce THD.

The ac currents during a power reversal transient are shown in Fig. 15(a). Prior to the event, the system is delivering 0.5 kW to the grid. A positive-to-negative step change is then applied to d-axis reference current. The high DBSRC regulation bandwidth causes both dc-link currents to settle within 1 ms, as shown in Fig. 15(b). This results in ac currents that receive 0.5 kW from the grid. The instantaneous active power is obtained from data points in Fig. 15(a) and plotted in Fig. 15(c). The small settling time on active power demonstrates fast system dynamics.

System efficiency and ac current THD are plotted against the active power in Fig. 16. Efficiency reaches 91% at 0.5 kW and continues to increase to 93% at 1.2 kW at both power-flow directions. Reasonable efficiency is maintained over a wide range of power due in part to low resonant tank current using MCT-based multiangle modulation in the DBSRC modules. It can be

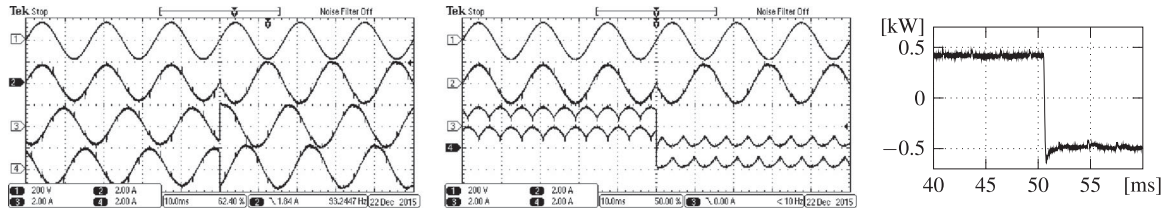


Fig. 15. Experimental waveforms for a step change in d-axis reference current to reverse active power from 0.5 to −0.5 kW. (a) Channels 1–4 are line-neutral voltage v_{an}, ac currents i_a, i_b, and i_c, respectively. (b) Channels 1 through 4 are v_{an}, i_a and dc-link currents i_{f1} and i_{f2} respectively. (c) Calculated instantaneous active power from waveforms.

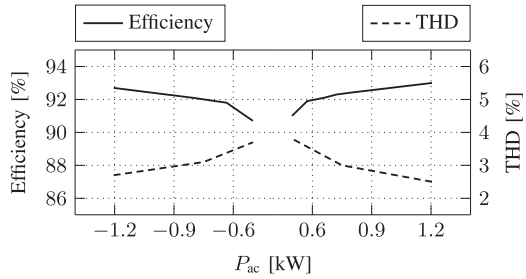


Fig. 16. System efficiency and ac current THD versus active power.

improved by further optimizing the DBSRC power stage component design and extending the soft-switching range. Minimum ac current THD of 2.5% is reached at 1.2 kW. The current distortions can be further reduced by controller optimization.

VIII. Conclusion

This paper presents an isolated bidirectional three-phase ac–dc converter system for integrating battery energy storage with the ac grid. The system originates as a modular dc–dc converter using DBSRC modules. The ac–dc and dc–ac capabilities are achieved by adding a three-phase unfolder to two DBSRC modules with parallel inputs and series outputs. The ac currents are indirectly controlled by regulating DBSRC output currents to track time-varying reference segments and reconstructing them using a three-phase unfolder. The required line filter to attenuate high-order current harmonics is smaller than that in a two-level VSI, due to DBSRC output currents modulated at twice and higher achievable switching frequency. The low-order harmonics are suppressed through controller optimizations to improve the tracking accuracy.

System operation is validated using a 1-kW hardware prototype. Steady-state results show acceptable efficiency and ac current quality. Transient tests verify fast system response. Origins of current distortions are summarized, and methods for improvement are provided.

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