Efficient Measurement of Thermal Coupling Effects on Multichip Light-Emitting Diodes

Hong-Li Lu, Yi-Jun Lu, Li-Hong Zhu, Yue Lin, Zi-Quan Guo, Tong Liu, Yu-Lin Gao, Guo-Long Chen, and Zhong Chen

***Abstract*—With the emerging market for multichip module based high-power LED systems, the demand for advanced thermal management techniques has been steadily growing. This paper presents a model developed by the authors for thermal coupling matrix that can calculate temperature distribution at a given heat power of each chip. The model significantly simplifies the task of measuring thermal coupling effect on multichip light-emitting diodes with symmetrical structure, while simultaneously preserving temperature accuracy. The modeling technique was validated experimentally on three-, four-, and six-chip rectangular modules, and a ten-chip circular module, by infrared thermography and transient thermal measuring system, respectively. The modeling technique was found to be more efficient especially for large systems. The model offers a rapid way to predict thermal coupling behaviors of multichip LED systems.**

***Index Terms*—Light-emitting diodes (LEDs), multichip modules (MCMs), temperature distribution, thermal coupling effect, thermal coupling matrix (TCM).**

I. Introduction

SOLID-STATE lighting is fast emerging as a substitute of traditional light sources, especially in the applications of high optical power output, where multichip modules (MCMs) are usually employed, such as the chip-on-board light-emitting diodes (LEDs), rather than single-chip LEDs [1]. Assembling multiple chips into one package as an MCM can overcome the power limit of single-chip LED and achieve ultrahigh light intensity [2]–[4]. But, the MCM has one issue: The conductive layer has to transfer thermal power, larger than that in a single-chip LED, dozens of times, as a result of which, and also because of ineffective heat dissipation, the temperatures of some junctions in the MCMs could be much higher than those in a single-chip LED. High junction temperature not only degrades the optical and electrical performances of LEDs, but also shortens the life expectancy [5]–[7]. With increase in power and chip packaging densities in solid-state lighting, the technology of thermal management of MCMs has become a popular research topic [8]–[10]. Consequently, testing methods have been widely studied, for instance, Poppe developed the multidomain compact modeling of LED chips and modules for transient thermal testing [11]–[15]. To achieve stability, striking the tradeoff between intense light output and extreme junction temperature is crucial. To achieve this, advanced thermal management techniques are required.

Normally an MCM comprises multiple heat sources at different locations, rendering experimental measurement of the junction temperature of each chip difficult. Such measurement is extremely time consuming, especially, in color-mixing LED system, whose LED devices have variable power or size. Besides, the temperature of a chip is contributed not only by self-heating, but also by mutual heat transfer among chips, namely the thermal coupling effect [16]–[18], which significantly affects the temperature of the chip and the thermal analysis of the system [19]–[22]. LED-based lighting product is by itself a complex system. The high junction temperature not only degrades the LED devices, but also immensely affects the electronic driver, mechanical housing (including assembly parts, such as thermal dissipation, electronic isolation, and final installation), and optical lens [23], [24]. For configuring switch mode driver, the effects of high temperature degradation of electrolytic capacitors on the driver have been investigated [25], as they play an important role in the dimming and color control technologies [23], [26]–[28]. In the linear mode high-power LED driver, the hot carrier injection has been found to be the main mechanism of degradation [29]. Therefore, for fine thermal management, understanding the fundamentals of thermal coupling effects and temperature distribution among chips is crucial. Within the limitations of the experiment, models that provide detailed description of the thermal coupling of multiple LED devices in variable structures would greatly contribute to optimization of the system design.

With the growing demand for higher power density, high-power LEDs are faced with thermal-related challenges that affect optical characteristics as well as reliability [30]. Thermal performance of MCMs is different from that of single-chip modules, possibly due to nonuniformity in temperature [31], [32].

Manuscript received November 24, 2016; accepted January 6, 2017. Date of publication January 16, 2017; date of current version August 2, 2017. This work was supported in part by the International Cooperation Project of Ministry of Science and Technology of China under Grant 2015DFG62190, in part by the National Natural Science Foundation of China under Grants 11104230, 61504212, 11604285, and 51605404, in part by the Major Science and Technology Project between University-Industry Cooperation in Fujian Province under Grant 2013H6024, and in part by the Natural Science Foundation of Fujian Province under Grant 2016R0091. Recommended for publication by Associate Editor S. Y. Hui. *(Corresponding authors: L.-H.Zhu, Y.-L. Gao.)*

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This paper has supplementary downloadable material available at http://ieeexplore.ieee.org.

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Digital Object Identifier 10.1109/TPEL.2017.2653193

Thermal resistance network has been established in the major direction of heat flow to analyze the theoretical thermal resistance of MCMs [33]. In particular, thermal spreading resistance of multichip packaging, resulting from discrete heat sources, is a key thermal resistance in the process of heat transfer [34], [35] and has been widely studied recently. Muzychka proposed a simple method for predicting mean and central heat source temperature [36]. Liu and coworkers proposed the multichip spreading resistance model to study the whole temperature field of LED packaging substrate [37]. To optimize LED systems, Hui and Qin proposed a photo-electro-thermal (PET) theory that combines the photometric, electrical, and thermal behaviors of an LED system and predicts the optimal operating point in terms of the maximum luminous flux [38]. Later, time domain was incorporated into the PET theory to study the decay of luminous output [39]. A three-dimensional (3-D) PET LED node model was developed to describe the nonuniform thermal distribution of the LEDs on the heatsink in a 3-D space system [40]. More recently, they came up with a modeling technique that merges the chromatic characteristics of an LED system with the PET theory. The improved PET theory can predict temperature distribution, luminous flux, and correlated color temperature of the LED systems [41]. For carrying out more accurate studies on complex interactions of heat, light, and power in LED systems, 3-D finite-element methods are usually used to simulate temperature distribution [33]–[36], [42]–[45]. Considering the need for systematic optimization of luminous output, the foregoing research works focused mainly on thermal modeling and measuring junction temperature. But, measurement of thermal interaction among chips, which is important for measuring the whole-field temperature, is often ignored, especially when the cost of apparatus or research time is considered.

In this study, a model is proposed to accurately predict the junction-temperature distribution of multichip LEDs. To model the lateral heat transfer, the equivalent electric circuit (EEC) of heat flow path was used in incorporating several essential factors of thermal coupling effect into the thermal coupling matrix (TCM) for LEDs array. The proposed model can precisely determine the temperature distribution of chips. After computer simulations, it was found that the number of independent chips in TCMs decreases significantly if the temperature is distributed in a symmetrical structure. Therefore, from measuring junction temperatures of independent chips in array systems, the temperature distribution of the whole system can be predicted, using TCMs. This model can rapidly predict thermal coupling behavior of multichip LED systems. In comparison with the traditional one-by-one measurement method, the proposed method improves the measurement efficiency significantly by reducing the number of measurement channels, as well as the time cost. Discrepancies between theoretical predictions and experimental results are also discussed.

II. Theoretical Method

A. Thermal Coupling Matrix

In the case of single-chip device, as shown in Fig. 1(a), the chip is mounted on a thermally conductive layer, e.g., the copper layer, or other interconnection layer in an LED package. When the LED is lit up, a thermal dissipating path goes downwards from the chip, through the conductive layers, to the heatsink. The encapsulation on the top can be considered adiabatic, because of its much low thermal conductivity, and as such little heat dissipates upwards. According to the 1-D heat-flow theory [46], this 1-D thermal system closely resembles the EEC, as shown in Fig. 1(b). The thermal resistance (*R*), mimicking the heat dissipating path, is defined as $R = \Delta T/P$, where *P* represents the heat dissipation power of the chip and ΔT is the temperature rise between the chip and the heatsink.

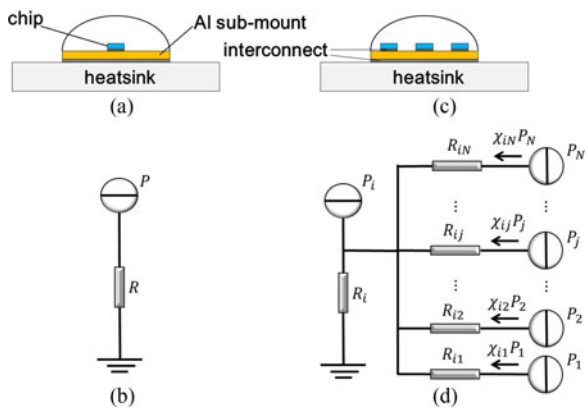

Fig. 1. (a) Schematic of single-chip LED package and (b) the corresponding EEC; (c) schematic of multichip LED package and (d) the corresponding EEC, where R_{ij} represents the lateral heat transfer path between *i*th and *j*th chips.

As illustrated in Fig. 1(c), when multiple chips are mounted on the same copper layer and lit up, vertical heat dissipation from each chip, as well as lateral thermal transfer among chips, occurs. With increasing number of chips, the volume of mutual thermal coupling increases rapidly, leading to a more complicated temperature distribution than that in the case of single chip. As shown in the multichip EEC of Fig. 1(d), *N* identical chips are mounted on the same copper layer. P_1 and P_2 to P_N denote heat dissipation power of chips. P_i raises the temperature of the *i*th chip by $\Delta T_i = P_i R_i$, and the *j*th chip among the rest of the $N-1$ ones transfers a proportion of χ_{ij} of its total power P_j to the *i*th chip through lateral heat path between them against a thermal resistance of R_{ij}. As a consequence, the extra temperature rise ΔT_{ij} of the *i*th chip, contributed by *j*th chip, is $\chi_{ij} P_j R_{ij}$. Hence, the total temperature rise of the *i*th chip can be expressed as

$$\Delta T_i = P_i R_i + \sum_{j=1, j\neq i}^{N} \Delta T_{ij} \ \ (i, j = 1, 2, 3, \ldots, N) \qquad (1)$$

where $\Delta T_{ij} = \chi_{ij} P_j R_{ij}$ $(i, j = 1, 2, 3, \ldots, N)$. Setting $\mu_{ij} = R_{ij}\chi_{ij}$ and $\chi_{ii} = 1$, a simpler expression of the total temperature rise for the *i*th chip is obtained as

$$\Delta T_i = \sum_{j=1}^{N} \mu_{ij} P_j \ \ (i, j = 1, 2, 3, \ldots, N) \qquad (2)$$

where μ_{ij} shares the same dimension with the thermal resistance. For an *N*-chip system, the TCM is established

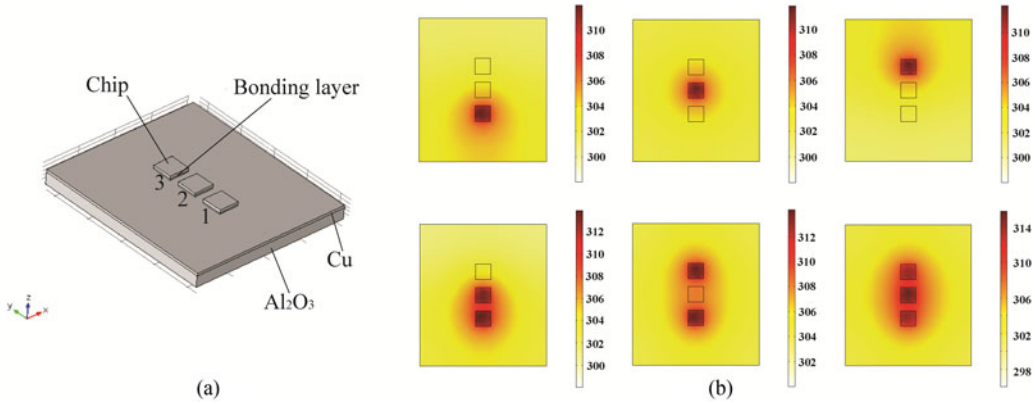

Fig. 2. (a) 3-D configuration of the LED module for simulation and (b) its results of temperature distribution of chips, lit up, in all the six cases.

as

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \vdots \\ \Delta T_N \end{pmatrix} = \begin{pmatrix} R_1 & \mu_{12} & \mu_{13} & \cdots & \mu_{1N} \\ \mu_{21} & R_2 & \mu_{23} & \cdots & \mu_{2N} \\ \mu_{31} & \mu_{32} & R_3 & \cdots & \mu_{3N} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ \mu_{N1} & \mu_{N2} & \mu_{N3} & \cdots & R_N \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ \vdots \\ P_N \end{pmatrix} \quad \text{or}$$

$$\Delta \vec{T} = \hat{U}_{\mathrm{TCM}} \vec{P}. \tag{3}$$

Equation (3) describes the relationship between the thermal power and temperature of each chip in an MCM. With this TCM, the junction-temperature distribution can be obtained from the heating powers of chips. As suggested in the literature, the lateral thermal resistance between any pair of *i*th and *j*th chips dominates the thermal coupling. From the EEC shown in Fig. 1(d), it is found that the larger the lateral resistance, the lesser would be the lateral thermal dissipation. In addition, the junction-temperature rise, induced by lateral heating, is associated with some other factors, such as the resistance between the chip and heatsink. In the current TCM, all these related factors are combined into one, which leads to one tensor: μ_{ij}.

B. Validation of TCM

The TCM presented in (3) is validated here by simulating the temperature distribution of LED MCMs with array and circular structures by using the commercial software COMSOL Multiphysics (COMSOL Inc., Sweden) [47]. To verify the thermal coupling between any two chips in MCMs and to deduce the universal rules of the TCM, several simulations on multichip models, with various chip numbers and arrangements, were conducted. A 1 × 3-chip model is presented here in Fig. 2(a) as an illustration. From this figure, it can be seen that three chips are laid down in a row and labeled as chip1#, 2#, and 3#. The results of thermal simulations for all the six cases of 1 × 3 chip model are illustrated in Fig. 2(b). The key parameters of the materials used for simulation are listed in Table I.

To characterize the TCM, the procedure followed in deriving mutual thermal coupling between any two chips is presented in the flowchart (see Fig. 3) (with ΔT_2 as an example).

According to (2), the temperature rise of chip 2# can be written as $\Delta T_2 = \mu_{21} P_1 + \mu_{22} P_2 + \mu_{23} P_3$. Theoretically, chips 2# and 3# (let $P_2 = P_3 = 0$ W) can be switched OFF and the temperature rise ΔT_2 measured with P_1 running at series powers and then the coefficient μ_{21} derived by linearly fitting $\Delta T_2 \sim P_1$ [See the slope shown in Fig. 4(a)]. To verify that μ_{21} is independent of P_2 and P_3, three more cases, i.e., $P_2 = 0$ W, $P_3 = 1$ W;

TABLE I
KEY PARAMETERS OF THE MATERIALS USED FOR SIMULATION

Material	Density ($\mathrm{kg \cdot m^{-3}}$)	Thermal Conductivity (W/(m·K))	Heat Capacity ($\mathrm{J \cdot K^{-1}}$)
Chip	3500	80	703
Bonding layer	N/A	3.25	N/A
Cu	8700	400	386
Al_2O_3	3400	20	700

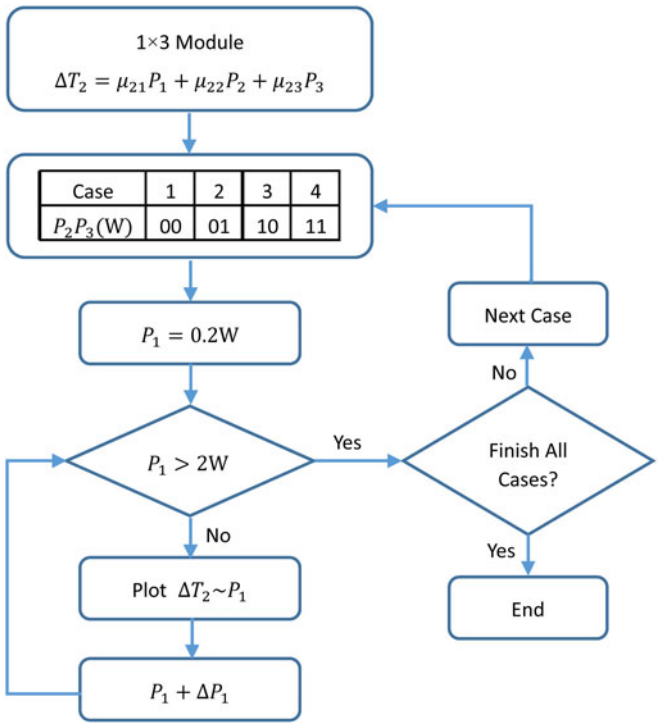

Fig. 3. Flowchart to retrieve the mutual thermal coupling between any two chips for the 1 × 3-chip model.

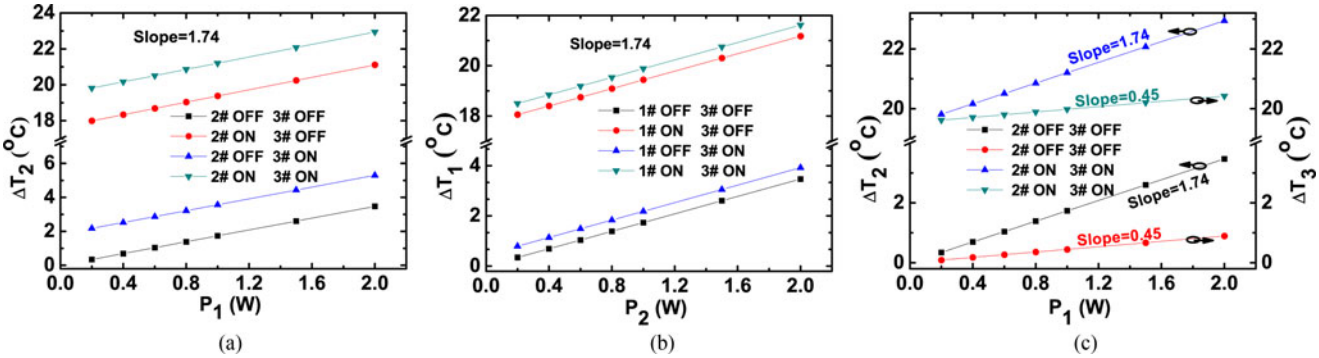

Fig. 4. (a) Temperature rise of chip 2# versus power of chip 1#. (b) Temperature rise of chip 1# versus power of chip2#, each under a different status. (c) Temperature rise of chip 2# and 3# versus power of chip 1#, each under a different status. Here, "ON" and "OFF" denote applied thermal power of 1.0 and 0 W, respectively.

$P_2 = 1$ W, $P_3 = 0$ W, and $P_2 = P_3 = 1$ W were added. For each case, the experiment $\Delta T_2 \sim P_1$ was repeated. The results of all the four cases were plotted [see Fig. 4(a)], where OFF and ON mean 0 and 1 W, respectively.

Similarly, μ_{12} can be derived by $\Delta T_1 \sim P_2$ [see Fig. 4(b)], μ_{31} by $\Delta T_3 \sim P_1$[see Fig. 4(c)], as well as other elements in the TCM. Finally, the three-order TCM for 1×3-chip model can be expressed as

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \end{pmatrix} = \begin{pmatrix} 17.70 & 1.74 & 0.45 \\ 1.74 & 17.64 & 1.83 \\ 0.45 & 1.83 & 18.68 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \end{pmatrix}. \quad (4)$$

From (4), it is found that $\mu_{12} = \mu_{21}$, $\mu_{13} = \mu_{31}$, and $\mu_{23} = \mu_{32}$.

As illustrated in Fig. 4(c), slope_$\Delta T_2 \sim P_1 >$ slope_$\Delta T_3 \sim P_1$, i.e., $\mu_{21} > \mu_{31}$, because the distance from chip 1# to chip 3# is more than that from chip 1# to chip 2# [see Fig. 2(a)]. In effect, the lateral thermal resistance between any two chips is directly proportional to the distance between them, and thus $R_{31} > R_{21}$. On the other hand, the thermal power transferred from chip 1# to chip 2# is larger than that from chip 1# to chip 3#, and this leads to the result $\chi_{31} < \chi_{21}$. Combining Fig. 4(a), (b), and (c), it is evident that μ_{21} was determined solely by the geometric positions of the two chips involved and is independent of the chips' power. In summary, the mutual thermal coupling between any two chips depends on the characteristics of TCM: 1) the thermal coupling is a linear effect, and 2) the TCM is a symmetric matrix, with the LEDs arranged in an array structure. In addition, the equivalent graphs (see Fig. 4) for the structure of 2×2 (Figs. S1 and S2 in supplementary material) demonstrates that TCM is available even in the situation of $m = n$ for an $m \times n$ LED array structure.

C. Simplifications of TCM for an $m \times n$ LED Array Structure

It is evident that the number of elements in TCM increases quadratically with the number of chips. If the number of chips is N, the number of μ_{ij} is N^2. Since the TCM is a symmetric matrix, the number of "nontrivial elements" can be reduced to $(N^2 + N)/2$. The workload can be further reduced by considering the possible symmetry of chip pattern. More clearly, the thermal field generated by one chip would also be symmetric with respect to that generated by its symmetric counterpart. Therefore, there is no need to visit all the chips to determine the thermal coupling of the whole matrix. Here, the minimum requirement to obtain TCM is "nontrivial chips." In other words, whole TCM can be obtained by applying thermal power only to the nontrivial chips. How to determine the nontrivial chips is discussed below.

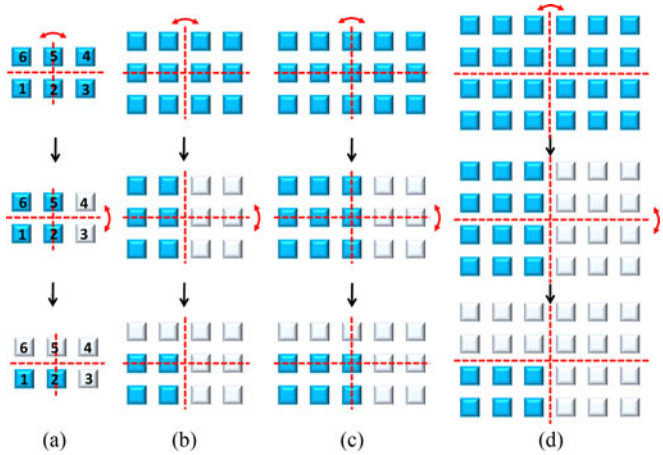

Fig. 5. Identification of the nontrivial chips when the number of rows and columns are (a) even–odd, (b) odd–even, (c) odd–odd, and (d) even–even. Those marked gray are trivial chips, and in the last stages, the blue ones are nontrivial. The red-dashed line and red double arrows mark the symmetry.

The degree of symmetry of the matrix depends on the number of rows *m* and columns *n* in the MCM. It is obvious that when $m = n$, the degree of symmetry is higher than when $m \neq n$. These two cases are discussed below:

1) Case: $m \neq n$*:* The LED chips are distributed, as shown in Fig. 5, in an array and the number of rows and columns are (a) even–odd, (b) odd–even, (c) odd–odd, and (d) even–even. Each case has two axes of symmetry: vertical and horizontal. If *n* is odd, the vertical axis will cross the chips located at the middle column, and if even, it will cross between the two middle columns. The same rule is applied to the horizontal axis and the row numbers *m*. Therefore, when *m* (or *n*) is even, the degenerate number becomes *m*/2 (or *n*/2), and when odd it becomes $(m + 1)/2$ [or $(n + 1)/2$], this shorting description is feasible because those chips in the middle row (or column) belong to both sides.

Bearing these in mind, the number of nontrivial chips n_i is calculated according to the following equation when $m \neq n$

$$n_i = \begin{cases} \frac{mn}{4} & \text{both } m \text{ and } n \text{ are even} \\ \frac{(m+1)n}{4} & m \text{ is odd and } n \text{ is even} \\ \frac{(m+1)(n+1)}{4} & \text{both } m \text{ and } n \text{ are odd.} \end{cases} \quad (5)$$

Here, taking 2×3 chips as an example, the values of the TCM will be obtained by simulating the temperature distribution of MCMs. According to the simplified method introduced above, only two nontrivial chips need to be tested to obtain the TCM, as shown in Fig. 5(a). Equation (6) is the result of testing all the six chips by the conventional method, while (7) is the result of testing only two nontrivial chips by the simplified method. A comparison of the values of the TCMs in (6) with those in (7) reveals that the two results are in good agreement. Here, the 2×3-chip model is taken as an example to explain how the matrix can be obtained. To obtain μ_{ij}, according to $\mu_{ij} = \Delta T_{ij}/P_j$, two nontrivial chips should be lit up individually. For example, in Fig. 5(a), when chip1# is lit up, the temperature of all the other chips rises to different degrees. Thus, the temperature rise of each chip, ΔT_{11} to ΔT_{61} and the resulting μ_{11} to μ_{61} are obtained. Likewise, when chip 2# is lit up, μ_{12} to μ_{62} are obtained. Then, the rest of the elements are calculated in the light of the symmetry of the TCM. The six-order TCM for 2×3-chip model is obtained using (7)

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \\ \Delta T_5 \\ \Delta T_6 \end{pmatrix} = \begin{pmatrix} 17.75 & 1.74 & 0.38 & 0.24 & 0.82 & 1.66 \\ 1.74 & 17.25 & 1.66 & 0.82 & 1.71 & 0.83 \\ 0.38 & 1.66 & 17.15 & 1.66 & 0.82 & 0.24 \\ 0.24 & 0.82 & 1.67 & 17.77 & 1.64 & 0.37 \\ 0.82 & 1.71 & 0.82 & 1.64 & 17.47 & 1.74 \\ 1.66 & 0.83 & 0.24 & 0.38 & 1.74 & 17.23 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \end{pmatrix} \quad (6)$$

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \\ \Delta T_5 \\ \Delta T_6 \end{pmatrix} = \begin{pmatrix} 17.75 & 1.74 & 0.38 & 0.24 & 0.82 & 1.66 \\ 1.74 & 17.25 & 1.66 & 0.82 & 1.71 & 0.83 \\ 0.38 & 1.66 & 17.75 & 1.66 & 0.82 & 0.24 \\ 0.24 & 0.82 & 1.66 & 17.75 & 1.66 & 0.38 \\ 0.82 & 1.71 & 0.82 & 1.66 & 17.25 & 1.74 \\ 1.66 & 0.83 & 0.24 & 0.38 & 1.74 & 17.75 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \end{pmatrix}. \quad (7)$$

2) Case: $m = n$: As illustrated in Fig. 6, LED chips are distributed in an array and the row/column number is (a) odd and (b) even. For convenience, $s = m = n$ is satisfied. In this case, in addition to the vertical and horizontal axes in case $m \neq n$, there are two more diagonal axes of symmetry, which further divide the matrix into eight parts, as shown in Fig. 6. Similar to the case $m \neq n$, the parity of s would affect the result. When it is odd, the chips in the middle column and row, belonging to each quarter are divided by the vertical and horizontal axes. Hence, the dimension of the matrix in the quarter, denoted as

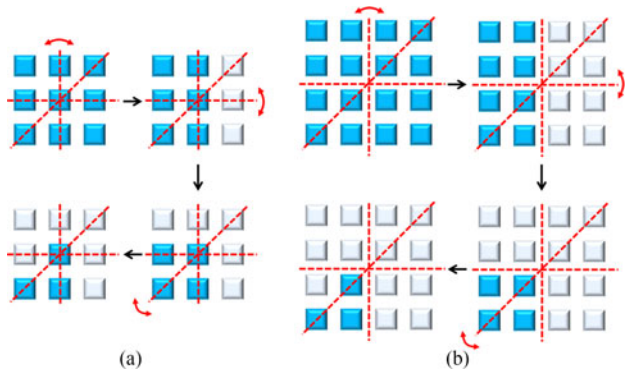

Fig. 6. Identification of nontrivial chips in a square matrix, where the row/column number is (a) odd and (b) even. Explanations for the marks are the same as those in Fig. 5.

s_q, is expressed as follows:

$$s_q = \begin{cases} \frac{s}{2} & s \text{ is even} \\ \frac{s+1}{2} & s \text{ is odd.} \end{cases} \quad (8)$$

Regardless of the parity of s or s_q, diagonal axes definitely go across the chips along the diagonal, indicating that the s_q chips lying along the diagonal axes are nontrivial. On the other hand, the chips in the triangular area will degenerate due to symmetry, and their number is $\sum_1^{s_q-1} i = s_q(s_q-1)/2$. Hence the nontrivial chips number will be $s_q^2 - \mathrm{s_q}(s_q-1)/2 = \mathrm{s_q}(s_q+1)/2$, i.e.

$$n_i = \begin{cases} \frac{s^2+2s}{2} & s \text{ is even} \\ \frac{s^2+4s+3}{2} & s \text{ is odd.} \end{cases} \quad (9)$$

Here, 2×2 chip case is taken as an example. The matrix in (10), derived from the conventional method by testing all the four chips, is compared with that in (11), derived from the simplified method by testing only one chip. It is evident that the following two matrices agree well with each other:

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{pmatrix} = \begin{pmatrix} 18.42 & 1.71 & 0.90 & 1.76 \\ 1.71 & 17.93 & 1.91 & 0.85 \\ 0.90 & 1.91 & 18.39 & 1.71 \\ 1.76 & 0.85 & 1.72 & 18.40 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{pmatrix} \quad (10)$$

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{pmatrix} = \begin{pmatrix} 18.42 & 1.71 & 0.90 & 1.76 \\ 1.71 & 18.42 & 1.91 & 0.85 \\ 0.90 & 1.91 & 18.42 & 1.71 \\ 1.76 & 0.85 & 1.71 & 18.42 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{pmatrix}. \quad (11)$$

The number of nontrivial chips is significantly reduced for the MCM with high symmetry, and so are the elements that need to be calculated in TCM. Taking the square-matrix arrangement as an example, the reduction rate of n_i/s^2 can be $1/8 + 1/4s$ when s is even and $1/8 + 1/2s + 3/8s^2$ when s is odd, and both the rates converge to 0.125 for a sufficiently large s.

To study the efficiency of the method, the reduction rate n_i/s^2 with an $m \times n$ array structure, in which m and n range from 1 to 20, were calculated (see Fig. 7). It is evident that most of

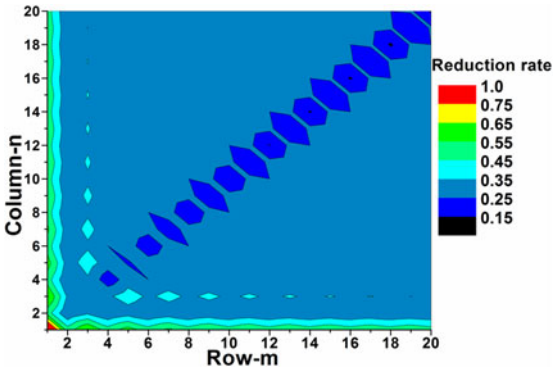

Fig. 7. Reduction rate of n_i/s^2 for $m \times n$ array with m and n ranging from 1 to 20.

the area is filled with the reduction rate that falls between 0.25 and 0.35. In particular, when m equals n, the reduction rate is low, ranging between 0.15 and 0.25. Moreover, when m and n are both even and are higher than 12, rates lower than 0.15 were achieved. Consequently, based on the TCM, the number of chips engaged in the calculation, as well as the workload, can be significantly reduced.

D. Simplifications of TCM for an m–n Circular LED Structure

Considering the practical application, the LED chips can also be arranged in a circular fashion and still a high degree of symmetry can be maintained. In the circular module, the LED chips are arranged as an ensemble of concentric rings on the printed circuit board (PCB). For this investigation, the typical circular module (see Fig. 8), referred to as the 4–6 circular module, was studied. It had four chips inside the ring, which

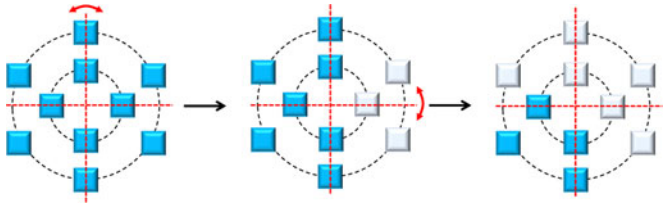

Fig. 8. Identification of nontrivial chips of 4–6 circular module. Those marked gray are trivial chips, and in the last stages, the blue ones are nontrivial. The red-dashed line and red double arrows mark the symmetry.

was composed of another six chips. The horizontal and vertical axes of the module are shown in the figure to facilitate the determination of the nontrivial chips and to simplify the TCM. For the case of 4–6 circular module, the number of nontrivial chips is four. One more example, namely 3–6 circular module, can be found in the "Supplementary Material."

With respect to the 4–6 circular module, the values of the TCM and simplified TCM were derived from simulation and expressed by (12) and (13), respectively. Equation (12) is the result of testing all the ten chips by the conventional method, while (13) is the result of testing the four nontrivial chips by the simplified method. The two results are mutually in good agreement. From the values of the TCM in (12) and (13), it is evident that the proposed TCM modeling technique is applicable to LED modules when the LED chips are arranged as an ensemble of concentric rings on the PCB. When the LED chips are so arranged, they show higher symmetry, such as 3–6 circular module, in which the number of the nontrivial chips, as also its workload, is reduced significantly, see (12) and (13) shown at the bottom of this page.

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \\ \Delta T_5 \\ \Delta T_6 \\ \Delta T_7 \\ \Delta T_8 \\ \Delta T_9 \\ \Delta T_{10} \end{pmatrix} = \begin{pmatrix} 19.58 & 1.73 & 0.79 & 1.69 & 1.86 & 0.83 & 0.29 & 0.17 & 0.28 & 0.78 \\ 1.73 & 19.56 & 1.64 & 0.79 & 0.47 & 1.56 & 1.49 & 0.42 & 0.20 & 0.20 \\ 0.79 & 1.64 & 19.96 & 1.73 & 0.18 & 0.29 & 0.80 & 1.76 & 0.83 & 0.28 \\ 1.69 & 0.79 & 1.73 & 19.74 & 0.44 & 0.21 & 0.20 & 0.44 & 1.43 & 1.42 \\ 1.86 & 0.47 & 0.18 & 0.44 & 16.29 & 0.71 & 0.10 & 0.04 & 0.09 & 0.62 \\ 0.83 & 1.56 & 0.29 & 0.21 & 0.71 & 16.86 & 0.68 & 0.09 & 0.05 & 0.10 \\ 0.29 & 1.49 & 0.83 & 0.20 & 0.10 & 0.68 & 17.91 & 0.62 & 0.09 & 0.05 \\ 0.17 & 0.42 & 1.86 & 0.47 & 0.04 & 0.09 & 0.71 & 17.46 & 0.71 & 0.09 \\ 0.28 & 0.20 & 0.83 & 1.43 & 0.09 & 0.05 & 0.09 & 0.64 & 17.00 & 0.65 \\ 0.78 & 0.20 & 0.28 & 1.42 & 0.62 & 0.10 & 0.05 & 0.09 & 0.65 & 16.91 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \\ P_7 \\ P_8 \\ P_9 \\ P_{10} \end{pmatrix} \tag{12}$$

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \\ \Delta T_5 \\ \Delta T_6 \\ \Delta T_7 \\ \Delta T_8 \\ \Delta T_9 \\ \Delta T_{10} \end{pmatrix} = \begin{pmatrix} 19.58 & 1.73 & 0.79 & 1.69 & 1.86 & 0.83 & 0.29 & 0.17 & 0.28 & 0.78 \\ 1.73 & 19.56 & 1.64 & 0.79 & 0.47 & 1.56 & 1.49 & 0.42 & 0.20 & 0.20 \\ 0.79 & 1.64 & 19.58 & 1.73 & 0.17 & 0.29 & 0.83 & 1.86 & 0.83 & 0.28 \\ 1.69 & 0.79 & 1.73 & 19.56 & 0.42 & 0.20 & 0.20 & 0.47 & 1.49 & 1.56 \\ 1.86 & 0.47 & 0.17 & 0.42 & 16.29 & 0.71 & 0.10 & 0.04 & 0.09 & 0.62 \\ 0.83 & 1.56 & 0.29 & 0.20 & 0.71 & 16.86 & 0.68 & 0.09 & 0.05 & 0.10 \\ 0.29 & 1.49 & 0.83 & 0.20 & 0.10 & 0.68 & 16.86 & 0.71 & 0.09 & 0.05 \\ 0.17 & 0.42 & 1.86 & 0.47 & 0.04 & 0.09 & 0.71 & 16.29 & 0.71 & 0.09 \\ 0.28 & 0.20 & 0.83 & 1.49 & 0.09 & 0.05 & 0.09 & 0.71 & 16.29 & 0.68 \\ 0.78 & 0.20 & 0.28 & 1.56 & 0.62 & 0.10 & 0.05 & 0.09 & 0.68 & 16.29 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \\ P_7 \\ P_8 \\ P_9 \\ P_{10} \end{pmatrix} \tag{13}$$

TABLE II
TEMPERATURE RISES OF 1 × 3–CHIP MODULE UNDER 350 MA

Conditions	Experimental data from T3ster(°C)			Temperature rise obtained by TCM(°C)			Deviation (%)		
	ΔT_1	ΔT_2	ΔT_3	ΔT_1	ΔT_2	ΔT_3			
$I_1 = 350$ mA	**12.92**	**1.35**	**0.61**	12.92	1.35	0.61	0	0	0
$I_2 = 350$ mA	**1.43**	**12.93**	**1.43**	1.36	13.03	1.44	4.99	0.77	0.77
$I_1 = I_2 = 350$ mA	14.66	14.42	2.16	14.28	14.38	2.06	2.60	0.25	4.55
$I_1 = I_3 = 350$ mA	13.94	2.66	13.98	13.53	2.78	13.50	2.96	4.45	3.24
$I_1 = I_2 = I_3 = 350$ mA	15.04	16.57	14.80	14.89	15.82	14.97	1.00	4.54	1.19

TABLE III
TEMPERATURE RISES OF 2 × 2-CHIP MODULE UNDER 350 MA

Conditions	Experimental datafrom T3ster (°C)				Temperature rise obtained by TCM (°C)				Deviation (%)			
	ΔT_1	ΔT_2	ΔT_3	ΔT_4	ΔT_1	ΔT_2	ΔT_3	ΔT_4				
$I_1 = 350$ mA	**12.55**	**1.39**	**1.02**	**1.60**	12.55	1.39	1.02	1.60	0	0	0	0
$I_1 = I_2 = 350$ mA	14.32	14.08	2.86	2.46	13.94	13.94	2.62	2.62	2.67	0.97	8.39	6.67
$I_1 = I_3 = 350$ mA	14.05	2.86	13.60	2.86	13.57	2.99	13.57	2.99	3.40	4.29	0.50	4.29
$I_1 = I_2 = I_3 = 350$ mA	15.01	14.73	14.69	4.05	14.97	15.54	15.17	4.01	0.27	5.46	3.28	1.01
$I_1 = I_2 = I_3 = I_4 = 350$ mA	16.23	15.88	16.50	16.64	16.56	16.56	16.56	16.56	2.02	4.30	0.39	0.49

TABLE IV
TEMPERATURE RISES OF 2 × 3–CHIP MODULE UNDER 350 MA

Conditions	Experimental data from T3ster (°C)						Temperature rise obtained by TCM (°C)						Deviation (%)					
	ΔT_1	ΔT_2	ΔT_3	ΔT_4	ΔT_5	ΔT_6	ΔT_1	ΔT_2	ΔT_3	ΔT_4	ΔT_5	ΔT_6						
$I_1 = 350$ mA	**13.19**	**1.47**	**0.65**	**0.37**	**1.11**	**1.58**	13.19	1.47	0.65	0.39	1.11	1.58	0	0	0	0	0	0
$I_2 = 350$ mA	**1.45**	**12.69**	**1.39**	**0.98**	**1.43**	**0.94**	1.47	12.69	1.39	0.98	1.43	0.94	1.57	0	0	0	0	0
$I_1 = I_2 = 350$ mA	14.13	13.80	1.92	1.31	2.78	2.70	14.66	14.16	2.05	1.35	2.54	2.52	3.73	2.62	6.64	3.13	8.63	6.82
$I_1 = I_2 = I_3 = 350$ mA	15.14	15.23	14.84	3.07	3.85	3.09	15.32	15.55	15.23	2.93	3.64	2.89	1.18	2.11	2.63	4.67	5.43	6.47
$I_1 = I_2 = I_3 = I_4 = 350$ mA	16.14	17.00	16.21	15.82	5.24	3.82	15.68	16.53	16.81	16.11	5.12	3.54	2.82	2.77	3.71	1.82	2.34	7.32
$I_1 = I_2 = I_3 = I_4 = I_5 = 350$ mA	17.03	18.23	17.24	16.92	17.44	5.29	16.79	17.97	17.91	17.59	17.80	5.01	1.39	1.46	3.88	3.96	2.11	5.29
$I_1 = I_2 = I_3 = I_4 = I_5 = I_6 = 350$ mA	18.60	19.15	18.32	18.03	19.22	18.48	18.36	18.91	18.28	18.24	19.28	18.20	1.25	1.28	0.19	1.19	0.32	1.51

E. Simplification of TCM for an m × n LED Array Structure With Different Thermal Powers

Apart from the single color case presented above, the general case was also considered, whose MCMs contain differently colored LEDs, e.g., red, green, and blue dice, which can be combined to generate either colored or white light. One of the key challenges in such applications is to maintain a defined color point over life and over all flux levels, which depend on the junction temperature of the LEDs. Normally, LED dice with different colors have different thermal powers, which result in unequal heat transmission between the dice. For example, the average heating of the green die by the red die might be different from the heating of the red die by the green die because of differences in their thermal powers.

Given the properties of the TCM, it was presumed that the LED dice with different colors in the MCM have different heat powers during operation. To demonstrate the symmetry of the TCM, 2×2 chips were taken as an example. In this module, the four chips had different thermal powers and the values of TCM were obtained by simulation. Equation (14) is the result of testing all the four chips under different heat powers ($P_1 = 0.29$ W, $P_2 = 0.86$ W, $P_3 = 1.46$ W, $P_4 = 2.22$ W) by the conventional method, while (15) is the result of testing the nontrivial chips by the simplified method. The two results are mutually in good agreement. In the general case of multiple LED chips with different colors, the dice with different colors can also differ in size. However, simplification of TCM for a 2×2-chip LED array structure, with different chip sizes, which is discussed briefly under "Supplementary Information," is not the main topic of this study

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{pmatrix} = \begin{pmatrix} 18.42 & 1.71 & 0.90 & 1.76 \\ 1.71 & 17.93 & 1.91 & 0.85 \\ 0.90 & 1.91 & 18.39 & 1.72 \\ 1.76 & 0.85 & 1.72 & 18.40 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{pmatrix} \quad (14)$$

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{pmatrix} = \begin{pmatrix} 18.42 & 1.71 & 0.90 & 1.76 \\ 1.71 & 18.42 & 1.91 & 0.85 \\ 0.90 & 1.91 & 18.42 & 1.71 \\ 1.76 & 0.85 & 1.71 & 18.42 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{pmatrix}. \quad (15)$$

TABLE V
TEMPERATURE RISES OF 4–6–CHIP MODULE UNDER 350 MA

Conditions	Experimental data from T3ster (°C)										Temperature rise obtained by TCM (°C)									
	ΔT_1	ΔT_2	ΔT_3	ΔT_4	ΔT_5	ΔT_6	ΔT_7	ΔT_8	ΔT_9	ΔT_{10}	ΔT_1	ΔT_2	ΔT_3	ΔT_4	ΔT_5	ΔT_6	ΔT_7	ΔT_8	ΔT_9	ΔT_{10}
$I_1 = 350$ mA	**12.18**	**0.93**	**0.62**	**1.08**	**1.29**	**0.67**	**0.42**	**0.33**	**0.38**	**0.68**	12.18	0.93	0.62	1.08	1.29	0.67	0.42	0.33	0.38	0.68
$I_2 = 350$ mA	**0.97**	**11.81**	**1.07**	**0.62**	**0.38**	**1.03**	**1.33**	**0.53**	**0.26**	**0.26**	0.97	11.81	1.07	0.62	0.38	1.03	1.33	0.53	0.26	0.26
$I_5 = 350$ mA	**1.30**	**0.36**	**0.28**	**0.39**	**10.72**	**0.56**	**0.26**	**0.19**	**0.27**	**0.54**	1.30	0.36	0.28	0.39	10.72	0.56	0.26	0.19	0.27	0.54
$I_6 = 350$ mA	**0.71**	**1.02**	**0.35**	**0.28**	**0.52**	**12.03**	**0.68**	**0.21**	**0.17**	**0.21**	0.71	1.02	0.35	0.28	0.52	12.03	0.68	0.21	0.17	0.21
$I_1 = I_2 = 350$ mA	14.24	12.77	1.68	1.68	1.70	1.66	1.66	0.79	0.60	0.90	13.15	12.75	1.69	1.70	1.67	1.70	1.74	0.86	0.64	0.94
$I_1 = I_2 = I_5 = 350$ mA	15.93	14.84	1.95	2.12	13.10	2.25	1.87	0.95	0.81	1.41	14.45	13.10	1.97	2.09	12.39	2.26	2.00	1.05	0.91	1.48
$I_1 = I_2 = I_5 = I_6 = 350$ mA	16.43	15.47	2.31	2.42	13.94	14.52	2.53	1.17	0.95	1.63	15.16	14.12	2.32	2.37	12.91	14.29	2.69	1.27	1.08	1.70

III. EXPERIMENTAL RESULTS

Experiments were designed to verify the TCM with Thermal Transient tester (T3Ster), combined with TeraLED (T3Ster TeraLED system), which is based on the widely accepted forward voltage method. The commercial thermal transient measurement product was provided by MicRed Ltd. [48]. For measurement, one module each of 1×3-chip LED, 2×2-chip LED, 2×3-chip LED and 4–6 circular LED was used by way of examples. Chips, with a size of 1 mm^2 with rated current 350 mA, were arranged symmetrically in these modules. It is worth mentioning that, to get a module with different thermal powers, the four chips in 2×2-chip module were driven with 150, 350, 550, and 750 mA, whose thermal powers are 0.29, 0.86, 1.46, and 2.22 W, respectively. Optical measurements were performed in thermal steady state with the TeraLED and once they were completed, the LED under test was switched OFF and its cooling transient was measured by the T3Ster equipment. For this study, heatsink was taken as the temperature reference node for the proposed model. The heatsink was a temperature-stabilized fixture, included in the TeraLED system employed. The fixture included an integrated thermal sensor, which can sink heat up to 10 W. Its temperature can be programmed between 10 and 90 °C with TeraLED software. Once the thermal power of the LED module under experiment was under 10 W, the LED module was mounted on the heatsink, which can maintain the temperature at 25 °C during measurement. For temperature-sensitive parameter calibration, namely, the *K*-factor calibration, the LED under test was measured by TeraLED in a stabilized state, at a programmed current of 3 mA and at a programmed temperature range of 25–55 °C with an increment of 10 °C. After that, the optical power of the LED's dice was measured at heating up current of 350 mA for a sufficiently long time, and at 25 °C temperature of heatsink. Then, after switching OFF the LED, the transient thermal measurement was started to record the cooling curve after driving the LED's dice individually with heating up current for a sufficiently long time, maintaining heatsink temperature at 25 °C. Finally, the actual temperature rise curve was obtained by evaluating the cooling curve, given the measured thermal power and *K*-factor. The thermal power was obtained by subtracting the optical power from the electrical power applied on the chips. The temperature differences in (3) were obtained by finding out the difference of the temperature between the thermal steady states at the two ends of the temperature-rise curves. TheT3ster contains eight measuring channels. On the parallel channels, measurement and data acquisition take place simultaneously, which is convenient for thermal coupling measurement. The experimental results are presented in Tables II through V for 1×3-chip, 2×2-chip, 2×3-chip, and 4–6 circular modules, respectively. In addition, Tables VI presents the results for the 2×2-chip module under four different thermal powers. Here, ΔT_n $(n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)$ is the temperature rise of each chip, and $I_{\rm n}$ $(n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)$ denotes the forward current applied on the *n*th chip. According to the simplified method proposed in this study, only "nontrivial chips" are needed to obtain the whole TCM. First, the "nontrivial chips" were lit up. The temperature rise of the remaining chips, due to thermal coupling effect, was obtained. For computing the TCM, the experimental results of "nontrivial chips" are listed in bold in Tables II–VI. Second, substituting these results into (3), the TCMs in (16) through (20) were obtained, based on the simplified method for 1×3-chip, 2×2-chip, 2×3-chip, 4–6 circular modules, and 2×2-chip module under four different thermal powers, respectively, where P_n $(n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)$ is the thermal power applied to chips. Third, with the TCM, the temperature rises of chips were calculated for some other situations, in which, say, two or more chips were simultaneously lit up. The results are presented under the first and second columns of Tables II–VI. The deviations between these two columns, that is "Experimental data from T3ster" and "Temperature rise obtained by TCM" under different conditions are presented in the third column of these Tables. As the maximum deviations are less than 5.0%, 8.4%, 8.7%, 11%, and 9.5% for 1×3-chip, 2×2-chip, 2×3-chip, 4–6 circular modules (see Table II–V) and 2×2-chip module under four different thermal powers (see Table VI), respectively, the accuracy is considered acceptable. Therefore, it follows that the TCM is a fast and effective method to describe thermal coupling, as well as temperature distribution, in LED modules

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \end{pmatrix} = \begin{pmatrix} 17.76 & 1.86 & 0.84 \\ 1.86 & 17.79 & 1.97 \\ 0.84 & 1.97 & 17.76 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \end{pmatrix} \tag{16}$$

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{pmatrix} = \begin{pmatrix} 17.26 & 1.91 & 1.41 & 2.20 \\ 1.91 & 17.26 & 2.20 & 1.41 \\ 1.41 & 2.20 & 17.26 & 1.91 \\ 2.20 & 1.41 & 1.91 & 17.26 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{pmatrix} \tag{17}$$

TABLE VI
TEMPERATURE RISES OF 2 × 2–CHIP MODULEUNDER 150, 350, 550, AND 750 MA

Conditions	Experimental data from T3ster (°C)				Temperature rise obtained by TCM (°C)				Deviation (%)			
	ΔT_1	ΔT_2	ΔT_3	ΔT_4	ΔT_1	ΔT_2	ΔT_3	ΔT_4				
$I_1 = 150$ mA	**4.64**	**0.51**	**0.38**	**0.61**	4.64	0.51	0.38	0.61	0	0	0	0
$I_2 = 350$ mA	1.51	13.83	1.52	0.96	1.48	13.83	1.51	0.91	1.99	0	0.66	5.211
$I_3 = 550$ mA	1.54	2.46	23.09	2.59	1.54	2.45	23.09	2.56	0	0	0	1.16
$I_4 = 750$ mA	3.73	2.53	3.79	38.62	3.73	2.35	3.73	38.62	0	7.11	1.58	0
$I_1 = 150$ mA, $I_2 = 350$ mA	5.96	14.30	1.78	1.46	6.15	14.34	1.90	1.57	3.19	0.28	6.74	7.53
$I_1 = 150$ mA, $I_3 = 550$ mA	6.31	2.82	23.43	2.95	6.18	2.96	23.47	3.2	2.06	4.96	0.17	8.47
$I_1 = 150$ mA, $I_4 = 750$ mA	8.36	3.11	3.93	36.01	8.37	3.24	4.17	39.23	0.12	4.18	6.11	8.94
$I_1 = 150$ mA, $I_2 = 350$ mA, $I_3 = 550$ mA	7.86	16.66	25.22	3.85	7.68	16.80	24.99	4.16	2.29	0.84	0.91	8.05
$I_1 = 150$ mA, $I_2 = 350$ mA $I_3 = 550$ mA, $I_4 = 750$ mA	11.46	19.30	28.83	39.12	11.42	19.53	28.77	42.78	0.35	1.19	0.21	9.36

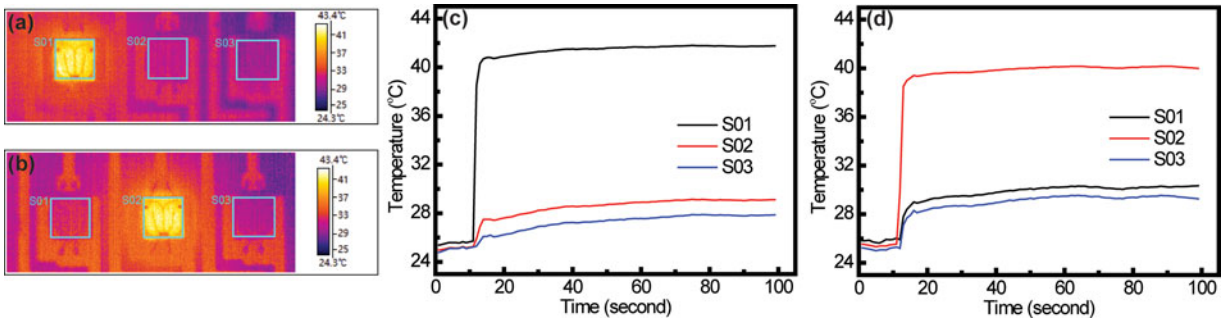

Fig. 9. (a) Temperature distribution of thermal images with S01 chip lit up as the heating source. (b) Temperature distribution of thermal images when the second chip lights up. (c) and (d) corresponding temperature variation trend of each chip in panel (a) and (b), respectively.

$$\begin{pmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\\ \Delta T_5\\ \Delta T_6\end{pmatrix} = \begin{pmatrix}18.14 & 2.03 & 0.90 & 0.51 & 1.52 & 2.17\\ 2.02 & 17.45 & 1.91 & 1.35 & 1.97 & 1.29\\ 0.90 & 1.91 & 18.14 & 2.17 & 1.52 & 0.51\\ 0.51 & 1.35 & 2.17 & 18.14 & 2.03 & 0.90\\ 1.52 & 1.97 & 1.52 & 2.03 & 17.45 & 2.03\\ 2.17 & 1.29 & 0.51 & 0.90 & 2.03 & 18.14\end{pmatrix}\begin{pmatrix}P_1\\ P_2\\ P_3\\ P_4\\ P_5\\ P_6\end{pmatrix}. \tag{18}$$

In (18), the TCM is not a fully symmetric matrix for the 2 × 3-chip module. The μ_{12} (i.e., the element in the first row and second column, which has a value of 2.03) is slightly different from μ_{21} (i.e., the element in the second row and first column, which has a value of 2.02), when the thermal coupling between chip 1# and chip 2# is considered. Given that the resolution of the thermal resistance $R_{\rm th}$ is 0.1 [K/W] in the T3ster TelaLED system, the deviation between μ_{12} and μ_{21} is attributable to the experimental error during measurement, which can be ignored. (19) shown at the bottom of the next page.

To demonstrate that the symmetry of the TCM in the MCM has different heat powers, an array of 2 × 2 chips was used as an example. In the module, the four chips had different thermal powers, as they were driven by 150, 350, 550, and 750 mA, respectively. The results are presented in Table VI

$$\begin{pmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\end{pmatrix} = \begin{pmatrix}17.26 & 1.73 & 1.30 & 2.08\\ 1.73 & 17.26 & 2.08 & 1.30\\ 1.30 & 2.08 & 17.26 & 1.73\\ 2.08 & 1.30 & 1.73 & 17.26\end{pmatrix}\begin{pmatrix}P_1\\ P_2\\ P_3\\ P_4\end{pmatrix}. \tag{20}$$

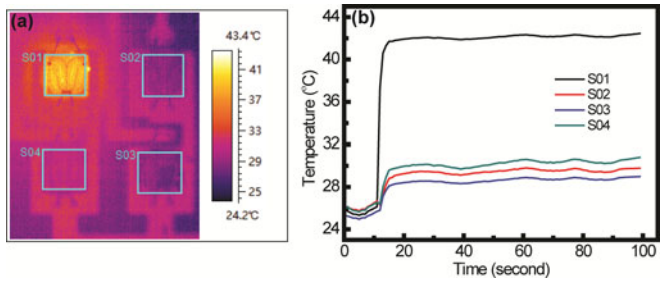

Fig. 10. (a) Temperature distribution of thermal images with S01 chip lit up as the heating source, and (b) corresponding temperature variation trend of each chip shown in (a).

In column 2, last row of Tables II–IV, the corresponding temperature rises of all the chips, which are quite different, are shown with all the LED chips working. Taking the 2 × 3 model as an example, the temperature rises of the six chips in Table IV are 18.60, 19.15, 18.32, 18.03, 19.22, and 18.48 °C, respectively. The differences in the temperature rise of the chips indicate that the temperature distribution in MCMs is inhomogeneous, implying thereby that the thermal coupling effect cannot be ignored. Such inhomogeneous temperature distribution can also be seen in the 4–6 circular module, which has many more chips. Especially, when the chips of a module have different thermal powers, the inhomogeneous temperature distribution (see Table VI) becomes more evident. The temperature rises of the four chips are 11.46, 19.30, 28.83, and 39.12 °C when the thermal powers are 0.29, 0.86, 1.46, and 2.22 W, respectively.

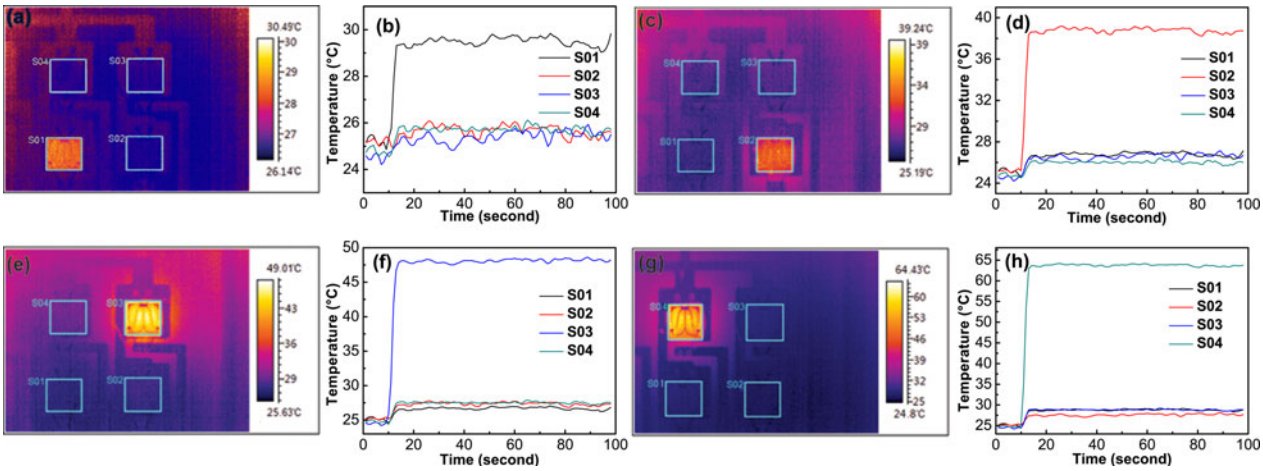

Fig. 11. (a) Temperature distribution of thermal images with S01 chip lit in 150 mA as the heating source, and (b) corresponding temperature variation trend of each chip shown in (a); (c) Temperature distribution of thermal images with S02 chip lit in 350 mA as the heating source and (d) corresponding temperature variation trend of each chip shown in (c); (e) Temperature distribution of thermal images with S03 chip lit in 550 mA as the heating source and (f) corresponding temperature variation trend of each chip shown in (e); (g) Temperature distribution of thermal images with S04 chip lit in 750 mA as the heating source and (h) corresponding temperature variation trend of each chip shown in (g).

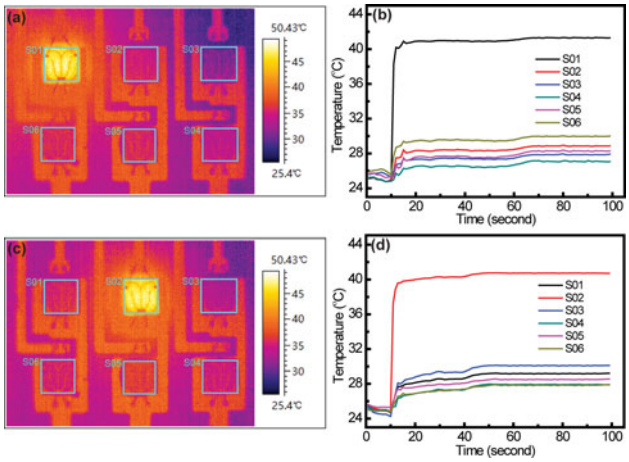

Fig. 12. (a) Temperature distribution of thermal images with S01 chip lit up as the heating source, and (b) corresponding temperature variation trend of each chip shown in (a); (c) temperature distribution of thermal images with S02 chip lit up as the heating source and (d) corresponding temperature variation trend of each chip shown in (c).

The simulation and experimental results show that the thermal coupling between neighboring dice has a significant influence on the temperature rise of chips. A comparative study was made between the thermal analysis results obtained by considering only the self-heating of the dice, and those obtained by the proposed method. Taking 1×3, 2×3-chip modules, and 4–6 circular modules as examples, the temperature rises obtained, with and without thermal coupling, were compared. The thermal coupling between neighboring dice was ignored and only the self-heating of the dice (i.e., the diagonal element of the resistance matrix) was considered. It is found that when the thermal coupling is considered, the temperature rises of the three chips are 14.89, 15.82, and 14.97 °C, respectively. Once the coupling was removed, the temperature rise became 12.92, 12.93, and 12.76 °C, resulting in the maximum difference of about 3 °C. Likewise, when the coupling was removed in the case of 2×3-chip module, the maximum difference reached was about 6 °C. As regards the 4–6 circular module, the maximum difference is about 6.5 °C, which, considering 1×3 and 2×3-chip modules, indicates that the thermal coupling was not negligible.

Combining simulated matrix values with those from the real prototype is useful for the design and thermal manage of LED MCMs. Thus, to evaluate the reliability of the simulation and the feasibility of the proposed method, the deviation between simulated matrices, such as (4), (6), and (10) and those obtained

$$\begin{pmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \\ \Delta T_5 \\ \Delta T_6 \\ \Delta T_7 \\ \Delta T_8 \\ \Delta T_9 \\ \Delta T_{10} \end{pmatrix} = \begin{pmatrix} 18.07 & 1.39 & 0.92 & 1.61 & 1.92 & 0.97 & 0.62 & 0.49 & 0.57 & 1.01 \\ 1.39 & 17.53 & 1.58 & 0.92 & 0.56 & 1.53 & 1.97 & 0.79 & 0.39 & 0.39 \\ 0.92 & 1.58 & 18.07 & 1.39 & 0.49 & 0.62 & 0.97 & 1.92 & 1.01 & 0.57 \\ 1.61 & 0.92 & 1.39 & 17.53 & 0.56 & 0.39 & 0.39 & 0.79 & 1.97 & 1.53 \\ 1.92 & 0.56 & 0.49 & 0.56 & 15.90 & 0.83 & 0.39 & 0.28 & 0.39 & 0.80 \\ 0.97 & 1.53 & 0.62 & 0.39 & 0.83 & 17.85 & 1.01 & 0.32 & 0.26 & 0.31 \\ 0.62 & 1.97 & 0.97 & 0.39 & 0.39 & 1.01 & 17.85 & 0.83 & 0.31 & 0.26 \\ 0.49 & 0.79 & 1.92 & 0.79 & 0.28 & 0.32 & 0.83 & 15.90 & 0.80 & 0.39 \\ 0.57 & 0.39 & 1.01 & 1.97 & 0.39 & 0.26 & 0.31 & 0.80 & 17.85 & 1.01 \\ 1.01 & 0.39 & 0.57 & 1.53 & 0.80 & 0.31 & 0.26 & 0.39 & 1.01 & 17.85 \end{pmatrix} \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \\ P_7 \\ P_8 \\ P_9 \\ P_{10} \end{pmatrix} \tag{19}$$

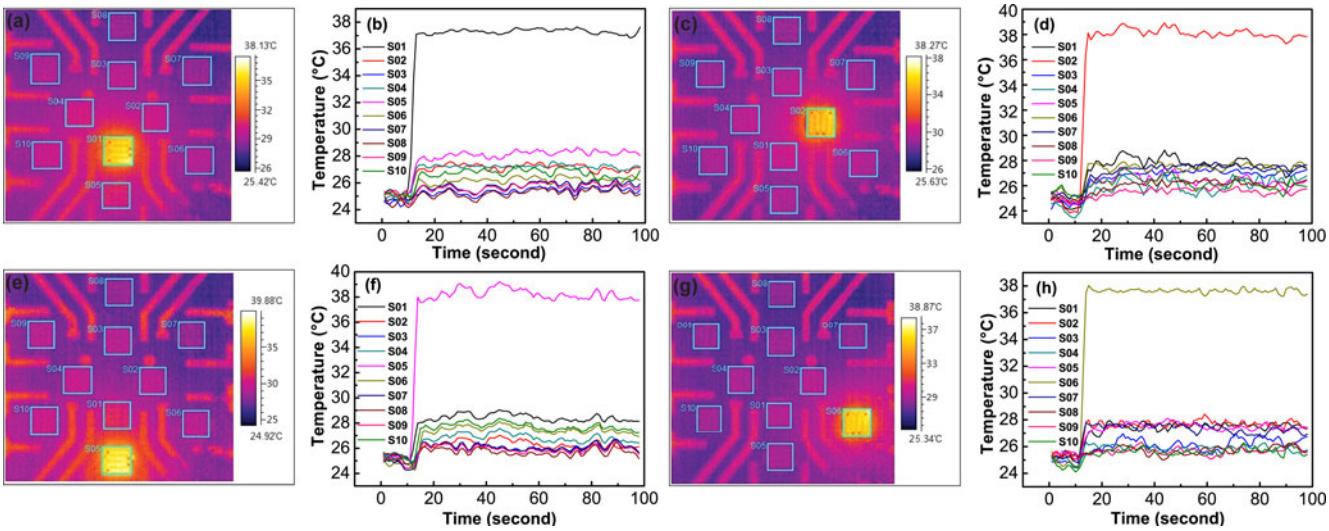

Fig. 13. (a) Temperature distribution of thermal images with the S01 chip lit up as the heating source and (b) corresponding temperature variation trend of each chip shown in (a); (c) temperature distribution of thermal images with the S02 chip lit up as the heating source and (d) corresponding temperature variation trend of each chip shown in (c); (e) temperature distribution of thermal images with the S05 chip lit up as the heating source and (f) Corresponding temperature variation trend of each chip shown in (e); (g) temperature distribution of thermal images with the S06 chip lit up as the heating source and (h) corresponding temperature variation trend of each chip shown in (g).

by experiment, such as (16), (17), and (18), was estimated with absolute average errors. For structures 1×3, 2×2, and 2×3, the absolute average errors are 0.27, 0.53, and 0.44, respectively, which are primarily due to inconsistency in parameters between the simulated and real systems, such as density, thermal conductivity, and heat capacity of thermal conductive layers. On the other hand, the symmetry of TCM in the experiment is not as good as that in simulation. For instance, the locations of the chips in the experiment are not exactly in the center of the copper layer. Besides, the symmetry in the arrangement of chips is not guaranteed. The deviation between simulation and experiment can be reduced further by future research.

In addition to T3ster, the temperature distribution over the surface was also investigated with a thermal imager (Research N2, Meisheng, China).The temperature of heatsink was set to 25 °C. To verify thermal coupling among the chips, the "nontrivial chips" were lighted up separately to obtain the temperatures of the chips from thermal images. Figs. 9 to 13 illustrate the temperature distribution of thermal images and the varying trends of chips' temperatures, when the "nontrivial chips" of 1×3-chip, 2×2-chip, 2×2-chip module under four different thermal powers, 2×3-chip, and 4–6 circular chip modules, were lit up. After a sufficiently long time, the temperature rise of each chip became stable. As illustrated in these figures, the results of temperature rise are in agreement with those obtained from T3ster. For example, in the 2×2-chip module (see Fig. 10), while chip "S01" was lit up as the heating source, the final temperature rises of chips "S02 to S04" are found to be proportional to their distance from "S01." Hence, the temperature rise of chip "S03" is the smallest, when compared with those of the other two chips ("S02", "S04"), because it was the farthest from"S01." These results are not in conformity with those obtained from T3ster. Current experiments demonstrate that the TCM and corresponding simplified measurements are effective for obtaining the temperature distribution of multichip LED modules.

IV. Conclusion

In summary, the TCM, based on electric equivalent circuit, has been presented to describe junction-temperature distribution in multichip LED modules. For the multichip LED module with symmetric arrangement, regardless of differences in thermal powers of chips, a simplified method is proposed to obtain the whole TCM, in which only the nontrivial chips need to be tested. Together with infrared thermography, the simulations by COMSOL, as also the experiments by T3ster, have validated the simplified method proposed in this study. The TCM, especially the one modeled with the simplified method, is effective in obtaining temperature distribution, rapidly and accurately, for the thermal analysis of large LED systems with array structures.

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