Bifurcation Phenomena and Stabilization With Compensation Ramp in Converter With Power Semiconductor Filter

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***Abstract*—A concept, named as power semiconductor filter, has been demonstrated to be an alternative to perform input harmonic filtering in switched-mode power converters. It utilizes a series pass device (SPD) to profile the wave shape of the supply current, while the voltage across the SPD is regulated at a threshold voltage between the linear and saturation regions of the SPD to minimize its power dissipation. Bulky passive components for input harmonic filtering can then be eliminated or shrunk with such active supply current control. For the sake of circuit elegancy, regulation of the SPD voltage is realized by a bang-bang (peak-voltage) controller to vary the input characteristics of the power conversion stage through adjusting some control parameters, such as duty cycle and switching frequency. Experiments reveal that the entire system might exhibit bifurcation phenomena under some supply and load conditions. This paper will derive a sampled-data model to characterize such system behaviors and to identify the onset of bifurcation and chaos. A compensation ramp will be proposed to introduce into the bang-bang controller to stabilize the system operation. Moreover, the slow-scale dynamics will be studied with small-signal models. The investigations will be exemplified on a 48 W, 40–140 V/24 V buck dc–dc converter prototype.**

***Index Terms*—Bifurcation, chaos, dc–dc power conversion, input filtering, power electronics, power semiconductor filter (PSF).**

I. Introduction

THE power conversion stage (PCS) of a switched-mode power converter consists of three main parts, including input filter, switching network, and output filter. With recent advances in semiconductor technology and network topologies, the switching frequency continues to increase. The size of the switching network continues to reduce. Then, the space occupied by the filters becomes a decisive factor in determining the power density of the overall system [1], [2]. The ever-increasing power density is straining design engineers' abilities to squeeze space for the filters without sacrificing the performance, being one of the design priorities [1], [2]. Furthermore, thermal management, acoustic noise, and electromagnetic coupling among components within confined space impose extra challenges.

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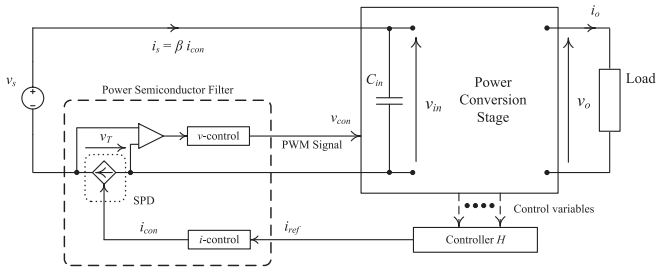

Fig. 1. Power electronics system with the PSF.

A large body of literature has been devoted to analyze, design, optimize, and integrate passive filters through sophisticated modeling techniques [3]–[5], experimentations [6], and simulations [7], [8]. In principle, the physical size of the filter decreases with an increase in the system order. It is thus a design strategy of using high-order filters to increase the system power density, energy efficiency, and dynamic response. However, due to high quality factor at multiple resonant frequencies, high-order filters would cause unwanted oscillations under external disturbances. A remedial measure to alleviate this problem is to use passive damping, active damping, or hybrid passive, and active noise cancellation circuits into the system [4], [9]–[11]. The stability analysis and filter optimization techniques are dominantly based on using an averaged model to characterize the nonlinear power electronic system. However, such model fails to characterize or predict the high-frequency system behaviors when the cutoff frequency of the filter is close to the switching frequency [12], [13]. Thus, many techniques, such as sampled-data model, that take high-frequency behaviors into account have been used to study the bifurcation phenomena and chaotic operations caused by the controller and interactions with the input filter [13]–[15].

As discussed in [1], active filtering techniques may be getting much more attention in the future. Recently, a concept, named as power semiconductor filter (PSF), has been proposed in [16]. Apart from the buck converter, it has also been applied to boost-type power factor corrector and flyback ac/dc converter [17], [18]. As depicted in Fig. 1, the principle is based on shaping the supply current actively with a series pass device (SPD). The ripple current is diverted to the input capacitor $C_{\rm in}$ in the

PCS. To minimize the power dissipation of the SPD, the voltage across the SPD is regulated around the threshold voltage between the linear and saturation regions through varying the input characteristics of the PCS. It has been demonstrated in [16]–[18] that considerable filter size reduction can be achieved with the energy efficiency similar to the passive filter. Besides, the PSF architecture has the merit that it is amenable to monolithic integration.

Apart from the PCS, the entire system consists of two control loops formed by the "*v*-control" and "*i*-control" controllers, respectively. The "*v*-control" controller is used to regulate the voltage across the SPD through varying the duty cycle and/or switching frequency of the switches in the PCS. The "*i*-control" controller is used to regulate the output voltage through adjusting the control signal to the SPD. Therefore, in order to reduce the power dissipation of the SPD, the response time of "*v*-control" should be fast. As depicted in [16], regulation of the SPD voltage is performed by a bang-bang (peak-voltage) controller, which generates the gate signal to the main switch of the buck converter to control the supply voltage to the PCS. Hence, the architecture and control principle are structurally different from traditional current-controlled or voltage-controlled buck converter [12], [19]–[21].

As described in [12], [19]–[21], the bifurcation phenomena and chaos would happen under some operating conditions. For example, when the duty cycle of the main switch is higher than 0.5, system instability would happen in current-controlled buck converter [19], [20]. Moreover, interactions between the input filter and the voltage-controlled buck converter would also cause such phenomena [12], [21].

Fan *et al.* [16] give the selection criteria of the SPD and discusses the slow-scale stability with small-signal model. This paper extends the investigation by deriving the fast-scale model with the sampled-date model to characterize the system behaviors and study the bifurcation phenomena and system stability. A discrete-time piecewise-linear model is derived by calculating the Jacobian matrix of the sampled-data model. The fast-scale instability is studied by determining the eigenvalues (i.e., pole locations) of the characteristic equation of the linearized model. A compensation ramp that can improve the system stability will be proposed to introduce into the bang-bang controller, and its effect on the system will be discussed [22], [23]. The slow-scale dynamics will then be studied with small-signal models [16]. The instability issue, accuracy of sampled-data model, and small-signal model will be verified experimentally on a 48 W, 40–140 V/24 V buck converter operating in continuous conduction mode (CCM).

II. Brief Overview on the Operation of PSF in Buck Converter

Fig. 2(a) shows the circuit schematic of the buck converter with PSF. The SPD, *T*, which is an *n*-channel MOSFET, is connected in series with a standard buck converter. A capacitor $C_{\rm in}$ is connected across the input of the buck converter. The quiescent point of the MOSFET is regulated at the boundary between its linear and saturation regions by the "*i*-control" and "*v*-control"

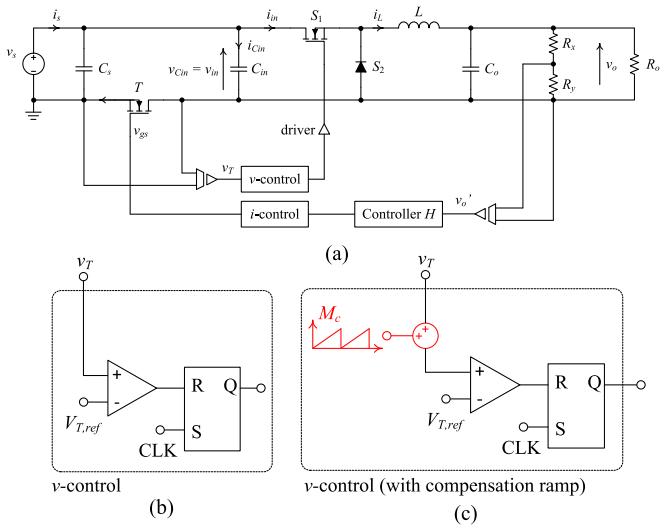

Fig. 2. Circuit schematic of buck converter with the PSF. (a) Buck converter with the PSF. (b) Peak-voltage controller. (c) With a compensation ramp.

TABLE I
Values and Part Numbers of the Components Used

Component	Value/Part No.	Component	Value/Part No.
C_s	1.47 μF	$C_{\rm in}$	3.47 μF
L	60 μH	C_o	81 μF
S_1	BSC500N20NS3G	S_2	STTH30R02DJF
T	IRF540N	v-control	Microcontroller PIC16F753

controllers. The "*i*-control" controller generates necessary driving signal $v_{\rm gs}$ to the SPD to control the wave shape of the supply current i_s. Its input is derived from an error amplifier, named as "*H* Controller." "Controller *H*" is a Type-II compensator for regulating the system output v_o, which is sensed and downscaled by a resistive network formed by R_x and R_y to derive the feedback voltage $v_o{}'$. It generates the current reference $i_{\rm ref}$ to the "*i*-control" controller. With such active current control, the function of $C_{\rm in}$ is used to absorb the high-frequency ripple current generated by the switching network in the buck converter, as i_s should normally be equal to the average supply current of the buck converter. The PSF thus performs the function of input harmonic filtering.

The "*v*-control" controller is used to limit the voltage across *T* below the reference voltage $V_{T,\rm ref}$ through dictating the state of the main switch $\rm S_1$. The value of $V_{T,\rm ref}$ is slightly higher than the saturation voltage of *T*, so that the power dissipation of *T* is minimized. Fig. 2(b) and (c) shows two modulators for the "*v*-control" controller. The first one is a bang-bang (peak-voltage) controller used in [16]. Detailed operation can be found in [16]. The second one has a compensation ramp introduced into the bang-bang controller. Performance characteristics of the system with two modulators will be discussed later.

Fig. 3 shows the photo of a 48 W, 40–140 V/24 V prototype. The switching frequency is 250 kHz. The values and part numbers of the components used are shown in Table I. The

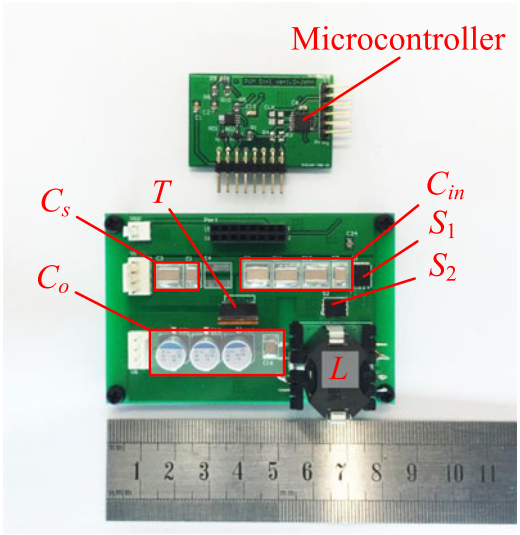

Fig. 3. Prototype buck converter with the PSF.

modulator is implemented with the analog peripherals of a microcontroller.

III. Analysis of Bifurcation and Chaotic Behavior

With the bang-bang control for the "v-control" controller, bifurcation phenomena and chaos are observed under certain operating conditions. Fig. 4 shows the waveforms of the output voltage ripple $v_{o,r}$, supply current i_s, inductor current i_L, and SPD voltage v_T of the prototype buck converter under different supply voltages. When the supply voltage v_s is 68 V, the system is in stable (period-1) operation. With v_s reduced from 68 to 67 V, period-doubling occurs. The waveforms are shown in Fig. 4(b). If v_s is further reduced, the system is found to be in chaotic operation. The waveforms are shown in Fig. 4(c). Fig. 5(a)–(c) shows the phase portrait of i_L and v_T using the results in Fig. 4(a)–(c). A period-2 attractor is observed in Fig. 5(b) and chaotic attractor is found in Fig. 5(c). The Poincare section of the condition in Fig. 4(c) for 2000 consecutive switching cycles with $v_o = 24\ \text{V} \pm\ 0.5\ \mu\text{V}$ is shown in Fig. 5(d). The scattered points reveal that the system is in chaotic operation.

Similar bifurcation phenomena are observed when there is a small change of the load resistance. Fig. 6 shows the phase portrait of the experimental result at the bifurcation point due to the change of the load R_o. Period doubling occurs when R_o is increased from 13 to 14 Ω. Fig. 7 shows the bifurcation diagrams of the initial value of i_L in each switching cycle $i_{L,n}$ against v_s and load value R_o, respectively. $i_{L,n}$ is chosen in the plots for observing the occurrence of border collision. Fig. 7(a) shows that period-2 limit cycle occurs when v_s is deceased to 67 V. With v_s further reduced to 50 V, the system will enter into chaotic region for a narrow range of v_s until it reached 48.5 V. Then, period-4 limit cycle follows when v_s is further reduced. Finally, chaotic operation appears again with $v_s < 46$ V. In Fig. 7(b), with $14\ \Omega\ < R_o \leq 27.5\ \Omega$, period-2 limit cycle occurs and the converter is in CCM. With $27.5\ \Omega < R_o \leq 50.5\ \Omega$,

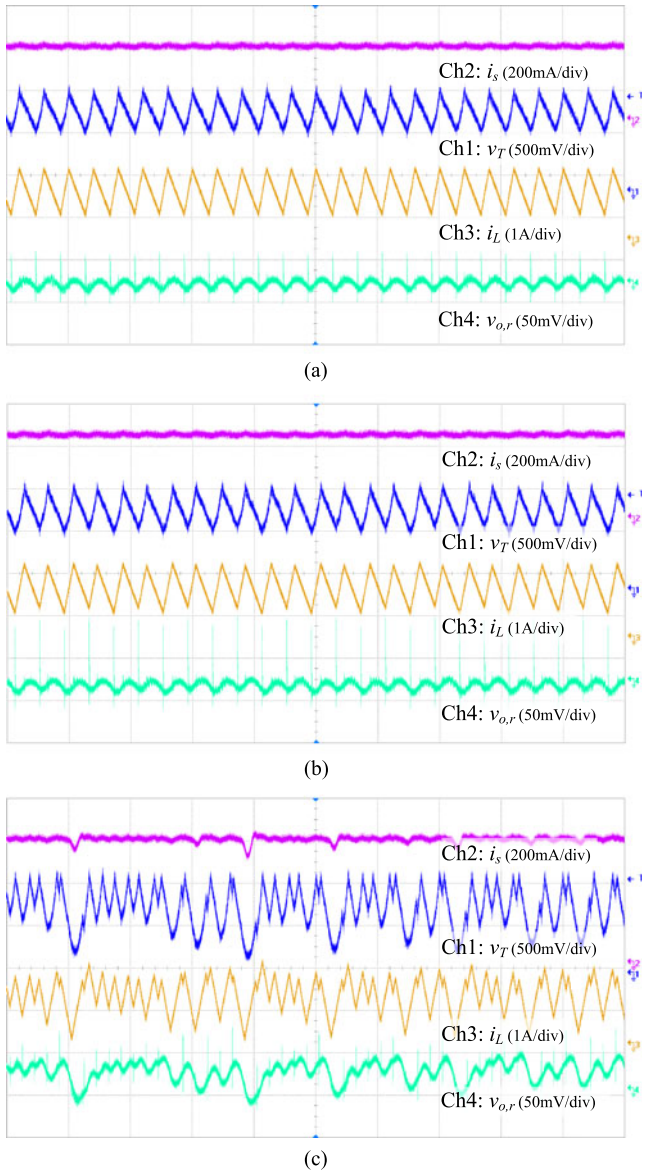

Fig. 4. Measured waveforms under different supply voltages ($R_o = 22\ \Omega$). (a) Stable operation with $v_s = 68$ V (Timebase: 10 μs/div). (b) Period doubling with $v_s = 67$ V (Timebase: 10 μs/div). (c) Chaotic operation with $v_s = 50$ V (Timebase: 20 μs/div).

border collision occurs [24]. The converter is switched between CCM and discontinuous conduction mode (DCM) alternately in every switching cycle. Finally, when $R_o > 50.5\ \Omega$, the converter is in DCM and in period-1 operation.

Fig. 8 shows the stability regions of the system under different values of the supply voltage v_s, load resistance R_o, percentage output power $\hat{P}_o$, and duty cycle d with $v_o = 24$ V. Fig. 8(a) shows the combinations of v_s and R_o with $v_o = 24$ V. Fig. 8(b) shows the combinations of $\hat{P}_o$ and d. In Region I, the system is in CCM and period-1 operation. In Region II, the converter is in DCM and stable period-1 operation. In Region III, bifurcation, limit cycles, or chaotic operation occurs. In Fig. 8(b), the system could enter into Region III when $d > 0.28$, showing different behaviors from the classical current-controlled buck converter

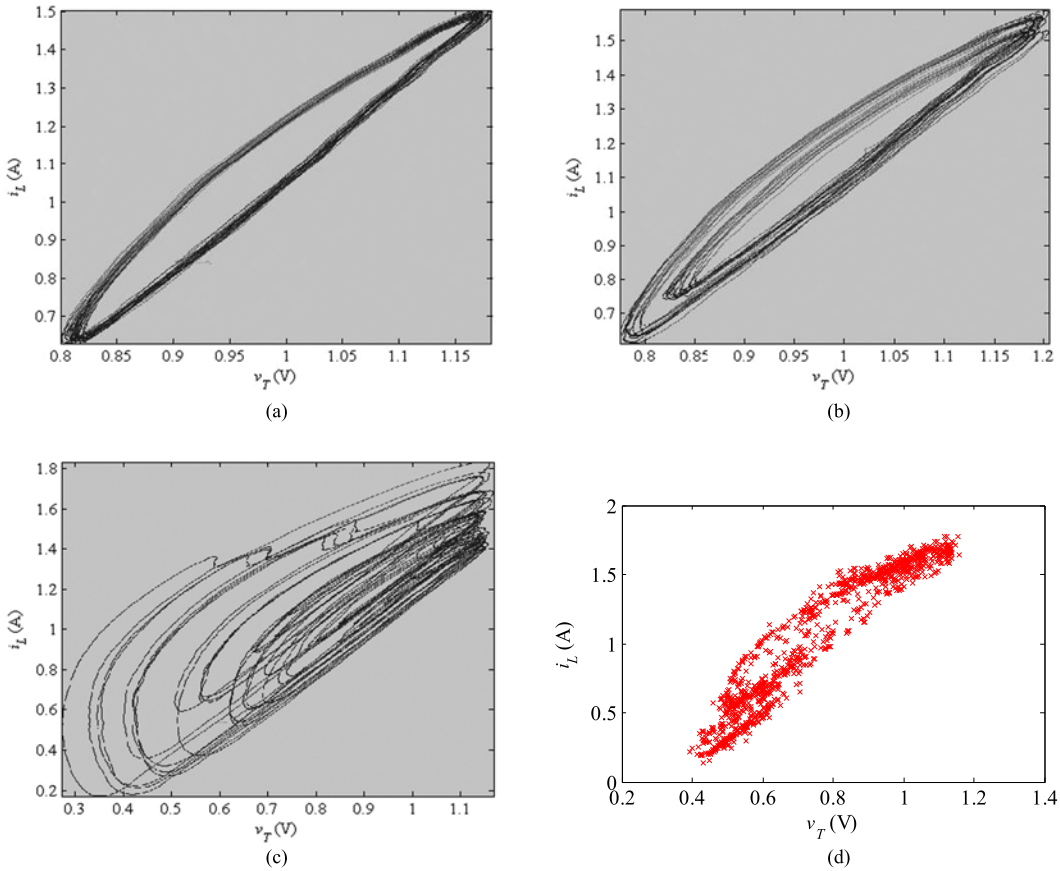

Fig. 5. Measured phase portrait and Poincare section of the prototype with $R_o = 22\ \Omega$ and nominal value of $v_o = 24$ V. (a) $v_s = 68$ V. (b) $v_s = 67$ V. (c) $v_s = 50$ V. (d) Poincare section for $v_s = 50$ V.

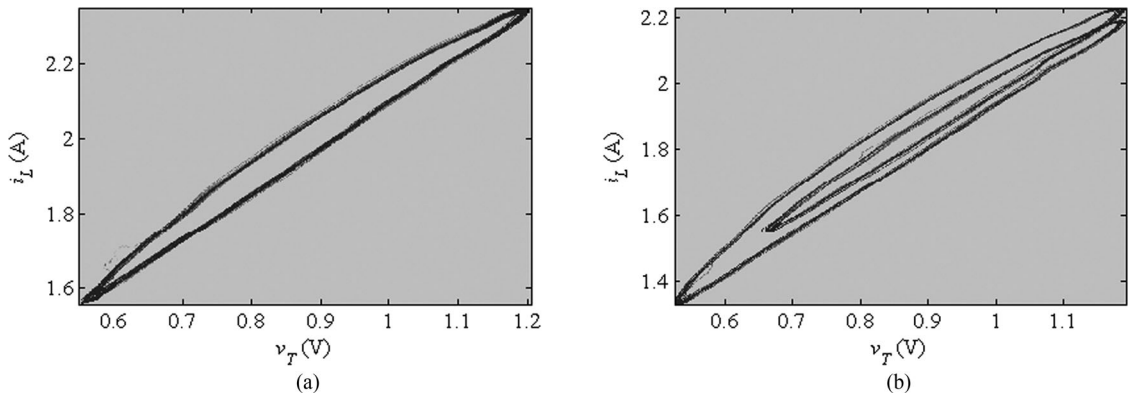

Fig. 6. Measured phase portrait in different $R_o\,(v_s = 60$ V). (a) $R_o = 13\ \Omega$. (b) $R_o = 14\ \Omega$.

that exhibits system instability with the duty cycle higher than 0.5 [20].

IV. Sampled-Data Model, Jacobian Matrix, and Eigenvalues

Fig. 9(a) and (b) shows the equivalent circuits of the system when the main switch S_1 is ON and OFF, respectively. The MOSFET T is modeled as a dependent current source and is considered as an input variable. When S_1 is ON, the state-space representation is

$$\begin{pmatrix} \frac{dv_{C\mathrm{in}}}{dt} \\ \frac{di_L}{dt} \\ \frac{dv_{\mathrm{Co}}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{C_{\mathrm{in}}} & 0 \\ \frac{1}{L} & 0 & -\frac{1}{L} \\ 0 & \frac{1}{C_o} & -\frac{1}{C_o R_o} \end{pmatrix} \begin{pmatrix} v_{C\mathrm{in}} \\ i_L \\ v_{\mathrm{Co}} \end{pmatrix} + \begin{pmatrix} \frac{1}{C_{\mathrm{in}}} \\ 0 \\ 0 \end{pmatrix} i_s \quad \text{for } n\,T_{\mathrm{sw}} \le t \le n\,T_{\mathrm{sw}} + t_{\mathrm{on}} \tag{1}$$

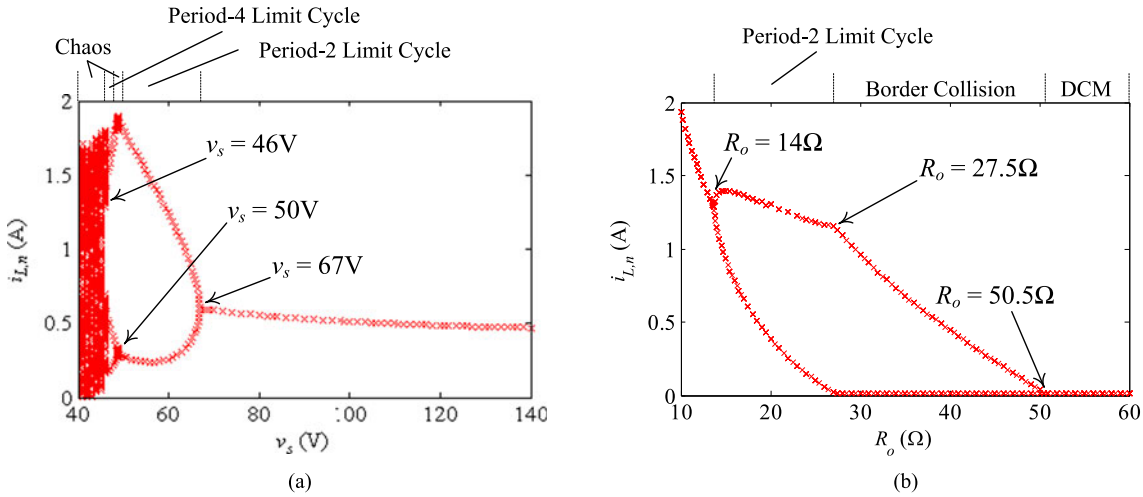

Fig. 7. Bifurcation diagrams. (a) $i_{L,n}$ versus v_s with $R_o = 22\ \Omega$. (b) $i_{L,n}$ versus R_o with $v_s = 60$ V.

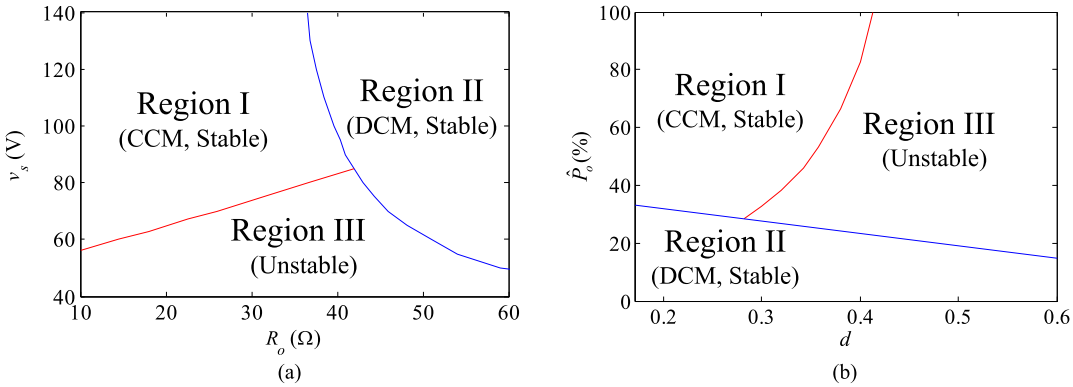

Fig. 8. Operating regions of the system. (a) v_s versus R_o. (b) Percentage output power versus d.

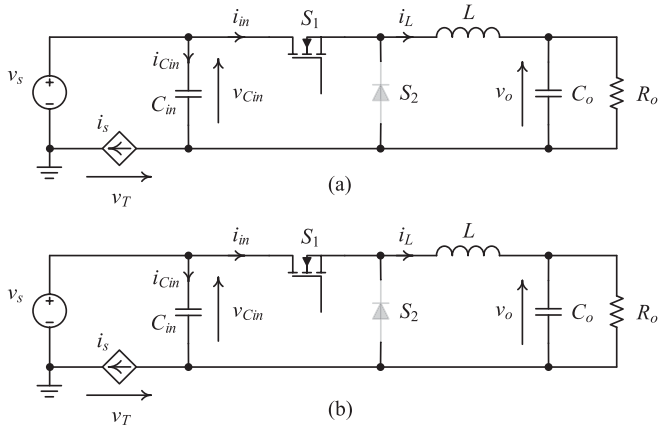

Fig. 9. Equivalent circuits. (a) S_1 is ON and S_2 is OFF. (b) S_1 is OFF and S_2 is ON.

where $v_{C\text{in}}$ is the voltage across the input capacitor C_{in}, i_L is the current through the inductor L, v_{Co} is the voltage across the output capacitor C_o, R_o is the load resistance, T_{sw} is the switching period, and t_{on} is the duration of S_1 in its ON state in nth switching cycle.

Based on (1)

$$\frac{d^3 v_{C\text{in}}}{dt^3} + \frac{1}{C_o R_o}\frac{d^2 v_{C\text{in}}}{dt^2} + \left(\frac{1}{C_{\text{in}} L} + \frac{1}{C_o L}\right)\frac{dv_{C\text{in}}}{dt} + \frac{1}{C_{\text{in}} C_o L R_o} v_{C\text{in}} = \frac{1}{C_{\text{in}} C_o L} i_s. \tag{2}$$

It can be shown that

$$v_{C\text{in,on}}(t) = R_o I_s + K_1 e^{m_1 t} + K_2 e^{m_2 t} + K_3 e^{m_3 t} \tag{3a}$$

$$i_{L,\text{on}}(t) = I_s - C_{\text{in}}(m_1 K_1 e^{m_1 t} + m_2 K_2 e^{m_2 t} + m_3 K_3 e^{m_3 t}) \tag{3b}$$

$$v_{Co,\text{on}}(t) = v_{C\text{in,on}}(t) + C_{\text{in}} L(m_1{}^2 K_1 e^{m_1 t} + m_2{}^2 K_2 e^{m_2 t} + m_3{}^2 K_3 e^{m_3 t}) \tag{3c}$$

where $v_{C\text{in,on}}(t)$, $i_{L,\text{on}}(t)$, and $v_{Co,\text{on}}(t)$ are the time-domain equations of $v_{C\text{in}}(t)$, $i_L(t)$, and $v_{\text{Co}}(t)$, respectively, m_1, m_2, and m_3 are the roots of the third-order characteristic equation given in (2), and K_1, K_2, and K_3 are coefficients obtained by solving (2) and are functions of $v_{C\text{in}}(t_n)$, $i_L(t_n)$, $v_{\text{Co}}(t_n)$, and i_s.

Similarly, when S_1 is OFF, the state-space representation is

$$\begin{pmatrix} \frac{dv_{C\text{in}}}{dt} \\ \frac{di_L}{dt} \\ \frac{dv_{\text{Co}}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L} \\ 0 & \frac{1}{C_o} & -\frac{1}{C_o R_o} \end{pmatrix} \begin{pmatrix} v_{C\text{in}} \\ i_L \\ v_{\text{Co}} \end{pmatrix} + \begin{pmatrix} \frac{1}{C_{\text{in}}} \\ 0 \\ 0 \end{pmatrix} i_s, \quad \text{for } n\,T_{\text{sw}} + t_{\text{on}} \le t \le (n+1)T_{\text{sw}}. \tag{4}$$

Based on (4)

$$\frac{d^2 i_L}{dt^2} + \frac{1}{C_o R_o}\frac{di_L}{dt} + \frac{1}{C_o L} i_L = 0. \tag{5}$$

It can be shown that

$$v_{C\text{in,off}}(t) = v_{C\text{in,on}}(t_{\text{on}}) + \frac{i_s}{C_{\text{in}}} t \tag{6a}$$

$$i_{L,\text{off}}(t) = K_4 e^{y_1 t} + K_5 e^{y_2 t} \tag{6b}$$

$$v_{Co,\text{off}}(t) = -L(y_1 K_4 e^{y_1 t} + y_2 K_5 e^{y_2 t}) \tag{6c}$$

where $v_{C\text{in,off}}(t)$, $i_{L,\text{off}}(t)$, and $v_{Co,\text{off}}(t)$ are the time-domain equations of $v_{C\text{in}}(t)$, $i_L(t)$, and $v_{\text{Co}}(t)$, respectively, y_1 and y_2 are the roots of second-order characteristic equation given in (5), and K_4 and K_5 are the coefficients obtained by solving (5) and are functions of $i_L(t_{\text{on}})$ and $v_{\text{Co}}(t_{\text{on}})$.

By approximating (3) and (6) with second-order Taylor expansions

$$v_{C\text{in,on}}(t) \simeq K_1 + K_2 + K_3 + R_o i_s + (m_1 K_1 + m_2 K_2 + m_3 K_3)t + \frac{1}{2}\left({m_1}^2 K_1 + {m_2}^2 K_2 + {m_3}^2 K_3\right) t^2 \tag{7a}$$

$$i_{L,\text{on}}(t) \simeq i_s - C_{\text{in}}(m_1 K_1 + m_2 K_2 + m_3 K_3) - C_{\text{in}}({m_1}^2 K_1 + {m_2}^2 K_2 + {m_3}^2 K_3)t - C_{\text{in}}({m_1}^3 K_1 + {m_2}^3 K_2 + {m_3}^3 K_3)t^2 \tag{7b}$$

$$v_{Co,\text{on}}(t) \simeq K_1\left(1 + {m_1}^2 C_{\text{in}} L\right) + K_2\left(1 + {m_2}^2 C_{\text{in}} L\right) + K_3\left(1 + {m_3}^2 C_{\text{in}} L\right) + R_o i_s + \left(K_1\left(m_1 + {m_1}^3 C_{\text{in}} L\right) + K_2\left(m_2 + {m_2}^3 C_{\text{in}} L\right) + K_3\left(m_3 + {m_3}^3 C_{\text{in}} L\right)\right) t + \frac{1}{2}\left(K_1\left({m_1}^2 + {m_1}^4 C_{\text{in}} L\right) + K_2\left({m_2}^2 + {m_2}^4 C_{\text{in}} L\right) + K_3\left({m_3}^2 + {m_3}^4 C_{\text{in}} L\right)\right) t^2 \tag{7c}$$

$$v_{C\text{in,off}}(t) \simeq v_{C\text{in}}(t_{\text{on}}) + \frac{t}{C_{\text{in}}} i_s \tag{8a}$$

$$i_{L,\text{off}}(t) \simeq K_4 + K_5 + (y_1 K_4 + y_2 K_5)\, t + \frac{1}{2}\left({y_1}^2 K_4 + {y_2}^2 K_5\right) t^2 \tag{8b}$$

$$v_{Co,\text{off}}(t) \simeq -L\left(y_1 K_4 + y_2 K_5\right) - L\left({y_1}^2 K_4 + {y_2}^2 K_5\right) t - \frac{1}{2} L\left({y_1}^3 K_4 + {y_2}^3 K_5\right) t^2. \tag{8c}$$

As shown in Fig. 2(b), the peak voltage across *T* is bounded by the comparator and the RS latch with reference voltage of $V_{T,\text{ref}}$. By using (7a), S_1 is switched from ON to OFF state when

$$v_s - V_{T,\text{ref}} = K_1 + K_2 + K_3 + R_o i_s + (m_1 K_1 + m_2 K_2 + m_3 K_3)\, dT_{\text{sw}} + \frac{1}{2}\left({m_1}^2 K_1 + {m_2}^2 K_2 + {m_2}^2 K_3\right) d^2 {T_{\text{sw}}}^2 \tag{9}$$

where $d = t_{\text{on}}/T_{\text{sw}}$ is the duty cycle.

The following sampled-data model is obtained by using (7)–(9) that

$$\begin{pmatrix} v_{C\text{in}}[n+1] \\ i_L[n+1] \\ v_{\text{Co}}[n+1] \end{pmatrix} = \begin{pmatrix} f_{11}(d[n]) & f_{12}(d[n]) & f_{13}(d[n]) \\ f_{21}(d[n]) & f_{22}(d[n]) & f_{23}(d[n]) \\ f_{31}(d[n]) & f_{32}(d[n]) & f_{33}(d[n]) \end{pmatrix} \times \begin{pmatrix} v_{C\text{in}}[n] \\ i_L[n] \\ v_{\text{Co}}[n] \end{pmatrix} + \begin{pmatrix} g_1(d[n]) \\ g_2(d[n]) \\ g_3(d[n]) \end{pmatrix} i_s \tag{10}$$

where $f_{11}, f_{12}, f_{13}, f_{21}, f_{22}, f_{23}, f_{31}, f_{32}, f_{33}, g_1, g_2,$ and g_3 are function of the duty cycle $d[n]$ in the *n*th switching period.

The nonlinear system in (10) is then linearized by calculating the Jacobian matrix *J* [15], [25]. *J* is defined as

$$J = \begin{pmatrix} \frac{\partial v_{C\text{in}}[n+1]}{\partial v_{C\text{in}}[n]} & \frac{\partial v_{C\text{in}}[n+1]}{\partial i_L[n]} & \frac{\partial v_{C\text{in}}[n+1]}{\partial v_{\text{Co}}[n]} \\ \frac{\partial i_L[n+1]}{\partial v_{C\text{in}}[n]} & \frac{\partial i_L[n+1]}{\partial i_L[n]} & \frac{\partial i_L[n+1]}{\partial v_{\text{Co}}[n]} \\ \frac{\partial v_{\text{Co}}[n+1]}{\partial v_{C\text{in}}[n]} & \frac{\partial v_{\text{Co}}[n+1]}{\partial i_L[n]} & \frac{\partial v_{\text{Co}}[n+1]}{\partial v_{\text{Co}}[n]} \end{pmatrix} = \begin{pmatrix} J_{11} & J_{12} & J_{13} \\ J_{21} & J_{22} & J_{23} \\ J_{31} & J_{32} & J_{33} \end{pmatrix} \tag{11}$$

$$J_{11} = f_{11} + \frac{\partial f_{11}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} v_{C\text{in}}[n] + \frac{\partial f_{12}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} i_L[n] + \frac{\partial f_{13}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} v_{\text{Co}}[n] + \frac{\partial g_1}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} i_s \tag{12}$$

$$J_{12} = f_{12} + \frac{\partial f_{11}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]} v_{C\text{in}}[n] + \frac{\partial f_{12}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]} i_L[n] + \frac{\partial f_{13}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]} v_{\text{Co}}[n] + \frac{\partial g_1}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]} i_s \tag{13}$$

$$J_{13} = f_{13} + \frac{\partial f_{11}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]} v_{C\text{in}}[n] + \frac{\partial f_{12}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]} i_L[n] + \frac{\partial f_{13}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]} v_{\text{Co}}[n] + \frac{\partial g_1}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]} i_s \tag{14}$$

$$J_{21} = f_{21} + \frac{\partial f_{21}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} v_{C\text{in}}[n] + \frac{\partial f_{22}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} i_L[n] + \frac{\partial f_{23}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} v_{\text{Co}}[n] + \frac{\partial g_2}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]} i_s \tag{15}$$

TABLE II
LOCATION OF EIGENVALUES FOR MODULATOR WITHOUT THE COMPENSATION RAMP

v_s	R_o	Location of λ			System operation
68 V	22 Ω	–0.9800	0.3317	0.9955	Period-1
67 V	22 Ω	–1.0173	0.3304	0.9955	Period-2 Limit Cycle
50 V	22 Ω	–1.5745	0.3541	0.9955	Chaos
60 V	13 Ω	–0.9896	0.4843	0.9925	Period-1
60 V	14 Ω	–1.0288	0.4673	0.9930	Period-2 Limit Cycle

$$J_{22} = f_{22} + \frac{\partial f_{21}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}v_{C\text{in}}[n] + \frac{\partial f_{22}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}i_L[n] + \frac{\partial f_{23}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}v_{\text{Co}}[n] + \frac{\partial g_2}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}i_s \quad (16)$$

$$J_{23} = f_{23} + \frac{\partial f_{21}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}v_{C\text{in}}[n] + \frac{\partial f_{22}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}i_L[n] + \frac{\partial f_{23}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}v_{\text{Co}}[n] + \frac{\partial g_2}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}i_s \quad (17)$$

$$J_{31} = f_{31} + \frac{\partial f_{31}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]}v_{C\text{in}}[n] + \frac{\partial f_{32}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]}i_L[n] + \frac{\partial f_{33}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]}v_{\text{Co}}[n] + \frac{\partial g_3}{\partial d[n]}\frac{\partial d[n]}{\partial v_{C\text{in}}[n]}i_s \quad (18)$$

$$J_{32} = f_{32} + \frac{\partial f_{31}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}v_{C\text{in}}[n] + \frac{\partial f_{32}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}i_L[n] + \frac{\partial f_{33}}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}v_{\text{Co}}[n] + \frac{\partial g_3}{\partial d[n]}\frac{\partial d[n]}{\partial i_L[n]}i_s \quad (19)$$

$$J_{33} = f_{33} + \frac{\partial f_{31}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}v_{C\text{in}}[n] + \frac{\partial f_{32}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}i_L[n] + \frac{\partial f_{33}}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}v_{\text{Co}}[n] + \frac{\partial g_3}{\partial d[n]}\frac{\partial d[n]}{\partial v_{\text{Co}}[n]}i_s. \quad (20)$$

The stability of the system is analyzed by studying the root locations of the characteristic equation

$$\left|\begin{pmatrix}\lambda & 0 & 0\\ 0 & \lambda & 0\\ 0 & 0 & \lambda\end{pmatrix} - \begin{pmatrix}J_{11} & J_{12} & J_{13}\\ J_{21} & J_{22} & J_{23}\\ J_{31} & J_{32} & J_{33}\end{pmatrix}\right| = 0. \quad (21)$$

Bifurcation phenomena appear if any one of the roots λ of (21) is outside the unit circle on the complex plane. In order to simplify the analysis, the supply current i_s is assumed to be a constant after the output voltage feedback loop has reached the steady state. The assumption is valid as the cutoff frequency of the error amplifier "*H* Controller" is lower than the switching frequency of the buck converter. i_s is almost constant even the system is in period-doubling or chaotic operation.

Based on the derived model, Table II shows the location of calculated eigenvalues λ under the conditions in Fig. 5. With $v_s = 68$ V, all eigenvalues are within the unit circle. With $v_s = 67$ V, an eigenvalue is outside the unit circle, showing system instability [26], [27]. With $v_s = 50$ V, an eigenvalue is away from the unit circle. Similar results are obtained for the operating conditions in Fig. 6. Thus, the experimental results confirm the validity of the sampled-data model and theoretical prediction. Fig. 10(a) and (b) shows the root locus of the eigenvalues with respect to v_s and R_o, respectively, under the condition described in the bifurcation diagram given in Fig. 7.

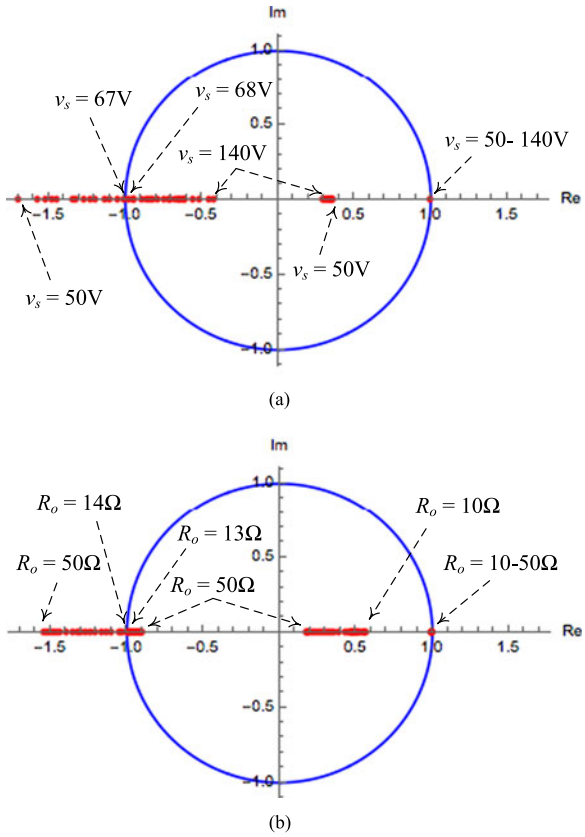

Fig. 10. Root locus of the eigenvalues without the compensation ramp. (a) v_s varies between 50 and 140 V with $R_o = 22$ Ω. (b) R_o varies between 10 and 50 Ω with $v_s = 60$ V.

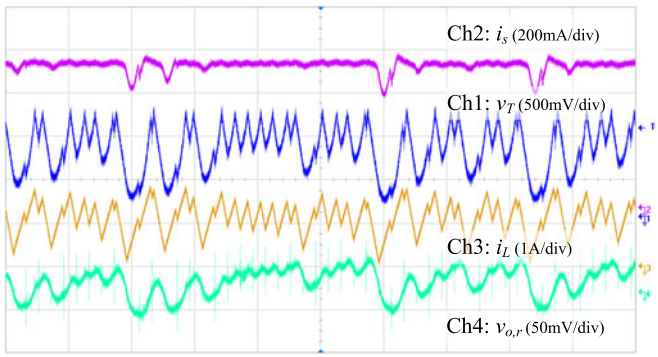

Fig. 11. Experimental waveform for $v_s = 40$ V (time base: 20 μs/div).

V. STABILIZATION WITH A COMPENSATION RAMP

Fig. 11 shows the experimental waveforms under half-load condition and with $v_s = 40$ V—the minimum supply voltage of

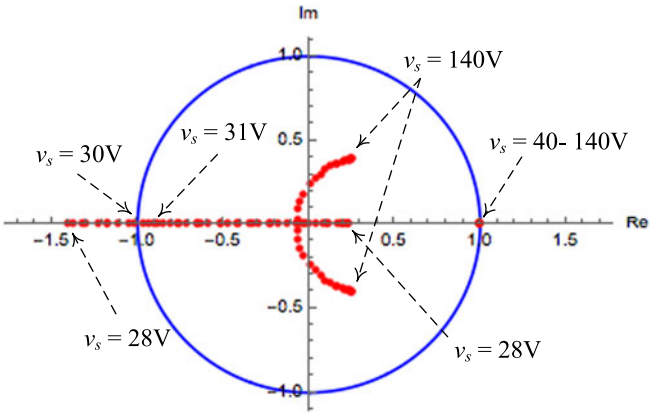

Fig. 12. Root locus of the eigenvalues w.r.t. v_s and $M_c = 0.2$ V/μs with $R_o = 22\ \Omega$.

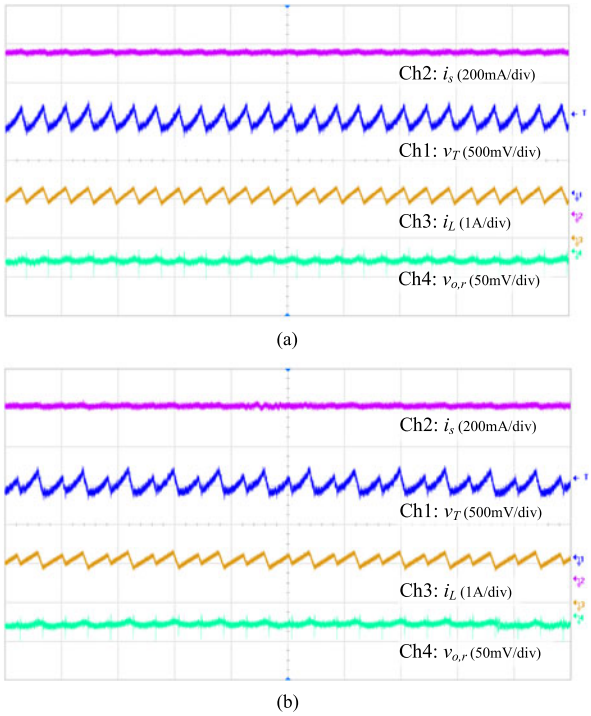

Fig. 13. Waveforms and eigenvalues with $M_c = 0.2$ V/μs under half-load condition. (a) $v_s = 31$ V (Timebase: 10 μs/div). (b) $v_s = 30$ V (Timebase: 10 μs/div).

the converter. The system is in chaotic operation. It is noted that i_s is still fairly constant under such chaotic operation, confirming the assumption made in Section IV. The instability problem of the peak-voltage controller is tackled by introducing a compensation ramp into the modulator. As shown in Fig. 2(c), the ramp is superimposed onto v_T to derive the gate signal. The main switch S_1 is switched from ON to OFF state when

$$v_s - V_{T,\mathrm{ref}} + M_c d T_{\mathrm{sw}} = C_1 + C_2 + C_3 + R_o i_s + (m_1 C_1 + m_2 C_2 + m_3 C_3)\, d T_{\mathrm{sw}} + \frac{1}{2}\left(m_1{}^2 C_1 + m_2{}^2 C_2 + m_2{}^2 C_3\right) d^2 T_{\mathrm{sw}}{}^2. \quad (22)$$

TABLE III
LOCATION OF EIGENVALUES FOR MODULATOR WITH $M_c = 0.2$ V/μs = 0.2 V/μs.

v_s	R_o	Location of λ			System Operation
40 V	22 Ω	$-0.0627 - 0.0973\,j$	$-0.0627 + 0.0973\,j$	0.9955	Period-1
31 V	22 Ω	−0.8856	0.1972	0.9955	Period-1
30 V	22 Ω	−1.0167	0.2104	0.9955	Period-2 Limit Cycle

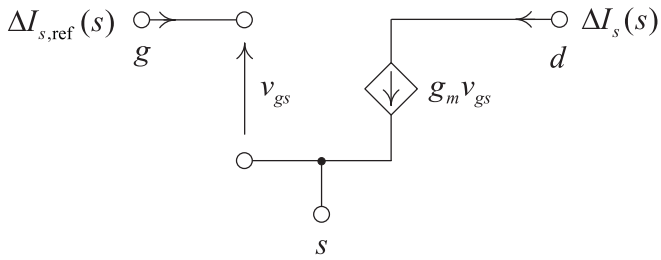

Fig. 14. Simplified small-signal model of MOSFET.

Fig. 12 shows the root locus plot of the system with compensation slope $M_c = 0.2$ V/μs. The minimum v_s, which can ensure stable operation, is extended from 68 to 31 V, and thus stable operation is ensured for $v_s = 40$ V. Fig. 13(a) and (b) shows the waveforms of v_T, i_s, i_L, and $v_{o,r}$ on the stability boundary calculated from the derived sampled-data model with v_s equal to 31 and 30 V, respectively. Table III shows the locations of the eigenvalues of the two operating conditions in Figs. 11 and 13. Again, the theoretical predictions are in close agreement with the experimental verifications.

VI. SLOW-SCALE DYNAMICS

The slow-scale dynamics with the stabilizing ramp in the modulator is studied in this section. It is based on using the small-signal model given in [16]. Fig. 14 shows the small-signal model of MOSFET [28], the transfer function of the MOSFET $H_{\mathrm{SPD}}(s)$ is

$$H_{\mathrm{SPD}}(s) = \frac{\Delta I_s}{\Delta I_{s,\mathrm{ref}}} = g_m \quad (23)$$

where g_m is the transconductance of MOSFET.

Fig. 15 shows the steady-state and perturbed waveform of the modified modulator shown in Fig. 2(c). For the sake of simplicity, it is assumed that the waveform of v_T, when S_1 is ON, is a straight line with the slope m_1 [29]

$$m_1 = \frac{\langle i_{L,\mathrm{on}} \rangle - i_s}{C_{\mathrm{in}}} \quad (24)$$

where $\langle i_{L,\mathrm{on}} \rangle$ is the average on-time current of the inductor L.

When S_1 is OFF

$$m_2 = \frac{i_s}{C_{\mathrm{in}}}. \quad (25)$$

TABLE IV
TRANSFER FUNCTIONS OF THE MODIFIED SMALL-SIGNAL MODEL

Parameter	Transfer function	Parameter	Transfer function
$H_{\rm vg}(s)$	$D\dfrac{R_o}{L\,C_o\,R_o\,s^2+L\,s+R_o}$	$H_{\rm vd}(s)$	$\dfrac{V_o}{D}\dfrac{R_o}{L\,C_o\,R_o\,s^2+L\,s+R_o}$
$Z_o(s)$	$\dfrac{L\,R_o\,s}{L\,C_o\,R_o\,s^2+L\,s+R_o}$	$H_{\rm ig}(s)$	$D\dfrac{C_o\,R_o\,s+1}{L\,C_o\,R_o\,s^2+L\,s+R_o}$
$H_{\rm id}(s)$	$\dfrac{V_o}{D}\dfrac{C_o\,R_o\,s+1}{L\,C_o\,R_o\,s^2+L\,s+R_o}$	$H_{\rm iL-io}(s)$	$\dfrac{R_o}{L\,C_o\,R_o\,s^2+L\,s+R_o}$
$H_{\rm iL}(s)$	D	$H_d(s)$	$\dfrac{V_o}{R_o}$
$H_m(s)$	$\dfrac{F_{\rm sw}}{M_c+\dfrac{(1-2D)I_o}{2C_{\rm in}}}$	$H_{\rm is}(s)$	$\dfrac{T_d}{C_{\rm in}}$
$H_{\rm iin}(s)$	$\dfrac{1}{C_{\rm in}}[\dfrac{D\,(1-D)}{2\,F_{\rm sw}}-T_d]$	$H_{C\,\rm in}(s)$	$\dfrac{1}{s\,C_{\rm in}}$
$H_v(s)$	$\dfrac{s\,C_2R_2+1}{s^2R_1R_2C_1C_2+s\,R_1(C_1+C_2)}$	$H_{\rm SPD}(s)$	g_m
$G_{\rm vo\text{-}is,OL}(s)$	$H_{\rm vg}(s)\,H_{C\,\rm in}(s)(1-H_{\rm iin-is}(s))+H_{\rm vd}(s)\,H_m(s)\,H_b(s)$		
$H_b(s)$	$H_{C\,\rm in}(s)-H_{\rm is}(s)-(H_{C\,\rm in}(s)+H_{\rm iin}(s))H_{\rm iin-is}(s)$		
$H_{\rm iin-is}(s)$	$\dfrac{H_{\rm iL}(s)\,H_{\rm ig}(s)\,H_{C\,\rm in}(s)+H_m(s)(H_{\rm iL}(s)\,H_{\rm id}(s)+H_d(s))(H_{C\,\rm in}(s)-H_{\rm is}(s))}{1+H_{\rm iL}(s)\,H_{\rm ig}(s)\,H_{C\,\rm in}(s)+H_m(s)(H_{\rm iL}(s)\,H_{\rm id}(s)+H_d(s))(H_{C\,\rm in}(s)+H_{\rm iin}(s))}$		

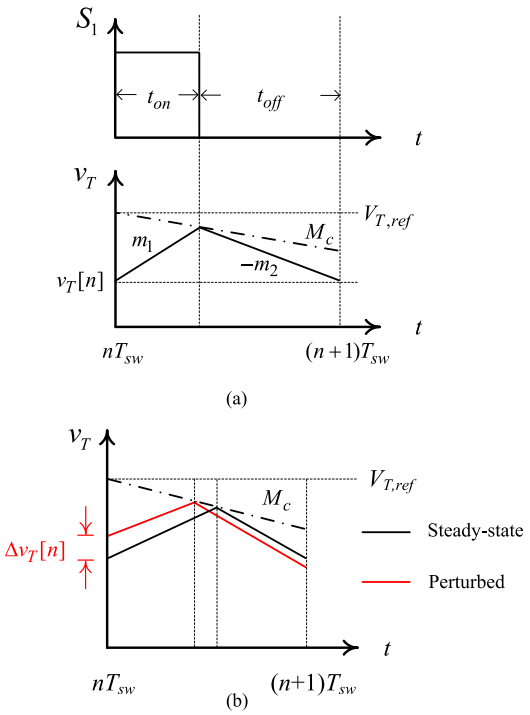

Fig. 15. Key waveforms of the modified modulator. (a) Key waveforms of the modulator in Fig. 2(c). (b) Modulator waveforms under small perturbation.

Based on Fig. 15, the transfer function of the modified modulator can be found to be

$$V_{T,\rm ref}+m_1T_d+\frac{M_cd}{F_{\rm sw}}=\frac{m_1d}{2F_{\rm sw}}-\frac{d}{2F_{\rm sw}}[m_1d-m_2(1-d)] \tag{26}$$

where d, T_d, and $F_{\rm sw}$ are the duty cycle, delay time of the modulator, and switching frequency of the converter, respectively.

By introducing small-signal perturbations into (24), (25) and duty cycle d

$$m_1 = M_1+\Delta m_1 = M_1+\frac{\Delta i_{\rm in}-\Delta i_s}{C_{\rm in}} \tag{27}$$

$$m_2 = M_2+\Delta m_2 = M_2+\frac{\Delta i_s}{C_{\rm in}} \tag{28}$$

$$d = D+\Delta d \tag{29}$$

where Δm_1, Δm_2, Δi_s, and $\Delta i_{\rm in}$ are the small-signal perturbations on m_1, m_2, i_s, and $i_{\rm in}$, respectively. M_1, M_2, and D are the steady state values of m_1, m_2, and D.

By substituting (27), (28), and (29) into (26), the modulator gain H_m is

$$H_m(s)=\frac{F_{\rm sw}}{M_c+\frac{(1-2D)I_o}{2C_{\rm in}}}. \tag{30}$$

Fig. 16 shows the small-signal model of the PSF system with the peak-voltage control [16]. The transfer function of the modified modulator and functional blocks in Fig. 16 are given in Table IV. Based on Fig. 16, the control-to-output transfer function $G_{\rm vo\text{-}isref,OL}(s)$ and open-loop gain of the whole system $G_{\rm OL}(s)$ are

$$G_{\rm vo\text{-}is,OL}(s)=\frac{\Delta V_o(s)}{\Delta I_s(s)} \tag{31}$$

$$G_{\rm vo\text{-}isref,OL}(s)=\frac{\Delta V_o(s)}{\Delta I_{s,\rm ref}(s)}=G_{\rm vo\text{-}is,OL}(s)H_{\rm SPD}(s) \tag{32}$$

$$G_{\rm OL}(s)=\frac{\Delta V_o(s)}{\Delta V_{o,\rm err}(s)}=K_sH_v(s)G_{\rm vo\text{-}isref,OL}(s) \tag{33}$$

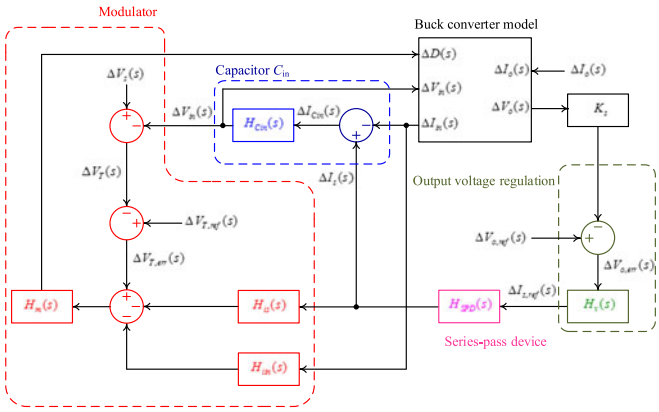

Fig. 16. Small-signal dynamical model.

TABLE V
PARAMETERS USED IN CALCULATION OF $G_{\text{vo-isref,OL}}(s)$

Parameter	Value	Parameter	Value
V_o	24 V	V_s	40 V
I_s	0.62 A	R_o	24 Ω
g_m	2.3	T_d	200 ns
M_c	0.2 V/μs	C_{in}	3.47 μF
L	60 μH	C_o	81 μF

where $G_{\text{vo-is,OL}}(s)$ is the open-loop input-current-to-output-voltage transfer function, K_s is the gain of the sensor, and $H_v(s)$ is the transfer function of Type-II compensator [16].

VII. Experimental Verification

The buck converter prototype shown in Fig. 3 is evaluated by using the PWM modulator in Fig. 2(c) with $M_c = 0.2$ V/μs. Based on the parameters given in Table V, Fig. 17 shows the simulated, calculated, and measured results of the open-loop transfer characteristics $G_{\text{vo-isref,OL}}(s)$ (without controller H) obtained by the modified model shown in Fig. 16. The simulated results are also obtained on PSIM. The theoretical predictions and experimental results are in close agreement. The gain margin of $G_{\text{vo-isref,OL}}(s)$ is 19.1 dB at 60 kHz and the phase margin is 83.2° at 7.48 kHz. The control parameters in $H_v(s)$ are designed by K-factor approach as described in [30].

Fig. 18 summarizes the power loss of the SPD P_{loss} against the output current under different supply voltage v_s and supply current ripple i_{ripple}. The power loss increases as the output current increases and the supply current ripple decreases. In general, the power loss is less than the power dissipation of a diode. As discussed in [16], although the power loss is slightly higher than the conventional passive filter, the PSF is amenable to monolithic integration for increasing the power density of the entire power converter system and can avoid possible acoustic noise.

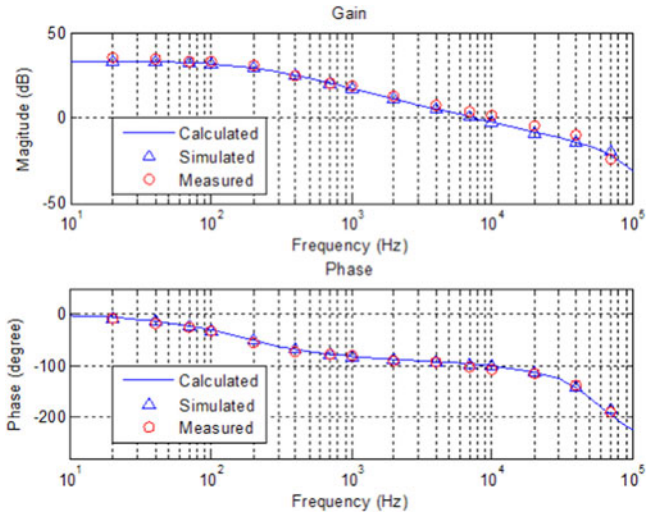

Fig. 17. Bode plot of $G_{\text{vo-isref,OL}}(s)$.

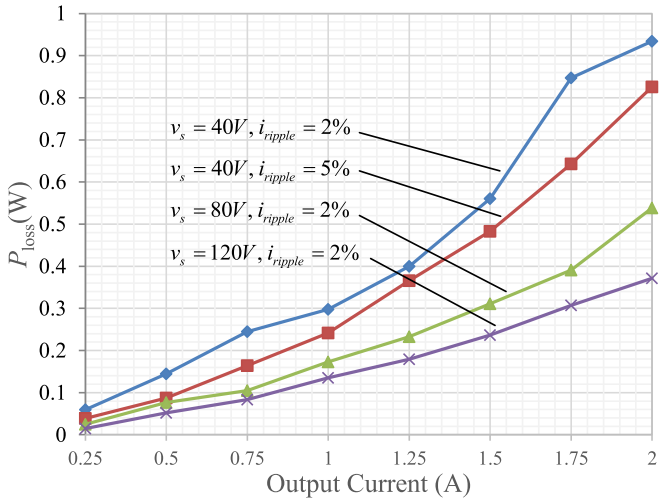

Fig. 18. Power dissipated on SPD versus output load current.

VIII. Conclusion

A sampled-data model is derived to study the onset of bifurcation phenomena and chaotic operation in switching converters with PSF. A compensation ramp is used to tackle such phenomenon has been proposed. The accuracy of the model is successfully demonstrated and verified on a 48 W, 40–140 V buck converter prototype. The small-signal modeling and analysis of the entire system have been discussed. The experimental results are in close agreement with the theoretical predictions. The theoretical frequency responses of the system are found to be accurate up to one-fifth of the switching frequency. The system behaviors of the buck converter with PSF were found to be different from the traditional current-controlled and voltage-controlled buck converter. The bifurcation phenomena and chaotic operation could happen with the duty cycle smaller or larger than 0.5.

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