An Expandable Two-Phase Interleaved Ultrahigh Step-Down Converter With Automatic Current Balance

K. I. Hwu, *Member, IEEE*, W. Z. Jiang, *Student Member, IEEE*, and P. Y. Wu

***Abstract*—In the high step-down voltage applications, the dc–dc converter with a high step-down voltage conversion ratio is usually used. Recently, a high step-down converter, named ultrahigh step-down converter, has been presented. As compared with the nonisolated tapped-inductor buck converter, the ultrahigh step-down converter has not only a higher voltage step-down gain but also a lower voltage spike. On the other hand, in the high-current applications, a multiple phase structure is preferable. Therefore, in this paper, a novel expandable two-phase interleaved ultrahigh step-down converter with automatic current balance is presented, which is derived from the existing single-phase ultrahigh step-down converter. There are four main advantages of the proposed converter. First, the step-down voltage gain is improved. Therefore, the turns ratio of each phase can be decreased. Second, due to the charge balance of the energy-transferring capacitor, the proposed two-phase ultrahigh step-down converter possesses an automatic current balance. Third, as compared with a single-phase ultrahigh step-down converter, the output current ripple can be reduced. Fourth, the phase number of the proposed converter can be expanded. Finally, the basic operating principle of the proposed converter is analyzed, and a prototype is constructed to verify its effectiveness by some experimental results.**

***Index Terms*—Automatic current balance, high step-down voltage conversion ratio, multiple phase, ultrahigh step-down converter.**

I. Introduction

THE step-down converter has been widely used in many applications, such as voltage regulator modules and electric vehicle chargers. In telecommunication applications, a 48-V dc bus voltage created from the ac–dc converter is a widely used as a nominal voltage. An isolated converter converts the bus voltage of 48 V to a lower voltage of 12 V, and then, nonisolated buck converters (point of load) transfer the voltage of 12 V to much lower voltages to supply loads. As for electric vehicle applications, a high step-down converter is also used to step down the high voltage generated by the electric generator to lower voltages so as to feed loads.

In the literatures [3]–[6], the two-stage buck converters are presented. A high step-down voltage can be effectively achieved by the two-stage buck converters. However, these converters use many components, leading to high cost, and, hence, the corresponding efficiency would be relatively low due to the fact that the overall efficiency is obtained by multiplying individual efficiencies. In order to further improve the voltage conversion ratio, the coupled inductor is applied to the synchronously-rectified (SR) buck converter [7]–[12]. Although the circuit shown in [7] has a higher step-down voltage conversion ratio than the traditional buck converter, the leakage inductance will cause a high-voltage spike. Accordingly, a coupled inductor is applied to the buck converter to achieve soft switching [13]. However, the step-down voltage gain of this converter is not improved.

As generally recognized, for the high-current applications, an interleaved converter, constructed by two phases or more, is preferable. The multiple-phase interleaved converters are sequentially controlled with phase difference of 360° divided by the number of phases, for adjacent two phases. For the multiple-phase interleaved converters, the input and output currents should be distributed evenly among phases so as to reduce the current stresses on the components as well as to enhance the efficiency, as compared with a single phase with the same system specifications. Furthermore, the output current ripple can be reduced, which leads to a smaller output capacitor.

Recently, there are many interleaved buck converters (IBC) to be proposed [14]–[19]. In the literatures [14] and [15], the coupled inductor is applied to the IBC, and, hence, the high step-down voltage conversion ratio can be achieved. In the literature [16], an improved IBC is presented, which uses several input capacitors as a voltage divider so as to obtain a high step-down voltage conversion ratio as well as to reduce the voltage stress on the switches. The literature [17] presents a two-phase step-down converter with automatic current balance based on the coupled inductor and the capacitor. However, this converter cannot achieve a desired high step-down voltage conversion ratio. Consequently, if a high step-down voltage conversion ratio is needed, the number of phases should be increased to at least 3 or more and the corresponding duty cycle will be relatively small. As for the literatures [8]–[12], [18], and [19], the presented circuits possess a high step-down voltage conversion

Manuscript received September 26, 2016; revised December 13, 2016; accepted January 13, 2017. Date of publication January 23, 2017; date of current version August 2, 2017. This work was supported by the Ministry of Science and Technology under Grant MOST 103-2221-E-027-040-MY3. Recommended for publication by Associate Editor F. Costa.

The authors are with the Department of Electrical Engineering, National Taipei University of Technology, Taipei 10608, Taiwan (e-mail: eaglehwu@ntut.edu.tw; newjerusalem333@gmail.com; boyingwu77@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2656938

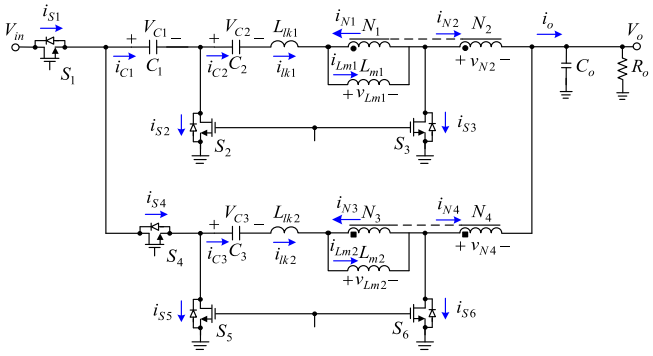

Fig. 1. Proposed two-phase interleaved step-down converter.

ratio with high nonlinear characteristics, and, hence, the corresponding controller design tends to be difficult. Concerning the literature [20], the ultrahigh step-down converter, belonging to a nonisolated single-stage topology, is presented, which is used for 48-V dc bus applications. However, for the dc microgrid to be considered, a 400-V dc bus can be a preferable choice. Consequently, up to now, the isolated topology has been generally adopted, such as the 400-V/24-V CLS100 dc–dc converter made by Current Logic Group, Ltd., the 400–900-/24-V LA313-2450-A dc–dc converter made by Powerex, Inc, etc. As to the 400-/24-V nonisolated topology, the circuit shown in [21] is presented whose ground is separated.

According to the preceding discussion, a two-phase converter, based on the ultrahigh step-down converter [20], is presented and used for 400-V/24-V nonisolated applications. The proposed two-phase interleaved ultrahigh step-down converter possesses not only an automatic current balance but also a higher step-down voltage conversion ratio than the single-stage ultrahigh step-down converter [20]. Furthermore, all the switches can achieve zero-voltage-switching (ZVS) turn-on. Moreover, the output current ripple can be reduced by the interleaved operation. Above all, the number of phases can be expanded to *k*, where *k* is larger than 2.

II. Basic Operating Principles

In this section, the operating principle and automatic current balance of the proposed converter are discussed in the following. Fig. 1 shows the proposed two-phase interleaved ultrahigh step-down converter, which consists of six switches S_1, S_2, S_3, S_4, S_5, and S_6, three energy-transferring capacitors C_1, C_2, and C_3, one output capacitor C_o, one coupled inductor composed of two windings N_1 and N_2, one leakage inductor L_{lk1} and one magnetizing inductor L_{m1}, and the other coupled inductor consisting of two windings N_3 and N_4, one leakage inductor L_{lk2}, and one magnetizing inductor L_{m2}. As for the load, it is constructed by one output resistor R_o. It is noted that the capacitor C_1 is used as not only an energy-transferring capacitor but also an automatic current balance capacitor. Also, it is noted that phase 1 is constructed by S_1, S_2, S_3, C_2, L_{lk1}, L_{m1}, N_1, and N_2, whereas phase 2 is built up by S_4, S_5, S_6, C_3, L_{lk2}, L_{m2}, N_3, and N_4.

There are some symbols and assumptions to be given as follows: 1) all the components are ideal except for the coupled inductors; 2) the input voltage is denoted by $V_{\rm in}$; 3) the output voltage is signified by V_o; 4) the values of C_1, C_2, and C_3 are large enough to be kept constant at V_{C1}, V_{C2}, and V_{C3}, respectively; 5) the voltages across L_{m1} and L_{m2} are expressed by v_{Lm1} and v_{Lm2}, respectively; 6) the currents flowing through S_1, S_2, S_3, S_4, S_5, and S_6 are represented by i_{S1}, i_{S2}, i_{S3}, i_{S4}, i_{S5}, and i_{S6}, respectively; 7) the currents flowing through L_{lk1}, L_{lk2}, L_{m1}, L_{m2}, N_1, N_2, N_3, and N_4 are indicated by i_{Llk1}, i_{Llk2}, i_{Lm1}, i_{Lm2}, i_{N1}, i_{N2}, i_{N3}, and i_{N4}, respectively; 8) the switching frequency is signified by f_s; 9) the turn-on time of S_1 is D_1T_s, the turn-on time of S_4 is D_2T_s, and the turn-on time of S_2 and S_3 is $(1-D_1)T_s$, and the turn-on time of S_5 and S_6 is $(1-D_2)T_s$, where D_1 and D_2 are the duty cycles for S_1 and S_4, respectively, and are both equal to D; 10) the signals v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}, v_{gs5}, and v_{gs6} are the gate driving signals for S_1, S_2, S_3, S_4, S_5, and S_6, respectively; 11) the turns ratios of the coupled inductors are the same and equal to $n\,(=N_2/N_1=N_4/N_3)$; and 12) the magnetizing inductor currents are always positive.

A. Converter Operating Principle

There are fourteen operating states, to be described below. Fig. 2 shows the key waveforms for the proposed converter operating with magnetizing inductors having no negative currents.

1) State 1 (negative i_{lk2}) $[t_0 \le t \le t_1]$: As shown in Fig. 3, S_1, S_5, and S_6 are ON, but S_2, S_3, and S_4 are OFF. For phase 1, the output is connected to the load. Hence, L_{m1} and L_{lk1} are magnetized due to positive voltages across them, and C_1 and C_2 are charged due to positive currents flowing through them, causing the currents i_{N1} and i_{N2} both to be increased continuously. At the same time, for phase 2, L_{m2} is demagnetized, L_{lk2} is demagnetized in the opposite direction, and C_3 is discharged, pumping energy to the load.

2) State 2 (phase 1 blanking time) $[t_1 \le t \le t_2]$: As shown in Fig. 4, S_5 and S_6 are ON, but S_1, S_2, S_3, and S_4 are OFF. This state is the blanking time of phase 1. During this state, C_2 is still charged, and L_{m1} and L_{lk1} are demagnetized, pumping energy to the load. At the same time, the body diodes of S_2 and S_3 are turned ON due to the continuous flow of i_{lk1}. As for phase 2, its operation is the same as state 1.

3) State 3 (S_2 and S_3 ZVS turn-on) $[t_2 \le t \le t_3]$: As shown in Fig. 5, S_2, S_3, S_5, and S_6 are ON, but S_1 and S_4 are OFF. S_2 and S_3 are turned ON with ZVS. During this state, for phase 1, C_2 is still charged, and L_{m1} and L_{lk1} are still demagnetized, pumping energy to the load. As for phase 2, its operation is the same as state 2.

4) State 4 (phase 2 blanking time) $[t_3 \le t \le t_4]$: As shown in Fig. 6, S_2 and S_3 are ON, but S_1, S_4, S_5, and S_6 are OFF. This state is the blanking time of phase 2. During this state, C_3 is still discharged, causing the body diodes of S_4 and S_6 to be turned ON and C_1 to be charged. Besides, C_2 is still charged. At the same time, L_{m1}, L_{m2}, and L_{lk1} are demagnetized due to the negative voltages across them, and L_{lk2} is demagnetized in the opposite direction due to a positive voltage across it.

5) State 5 (S_4 ZVS turn-on and positive i_{lk2}) $[t_4 \le t \le t_5]$: As shown in Fig. 7, S_2, S_3, and S_4 are ON, but S_1, S_5, and

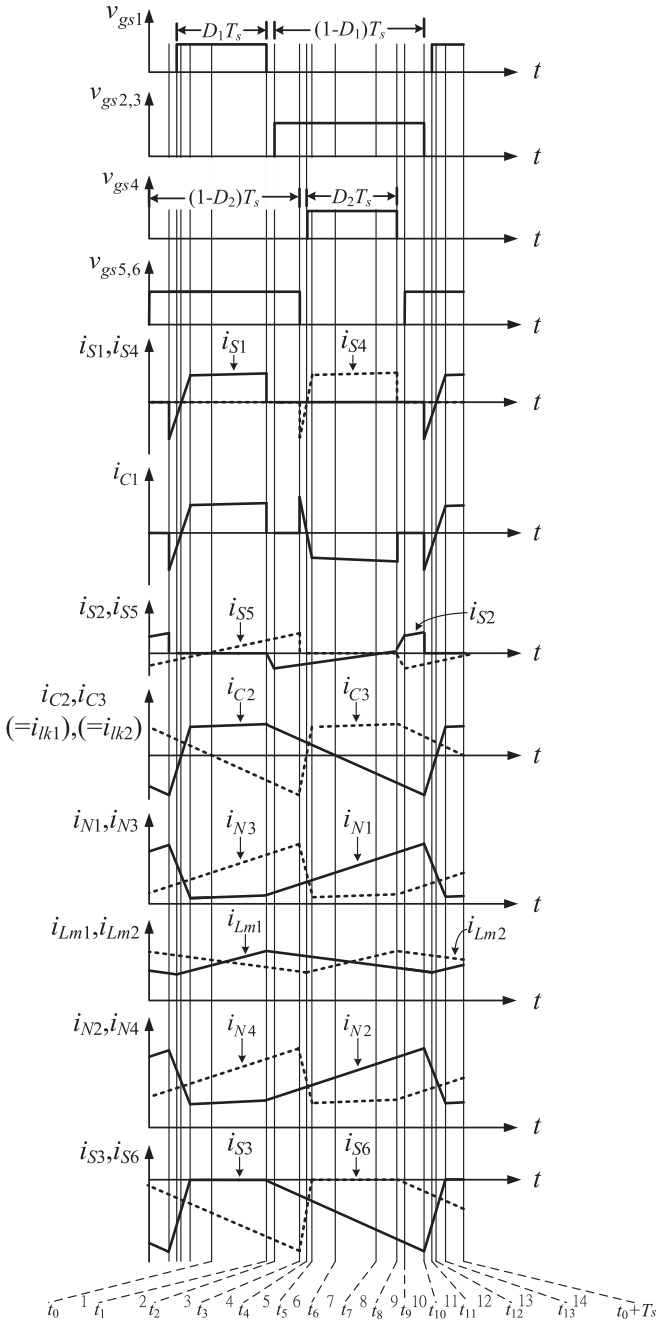

Fig. 2. Illustrated waveforms for the proposed converter over one switching period.

S_6 are OFF. S_4 is turned ON with ZVS and the body diode of S_6 is still ON. During this state, C_2 keeps charged and C_1 begins to charge C_3. At the same time, L_{m2} and L_{lk2} are magnetized, whereas L_{m1} and L_{lk1} are demagnetized, pumping energy to the load. Once the current in the body diode of S_6 is zero, the operating state goes to state 6.

6) State 6 (zero i_{S6}) $[t_5 \le t \le t_6]$: As shown in Fig. 8, S_2, S_3, and S_4 are still ON, but S_1, S_5, and S_6 are still OFF. The operation of this state is the same as that of state 5 except that the current in the body diode of S_6 is zero. As soon as i_{lk1} or i_{C2} fall to zero, the operating state proceeds to State 7.

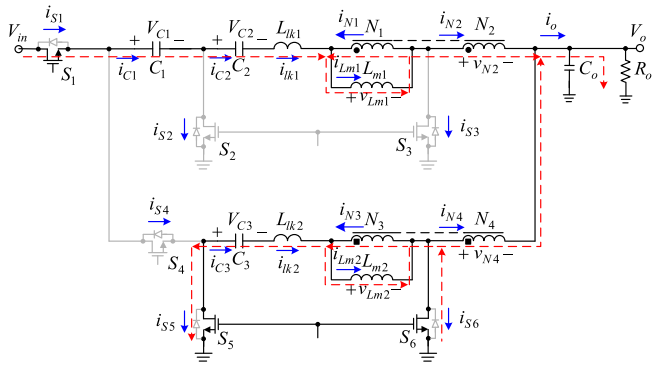

Fig. 3. Current flow in state 1.

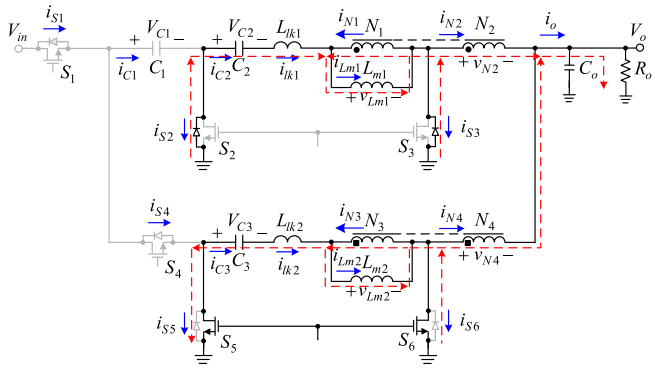

Fig. 4. Current flow in state 2.

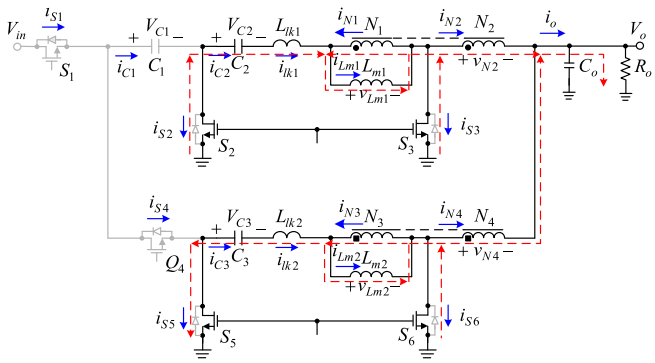

Fig. 5. Current flow in state 3.

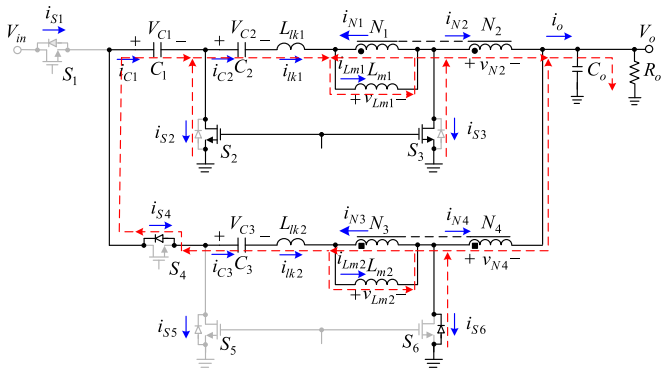

Fig. 6. Current flow in state 4.

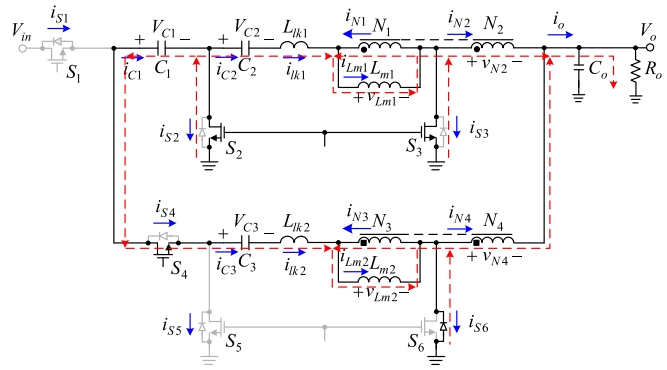

Fig. 7. Current flow in state 5.

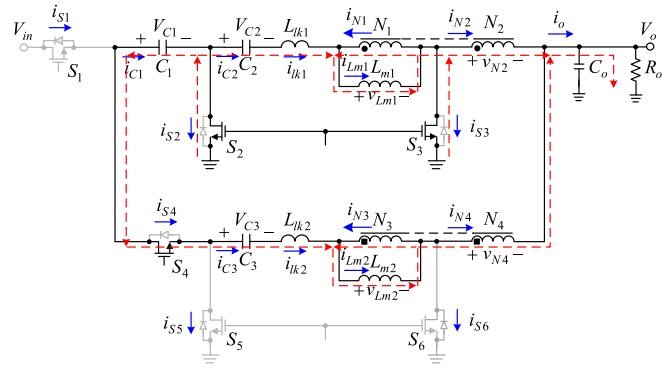

Fig. 8. Current flow in state 6.

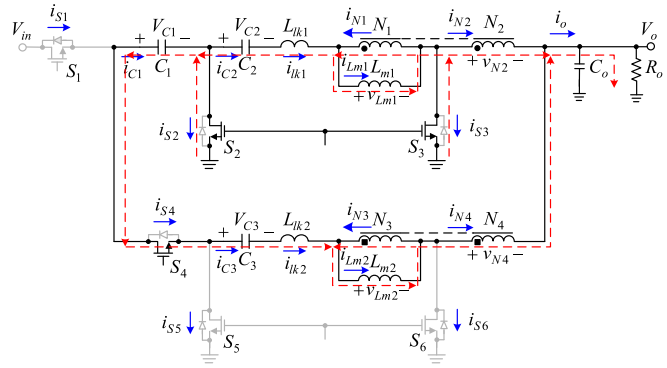

Fig. 9. Current flow in state 7.

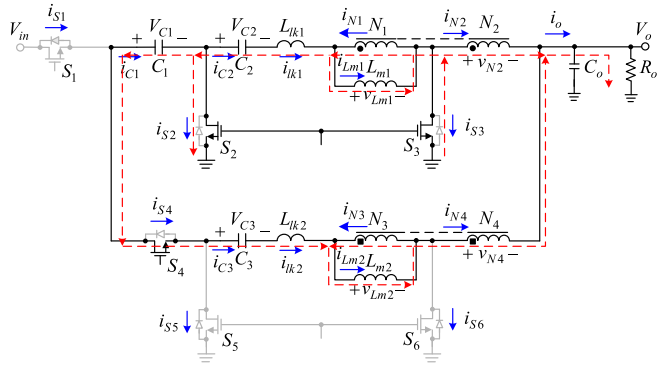

Fig. 10. Current flow in state 8.

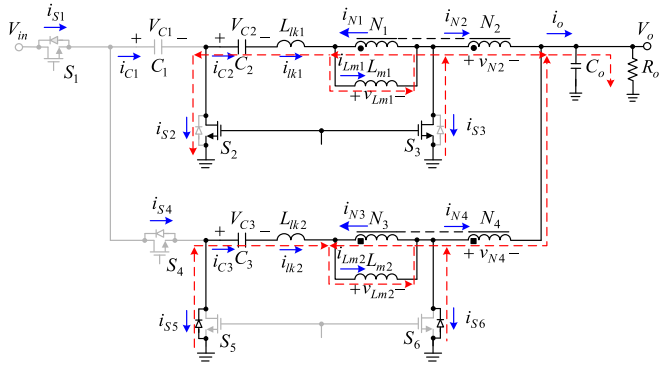

Fig. 11. Current flow in state 9.

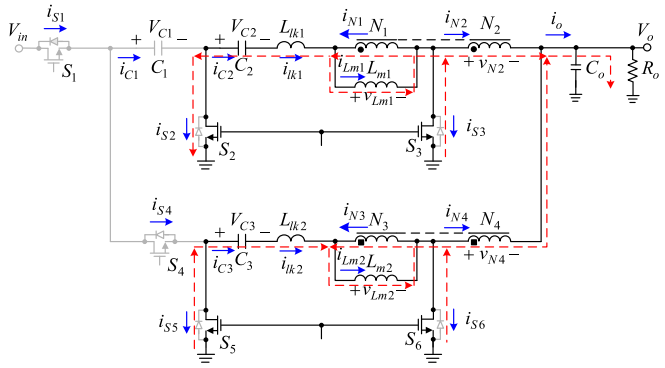

Fig. 12. Current flow in state 10.

7) State 7 (negative i_{lk1}) $[t_6 \le t \le t_7]$*:* As shown in Fig. 9, S_2, S_3, and S_4 are still ON, but S_1, S_5, and S_6 are still OFF. During this state, C_2 begins to be discharged with the current flowing through N_1 and N_2, pumping energy to the load. Hence, i_{N1} and i_{N2} are still increased continuously and L_{m1} is demagnetized due to the negative voltage across it. At the same time, C_1 is still discharged with the corresponding current charging C_3, passing energy to the load via N_3 and N_4. Therefore, i_{N3} and i_{N4} are increased continuously. In addition, L_{m2} and L_{lk2} are magnetized, and L_{lk1} is magnetized in the opposite direction.

8) State 8 (positive i_{S2}) $[t_7 \le t \le t_8]$*:* As shown in Fig. 10, S_2, S_3, and S_4 are still ON, but S_1, S_5, and S_6 are still OFF. The operation of this state is the same as that of state 7 except that C_2 is discharged via S_2 and C_1, pumping energy to the load. Once S_4 is OFF, the operating state goes to state 9.

9) State 9 (phase 2 blanking time) $[t_8 \le t \le t_9]$*:* As shown in Fig. 11, S_2 and S_3 are ON, but S_1, S_4, S_5, and S_6 are OFF. This state is the blanking time of phase 2. During this state, there is no energy stored in C_1. At the same time, C_3 is still charged, and L_{m2} and L_{lk2} are demagnetized, pumping energy to the load. Due to the continuity of i_{lk2}, the body diodes of S_5 and S_6 are turned ON. In addition, the operation of phase 1 is the same as state 8. Once S_5 and S_6 are ON, the operating state goes into state 10.

10) State 10 (S_5 and S_6 ZVS turn-on) $[t_9 \le t \le t_{10}]$*:* As shown in Fig. 12, S_2, S_3, S_5, and S_6 are ON, but S_1 and S_4 are OFF. During this state, S_5 and S_6 are turned ON with

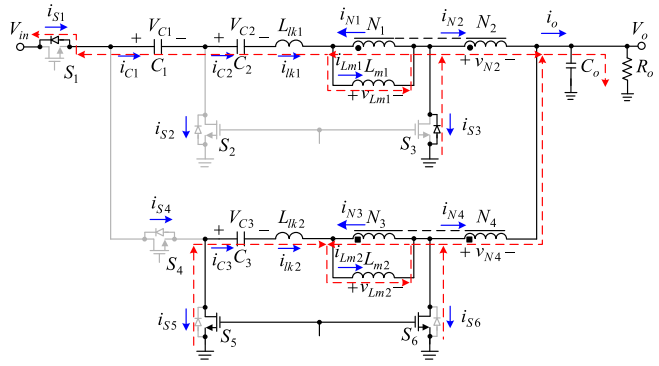

Fig. 13. Current flow in state 11.

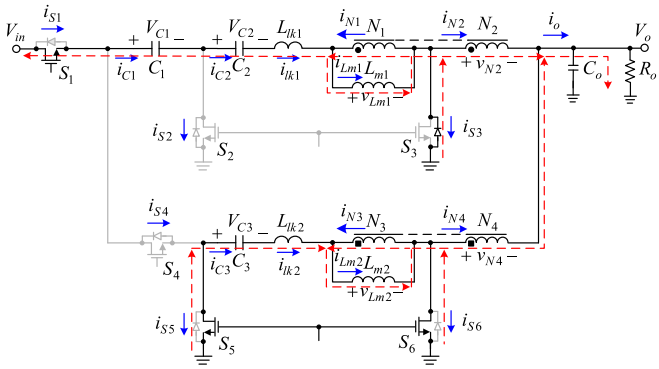

Fig. 14. Current flow in state 12.

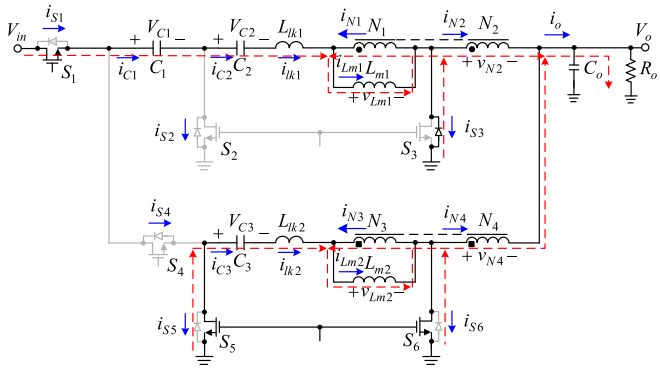

Fig. 15. Current flow in state 13.

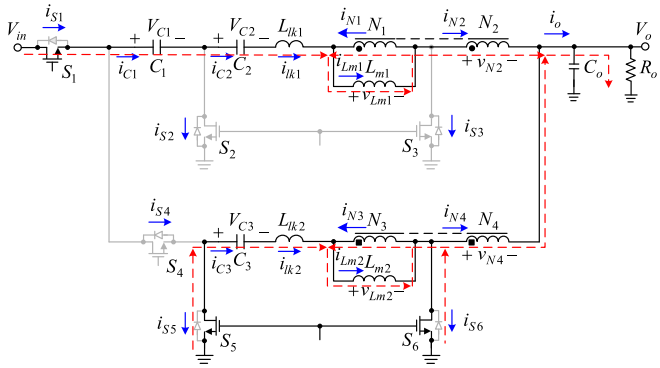

Fig. 16. Current flow in state 14.

ZVS. At the same time, C_3 is still charged, and L_{m2} and L_{lk2} are still demagnetized, pumping energy to the load. Moreover, the operation of phase 1 is the same as state 9.

11) State 11 (phase 1 blanking time) $[t_{10} \le t \le t_{11}]$*:* As shown in Fig. 13, S_5 and S_6 are ON, but S_1, S_2, S_3, and S_4 are OFF. This state is the blanking time of phase 1. At the same time, C_1 and C_2 begin to be discharged, with the currents flowing through the body diodes of S_1 and S_3, thereby causing the energy stored in L_{lk1} to be released to the input. L_{m1} is still demagnetized, and L_{lk1} is demagnetized in the opposite direction. Moreover, the operation of phase 2 is the same as state 10.

12) State 12 (S_1 ZVS turn-on) $[t_{11} \le t \le t_{12}]$*:* As shown in Fig. 14, S_1, S_5, and S_6 are ON, but S_2, S_3, and S_4 are off. S_1 is turned ON with ZVS. During this state, C_1 and C_2 are discharged. At the same time, L_{m1} is magnetized, and L_{lk1} is still demagnetized in the opposite direction. In addition, the operation of phase 2 is the same as state 11.

13) State 13 (positive i_{lk1}) $[t_{12} \le t \le t_{13}]$*:* As shown in Fig. 15, S_1, S_5, and S_6 are ON, but S_2, S_3, and S_4 are OFF. During this state, the input voltage begins to charge C_1 and C_2, and L_{m1} and L_{lk1} are magnetized. At the same time, the operation of phase 2 is the same as state 12. As soon as the current i_{S3} rises to zero, the operation goes into state 14.

14) Sate 14 (zero i_{S3}) $[t_{13} \le t \le t_{14}]$*:* As shown in Fig. 16, S_1, S_5, and S_6 are ON, but S_2, S_3, and S_4 are OFF. The operation of this state is the same as state 13 except that $i_{S3} = 0$.

TABLE I
BEHAVIOR OF C_1, C_2, AND C_3

State	1	2	3	4	5	6	7	8	9	10	11	12	13	14
C_1	C	i	i	c	d	d	d	d	i	i	d	d	c	c
C_2	C	c	c	c	c	c	d	d	d	d	d	d	c	c
C_3	D	d	d	d	c	c	c	c	c	c	c	c	c	c

TABLE II
BEHAVIOR OF S_2, S_3, S_5, AND S_6

State	1	2	3	4	5	6	7	8	9	10	11	12	13	14
S_2	n	s	s	s	s	s	s	r	r	r	n	n	n	n
S_3	n	s	s	s	s	s	s	s	s	s	s	s	s	n
S_5	r	r	r	n	n	n	n	n	s	s	s	s	s	s
S_6	s	s	s	s	s	n	n	n	s	s	s	s	s	s

In the following, Table I is used to further understand the behavior of the capacitors C_1, C_2, and C_3, where "c" implies "charge," "d" implies "discharge," and "i" implies "idle."

In addition, Table II is used to further understand the behavior of the SR switches, where "s" means "SR behavior with current flowing from source to drain," "r" means "regular MOSFET behavior with current flowing from drain to source," and "n" means "no current."

In order to obtain the voltage conversion ratio and the voltages across C_1, C_2, and C_3, the blanking times and the leakage inductances are ignored. Thus, only states 1 and 8 are taken into account.

From state 1, v_{Lm1} and v_{Lm2} can be expressed as

$$v_{Lm1} = (V_{\text{in}} - V_{C1} - V_{C2} - V_o) \cdot \frac{N_1}{N_1 + N_2} \tag{1}$$

$$v_{Lm2} = -V_{C3} = -V_o \cdot \left(\frac{N_3}{N_4}\right). \tag{2}$$

From state 8, v_{Lm2} and v_{Lm1} can be represented by

$$v_{Lm2} = (V_{C1} - V_{C3} - V_o) \cdot \frac{N_3}{N_3 + N_4} \tag{3}$$

$$v_{Lm1} = -V_{C2} = -V_o \cdot \left(\frac{N_1}{N_2}\right). \tag{4}$$

Based on (1) and (4), and by applying the volt–second balance to L_{m1}, the following equation can be obtained:

$$D \cdot (V_{\text{in}} - V_{C1} - V_{C2} - V_o) \cdot \left(\frac{N_1}{N_1 + N_2}\right) = (1 - D) \cdot V_o \cdot \left(\frac{N_1}{N_2}\right). \tag{5}$$

Similarly, based on (2) and (3) and by applying the volt–second balance to L_{m2}, the following equation can be obtained:

$$(1 - D) \cdot (V_{C1} - V_{C3} - V_o) \cdot \frac{N_3}{N_3 + N_4} = D \cdot V_o \cdot \left(\frac{N_3}{N_4}\right). \tag{6}$$

Based on (2), (4), (5), (6) and $N_2/N_1 = N_4/N_3$, the voltage V_{C1} can be obtained

$$V_{C1} = \frac{V_{\text{in}}}{2}. \tag{7}$$

By substituting (4) and (7) into (5), the voltage conversion ratio can be obtained to be

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{2} \cdot \left(\frac{N_2}{N_1 + N_2}\right). \tag{8}$$

From (8), it can be seen that the two-phase interleaved ultrahigh step-down converter has higher step-down voltage conversion ratio than that of the single-phase ultrahigh step-down converter [20].

C. Boundary Condition for L_{m1} and L_{m2}

The boundary condition for L_{m1} can be described as follows:

$$\begin{cases} 2I_{Lm1} \geq \Delta i_{Lm1}, & \text{for } L_{m1} \text{ operating without negative current} \\ 2I_{Lm1} < \Delta i_{Lm1}, & \text{for } L_{m1} \text{ operating with negative current} \end{cases} \tag{9}$$

where I_{Lm1} and Δi_{Lm1} are dc and ac components of i_{Lm1}.

For analysis convenience, it is assumed that the input power is equal to the output power and the load current is evenly distributed between the two phases. According to the volt–second balance for the coupled inductor and the ampere–second balance for the capacitor, the dc component of the voltage across the coupled inductor and the dc component of the current in the capacitor are zero, as shown in Figs. 17 and 18, respectively.

Therefore, the dc component of the secondary current i_{N2}, I_{N2}, is half of the dc component of i_o, I_o. Also, the dc

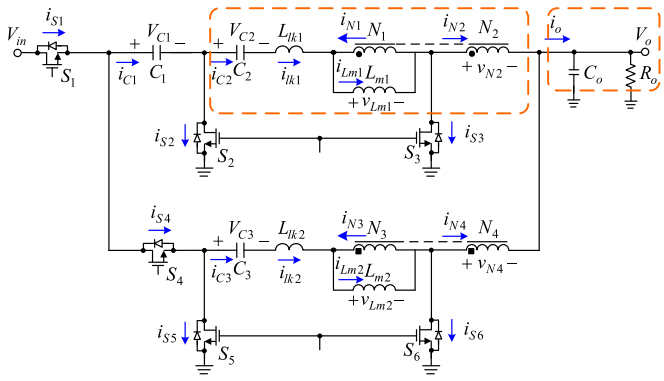

Fig. 17. Circled zones used to explain the relationship between I_{Lm1} and I_o.

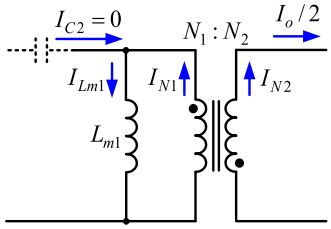

Fig. 18. Equivalent model for dc analysis of the coupled inductor.

component of the magnetizing current i_{Lm1}, I_{Lm1}, is equal to the dc component of the primary current i_{N1}, I_{N1}. That is

$$I_{N1} = \frac{N_2}{N_1} \cdot I_{N2} = \frac{N_2}{N_1} \cdot \frac{I_o}{2} \tag{10}$$

$$I_{Lm1} = I_{N1} = \frac{N_2}{N_1} \cdot \frac{I_o}{2} \tag{11}$$

where

$$I_o = \frac{V_o}{R_o}. \tag{12}$$

Substituting (12) into (11) yields

$$I_{Lm1} = I_{N1} = \frac{N_2}{N_1} \times \frac{V_o}{2R_o}. \tag{13}$$

1) Boundary condition for L_{m1}: The current ripple of i_{Lm1}, Δi_{Lm1}, can be represented by

$$\Delta i_{Lm1} = \frac{v_{Lm1}\Delta t}{L_{m1}} = \frac{\frac{N_1}{N_2} \times V_o \times (1 - D)T_s}{L_{m1}} = \frac{\frac{N_1}{N_1 + N_2} \times V_{\text{in}} \times \frac{D}{2} \times (1 - D)T_s}{L_{m1}}. \tag{14}$$

As $2I_{Lm1} \geq \Delta i_{Lm1}$, L_{m1} operates without negative current. Hence

$$\begin{aligned} & 2I_{Lm1} \geq \Delta i_{Lm1} \\ \Rightarrow & \frac{N_2}{N_1} \times \frac{V_o}{R_o} \geq \frac{\frac{N_1}{N_1 + N_2} V_{\text{in}} \times \frac{D}{2} \times (1 - D)T_s}{L_{m1}} \\ \Rightarrow & \frac{2L_{m1}}{R_o T_s} \geq 2\left(\frac{N_1}{N_2}\right)^2 (1 - D) \\ \Rightarrow & K_1 \geq K_{\text{crit1}}(D) \end{aligned} \tag{15}$$

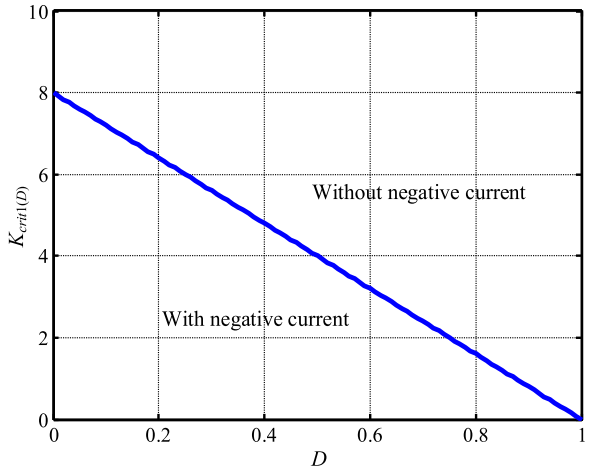

Fig. 19. Boundary curve for L_{m1} operating modes.

where $K_1 = \frac{2L_{m1}}{R_o T_s}$ and $K_{\text{crit1}}(D) = 2(\frac{N_1}{N_2})^2(1-D)$.

From (15), it can be seen that as $K_1 \geq K_{\text{crit1}}(D)$, L_{m1} operates without negative current; otherwise, L_{m1} operates with negative current. Accordingly, the corresponding boundary curve can be drawn as shown in Fig. 19, where $N_2/N_1 = 0.5$.

2) Boundary condition for L_{m2}: The analysis of the boundary condition for L_{m2} is the same as that for L_{m1}.

D. Analysis of Automatic Current Balance

The current balance can be achieved by applying the amp–second balance to the energy-transferring capacitor C_1. Therefore, the duty cycle $D\,(=D_1=D_2)$ should be smaller than 0.5.

Based on the converter operating principle in Section II–A, C_1 is charged during the time interval of D_1T_s and discharged during the time interval of D_2T_s. In the following analysis, the time intervals created from L_{lk1} and L_{lk2} are omitted. Accordingly, the associated current waveforms are shown in Fig. 20.

According to the converter operating principle shown in Section II–A and Fig. 20, it can be seen that during the time interval of D_1T_s, the current in C_1, $I_{C1,D1Ts}$, is the same as the current in N_2, $I_{N2,D1Ts}$. That is

$$I_{C1,D1Ts} = I_{N2,D1Ts} \tag{16}$$

where

$$\begin{aligned} I_{Lm1,D1Ts} &= I_{C1,D1Ts} + I_{N1,D1Ts} \\ &= I_{C1,D1Ts} + I_{N2,D1Ts}\frac{N_2}{N_1}. \end{aligned} \tag{17}$$

Substituting (16) into (17) yields

$$\begin{aligned} I_{Lm1,D1Ts} &= I_{C1,D1Ts} + I_{C1,D1Ts}\frac{N_2}{N_1} \\ &= I_{C1,D1Ts}\cdot\left(1+\frac{N_2}{N_1}\right). \end{aligned} \tag{18}$$

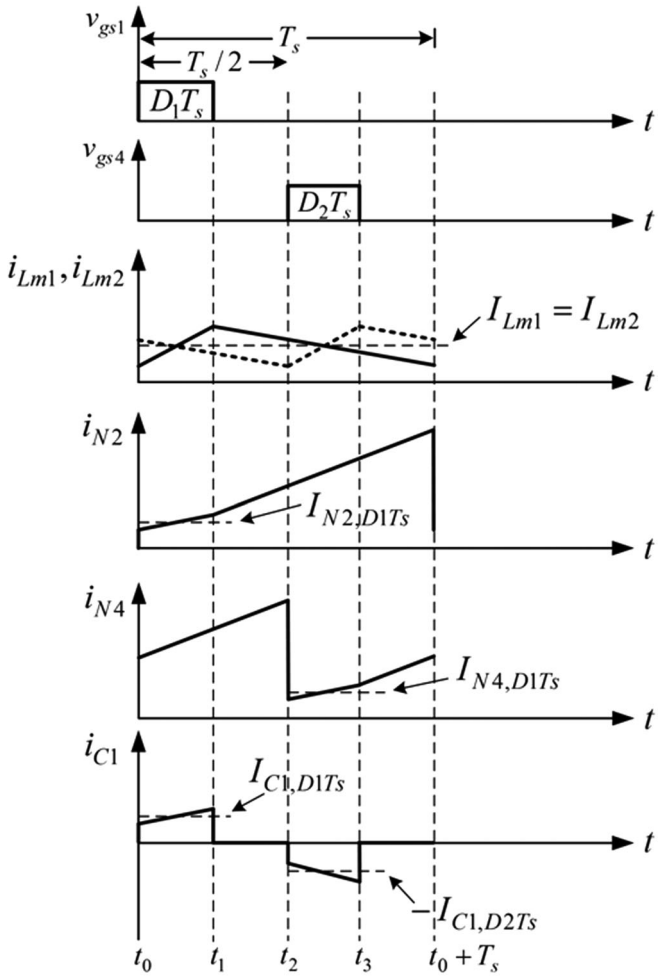

Fig. 20. Current waveforms related to the energy-transferring capacitor C_1 without considering leakage inductances.

Based on (18), the charging current $I_{C1,D1Ts}$ can be expressed by

$$\text{Charging}: \; I_{C1,D1Ts} = \frac{I_{Lm1,D1Ts}}{1+\frac{N_2}{N_1}}. \tag{19}$$

According to the converter operating principle shown in Section II–A and Fig. 20, it can be seen that during the time interval of D_2T_s, the current in C_1, $I_{C1,D2Ts}$, is the same as the current in N_4, $I_{N4,D2Ts}$. That is

$$I_{C1,D2Ts} = I_{N4,D2Ts} \tag{20}$$

where

$$\begin{aligned} I_{Lm2,D2Ts} &= I_{C1,D2Ts} + I_{N3,D2Ts} \\ &= I_{C1,D2Ts} + I_{N4,D2Ts}\frac{N_4}{N_3}. \end{aligned} \tag{21}$$

Substituting (20) into (21) yields

$$\begin{aligned} I_{Lm2,D1Ts} &= I_{C1,D2Ts} + I_{C1,D2Ts}\frac{N_4}{N_3} \\ &= I_{C1,D2Ts}\cdot\left(1+\frac{N_4}{N_3}\right). \end{aligned} \tag{22}$$

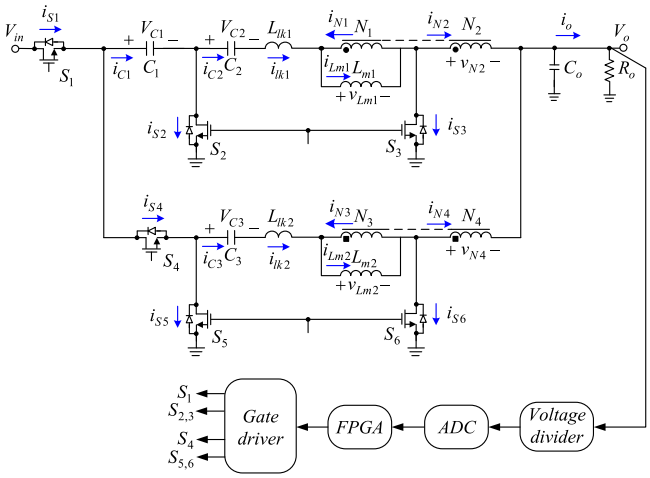

Fig. 21. Overall system under voltage-mode control.

During the time interval of D_2T_s, the discharging current $-I_{C1,D2Ts}$ can be expressed by

$$\text{Discharging}: \quad -I_{C1,D2Ts} = -\frac{I_{Lm2,D2Ts}}{1+\frac{N_4}{N_3}}. \tag{23}$$

By applying the amp–second balance to C_1, the following equation can be obtained:

$$I_{C1,D1Ts} - I_{C1,D2Ts} = 0. \tag{24}$$

Based on (19), (23), (24), $D_1 = D_2 = D$ and $N_2/N_1 = N_4/N_3$, the following equation can be obtained:

$$I_{Lm1,D1Ts} = I_{Lm2,D2Ts}. \tag{25}$$

Namely,

$$I_{Lm1} = I_{Lm2}. \tag{26}$$

By substituting (11) into (26), the following equation can be obtained:

$$I_{Lm1} = I_{Lm2} = \frac{N_2}{N_1} \cdot \frac{I_o}{2}. \tag{27}$$

According to (27), it can be found that the load current can be evenly distributed between the two phases.

III. Overall System

Fig. 21 shows the overall system, containing the main power stage and the feedback circuit. The main power stage is the proposed two-phase interleaved ultrahigh step-down converter whose operating principle has been mentioned in Section II–A. In the following, only the operation of the feedback circuit is described. The analogue output voltage is obtained by the voltage divider. Afterward, this obtained voltage is sent to the analogue-to-digital converter and then converted to the digital signal. The digital signal is sent to the field-programmable gate array (FPGA) and then calculated so that the corresponding gate driving signals are created. Therefore, the output voltage can be kept almost constant at a desired value all over the load range.

The parameters of the proportional-integral controller embedded in the FPGA are obtained by offline tuning, which is widely used in the industry. There are three steps to be mentioned as follows:

1) Step 1: The proportional gain k_p is tuned from zero to the value which makes the output voltage close to about 80% of the desired value. Hence, the value of k_p is chosen to be 6 temporarily.

2) Step 2: The integral gain k_i is also tuned from zero to the value which makes the output voltage very close to the desired value. Hence, the value of k_i is chosen to be 0.5 temporarily.

3) Step 3: Afterward, the values of k_p and k_i are checked and modified from the light load to the rated load. Finally, the value of k_p is set at 5 and k_i is set at 0.8.

TABLE III
System Specifications

Operating mode	Without negative current
Input voltage (V_{in})	400 V
Output voltage (V_o)	24 V
Rated output current ($I_{o,\text{rated}}$)	10 A
Minimum output current ($I_{o,\text{min}}$)	2 A
Switching frequency (f_s)/period (T_s)	100 kHz/10 μs

TABLE IV
Component Specifications

Components		Specifications
MOSFETs	S_1, S_2, S_5	IRFB4137PbF
	S_4	FCPF20N60
	S_3, S_6	IRFB4227PbF
Energy-transferring capacitors	C_1	33-μF/250-V Rubycon electrolytic capacitor
	C_2, C_3	10-μF/50-V MLCC capacitor
Output capacitor	C_o	470-μF/50-V electrolytic capacitor
Coupled inductor		Core: PQ26/25-3C90 $N_1 : N_2 = N_3 : N_4 = 2:1$ $L_{m1} = L_{m2} = 398\ \mu H$ $L_{lk1} = L_{lk2} = 1.15\ \mu$H
Gate drivers	S_1, S_4	TLP250
	S_2, S_3, S_5, S_6	TC4420

IV. Design Considerations

In order to demonstrate the effectiveness of the proposed two-phase interleaved ultrahigh step-down converter, a prototype was build up and tested. The system specifications are shown in Table III, and the component specifications are shown in Table IV.

A. Design of Turns Ratio

From (8), the duty cycle $D\,(=D_1=D_2)$ can be expressed by

$$D = \frac{2(N_1+N_2)V_o}{N_2 V_{\text{in}}}. \tag{28}$$

It is assumed that D locates between 0.3 and 0.4. Substituting the system specifications shown in Table III into (28)

yields

$$0.3 \le \frac{2(N_1+N_2)V_o}{N_2 V_{\text{in}}} \le 0.4$$
$$\Rightarrow 0.3 \le \frac{2\times(N_1+N_2)\times 24}{N_2\times 400} \le 0.4$$
$$\Rightarrow 2.5 \le \frac{N_1+N_2}{N_2} \le 3.33. \quad (29)$$

According to (29) and taking $N_1 : N_2 = 2:1$, the turns ratio *n* is

$$n = \frac{N_1}{N_2} = 2. \quad (30)$$

By substituting (30) and the system specifications shown in Table III into (28), the duty cycle *D* can be figured out to be

$$D = \frac{2(N_1+N_2)V_o}{N_2 V_{\text{in}}} = \frac{2\times(2+1)\times 24}{1\times 400} = 0.36. \quad (31)$$

B. Calculation of Magnetizing Inductances L_{m1} and L_{m2}

Based on (15), if the magnetizing inductors operate without negative current, the value of L_{m1} should satisfy the following criterion:

$$L_{m1} \ge 2\left(\frac{N_1}{N_2}\right)^2 (1-D)\times\frac{R_{o,\max}T_s}{2}$$
$$\Rightarrow L_{m1} \ge \left(\frac{N_1}{N_2}\right)^2 (1-D)\times\frac{V_o}{I_{o,\min}}\times T_s. \quad (32)$$

By substituting (30), (31) and the specifications shown in Table III into (32), the value range of L_{m1} can be obtained to be

$$L_{m1} \ge 2\left(\frac{2}{1}\right)^2 (1-0.36)\times\frac{24}{2}\times 10\ \mu\text{H}$$
$$\Rightarrow L_{m1} \ge 307.2\ \mu\text{H}. \quad (33)$$

Finally, the values of L_{m1} and L_{m2} are measured to be 398 μH.

C. ZVS Criteria for S_2, S_3, S_5, and S_6

In the proposed converter, the switches S_2, S_3, S_5, and S_6 function as SR switches to do freewheeling. This behavior is similar to the low-side switch of the traditional SR buck converter, which inherently possesses ZVS turn-on.

D. ZVS Criteria for S_1 and S_4

From Fig. 2 and state 11 in Section II–A, it can be seen that in this state, the minimum value of i_{lk1} called $I_{lk1,\min}$ should be satisfied with the following equation:

$$\frac{1}{2}L_{lk1}I_{lk1,\min}^2 \ge \frac{1}{2}C_{\text{oss1}}V_{ds1}^2 \Rightarrow |I_{lk1,\min}| \ge \sqrt{\frac{C_{\text{oss1}}}{L_{lk1}}}V_{ds1}. \quad (34)$$

Based on the IRFB4137PbF datasheet and $V_{ds1} = 200$ V, the value of C_{oss1} is estimated to be 170 pF. Also, the value is measured to be 1.15 μH. Therefore, based on (34), the criterion of $|I_{lk1,\min}|$ can be obtained to be

$$|I_{lk1,\min}| \ge \sqrt{\frac{170\ pF}{1.15\ \mu\text{H}}}\times 200 \approx 2.43A. \quad (35)$$

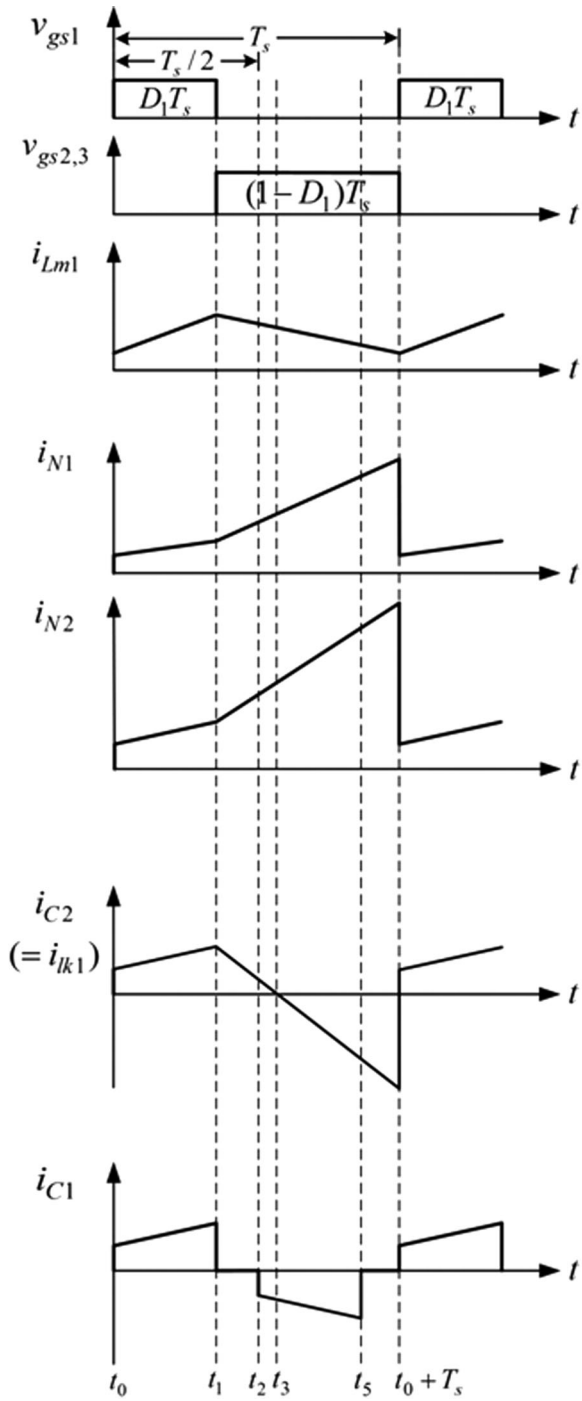

Fig. 22. Key waveforms for phase 1 without leakage inductors and blanking times considered.

For calculation convenience in the following, the leakage inductors and blanking times are negligible so the number of operating states can be reduced to 5, as shown in Fig. 22. In Fig. 22, only the key waveforms of phase 1 are taken into

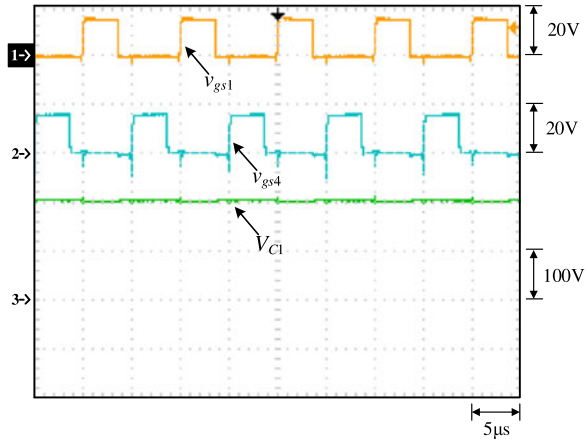

Fig. 23. Measured waveforms: (1) v_{gs1}; (2) v_{gs4}; and (3) V_{C1}.

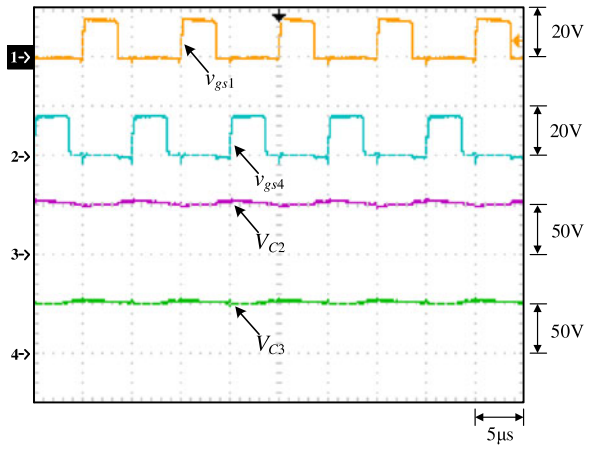

Fig. 24. Measured waveforms: (1) v_{gs1}; (2) v_{gs4}; (3) V_{C2}; and (4) V_{C3}.

consideration. At the end of state 5 (from t_4 to $t_0 + T_s$), the relationship between i_{lk1}, i_{Lm1}, and i_{N1} is

$$i_{lk1} = i_{Lm1} - i_{N1}. \tag{36}$$

Therefore

$$|I_{lk1,\min}| = I_{N1,\max} - I_{Lm1,\min}. \tag{37}$$

Based on Fig. 22, at rated load, the values of $I_{N1,\max,\text{rated}}$ and $I_{Lm1,\min,\text{rated}}$ can be figured out after complicated calculations to be 5.88 and 2 A, respectively. Hence, the value of $|I_{lk1,\min,\text{rated}}|$ can be obtained to be

$$\begin{aligned} |I_{lk1,\min,\text{rated}}| &= I_{N1,\max,\text{rated}} - I_{Lm1,\min,\text{rated}} \\ &= 5.88 - 2 = 3.88A. \end{aligned} \tag{38}$$

The minimum blanking time called $t_{b,\min}$ should be also taken into account to achieve ZVS of S_1. The value of $t_{b,\min}$ can be found to be

$$\begin{aligned} t_{b,\min} &= 0.5\pi\sqrt{L_{lk1}C_{\text{oss1}}} = 0.5\pi\sqrt{1.15\ \mu\text{H} \times 170\ \text{pF}} \\ &= 21.95\ \text{ns}. \end{aligned} \tag{39}$$

However, the shoot-through issue should be taken into account, and finally, the value of the blanking time is selected to be 150 ns.

Based on the fact that the chosen blanking time is larger than the value shown in (39), and the value shown in (38) is larger than the value shown in (35), it is known that the ZVS turn-on of S_1 can be realized at rated load. By the same way, we can know that the criterion for S_4 to achieve ZVS turn-on at rated load is the same as that for S_1.

V. Experimental Results

At rated load, Fig. 23 shows the gate driving signals for S_1 and S_4 called v_{gs1} and v_{gs4} and the voltages across C_1 called V_{C1}. Fig. 24 shows the gate driving signals for S_1 and S_4 called v_{gs1} and v_{gs4} and the voltages across C_2 and C_3 called V_{C2} and V_{C3}. Fig. 25 shows the gate driving signals for S_1 and S_4 called v_{gs1} and v_{gs4} and the currents in L_{lk1} and L_{lk2} called i_{lk1} and i_{lk2}. Fig. 26 shows the gate driving signals

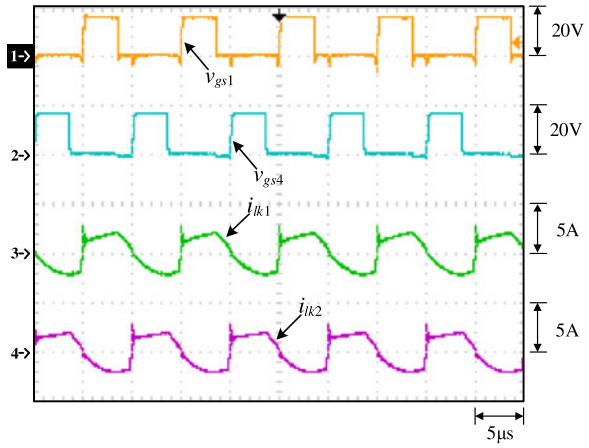

Fig. 25. Measured waveforms: (1) v_{gs1}; (2) v_{gs4}; (3) i_{lk1}; and (4) i_{lk2}.

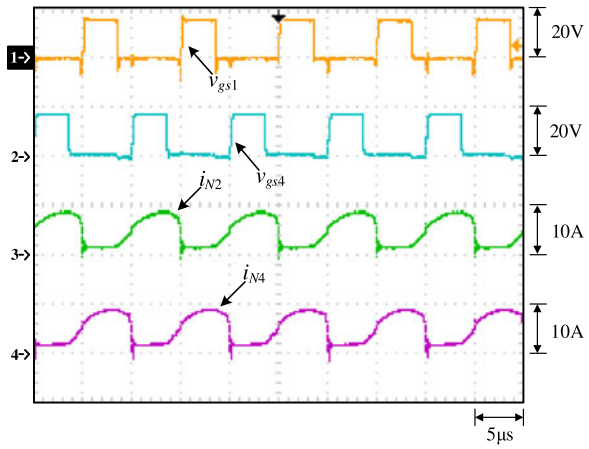

Fig. 26. Measured waveforms: (1) v_{gs1}; (2) v_{gs4}; (3) i_{N2}; and (4) i_{N4}.

for S_1 and S_4 called v_{gs1} and v_{gs4} and the currents in N_2 and N_4 called i_{N2} and i_{N4}. Fig. 27 shows the gate driving signals for S_1 and S_4 called v_{gs1} and v_{gs4} and the output current i_o. Fig. 28 shows the input voltage V_{in} and the output voltage V_o. Fig. 29 shows the ZVS turn-on of S_1. Fig. 30 shows the ZVS turn-on of S_2. Fig. 31 shows the ZVS turn-on of S_3. Fig. 32 shows the

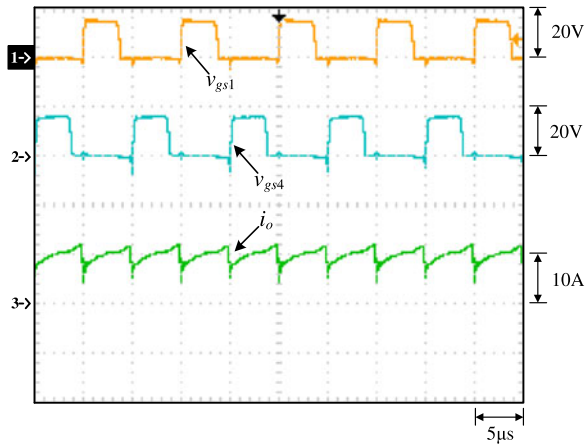

Fig. 27. Measured waveforms: (1) v_{gs1}; (2) v_{gs4}; and (3) i_o.

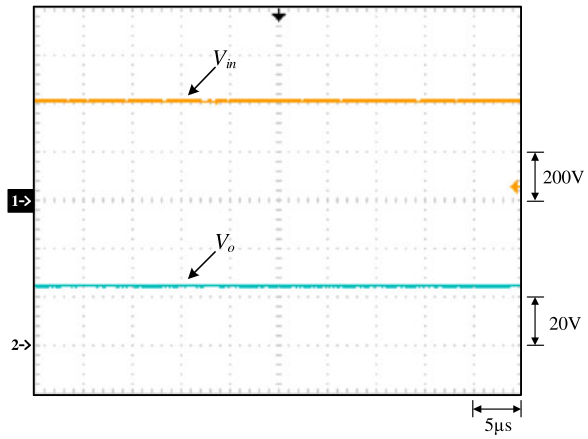

Fig. 28. Measured waveforms: (1) $V_{\rm in}$ and (2) V_o.

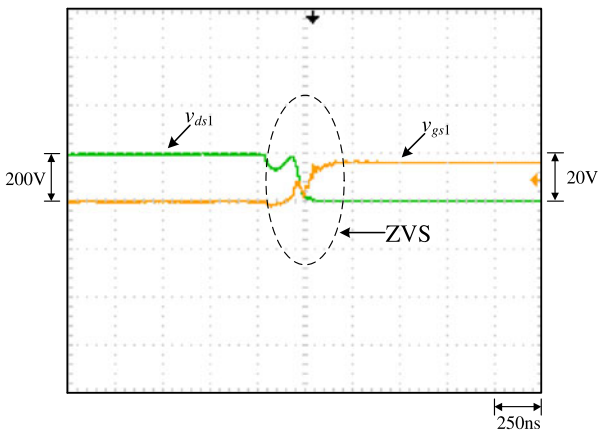

Fig. 29. Turn-on transient of $\rm S_1$: (1) v_{gs1} and (2) v_{ds1}.

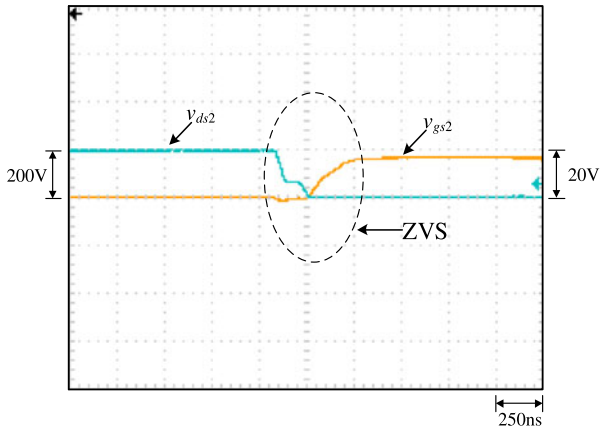

Fig. 30. Turn-on transient of $\rm S_2$: (1) v_{gs2} and (2) v_{ds2}.

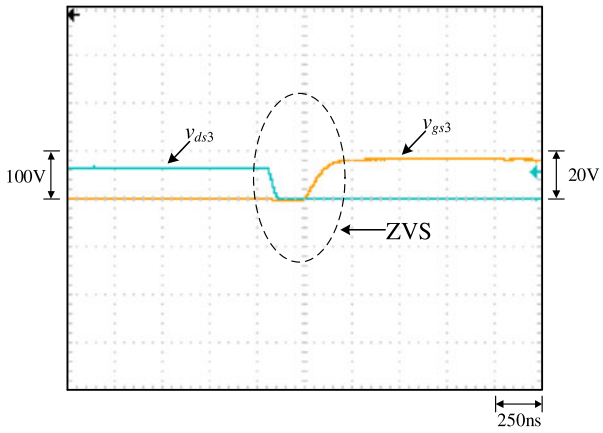

Fig. 31. Turn-on transient of S_3: (1) v_{gs3} and (2) v_{ds3}.

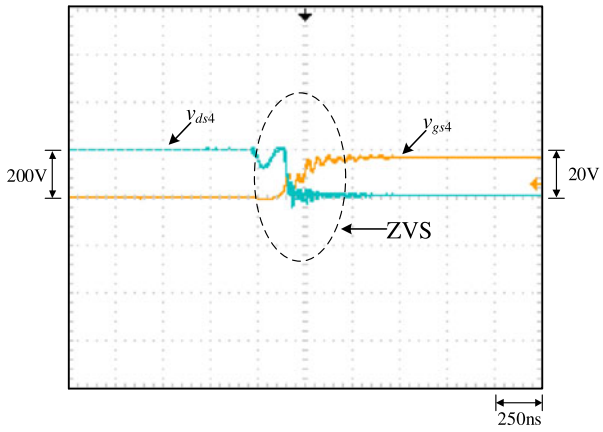

Fig. 32. Turn-on transient of $\rm S_4$: (1) v_{gs4} and (2) v_{ds4}.

ZVS turn-on of $\rm S_4$. Fig. 33 shows the ZVS turn-on of $\rm S_5$. Fig. 34 shows the ZVS turn-on of $\rm S_6$. Fig. 35 shows a curve of efficiency versus load current.

From Figs. 23 and 24, it can be seen that the values of V_{C1}, V_{C2}, and V_{C3} are about 200, 48, and 48 V, respectively, corresponding to the theoretical values. From Fig. 25, it can be seen that the leakage inductor currents of two phases called i_{lk1} and i_{lk2} are almost identical except for phase difference of 180°, whereas from Fig. 26, it can be seen that the output currents of two phases called i_{N2} and i_{N4} are almost identical except for phase difference of 180°. From Fig. 27, it can be seen that the output current i_o is the sum of i_{N2} and i_{N4} and has double the frequency of i_{N2} or i_{N4}. From Fig. 28, it can be seen that the value of V_o is 24 V, corresponding to the system specifications. From Figs. 29 to 34, all the switches have ZVS

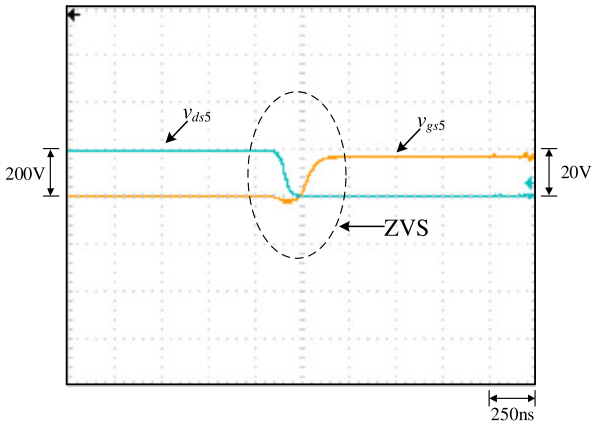

Fig. 33. Turn-on transient of S_5: (1) v_{gs5} and (2) v_{ds5}.

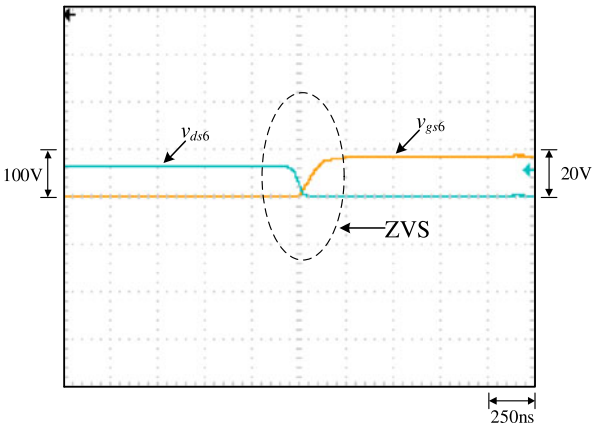

Fig. 34. Turn-on transient of S_6: (1) v_{gs6} and (2) v_{ds6}.

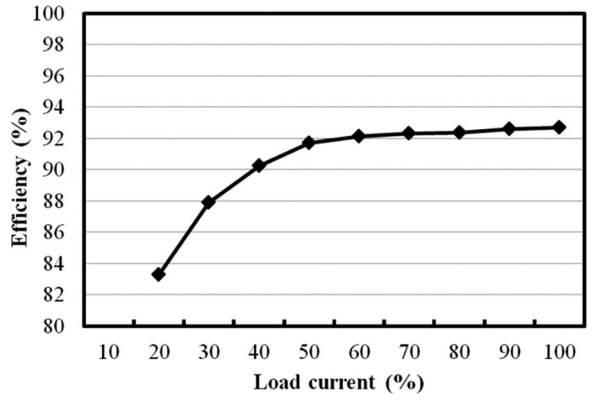

Fig. 35. Curve of efficiency versus load current.

turn-on and lower voltage stresses than the traditional buck converter. Since a parasitic inductance exists between the source of S_1 and the ground and resonates with the input capacitance plus output capacitance of S_1, the waveforms of v_{gs1} and v_{ds1} have voltage rings, as shown in Fig. 29. This phenomenon can also be found in the waveforms of v_{gs4} and v_{ds4} for S_4, as shown in Fig. 32.

From Fig. 35, it can be seen that the efficiency is above 83.3% all over the load range, and the efficiency can be up to 92.7%. The efficiency distribution in Fig. 35 is to be described

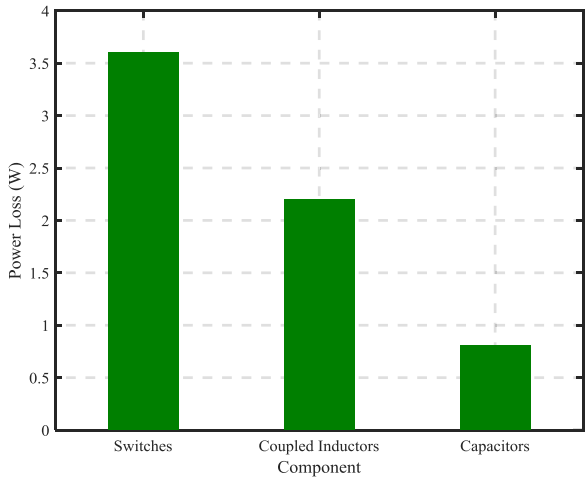

Fig. 36. Loss breakdown at rated load.

as follows. The efficiency can be expressed as

$$\eta = \frac{P_o}{P_i} \times 100\% = \frac{P_o}{P_o + P_l} \times 100\% \tag{40}$$

where P_o is the output power, P_i is the input power, and P_l is the power loss, which contains conduction loss, switching loss, core loss, and stray loss.

In Fig. 35, below the half load, the efficiency is mainly influenced by relatively high switching loss and increases as the load goes up, whereas above the half load, the efficiency is mainly influenced by relatively low switching loss and increases as the load goes up. Fig. 36 shows the loss breakdown at rated load. From Fig. 36, it can be seen that the largest power loss comes from switches mainly due to the turn-off switching loss and the circulating current conduction loss.

VI. Discussion

A. Relationship Between D and k

In the proposed converter, the value of *k* also influences the voltage conversion ratio. This can be seen as follows:

$$\frac{V_o}{V_i} = \frac{D}{k} \cdot \frac{1}{1 + \frac{N_1}{N_2}}. \tag{41}$$

According to (41), we can see that under the same voltage gain and turns ratio, the more the value of *k*, the larger the value of *D*. This renders the duty cycle not too small, thereby making the converter easy of control as well as free from the noise interruption.

On the other hand, the maximum duty cycle $D_{\max}$ can be expressed to be

$$D_{\max} = \frac{1}{k}. \tag{42}$$

Based on (42), we can see that the more the value of *k*, the smaller the value of $D_{\max}$. Hence, if the transient responses are taken into account, the value of *k* would be limited to some extent.

In this paper, the value of *k* is 2, and, hence, the corresponding voltage conversion ratio, with the maximum duty cycle limited

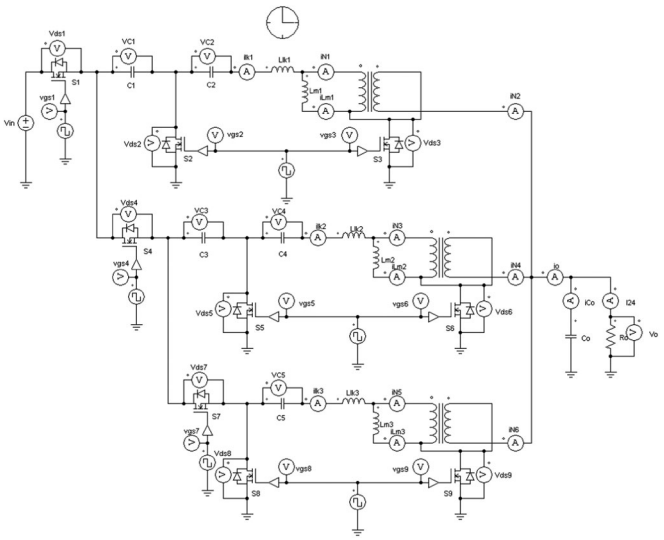

Fig. 37. Simulation of the three-phase converter.

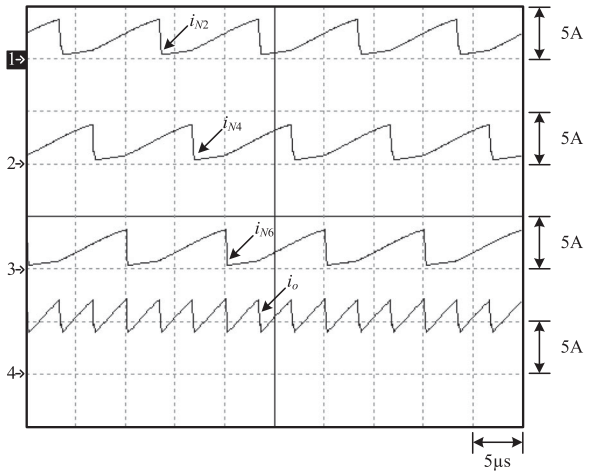

Fig. 38. Simulated waveforms: (1) i_{N2}; (2) i_{N4}; (3) i_{N6}; and (4) i_o.

to 0.5, can be represented by

$$\frac{V_o}{V_i} = \frac{D}{2} \cdot \frac{1}{1 + \frac{N_1}{N_2}}. \tag{43}$$

As the proposed converter is expanded to three phases, as shown in Fig. 37, the corresponding voltage conversion ratio, with the maximum duty cycle limited to 0.33, can be expressed by

$$\frac{V_o}{V_i} = \frac{D}{3} \cdot \frac{1}{1 + \frac{N_1}{N_2}}. \tag{44}$$

By taking $D = 0.3$ and $N_1/N_2 = 2$, the output voltage is calculated out to be 13.3 V based on (44). By simulation, Fig. 38 shows the output currents of three phases called i_{N2}, i_{N4}, and i_{N6}. From Fig. 38, it can be seen that the currents i_{N2}, i_{N4}, and i_{N6} are almost identical except a phase difference of 120° for any two adjacent phases. Also, from Fig. 38, it can be seen that the output current i_o is the sum of i_{N2}, i_{N4}, and i_{N6} and has triple the frequency of i_{N2}, i_{N4}, or i_{N6}. Fig. 39 shows the

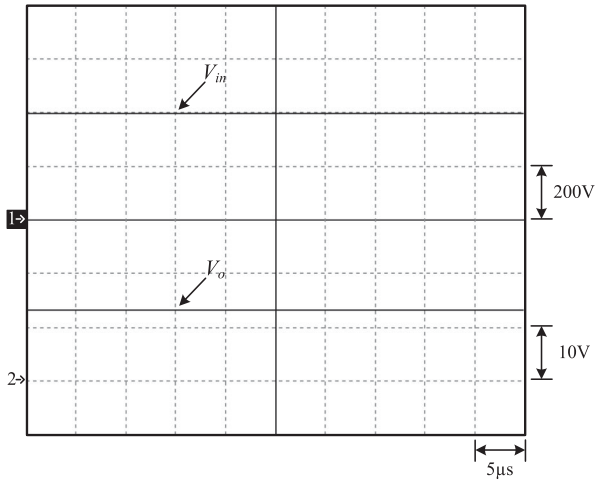

Fig. 39. Simulated waveforms: (1) $V_{\rm in}$ and (2) V_o.

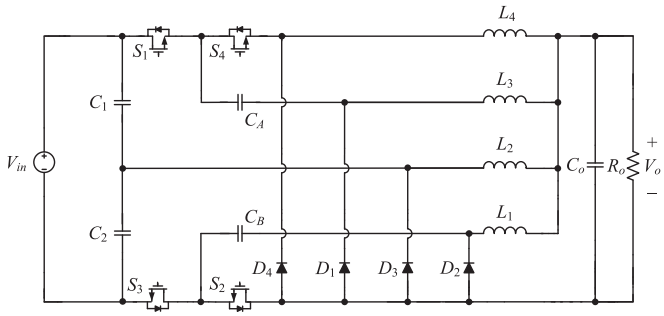

Fig. 40. Step-down circuit in [21] as a comparison.

input voltage and the corresponding output voltage, about 400 and 13.3 V, respectively.

B. Converter Comparison

Although the component count and circuit size of the proposed converter increase due to two phases, the proposed converter inherently possesses not only the advantages of the interleave structure, meaning that the output ripple frequency and the output current handling capability can be increased, but also the voltage conversion ratio of the proposed converter is half of that of the converter shown in [20], meaning that the duty cycle of the proposed converter can be enlarged under the same voltage conversion ratio and turns ratio as compared with the converter shown in [20].

In the following, an efficiency comparison between the existing circuit shown in Fig. 40 [21] and the proposed circuit shown in Fig. 41 is made. Both circuits have the same system specifications: input voltage of 400 V, output voltage of 24 V, and switching frequency of 100 kHz. In addition, the component specifications for the compared converter are shown in Table V, whereas the component specifications for the proposed converter are shown in Table VI.

From Fig. 42, it can be seen that the compared converter has better efficiency performance than the proposed converter except the rated load. At light load, the proposed converter has

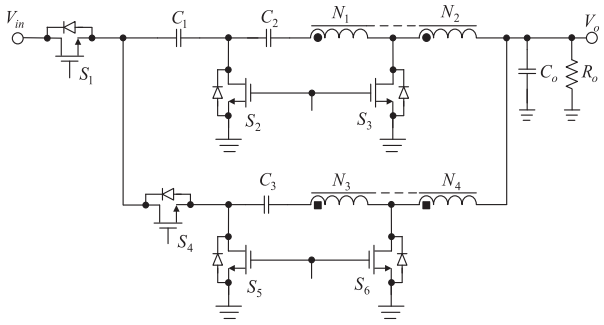

Fig. 41. Proposed step-down circuit.

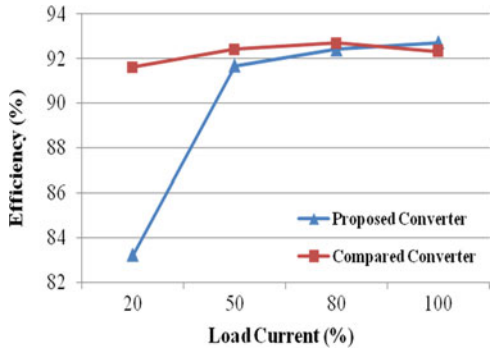

Fig. 42. Curves of efficiency versus load current for the compared and proposed converters.

TABLE V
COMPONENT SPECIFICATIONS FOR THE COMPARED CONVERTER

Components		Specifications
MOSFETs	S_1, S_3, S_4	IXFH100N25P
	S_2	IXFH150N15P
Diodes	D_1, D_2, D_3, D_4	DSSK60-02A
Blocking Capacitors	C_A, C_B	10-μF/250-V MLCC capacitor
Input Capacitors	C_1, C_2	10-μF/250-V MLCC capacitor
Output Capacitor	C_o	220-μF/250-V electrolytic capacitor
Inductors		Core: M467060 $L_1 = L_2 = L_3 = L_4 = 250$ μH

TABLE VI
COMPONENT SPECIFICATIONS FOR THE PROPOSED CONVERTER

Components		Specifications
MOSFETs	S_1, S_2, S_5	IRFB4137PbF
	S_4	FCPF20N60
	S_3, S_6	IRFB4227PbF
Energy-Transferring Capacitors	C_1	33-μF/250-V electrolytic capacitor
	C_2, C_3	10-μF/50-V MLCC capacitor
Output Capacitor	C_o	470-μF/50-V electrolytic capacitor
Coupled Inductors		Core: PQ26/25-3C90
		$n = 2$, $L_{m1} = 398$ μH, $L_{lk1} = 1.15$ μH
		$n = 2$, $L_{m2} = 398$ μH, $L_{lk2} = 1.15$ μH

much worse efficiency performance than the compared converter due to switching losses. As generally recognized, the circuit efficiency is determined by component selection, layout structure, power level, etc. Basically, the proposed circuit has relatively low efficiency at light load. Hence, how to improve the light-load efficiency will be further studied in the future.

However, as compared with the converter shown in [21], some main merits of the proposed converter can be seen from the voltage conversion ratio as shown.

The voltage conversion ratio of the compared converter is

$$\frac{V_o}{V_i} = \frac{D}{4} \tag{45}$$

and the voltage conversion ratio of the proposed converter is

$$\frac{V_o}{V_i} = \frac{D}{2}\left(\frac{N_2}{N_1 + N_2}\right). \tag{46}$$

According to the system specifications, if $N_1 = 2$ and $N_2 = 1$, the corresponding duty cycle for the compared and proposed converters are 0.24 and 0.36, respectively, but if the output voltage is assumed to be 6 V and $N_1 = 4$ and $N_2 = 1$, the resulting duty cycles are 0.06 and 0.15 for the compared and proposed converters, respectively. Thus, the control of the compared converter would be harder than that of the proposed converter due to smaller duty cycle.

Furthermore, the proposed converter has the smaller number of components than the compared converter by 5 if the coupling inductor is considered as one component. In addition, the proposed converter has the smaller number of isolated gate drivers than the compared converter by 3, and the ground of the compared converter is separated so the isolated device is needed to sense the output voltage.

Above all, in the proposed circuit, the capacitors C_1, C_2, and C_3 possess functions of high-voltage isolation. As the switchs S_1 or S_4 are shorted for some time, no high input voltage is imposed on the load. That is, the proposed circuit has an inherent advantage of high safety for the load.

VII. CONCLUSION

In this paper, the two-phase interleaved ultrahigh step-down converter is presented. Due to the capacitor C_1, the load current can be evenly distributed among the two phases as well as a higher step-down voltage gain can be achieved. Moreover, the operating principle, coupled inductor analysis, and automatic current balance principle of the proposed converter are described. Finally, a prototype with the input voltage of 400 V, the output voltage of 24 V, and the output current of 10 A is built up and tested. The experimental results show that the key waveforms match the theoretical analyses, and automatic current balance and ZVS turn-on can be achieved. Above all, the proposed two-phase converter can be extended to *k* phases, where *k* is 3 or more, and the step-down voltage conversion ratio will be decreased further as the value of *k* is increased further.

REFERENCES

[1] D. Sigmund, A. Lohner, and M. Boh, "Simulation-based development of an energy-management-system for a drive train of a parallel hybrid electric vehicle," in *Proc. IEEE Power Electron. Motion Control Conf.*, 2014, pp. 822–827.

[2] Y. Hu, C. Gan, W. Cao, C. Li, and S. J. Finney, "Split converter-fed SRM drive for flexible charging in EV/HEV applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6085–6095, Oct. 2015.

[3] Y. Ren, M. Xu, K. Yao, Y. Meng, F. C. Lee, and J. Guo, "Two-stage approach for 12 V VR," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, vol. 2, pp. 1306–1312.
[4] Y. Ren, M. Xu, K. Yao, and F. C. Lee, "Two-stage 48 V power pod exploration for 64-bit microprocessor," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, vol. 1, pp. 426–431.
[5] Y. Ren, M. Xu, Y. Meng, and F. C. Lee, "12 V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 2635–2641.
[6] H. Mao, J. A. Abu-Qahouq, S. Luo, and I. Batarseh, "Zero-voltage-switching (ZVS) two-stage approaches with output current sharing for 48 V input DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, vol. 2, pp. 1078–1082.
[7] K. Yao, M. Ye, M. Xu, and F. C. Lee, "Tapped-inductor buck converter for high-step-down DC-DC conversion," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 775–780, Jul. 2005.
[8] D. A. Grant, Y. Darroman, and J. Suter, "Synthesis of tapped-inductor switched-mode converters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1964–1969, Sep. 2007.
[9] S. Ye, W. Eberle, and Y. F. Liu, "A novel non-isolated full bridge topology for VRM applications," *IEEE Trans. Ind. Electron.*, vol. 23, no. 1, pp. 427–437, Jan. 2008.
[10] K. Nishijima, D. Ishida, K. Harada, T. Nabeshima, T. Sato, and T. Nakano, "A novel two-phase buck converter with two cores and four windings," in *Proc. IEEE Telecommun. Energy Conf.*, 2007, pp. 861–866.
[11] P. Xu, J. Wei, and F. C. Lee, "The active-clamp couple-buck converter—A novel high efficiency voltage regulator modules," in *Proc. IEEE Appl. Power Electron. Conf.*, 2001, vol. 1, pp. 252–257.
[12] K. W. E. Cheng, "Tapped inductor for switched-mode power converters," in *Proc. IEEE Power Electron. Syst. Appl. Conf.*, 2006, pp. 14–20.
[13] H. L. Do, "Zero-voltage-switching synchronous buck converter with a coupled inductor," *IEEE Trans. Power Electron.*, vol. 58, no. 8, pp. 3440–3447, Aug. 2011.
[14] P. Xu, J. Wei, and F. C. Lee, "Multiphase coupled-buck converter—A novel high efficient 12 V voltage regulator module," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 74–82, Jan. 2003.
[15] F. Marvi, E. Adib, and H. Farzanehfard, "Interleaved zero voltage switching coupled inductor buck converter for low voltage-high current applications," in *Proc. IEEE Power Electron., Drive Syst. Technol. Conf.*, 2013, pp. 236–241.
[16] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "Interleaved buck converter with continuous input current, extremely low output current ripple, low switching losses, and improved step-down conversion ratio," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1474–1485, Aug. 2015.
[17] K. Matsumoto, K. Nishijima, T. Sato, and T. Nabeshima, "A two-phase high step down coupled-inductor converter for next generation low voltage CPU," in *Proc. IEEE Int. Conf. Power Electron. ECCE ASIA*, 2011, pp. 2813–2818.
[18] C.-T. Tsai and C.-L. Shen, "Interleaved soft-switching buck converter with coupled inductors," in *Proc. IEEE Int. Conf. Sustainable Energy Technol.*, 2008, pp. 877–882.
[19] H. Cheng, K. M. Smedley, and A. Abramovitz, "A wide-input-wide-output (WIWO) DC-DC converter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 280–289, Feb. 2010.
[20] K. I. Hwu, W. Z. Jiang, and Y. T. Yau, "Ultrahigh step-down converter," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3262–3274, Jun. 2015.
[21] C. F. Chuang, C. T. Pan, and H. C. Cheng, "A novel transformer-less interleaved four-phase step-down DC converter with low switch voltage stress and automatic uniform current sharing characteristics," *IEEE Trans. Ind. Electron.*, vol. 31, no. 1, pp. 406–417, Jan. 2016.

K. I. Hwu (M'06) was born in Taichung, Taiwan, on August 24, 1965. He received the B.S. and Ph.D. degrees in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1995 and 2001, respectively.

From 2001 to 2002, he was the Team Leader of the Voltage-Regulated Module, AcBel Company. From 2002 to 2004, he was a Researcher with the Energy and Resources Laboratories, Industrial Technology Research Institute. He is currently a Professor with the Institute of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan, where he was the Chairman of the Center for Power Electronics Technology from 2005 to 2006. His research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control.

Dr. Hwu has been a Member of the Program Committee of the *IEEE Applied Power Electronics Conference and Exposition* since 2005. He has also been a Member of the Technical Review Committee of the Bureau of Standards, Metrology, and Inspection since 2005. Since 2008, he has been a Member of the IET.

W. Z. Jiang (S'12) was born in Changhua, Taiwan, on May 9, 1989. He received the B.S. and M.S. degrees in electrical engineering from the National Taipei University of Technology, Taipei, Taiwan, in 2011 and 2013, respectively, where he is currently working toward the Ph.D. degree.

His research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control.

P. Y. Wu was born in Taipei, Taiwan, on July 7, 1992. He received the B.S. and M.S. degrees in electrical engineering from the National Taipei University of Technology, Taipei, in 2014 and 2016, respectively.

His research interests include power electronics and digital control.