

Letters

An Adaptive High-Precision OCP Control Scheme for Flyback AC/DC Converters

Qiang Wu and Zhangming Zhu, *Member, IEEE*

Abstract—Flyback topology has been widely used in low-power applications due to its simplicity, wide input voltage range, low cost, and low standby power. However, conventional over current protection (OCP) control scheme in flyback converters cannot meet the high precision constant current (CC) requirement in battery charger and LED applications. The proposed adaptive high-precision OCP control scheme can be widely used in ac/dc flyback converters to improve their CC accuracy. It consists of an OCP-Comp circuit and a V_{pump} circuit to detect the primary current in current cycle and adjust it in next cycle adaptively. The proposed OCP control scheme has been implemented in a controller IC adding no extra pin and achieves a significant improvement in output current accuracy compared to conventional OCP schemes. Test results show that the output current variation of the proposed prototype is less than $\pm 0.6\%$ when the input line voltage changes from 85 to 265 Vac.

Index Terms—AC/DC, constant current (CC), flyback converter, over current protection (OCP).

I. INTRODUCTION

FLYBACK converters are commonly used in many applications especially in battery charger and LED driver. This type of converter features simplicity, wide input voltage range, low cost, and low standby power [1]–[3]. In many applications, especially for battery charger and LED driver, high accurate output current and overpower protection are needed. These days, with increasing number of consumer electronics, demand for LED drivers and battery chargers are increasing rapidly. In LED driving applications, excessive current will greatly shorten the service life of LEDs, while insufficient current will reduce lights brightness. In battery charging application, the battery will first be charged by a large constant current (CC). Furthermore, an accurate overpower protection is also needed to meet system safety requirements. As a result, requirement for current accuracy in power supplies is growing ever higher. However, conventional flyback converters suffer the inaccuracy of output current regulation when the input voltage varies [4]–[6]. There are many reasons can cause the variation of the output current such as propagation delay, leakage inductor, and sensing resistor. Many researchers have proposed different methods to improve the accuracy of the output current [7]–[11]. However, the error caused by

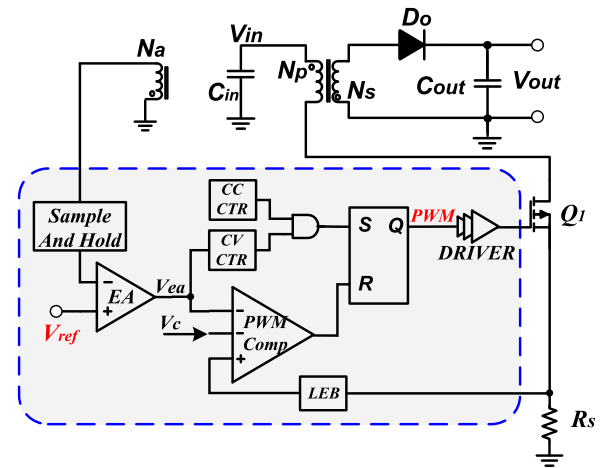


Fig. 1. Schematic of PSR flyback converter.

the leakage inductor still cannot be eliminated. This paper proposes an adaptive high-precision over current protection (OCP) control scheme to improve the output current accuracy, which can eliminate the error caused by propagation delay and leakage inductor.

This paper is organized as follows. Section II describes the inaccuracy of output current caused by the propagation delay and leakage inductor. Circuit implementations of the proposed scheme are illustrated in Section III. Experiments results are shown in Section IV. Conclusions are made in Section V finally.

II. CC INACCURACY

Fig. 1 shows a circuit diagram of a current mode primary-side regulated (PSR) flyback converter which can regulate constant output voltage and CC. A current sensing resistor R_s is used to obtain the primary current. The output voltage can be sensed indirectly through the auxiliary winding. By comparing the auxiliary winding voltage with a reference voltage V_{ref} , the output of error amplifier (EA) is V_{ea} . The leading-edge blanking block is adopted to shield the spike voltage when the power switch turns ON and prevent false trigger of the controller. In constant voltage (CV) mode, V_{ea} controls the primary current and the Constant-Voltage Control (CV-CTR) block to regulate the output voltage to be constant. In CC mode, a CV V_c takes over from V_{ea} to set the primary current, and Constant-Current Control (CC-CTR) turns the switch $Q1$ OFF. As a result, the primary current is set to be V_c/R_s in ideal circuit. However, in real circuit, the propagation delay T_d , and the leakage inductor will cause the actual primary current to be greater than the preset one. Since the output current highly depends on the primary current, it can vary enormously when the input voltage changes.

Manuscript received February 8, 2017; revised March 22, 2017; accepted May 2, 2017. Date of publication May 4, 2017; date of current version August 2, 2017. This work was supported by the National Natural Science Foundation of China under Grant 61625403. (Corresponding Author: Zhangming Zhu.)

The authors are with the School of Microelectronics, Xidian University, Xi'an 710071, China (e-mail: wuqiang1988@gmail.com; zhangmingzhu@xidian.edu.cn).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2017.2701507

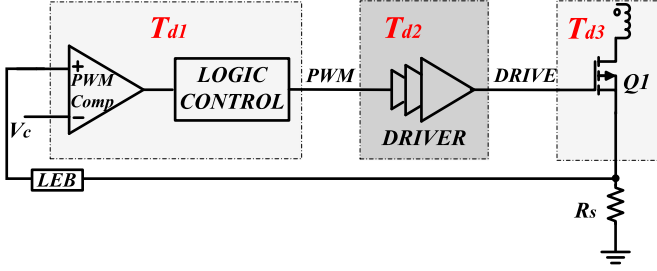


Fig. 2. Driving signal propagation delay.

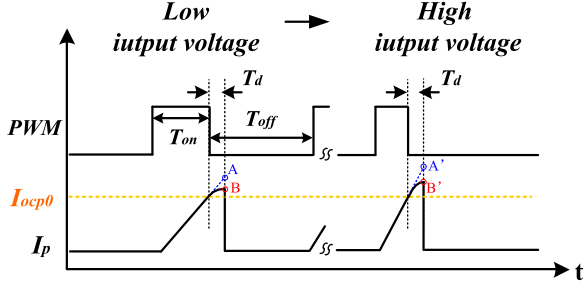


Fig. 3. Inductor current waveforms for high and low line voltages.

A. Propagation Delay

In CC mode, a constant threshold voltage V_c is used to implement cycle-by-cycle over current limit I_{ocp0} ($I_{ocp0} = V_c / R_s$). As shown in Fig. 3, there is a turn-OFF delay after the primary current rising up to I_{ocp0} , which is caused by the propagation delay T_d in real circuits. As shown in Fig. 2, the propagation delay T_d contains three parts

$$T_d = T_{d1} + T_{d2} + T_{d3} \quad (1)$$

where T_{d1} is the logic delay, T_{d2} is the driver delay, and T_{d3} is the switching delay. Conventionally, T_{d3} is much larger than T_{d1} and T_{d2} , so T_d is mainly caused by T_{d3} , which is generated by the parasitic gate capacitor of power switch. It can be calculated by

$$T_{d3} = \frac{V_{DRIVE} \cdot C_g}{I_{sink}} \quad (2)$$

where V_{DRIVE} is the driving voltage, C_g is the value of parasitic gate capacitor of power switch, and I_{sink} is sink current generated by the driver. Since these three parameters are totally different in different converter systems, it is hard to measure and predict the value of T_d .

As shown in Fig. 3, although the driving signal (PWM) is turned OFF, the primary current (I_p) continues to increase during the propagation delay. In low input voltage and high input voltage, I_p rises up to point A and point A', respectively. Since the rising slope of I_p is proportional to the input voltage, A' is higher than A significantly. As a result, the output current can vary a great deal when input voltage changes.

B. Leakage Inductor

In Fig. 1, when power switch Q1 is turned OFF, all the energy stored in ideal transformer will be transferred to the secondary side. However, a real transformer is not ideal and a small portion of primary current will flow to the ground. As shown in Fig. 4, the primary inductor can be divided into two parts: the main inductor L_p and leakage inductor L_k . Because of the leakage inductor, the energy cannot be transferred immediately after the switch is turned OFF. There is a transfer delay t_1 caused by the leakage inductor. Fig. 4 shows that the peak primary

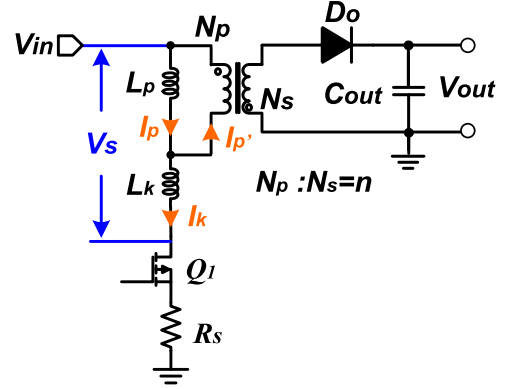


Fig. 4. Simplified flyback transformer model.

current is divided into two branches: $I_{p'}$ and I_k . $I_{p'}$ flows through the primary winding and I_k flows through the leakage inductor. After the switch is turned OFF, I_k decreases from peak current to zero. The falling slope is determined by

$$k_f = \frac{V_s - nV_{out}}{L_k} \quad (3)$$

where k_f is the falling slope of I_k , V_s is the voltage between V_{in} and the drain of the switch, n is the turns ratio of primary winding and secondary winding, V_{out} is the output voltage. So the transfer delay t_1 is derived by

$$t_1 = \frac{I_{pp}}{k_f} = \frac{L_k}{V_s - nV_{out}} \cdot I_{pp} \quad (4)$$

where I_{pp} is the peak primary current. When I_k decreases down to zero, $I_{p'}$ can be calculated by

$$I_p |_{I_k=0} = I_{pp} - t_1 \cdot k_{f'} \quad (5)$$

where $k_{f'}$ is the falling slope of I_p , and it is determined by

$$k_{f'} = \frac{nV_{out}}{L_m} \quad (6)$$

From (4)–(6), considering the leakage inductor, the actual peak primary current $I_{pp'}$ is as

$$I_{pp'} = I_p |_{I_k=0} = \left(1 - \frac{L_k}{V_s - nV_{out}} \cdot \frac{nV_{out}}{L_m}\right) I_{pp} \quad (7)$$

So the actual waveform of primary current will be distorted. As shown in Fig. 3, real I_p will rise up to B and B' instead of A and A' because of the distortion.

III. PROPOSED OCP CONTROL SCHEME

The error of cycle-by-cycle over current limit is mainly caused by the propagation delay and the leakage inductor. Many researchers have proposed different methods to improve the output current accuracy including compensating the error of propagation delay [8], [9]. However, the error caused by the leakage inductor is hard to measure and compensate because it is highly depends on the transformer specification. This paper proposes a new method to compensate both errors.

A. Proposed Algorithm to Eliminate Current Error

Fig. 5 illustrates an algorithm flow chart to adjust the cycle-by-cycle over current limit to be constant. Assume that the cycle-by-cycle over current limit voltage is set to be V_c . The proposed algorithm detects

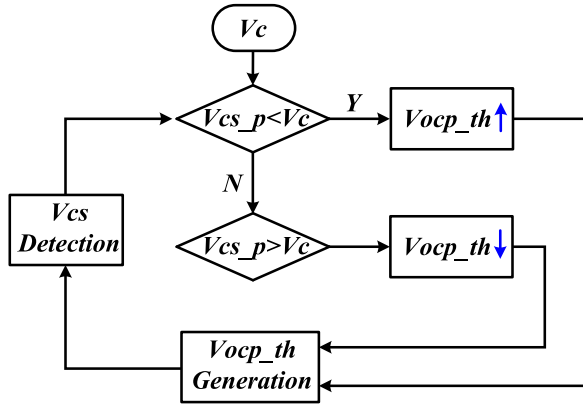
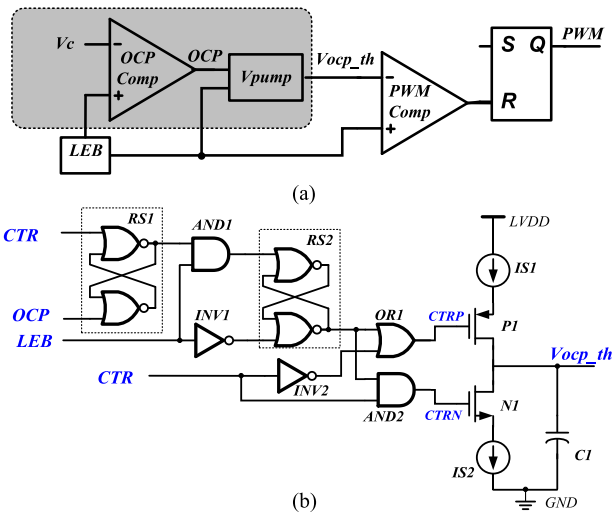


Fig. 5. Proposed algorithm flow chart.


 Fig. 6. Implementation of the proposed OCP control scheme. (a) Architecture of the proposed circuit. (b) V_{pump} circuit.

the peak primary voltage $V_{cs,p}$ in every switching cycle, and compares it with the voltage limit V_c . When $V_{cs,p}$ is lower than V_c , the controller will pull up the cycle-by-cycle over current threshold voltage $V_{ocp,th}$. If $V_{cs,p}$ is higher than V_c , the controller will pull down $V_{ocp,th}$. A few switching cycles later, the peak primary voltage is set to be nearly V_c . The variation of peak primary current between continues two switching cycles is little so it will do not influence the system stability. Since the sensed peak primary voltage is the actual voltage containing the error of propagation delay and leakage inductor, this algorithm can eliminate both errors.

B. Implementation of Proposed OCP Control Scheme

As shown in Fig. 6(a), the circuit in the shadow is designed based on the aforementioned algorithm. *OCP-Comp* is used to detect primary peak voltage and compares it with V_c . *Vpump* block is used to adjust cycle-by-cycle over current threshold voltage $V_{ocp,th}$ based on the comparison result. Main waveforms are shown in Fig. 7.

Cycle-by-cycle over current protection happens when the voltage across the sensing resistor R_s exceeds the preset voltage V_c . Every time that over current protection happens, the signal *OCP* changes from low to high. Fig. 6(b) shows the circuit implementation of *Vpump*, which is used to adjust $V_{ocp,th}$. The comparison result of $V_{cs,p}$ and V_c in current switching cycle is delivered to *RS1* and

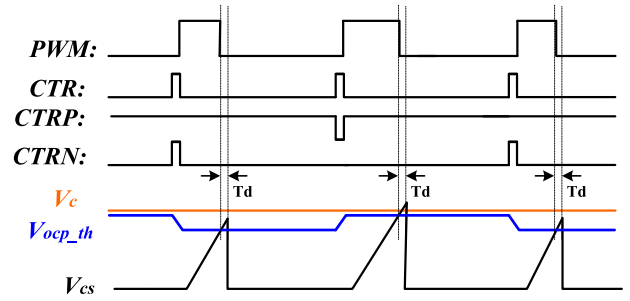


Fig. 7. Main waveforms.

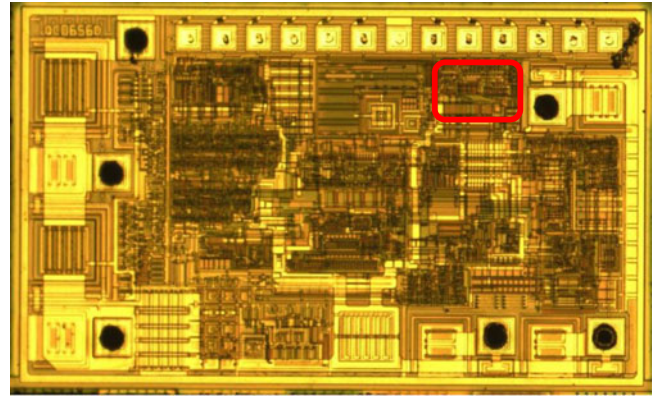


Fig. 8. Micrograph of the proposed IC controller.

 TABLE I
DESIGN SPECIFICATIONS

Input Line Voltage Range	85~265 V
Output power	5 V * 2 A
Primary inductor (L_p)	1.5 mH
Primary winding turns (N_p)	130T
Secondary winding turns (N_s)	9T
Auxiliary winding turns (N_a)	27T
Current sense resistor (R_s)	1.5 Ω
Output capacitor (C_{out})	1.6 mF

RS2, and it will be stored on the output of *RS2*. As shown in Fig. 7, Constant-Current Control (*CTR*) is a pulse signal, the high level time of which comes before the rising edge of driving signal *PWM*. During the high level time of *CTR*, if the output of *RS2* is high, the and-gate *AND2* will turn the *NI* ON and discharge the capacitor *CI*. On the contrary, if the output of *RS2* is low within the high level of *CTR*, the or-gate *ORI* will turn *P1* ON and charge the capacitor *CI*. Through the above process, the primary peak voltage is adjusted to be nearly the preset voltage of V_c , finally.

IV. EXPERIMENTAL RESULTS

A PSR IC controller based on the proposed OCP control scheme is implemented. Fig. 8 shows the layout of the proposed IC in which the enclosed area by red box is the proposed OCP circuit. To verify the performance of the proposed OCP circuit, a 5V/2A PSR flyback converter is designed for operating under the universal input line voltage (85~265 V_{ac}). The schematic of the converter can be referred to Fig. 1. In CC mode, *CC-CTR* block is used to turn ON the power switch and ensures that the switch period is fixed at twice the duration of the

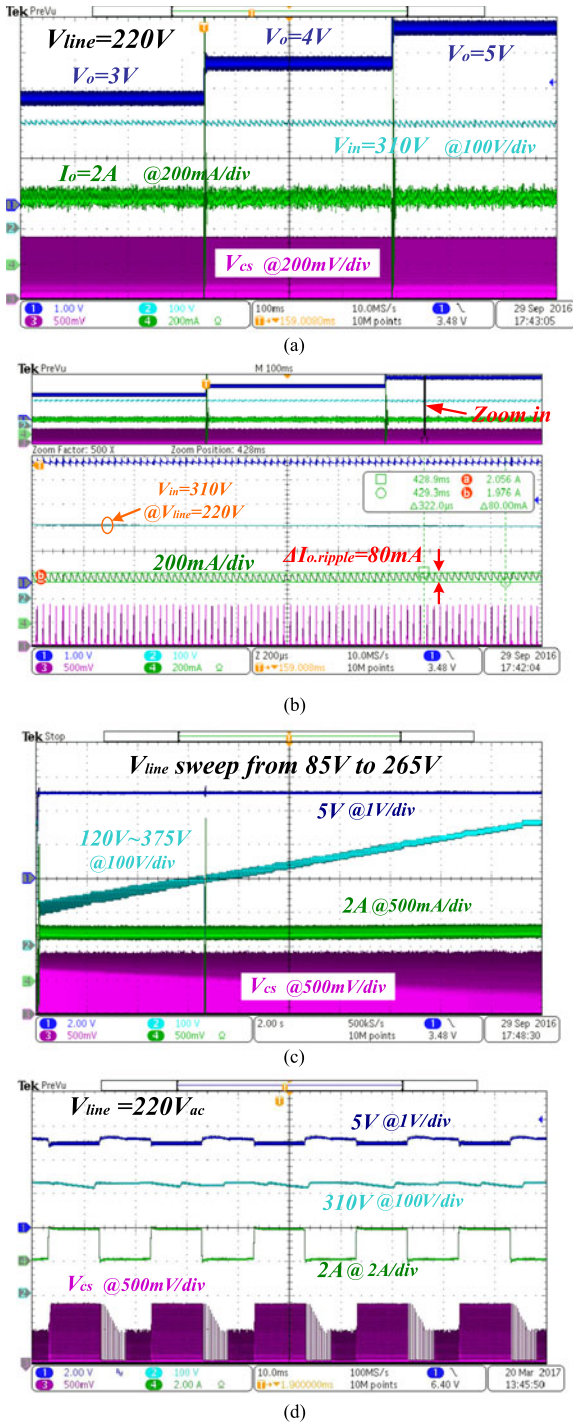


Fig. 9. Test waveforms of the proposed prototype. (a) CC mode with different output voltages. (b) Zoomed-in detailed view of waveforms in (a). (c) CC mode with different line voltages. (d) Dynamic test.

demagnetization time. Working principle of *CC-CTR* can refer to [13] and [14]. Key component parameters of the IC controller are listed in Table I.

Fig. 9(a) shows the load regulation test waveforms including output voltage V_o , input voltage V_{in} , output current I_o , and primary voltage V_{cs} . During the test, the line voltage is fixed to be 220 Vac, and the output voltage is clamped at 3, 4, and 5 V, respectively, by an electronic load. From Fig. 9(a), V_{cs} and I_o change very little in different output

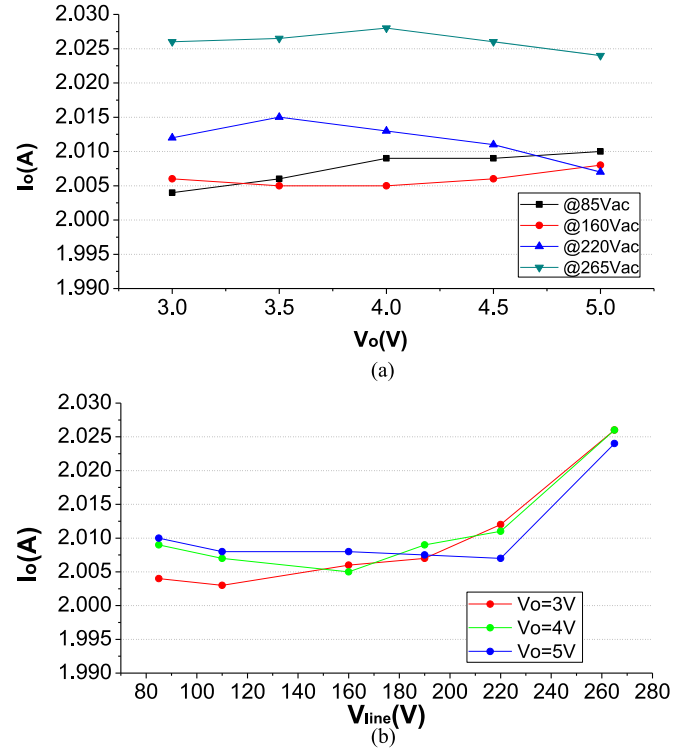


Fig. 10. Test results of CC precision. (a) Measured output current versus output voltage. (b) Measured output current versus line voltage.

voltages. There is a big current spike caused by the electronic load when the output voltage changes from 3 to 4 V, and from 4 to 5 V. Fig. 9(b) is the zoomed-in figure of Fig. 9(a). The output current ripple shown in Fig. 9(b) is less than 80 mA. Compared to the prior arts, it is much lower than that seen in [11] and [12]. Fig. 9(c) shows the line regulation test results. The line voltage V_{line} in the test is set to increase from 85 to 265 Vac, so V_{in} changes from 120 to 375 V. At the same time, V_o is locked to be 5 V. The large voltage spike, shown in Fig. 9(c), is caused by the voltage supply when it changes from low gear (less than 120 Vac) to high gear (higher than 120 Vac). Waveforms under dynamic test are illustrated in Fig. 9(d). During the test, load changes between high and low periodically with a 2 A output current lasting for 10 ms and a 0.1 A output current lasting for 10 ms. Test results show that the system is stable and responds quickly when load changes.

More detailed test results are shown in Fig. 10. Fig. 10(a) depicts the load regulation under different line voltages. It can be calculated that the load regulation of the proposed converter is less than 0.4%. Fig. 10(b) illustrates the line regulation under different output voltages. From Fig. 10(b), the variation of the output current is less than 25 mA under universal input voltages, which gives rise to the current line regulation is as good as $\pm 0.6\%$. The comparisons of the proposed converter with the prior arts are made in Table II. The main concept of the proposed circuits in [8] and [9] is to use the slope of the primary-side current, and then add a td compensation time to obtain the accurate peak current measurement. By adopting the intelligent charging and discharging circuit, [12] keeps a high precision fixed ratio between the secondary winding demagnetization time and switching period to achieve high-precision constant output current. A ring detecting and a demagnetization portion control technique are proposed in [11], so the ending time of demagnetization can be accurately determined and the portion of demagnetization in a switching period remains precisely the same. However, Table II shows that the proposed converter per-

TABLE II
COMPARISONS BETWEEN THE PROPOSED METHOD AND THE PRIOR ARTS

Parameter	This work	[11]	[8]	[12]	[9]
Topology	Flyback	Flyback	Flyback	Flyback	Flyback
Primary-side inductance	1.5 mH	N/A	1.6 mH	2.45 mH	N/A
AC input voltage	85–265 Vac	85–264 Vac	90–270 Vac	85–264 Vac	90–380 Vdc
Output power	10 W	10 W	8.4 W	3 W	65 W
Average Efficiency	83.9%	N/A	N/A	83.6%	N/A
Output current ripple (220 Vac)	80 mA	100 mA	N/A	280 mA	N/A
CC accuracy	±0.6%	±1.50%	±2%	±1%	±2%

forms much better than previous solutions especially in output current accuracy.

V. CONCLUSION

This paper proposes an adaptive high-precision OCP control scheme, which can be widely used in flyback ac/dc converters. It consists of an OCP-Comp circuit and a V_{p_ump} circuit to detect the primary current in current cycle and adjust it in next cycle adaptively. To verify the proposed OCP control scheme, it has been implemented in a PSR controller prototype. Test results show that the variation of the output current is less than ±0.6%, which is much better than the prior arts. Since the proposed circuit can be added into an IC controller without adding any extra pins, it can replace the conventional OCP circuits perfectly. Therefore, the combination of the proposed scheme and the flyback configuration will make the entire proposal a viable contender for many low power applications in which simple structure, low cost, low standby power, high efficiency, and compact volume are required.

REFERENCE

- [1] J. C. W. Lam and P. K. Jain, "A high power factor, electrolytic capacitorless AC-input LED driver topology with high frequency pulsating output current," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 943–955, Feb. 2015.
- [2] H. Lee and G.-W. Moon, "Zero no-load power AC/DC adapter for electronic equipment with embedded battery," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3073–3076, Jul. 2013.
- [3] J. P. Hong and G. W. Moon, "A digitally controlled soft valley change technique for a flyback converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 966–971, Feb. 2015.
- [4] J.-W. Yang and H.-L. Do, "High-efficiency ZVS AC-DC LED driver using a self-driven synchronous rectifier," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 61, no. 8, pp. 2505–2512, Aug. 2014.
- [5] P.-L. Huang, D. Chen, C.-J. Chen, and Y.-M. Chen, "An adaptive high-precision overpower protection scheme for primary-side controlled flyback converters," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2817–2824, Oct. 2011.
- [6] H. S. Choi and D. Y. Huh, "Protection schemes for various fault conditions for off-line flyback converters," in *Proc. Int. Conf. IEEE Power Electron. Spec.*, Jun. 2004, pp. 4355–4359.
- [7] Y.-C. Li and C.-L. Chen, "A novel primary-side regulation scheme for single-stage high-power-factor AC-DC LED driving circuit," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4978–4986, Oct. 2013.
- [8] C.-N. Wu, Y.-L. Chen, and Y.-M. Chen, "Primary-side peak current measurement strategy for high-precision constant output current control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 967–975, Feb. 2015.
- [9] P.-L. Huang, C.-J. Chen, and Y.-M. Chen, "An adaptive high-precision overpower protection scheme for primary-side controlled flyback converters," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2817–2824, Oct. 2011.
- [10] Y. Wang, J. Jiang, and L. He, "High-precision constant current controller for primary-side feedback LED drivers," in *Proc. Int. Symp. Ind. Electron.*, 2013, pp. 1–5.
- [11] Z. Wang, X. Lai, and H. He, "High precision control technique for constant current regulation in primary-side regulation systems," *IET Electron. Lett.*, vol. 50, no. 24, pp. 1870–1872, Nov. 2014.
- [12] Y. Chen and P. Yang, "A novel primary-side controlled universal-input AC-DC LED driver based on a source-driving control scheme," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4327–4335, Aug. 2015.
- [13] Q. Wu, Y. Li, W. Guo, and Z. Zhu, "A low standby power primary-side regulated flyback controller with fast dynamic response," *J. Circuit. Syst. Comp.*, vol. 24, no. 5, 2015, Art. no. 1550069.
- [14] Q. Wu and Z. Zhu, "A versatile OCP control scheme for discontinuous conduction mode flyback AC/DC converters," *IEEE Trans. Ind. Electron.*, vol. pp, no. 99, pp. 1–1., 2017, doi: 10.1109/TIE.2017.2682011.