Single Switch Nonisolated Ultra-Step-Up DC–DC Converter With an Integrated Coupled Inductor for High Boost Applications

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***Abstract*—This paper introduces a new single-switch nonisolated dc–dc converter with very high voltage gain and reduced semiconductor voltage stress. The converter utilizes an integrated autotransformer and a coupled inductor on the same core in order to achieve a very high voltage gain without using extreme duty cycle. Furthermore, a passive lossless clamp circuit recycles the leakage energy of the coupled magnetics and alleviates the voltage spikes across the main switch. This feature along with low stress on the switching device enables the designer to use a low voltage and low $R_{\mathrm{DS-on}}$ MOSFET, which reduces cost, as well as conduction and turn on losses of the switch. The principle of operation, theoretical analysis, and comparison supported by some key simulation and experimental results of a 500 W prototype are presented.**

***Index Terms*—Coupled inductor, distributed generation, high step-up dc–dc converter, switched-mode power supply.**

I. Introduction

A DC–DC converter with high voltage gain and efficiency is required in many applications such as the front-end converter for intermittent renewable and distributed power generations including solar photovoltaic (PV), fuel cells and power systems based on battery bank, and supercapacitors [1], [2]. In addition, hybrid electric vehicle (HEV), high voltage light emitting diode (LED) lamps, and uninterruptible power supply also require a highly efficient high boost dc–dc converter to convert the low and varying voltage of the battery (12–48 V) and fuel cell (25–50 V) to standard dc bus voltage of 380–400 V [3]. Similarly, in HEV and other electric traction systems, a voltage of 14 or 42 V from batteries, fuel cells, and/or supercapacitors needs to be raised to 200 V_{dc} or 500 V_{dc} during various modes of operation [4]. In addition, the emergence of a 380 V dc distribution system instead of conventional 48 V dc distribution systems for data and communication center subsequently increases demand for high step-up dc–dc converters [5]. The conventional boost converter for such higher voltage gain applications (in the range of 10–20 times) is not sufficient to boost the input voltage due to high losses and associated stress on the switching devices. Furthermore, higher stress on the switch(es) demands a higher voltage switch, which contributes to higher conduction losses due to larger $R_{\mathrm{DS-on}}$.

Various high step-up dc–dc converter topologies are presented in the literature using various voltage boosting techniques such as multilevel, interleaved, cascaded or using voltage multiplier cells (VMCs), switched capacitor, and coupled inductor [6]–[15]. Fig. 1 shows the various voltage boosting techniques used for such high boost applications. These voltage boosting techniques have their own advantages and disadvantages and should be selected based on the application and requirements, such as isolated/nonisolated, hard switch/soft switched, unidirectional/bidirectional as well as with or without minimum phase characteristics [16]. For example, the numbers of components to design multilevel, interleaved, cascaded including VMCs and switched capacitor are large, especially the switch and associated driving circuitry. In addition, the voltage stress on the switch is high and suffers from high conduction losses [10]. Moreover, with the increasing number of power processing stages (e.g., in cascaded or multilevel structures), the complexity in control and circuit design (driving circuitries) increases.

Considering the above aspects and to meet the growing demand of high boost converter for various power applications, a magnetic coupling (using coupled inductor or transformer) could be an attractive option among the voltage boosting techniques for high boost converter design. This reduces the number of components, especially switching devices (MOSFETs and diodes) and complexity in the circuit. In addition, the converter with coupled magnetics has a higher design freedom, e.g., voltage gain can be tuned with duty cycle, turns ratio, and the winding arrangements. Moreover, the switch can be implemented at the low voltage side of the circuit, which reduces the conduction loss by replacing high voltage and high $R_{\mathrm{DS-on}}$ switch with low voltage and low $R_{\mathrm{DS-on}}$ switch. However, with these advantages, converters with coupled magnetics are prone to leakage inductance, and cause voltage spikes across the switching devices and also lower the converter efficiency. This leakage effect cannot be eliminated completely; however, it can be mitigated by using an active clamp circuit. The extra active clamp circuit can effectively recycle the leakage energy and reduce the main switch voltage stress, but at the expense of circuit complexity and loss in the extra circuitry. In addition, some converters require high voltage rated switches [12]. Moreover, the turns ratio of the coupled magnetics must usually be increased in order to

Manuscript received June 4, 2016; revised October 31, 2016; accepted December 27, 2016. Date of publication December 29, 2016; date of current version June 23, 2017. Recommended for publication by Associate Editor Gerry Moschopoulos.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2646382

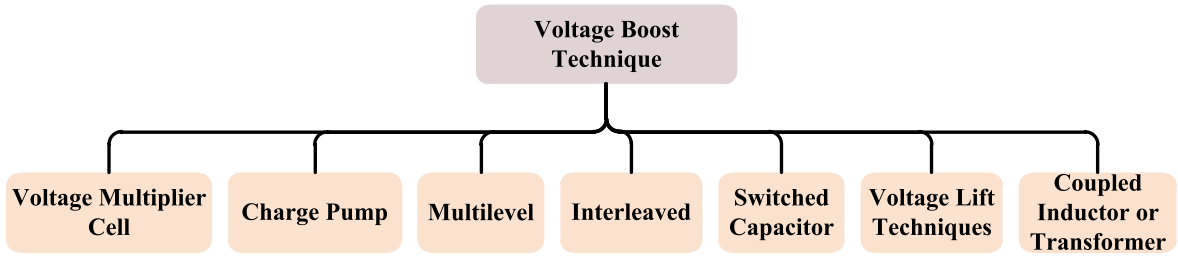


Fig. 1. Broad categorization of voltage boost techniques used in high step up dc–dc converters.

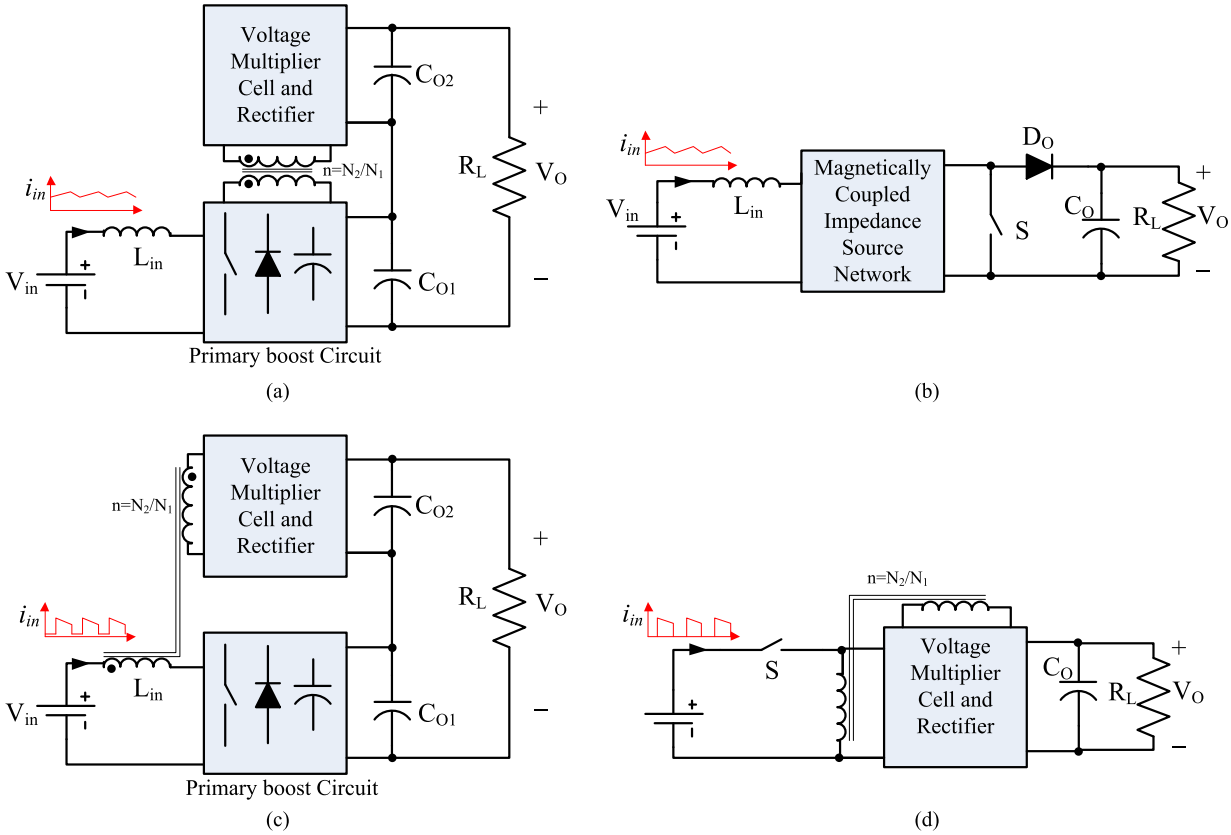


Fig. 2. General topology variation of different coupled inductor based high boost dc–dc converter (a) continuous input current type (saw-tooth) [18]–[25], (b) continuous input current type using magnetically coupled impedance source (MCIS) networks [37], (c) continuous input current type (with offset pulsating) [26]–[35], and (d) discontinuous input current type [36].

obtain a higher voltage gain, which may in turn lead to more costly and volumetric magnetics because of the many winding turns involved.

Fig. 2 shows the general topology variation of different coupled inductors based on a high boost dc–dc converter. The variation is basically due to the nature of the current (i_{in}) drawn from the source, winding arrangements, and the integrated VMC. VMCs are generally added in the coupled magnetic converter to further assist in voltage boost, whilst clamping the voltage spikes and leakage energy recovery. These cells only consist of diodes and capacitors and hence are known as switched/diode capacitor VMCs. Some common VMCs are shown in Fig. 3. In such VMCs, the secondary winding acts as a voltage source which is in series with the power branch, while the clamp capacitor and diode are used to recover the leakage energy. The clamp capacitor can be shifted in the circuit in all placements, where the clamping function is similar and the leakage energy can effectively be recycled directly or through the secondary winding to the load [3]. These circuits can be used at the output stage of converters with ac or pulsating dc inputs (both half-wave and full-wave). Therefore, they are known as voltage multiplier rectifiers also. Although the voltage stresses in the middle stages are reduced, the voltage stress of output diode and capacitor remained identical to the high output voltage level. Therefore, high-order multiplication may cause increased power loss, cost, and size of the circuit.

As mentioned above, the drawbacks associated with such a high boost converter using different voltage boosting techniques

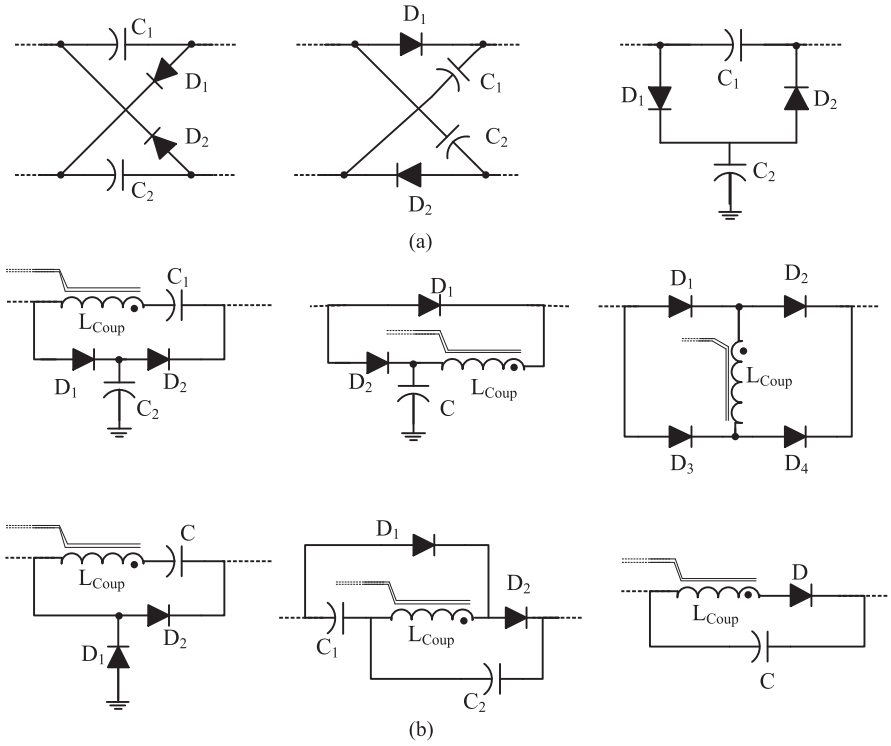


Fig. 3. Some common voltage multiplier cells used with magnetically coupled dc–dc converter for higher gain application (a) switched capacitor VMC and (b) integrated coupled type VMC. (a) Switched capacitor VMC and (b) magnetically coupled VMC.

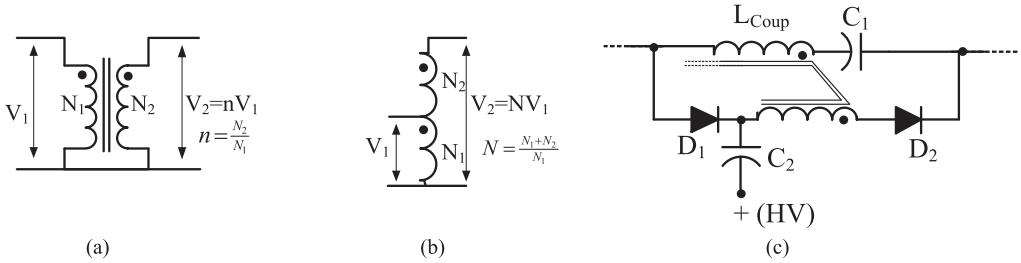


Fig. 4. Schematic illustration of the autotransformer-type coupled inductor and modified integrated voltage multiplier cell with high boost and integration ability (a) normal coupled inductor, (b) autotransformer-type coupled inductor, and (c) modified voltage multiplier cell.

encourage to investigate a new high boost converter topology, which enables to use a lower voltage rating, lower $R_{\mathrm{DS-on}}$ MOSFET, with lower overall component count, complexity, and higher efficiency. To address this issue, a very high voltage gain dc–dc converter is proposed using an integrated coupled inductor with autotransformer-type winding and a modified VMC [see Fig. 5(a)]. The integrated passive lossless clamp with VMC in the circuit recycles the leakage energy of the coupled magnetics, which increases the efficiency and avoids extra lossy snubber or active-clamp circuit. The prominent advantages of the new topology are

1) Autotransformer-type winding in the coupled inductor helps to reduce the total number of turns and hence the size of the magnetics in the converter circuit. This helps to improve the power density of the circuit.
2) A very high voltage gain can be achieved, which is particularly suitable for a) low voltage output fuel cell (25–50 V) to stabilize the output voltage to 400 V_{dc} and b) high voltage LED lamps (which require 100–600 V for a series/parallel string of LED from a 12–24 V battery input).
3) A low voltage stresses on the switch (Q), which helps to choose a low voltage and low R_{DSon} MOSFET.
4) No voltage spikes across the switch. The secondary winding acts as a voltage source, which is in series with the power branch, while the clamp capacitor and diode are used to recover the leakage energy to the load.
5) Only eight components are required to design the converter. In addition, the magnetic design is simplified by winding the autotransformer and coupled inductor on the same core that not only reduces the space and overall component count, but also the current stress in the switching devices.

The above advantages of the new topology open a new horizon in the area of switch mode power supply to design a compact

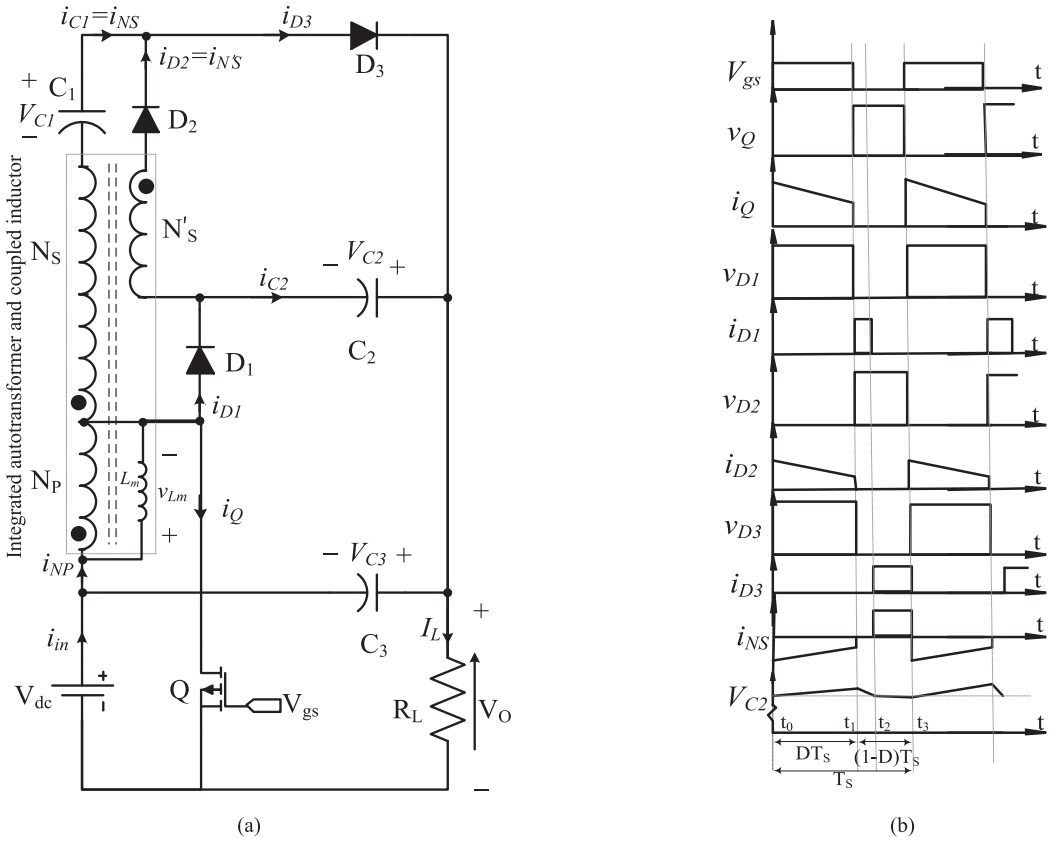


Fig. 5. Proposed ultra-step-up dc–dc converter (a) schematic circuit and its (b) steady-state waveforms during CCM.

and highly efficient dc–dc converter for high voltage gain applications. A mathematical derivation of the proposed converter is documented in Section II with detail comparison and design rules in Section III, which are further validated by simulated and experimental results in Section IV, and the findings drawn are finally concluded in Section V.

II. Proposed Topology and Analysis

A. Basic Principle of Operation

Fig. 4 shows different coupled inductors with different winding arrangements. Using the principle of an autotransformer, the coupled inductor shown in Fig. 4(b) can achieve higher voltage gain $(V_2/V_1 = N = n + 1)$ compared to the normal coupled inductor $(V_2/V_1 = n)$ as shown in Fig. 4(a). With such a simple modification in the winding and its arrangement and combining it with a charge pump and switched capacitor with coupled inductor VMC as shown in Fig. 4(c), a high step-up gain can be achieved at the converter output. Furthermore, the integrated VMC recycles the leakage energy to the load and helps to reduce the voltage and current stress across the switch and improves the overall efficiency.

The principle and circuit components as described above are used in the proposed converter, which is illustrated in Fig. 5(a) to achieve the desired performances. In addition to charge pump and integrated three winding coupled inductor, the circuit consists of a power switch, three diodes, three capacitors, and an input voltage $V_{\rm in}$.

To simplify the circuit analysis, the following conditions are assumed:

1) Capacitors C_1, C_2, and C_3 are large enough to keep V_{C1}, V_{C2}, and V_{C3} constant in one switching period.
2) The power MOSFET and diodes are treated ideal. ON-state resistance $R_{\rm DS-on}$ and parasitic capacitances of the main switch Q are neglected. In addition, the forward voltage drops of the diodes D_0–D_3 are ignored.
3) Equivalent series resistances (ESRs) of all capacitors are neglected.
4) The coupling coefficient $(k = L_m/(L_m + L_{k1}))$ of the coupled inductor is 1.

B. Continuous Conduction Mode (CCM)

Based on the aforementioned assumptions, there are three major operating modes in one switching period of the proposed circuit under continuous conduction mode (CCM). The equivalent circuit of the converter in each operating mode is shown in Fig. 6. Fig. 5(b) illustrates some typical key waveforms under CCM operation in one switching period. The different operating modes are described as follows in detail:

Mode 1 ($[t_0 - t_1]$)*:* During this interval, the switch Q turns ON and the current flows through the primary winding, secondary winding of the autotransformer and to the coupled inductor

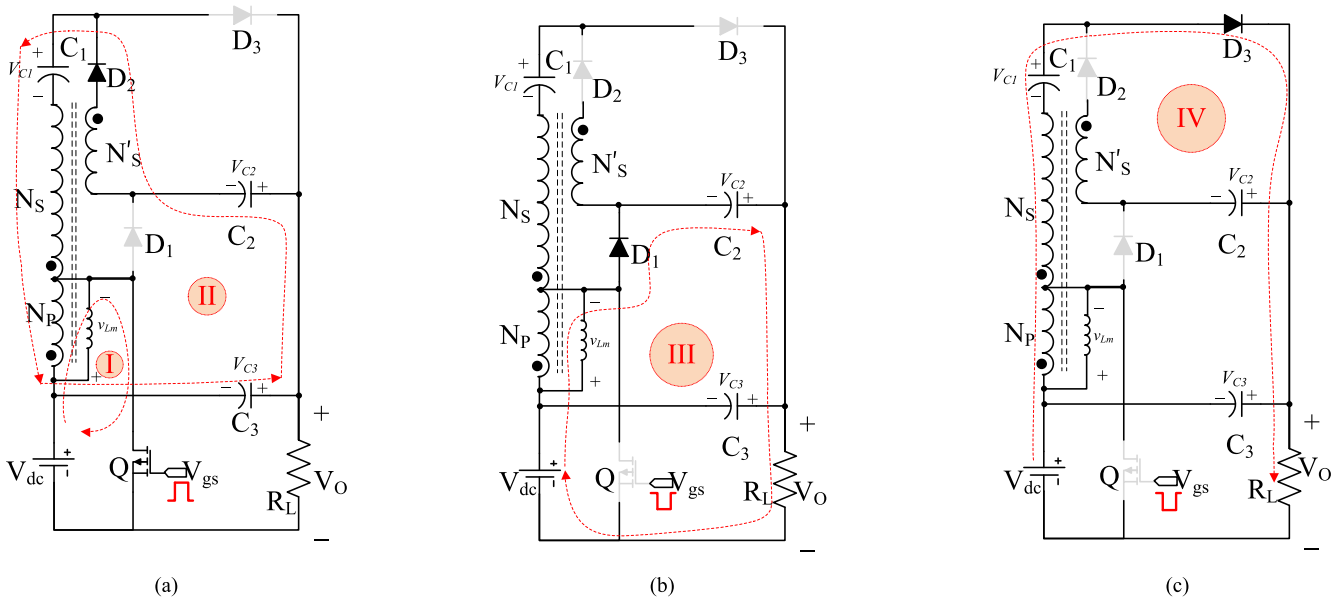


Fig. 6. Equivalent circuit of the proposed converter in CCM during different modes. (a) Mode 1 [t_0–t_1], (b) (b) Mode 2 [t_1–t_2], and (c) Mode 3 [t_2–t_3].

through diode D_2 and charges capacitors C_1 and C_2. Diodes D_1 and D_3 are reversed biased. There are two closed loops for the current to flow as shown in Fig. 6(a). The relevant circuit expressions for this mode can then be written as

$$\frac{N_S}{N_P}v_{\rm Lm} + V_O - V_{C2} + \frac{N'_S}{N_P}v_{\rm Lm} - V_{C1} = 0$$
$$\Rightarrow \quad v_{\rm Lm} = \frac{V_{C1} + V_{C2} - V_O}{\frac{N_S + N'_S}{N_P}} \tag{1}$$

and

$$v_{\rm Lm} = V_{\rm dc} \tag{2}$$

where $v_{\rm Lm}$ is the voltage across the magnetizing inductance.From (1) and (2)

$$V_{C1} + V_{C2} = \frac{N_S + N'_S}{N_P}V_{\rm dc} + V_O. \tag{3}$$

Mode 2 ($[t_1 - t_2]$)*:* The switch is turned-OFF during this interval [see Fig. 6(b)]. Diode D_2 is reverse biased, whilst the diode D_3 continues to be reverse biased until the end of this mode. The load current flows through diode D_1 and primary winding of the autotransformer, and discharges the capacitor C_2. The circuit expression for this mode can then be written as

$$V_{\rm dc} - v_{\rm Lm} + V_{C2} - V_O = 0$$
$$\Rightarrow \quad v_{\rm Lm} = V_{\rm dc} + V_{C2} - V_O. \tag{4}$$

Mode 3 ($[t_2 - t_3]$)*:* The diode D_1 remains in the previous mode until the capacitor C_2 is discharged to V_{C2}. This reverse biased the diode D_1 and the load current path changes to loop IV as shown in Fig. 6(c). The circuit expression for this mode can then be written as

$$V_{\rm dc} - v_{\rm Lm} - \frac{N_S}{N_P}v_{\rm Lm} + V_{C1} - V_O = 0$$
$$\Rightarrow \quad v_{\rm Lm} = -\frac{V_O - V_{C1} - V_{\rm dc}}{\frac{N_S + N_P}{N_P}}. \tag{5}$$

Applying volt-second balance to the magnetizing inductance L_m using (2) and (4) will result in

$$\int_0^{DT_s} v_{\rm Lm}\,dt + \int_{DT_s}^{T_s} v_{\rm Lm}\,dt = 0$$
$$\Rightarrow \quad V_{C2} = \frac{V_O\,(1\ -\ D) - V_{\rm dc}}{1\ -\ D}. \tag{6}$$

Applying volt-second balance to the magnetizing inductance L_m using (1) and (5) results in

$$\int_0^{DT_s} v_{\rm Lm}\,dt + \int_{DT_s}^{T_s} v_{\rm Lm}\,dt = 0$$
$$D\frac{V_{C1} + V_{C2} - V_O}{\frac{N_S + N'_S}{N_P}} - (1\ -\ D)\,\frac{V_{C1} - V_O - V_{\rm dc}}{\frac{N_S + N_P}{N_P}} = 0. \tag{7}$$

Using (6) and (7)

$$V_{C1} = \left[\frac{N_S + N'_S}{N_P} + \frac{1}{1\ -\ D}\right]V_{\rm dc}. \tag{8}$$

Which gives the voltage ratio between two capacitors as

$$\frac{V_{C2}}{V_{C1}} = \frac{N_S + N_P + N'_S\,(1\ -\ D)}{(N_S + N'_S)\,(1\ -\ D) + 1}. \tag{9}$$

The voltage gain ($G_{\rm v\_CCM}$) and hence the voltage transfer characteristics equation of the converter during CCM is found by solving (3) and (7) as

$$G_{\rm v\_CCM} = \frac{V_O}{V_{\rm dc}} = \left[\frac{1\ +\ N}{1\ -\ D} + m\right] \tag{10}$$

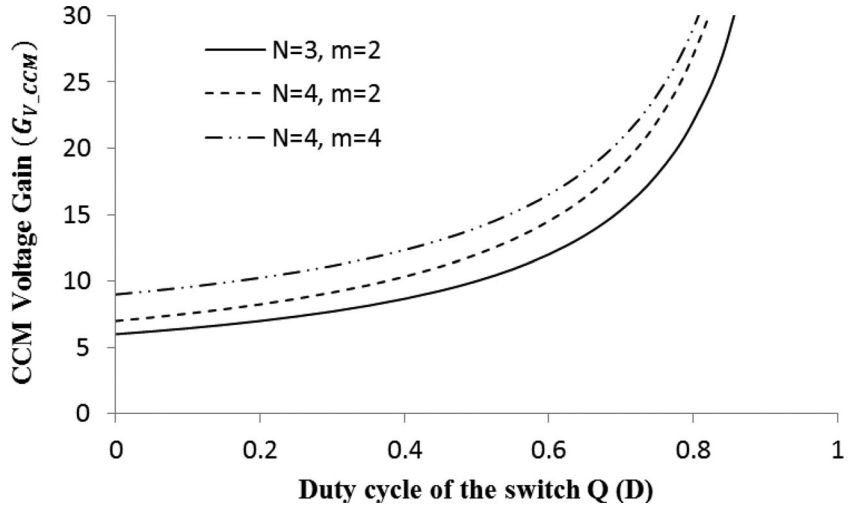


Fig. 7. Theoretical voltage transfer characteristics of the proposed converter with varying *N*, *m*, and *D* during CCM.

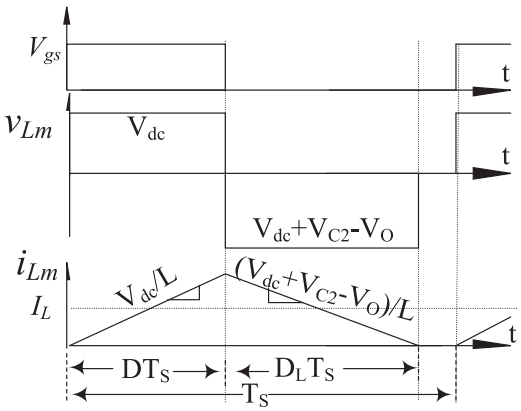


Fig. 8. Inductor voltage and current of the proposed dc–dc converter in DCM mode.

where $N = (N_P + N_S)/N_P$ is the autotransformer voltage transfer constant and $m = N'_S/N_P$ is the turns ratio of the coupled inductor. The voltage transfer characteristic of the proposed converter is shown in Fig. 7 with varying *N*, *m*, and *D*.

Furthermore, since $P_{\rm in} = P_O = V_{\rm dc} I_{\rm in} = V_O I_O$ for a lossless converter, the dc input-to-output current gain $G_{\rm I\_CCM} = I_O/{\rm I_{in}}$ can be expressed as

$$G_{\rm I\_CCM} = \frac{1 \ - \ D}{1 + N + m\,(1 \ - \ D)}. \tag{11}$$

C. Discontinuous Conduction Mode (DCM)

Typical waveforms of the inductor voltage and current during discontinuous conduction mode (DCM) are shown in Fig. 8. When $0 \le t \le DT_S$, *Q* is turned ON, which results in the following equations for representing its operation:

$$v_{\rm Lm} = \frac{V_{C1} + V_{C2} - V_O}{\frac{N_S + N'_S}{N_P}} \tag{12}$$

$$\text{and}\, v_{\rm Lm} = {\rm V_{dc}}. \tag{13}$$

From (12) and (13)

$$V_{C1} + V_{C2} - V_O = \frac{N_S + N'_S}{N_P} V_{\rm dc}. \tag{14}$$

Similarly, (15) and (16) are valid when *Q* is OFF in the adjacent interval $DT_S \le t \le (D + D_L)T_S$:

$$v_{\rm Lm} = V_{\rm dc} + V_{C2} - V_O \tag{15}$$

$$v_{\rm Lm} = -\frac{V_O - V_{C1} - V_{\rm dc}}{\frac{N_S + N_P}{N_P}}. \tag{16}$$

Applying the volt-second balance to the magnetizing inductance L_m using (13) and (15), it then results in the following expression for computing V_{C2} as

$$\int_0^{DT_s} v_{\rm Lm}\,dt + \int_{DT_s}^{(D+D_L)T_S} v_{\rm Lm}\,dt = 0$$

$$\Rightarrow \quad V_{C2} = V_O - \frac{D + D_L}{D_L} V_{\rm dc}. \tag{17}$$

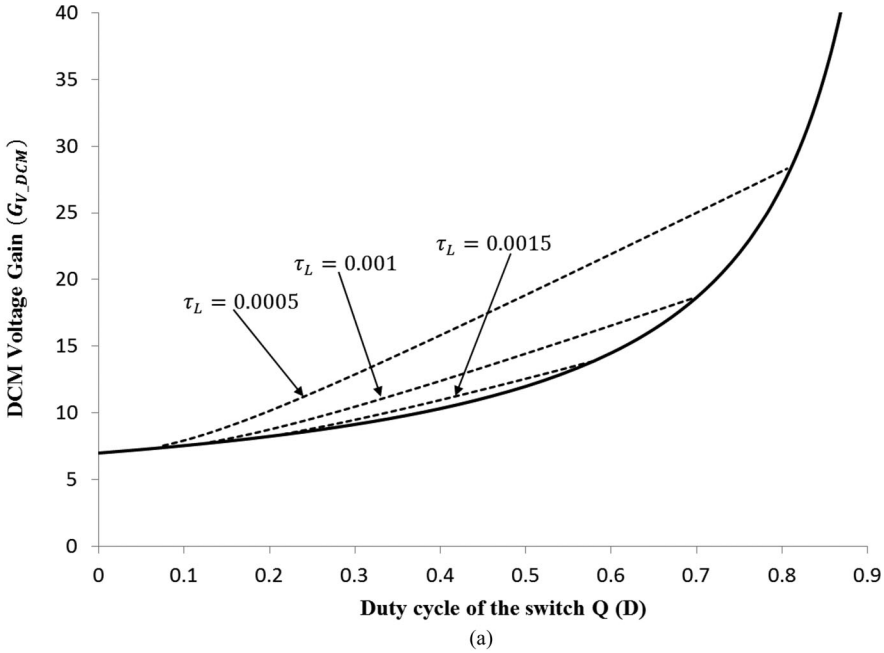
Now using (14) and (17), V_{C1} can be found as

$$V_{C1} = \left[\frac{N_S + N'_S}{N_P} + \frac{D + D_L}{D_L}\right] V_{\rm dc}. \tag{18}$$

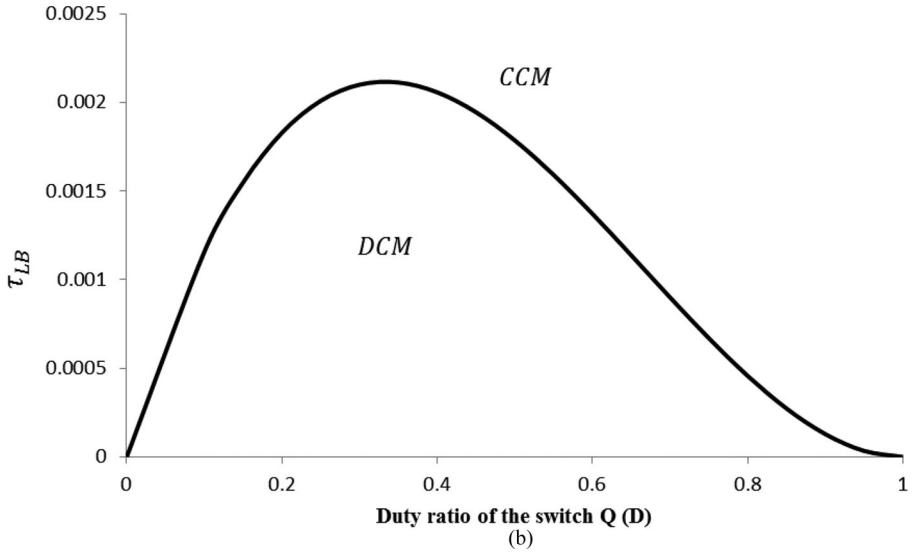
Using (18) and reapplying the volt-second balance to the magnetizing inductance L_m using (14) and (16), it results in the following expression to calculate D_L in Fig. 8:

$$\int_0^{DT_s} v_{\rm Lm}\,dt + \int_{DT_s}^{(D+D_L)T_S} v_{\rm Lm}\,dt = 0$$

$$\Rightarrow \quad D_L = \frac{D\,(1 \ - \ N)\,V_{\rm dc}}{V_o\,(N + m + 1)\,V_{\rm dc}}. \tag{19}$$



(a)



(b)

Fig. 9. DCM operation of the converter showing its (a) voltage gain versus duty ratio at various τ_L values, and (b) boundary normalized inductor time constant (τ_{LB}) versus the duty ratio of the switch ($N = 4$, $m = 2$).

Using (19), the voltage and current gain during DCM can be found by assuming $P_{\mathrm{in}} = P_O$ as

$$G_{\mathrm{V\_DCM}} = \frac{V_O}{V_{\mathrm{in}}} = (1 + N)\frac{D + D_L}{D_L} + m \tag{20}$$

$$G_{\mathrm{I\_DCM}} = \frac{I_O}{I_{\mathrm{in}}} = \frac{D_L}{(1 + N)(D + D_L) + mD_L}. \tag{21}$$

From Fig. 8, the average input current can written as

$$I_{\mathrm{in}} = \frac{v_{\mathrm{Lm}}}{2L_m} DT_S (D + D_L). \tag{22}$$

Using (20)–(22), the voltage gain expression of the converter during DCM can be derived as

$$G_{\mathrm{V\_DCM}} \approx \frac{N + m + 1}{2} + \sqrt{\left[\frac{N + m + 1}{2}\right]^2 + \frac{D^2}{2\tau_L}} \tag{23}$$

where the normalized inductor time constant τ_L is given as

$$\tau_L = \frac{L_m}{RT_s} = \frac{L_m f_s}{R} \tag{24}$$

where f_s is the switching frequency and *R* is the equivalent load resistance. Curves plotted using (23) are given in Fig. 9(a) for different τ_L values during DCM. They collectively confirm

TABLE I
VOLTAGE AND CURRENT STRESS ACROSS THE COMPONENT OF THE PROPOSED DC/DC CONVERTER

Components	Normalized Voltage Stress	Current Stress
Switch Q	$\frac{1}{1-D}V_{\rm dc}$	$\approx \frac{N+m+D}{D(1+N+m)}I_{\rm in}$
Diode D_1	$\frac{1}{1-D}V_{\rm dc}$	$\approx \frac{1}{1-D}I_O$
Diode D_2	$\frac{1}{1-D}\left[\frac{N_S+N_P+N'_S}{N_P}\right]V_{\rm dc}$	$\approx \frac{N+m+D}{ND(1+N+m)}I_{\rm in}$
Diode D_3	$\frac{N}{1-D}V_{\rm dc}$	$\approx \frac{1}{1-D}I_O$
Capacitor C_1	$\left[\frac{N_S+N'_S}{N_P}+\frac{1}{1-D}\right]V_{\rm dc}$	$\approx \frac{1}{1-D}I_O$
Capacitor C_2	$\frac{N+m(1-D)}{1-D}V_{\rm dc}$	$\approx \frac{N+m+D}{D(1+N+m)}I_{\rm in}$
Capacitor C_3	$\frac{N+m+D}{1-D}V_{\rm dc}$	$\approx \frac{N+m+D}{D(1+N+m)}I_{\rm in}$

that the converter is load-dependent because of τ_L. DCM is thus not recommended in general.

If the proposed converter is operated in the boundary condition mode, then the voltage gain of the CCM operation is equal to the voltage gain of the DCM operation. From (10) and (23), the boundary normalized inductor time constant $(\tau_{\rm LB})$ can be derived as

$$\tau_{\rm LB} \approx \frac{D(1\ -\ D)^2}{2\,(N\ +\ 1)\,(N+m+1)}. \tag{25}$$

Fig. 9(b) shows the plot of the boundary normalized inductor time constant versus the duty ratio under $N=4$, $m=2$. The proposed converter operates in CCM if $\tau_L > \tau_{\rm LB}$, and otherwise it operates in DCM.

D. Component Stress

From Fig. 6, the normalized voltage stress experienced by switch Q can be written as

$$V_{\rm dc} - {\rm v}_{\rm Lm} = v_Q$$
$$\Rightarrow \quad \frac{v_Q}{V_{\rm dc}} = \frac{1}{1\ -\ D}. \tag{26}$$

Similarly, voltage stress across diode D_1 can be derived as

$$v_{D1} = \frac{V_{\rm dc}}{1\ -\ D} \tag{27}$$

$$v_{D2} = \frac{V_{\rm dc}}{1\ -\ D}\left[\frac{N_S+N_P+N'_S}{N_P}\right] \tag{28}$$

$$v_{D3} = \frac{N}{1\ -\ D}V_{\rm dc}. \tag{29}$$

Other voltage stresses experienced by components of the converter are summarized in Table II. It is to be noted that the winding N_1 and switch are the only component in the converter with higher current stress $(i_Q \approx i_{\rm NP} \approx \frac{I_{\rm in}}{D})$, the rest of all other components (diodes, capacitors, and secondary windings of the coupled inductor N_S and N'_S) experience very low current $(\approx \frac{I_o}{1-D})$. This helps the proposed circuit to achieve a better efficiency even at higher voltage gain.

E. Proposed Converter Versus Other Converters

Table II summarizes some key features of the proposed converter along with other recent very high boost type dc–dc converters [9]–[36]. The expressions included in Table II are based on an ideal coupled inductor with zero leakage inductance (or $k=1$) and in CCM. Related voltage gains of the converters are plotted over a wide range of D in Fig. 10, which together with Table II shows the proposed topology producing a higher gain than most of the conventional topologies. For $D > 0.6$, the topology proposed in [13]–[15], [17], [30], and [33] has a higher gain. However, the lower duty cycle gain is much less than the proposed topology. In addition, [14] and [33] require an additional switch with higher voltage rating and [17] and [30] require additional diode and capacitor. The converter presented in [13] and [15] has also a higher gain for $D > 0.65$. However, the number of switch and inductor increases with the corresponding voltage stress [15]. On the other hand, the converter with quadratic boost expressions [22]–[24] has a higher gain at elevated duty cycle; however, the voltage stress on the switch increases exponentially. In addition, the extra diode and capacitor with higher rms current lead to a poor efficiency at higher voltage gain. In summary, the proposed converter has higher conversion ratio, lower switch voltage stress, and can be realized with a comparatively smaller number of components compared to other higher boost topologies (for comparison with other converter topologies $N_P = N_1$, $N_S = N_2$, and $N'_S = N_3$).

III. DESIGN GUIDELINES

A. Coupled Inductor

Figs. 7 and 9, and (10) can help to find the appropriate values for N, m, and D, while producing the desired voltage conversion ratio. It should be noted from the gain expression (10) that the primary turns are required to be low in order to achieve higher voltage gains. This not only increases the voltage conversion capability, but also helps to reduce the cupper loss in the high current side of the converter. Furthermore, the following equation helps to choose the proper dimension of the primary and secondary side winding wires with respect to power and voltage conversion ratio:

$$\left[\frac{I_{\rm NP}}{I_{\rm NS}}\right]_{\rm rms} \approx \left[\frac{I_{\rm NP}}{I_{\rm NS'}}\right]_{\rm rms} \approx \frac{1+N+m\,(1\ -\ D)}{\sqrt{D\,(1\ -\ D)}}. \tag{30}$$

In general, $N \geq 2$ and $m \geq 1$. Higher value of N ($N \geq 5$) with higher N_S results in higher rms winding ($i_{\rm NP}$, $i_{\rm NP}$, and $i_{\rm NS\prime}$) and switch (i_Q) currents, which also draws a higher rms current from the source. Fig. 11 illustrates the effect of N and m on the winding and switch currents with different N_S and N'_S, whilst keeping the same overall voltage gain and duty cycle. This higher N_S unnecessarily increases the conduction losses in the high current path of the circuit (consist of the primary winding and the switch). To mitigate this, the secondary winding of the coupled inductor N'_S should be increased in the range of $1 \leq N'_S \leq 4$ for a converter with a medium voltage gain ($G_v \leq 20$) requirement. A higher $N'_S > 5$ could lead to volumetric inductor with higher cost and lower power density. While choosing N and

TABLE II
COMPARISON OF THE PROPOSED CONVERTER WITH SOME OF THE HIGH STEP-UP DC–DC CONVERTER

References	Voltage Gain $\left(G_v = \frac{V_O}{V_{dc}}\right)$	Voltage StressonSwitch	No. of components				
			Coupled-inductor	Inductor	Diode	Capacitor	Switch
Proposed Converter	$\left[\frac{1+\frac{N_1+N_2}{N_1}}{1-D}+\frac{N_3}{N_1}\right]$	$V_{\rm dc}/(1-D)$	1	0	3	3	1
Converter in [9]	$\left[1+\frac{N_3}{N_1}+\frac{1}{1-D}+\frac{D}{1-D}\frac{N_2}{N_1}\right]$	$V_{\rm dc}/(1-D)$	1	0	3	4	1
Converter in [10]	$\left[\frac{2-D+\frac{N_2}{N_1}}{1-D}+\frac{N_3}{N_1}\right]$	$V_{\rm dc}/(1-D)$	1	0	4	4	1
Converter in [11]	$\frac{3+D}{1-D}$	$\frac{2V_{\rm dc}}{3+D}$	0	2	5	4	1
Converter in [13]	$\frac{D\left(2\frac{N_2}{N_1}+1\right)+1}{1-D}$	$V_{\rm dc}/(1-D)$	2	0	2	2	2
Converter in [14], [33]	$\frac{2\left(1+\frac{N_2}{N_1}D\right)}{1-D}$	$\frac{1+\frac{N_2}{N_1}D}{1-D}V_{\rm dc}$	1	0	4	2	2
Converter in [15]	$\frac{D\left(2\frac{N_2}{N_1}+1\right)+1}{1-D}$	$\frac{V_{\rm dc}+V_o}{2}$	2	0	7	1	2
Converter in [17], [30]	$\frac{1+\frac{N_2}{N_1}+\frac{N_2}{N_1}D}{1-D}$	$V_{\rm dc}/(1-D)$	1	0	4	4	1
Converter in [18], [19]	$\frac{1+\frac{N_2}{N_1}D}{1-D}$	$V_{\rm dc}/(1-D)$	1	1	2	3	1
Converter in [20]	$\frac{2+\frac{N_2}{N_1}}{1-D}$	$V_{\rm dc}/(1-D)$	1	1	3	4	1
[26], [29]			1	0	3	3	1
Converter in [21]	$\frac{2+(1-D)\frac{N_2}{N_1}+\frac{N_3}{N_1}}{1-D}$	$V_{\rm dc}/(1-D)$	1	0	5	5	1
Converter in [22]	$\frac{1+\frac{N_2}{N_1}}{(1-D)^2}$	$V_{\rm dc}/(1-D)^2$	1	1	5	4	1
Converter in [23]	$\frac{1+\frac{N_2}{N_1}D}{(1-D)^2}$	$V_{\rm dc}/(1-D)^2$	1	1	4	3	1
Converter in [24]	$\frac{2+\frac{N_2}{N_1}}{(1-D)^2}$	$V_{\rm dc}/(1-D)^2$	1	1	5	4	1
Converter in [28]	$\frac{2+\frac{N_2}{N_1}(1+D)}{1-D}$	$V_{\rm dc}/(1-D)$	1	0	3	3	1
Converter in [31]	$\frac{1+2\frac{N_2}{N_1}-\frac{N_2}{N_1}D}{1-D}$	$V_{\rm dc}/(1-D)$	1	0	3	3	2
Converter in [34]	$\frac{1+\frac{N_2}{N_1}+\frac{N_3}{N_1}}{1-D}$	$V_{\rm dc}/(1-D)$	1	0	4	5	1
Converter in [36]	$\frac{1+\frac{N_2}{N_1}}{1-D}$	$V_{\rm dc}/(1-D)$	1	0	3	3	1

m, the possibility of minimizing the leakage inductance should also be considered, which in [1] has suggested to be a bifilar winding method for improving coupling. Once this is done with *N* and *m* confirmed, an estimation of the converter duty cycle D can be inferred as

$$D = \frac{G_{\rm v\_CCM} - (1+N+m)}{G_{\rm v\_CCM} - m}. \tag{31}$$

Usually, *D* should be smaller than 75% of its maximum value. Similar to the conventional dc–dc converter, the loss beyond 75% duty cycle becomes higher due to the large current drawn from the source.

B. Active Switch and Diode

Voltage and current ratings of the active and passive components can be deduced from Table I. While deciding, it should also be noted that although diode D_1 and capacitor C_2 with the load resistor help to curb voltage spikes across the switch, there will still be some small spikes, in practice, caused by stray inductances and capacitances. This requires an ultrafast Schottky diode with both small forward and reverse recovery times. To retain a comfortable safety margin, voltage and current ratings of the selected power devices should, therefore, be set at 150% of their theoretically computed values.

It should also be noted that the switch Q is also burdened by the large input current $I_{\rm in}$ and it is primarily considered with respect to the cost and the efficiency. As presented in (32) and Fig. 12, the rms value of switch current is decreased as the duty cycle D increases. This means a larger D is of the benefit for reducing the switch conduction loss. However, this will increase the switch voltage stresses (26), and requires higher voltage switch having larger ON-resistance in return. As a result,

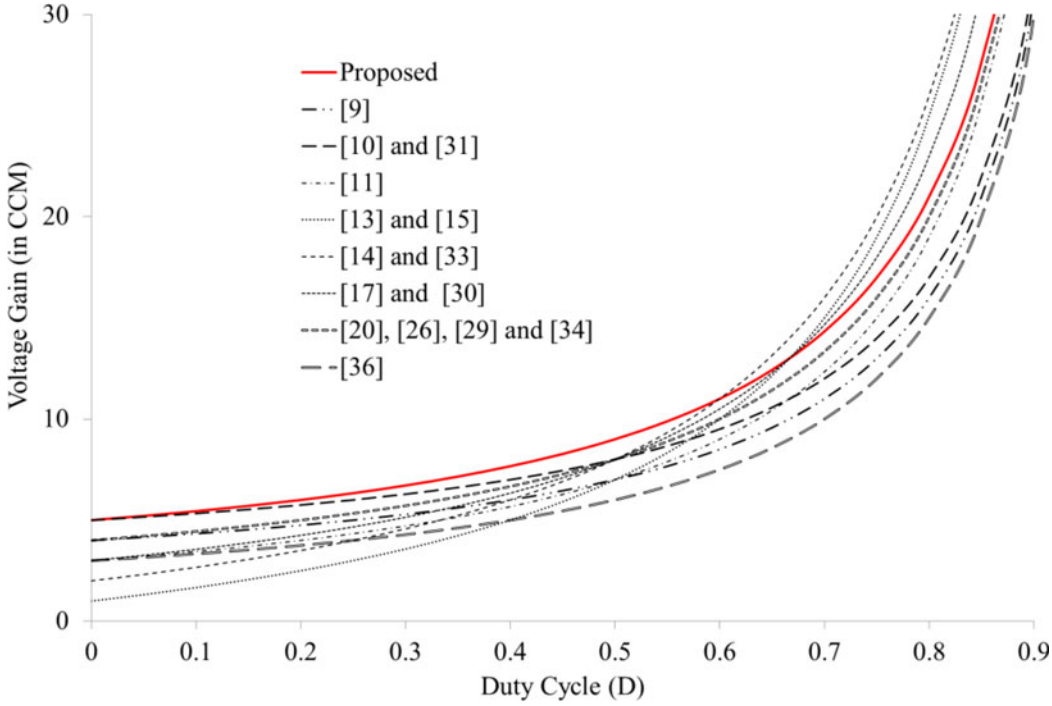


Fig. 10. Comparison of voltage gain of the proposed converter with different high boost dc–dc converters in CCM ($N_1 = 1,\ \ N_2 = 2,\ \ N_3 = 1$).

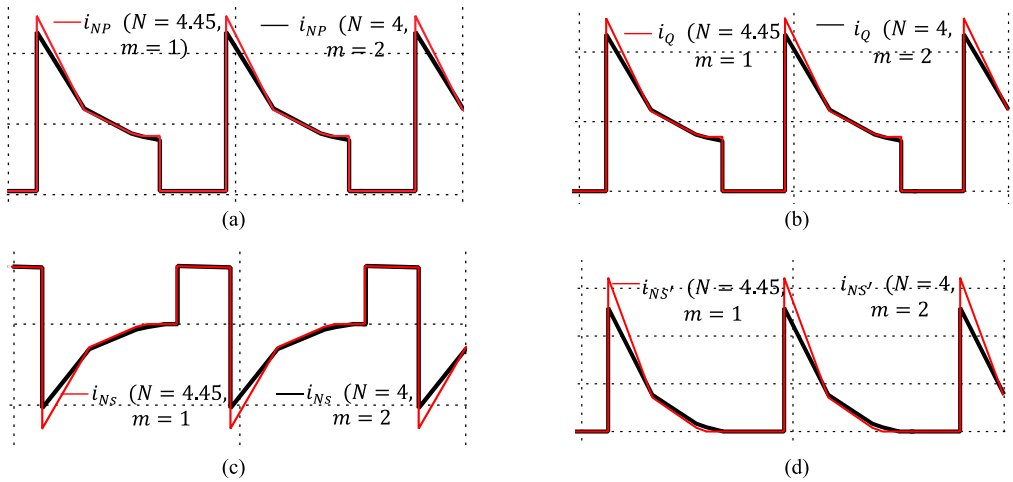


Fig. 11. Illustration of the effect of *N* and *m*; specially, the secondary winding turns N_S and N'_S on winding and switch current, whilst keeping the same overall voltage gain and duty cycle ($G_v = 16,\ D = 0.65$): (a) current through N_P ($i_{\rm NP}$), (b) current through switch Q (i_Q), (c) current through N_S ($i_{\rm NS}$), and (d) current through N'_S ($i_{\rm NS\prime}$). The solid line shows the current with lower *N* and high *m* (1:3:2) and the dash line shows the current with higher *N* and lower *m* (1:3.35:1).

a compromise should be made to have low voltage stress, while still having a low rms value of the switch current:

$$I_{\rm Qrms} \approx \frac{G_{\rm V\_CCM} - 1}{\sqrt{D}} I_O. \tag{32}$$

C. Capacitor

Capacitors are sized mainly according to their permitted voltage ripples during the $t_{\rm on}$ interval. Assuming a common permitted capacitor ripple voltage of $\Delta VC \le x\% \times VC$, $C > P_{\rm max}/(V_C \Delta V_C f_s)$ can hence be used for computing the capacitances. Another parameter that needs to be determined is the rms current through the capacitor, so that the capacitor $I_{\rm rms}$ rating is not exceeded. From the capacitor current waveforms, the rms current through C_1, C_2, and C_3 can be calculated approximately as

$$I_{C1\rm rms} \approx \sqrt{\frac{D}{1-D}} \frac{1}{G_{\rm V\_CCM} - 1} I_{\rm in} \tag{33}$$

$$I_{C2\rm rms} = I_{C3\rm rms} \approx \sqrt{\frac{D}{1-D}} \frac{m}{G_{\rm V\_CCM} - 1} I_{\rm in}. \tag{34}$$

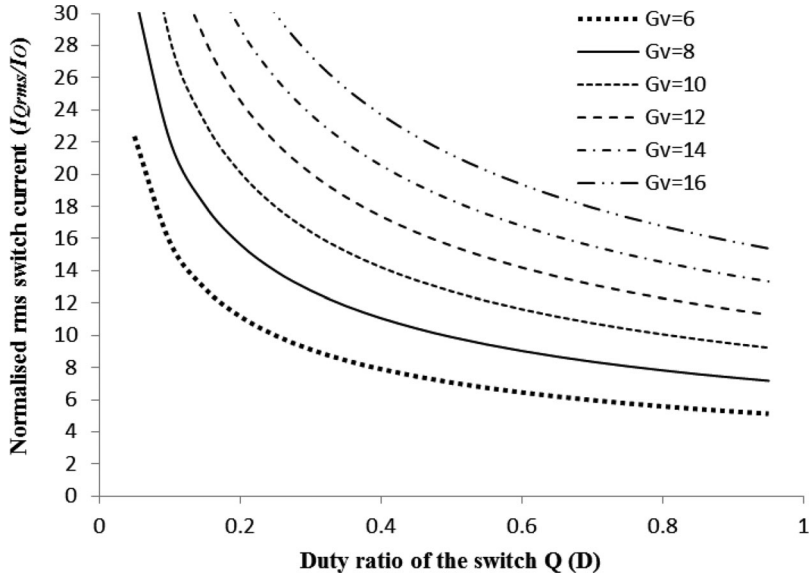


Fig. 12. Normalized rms current of the switch Q ($I_{\mathrm{Q\,rms}}/I_O$) at varying voltage gain of the converter (G_v) and duty ratio (D).

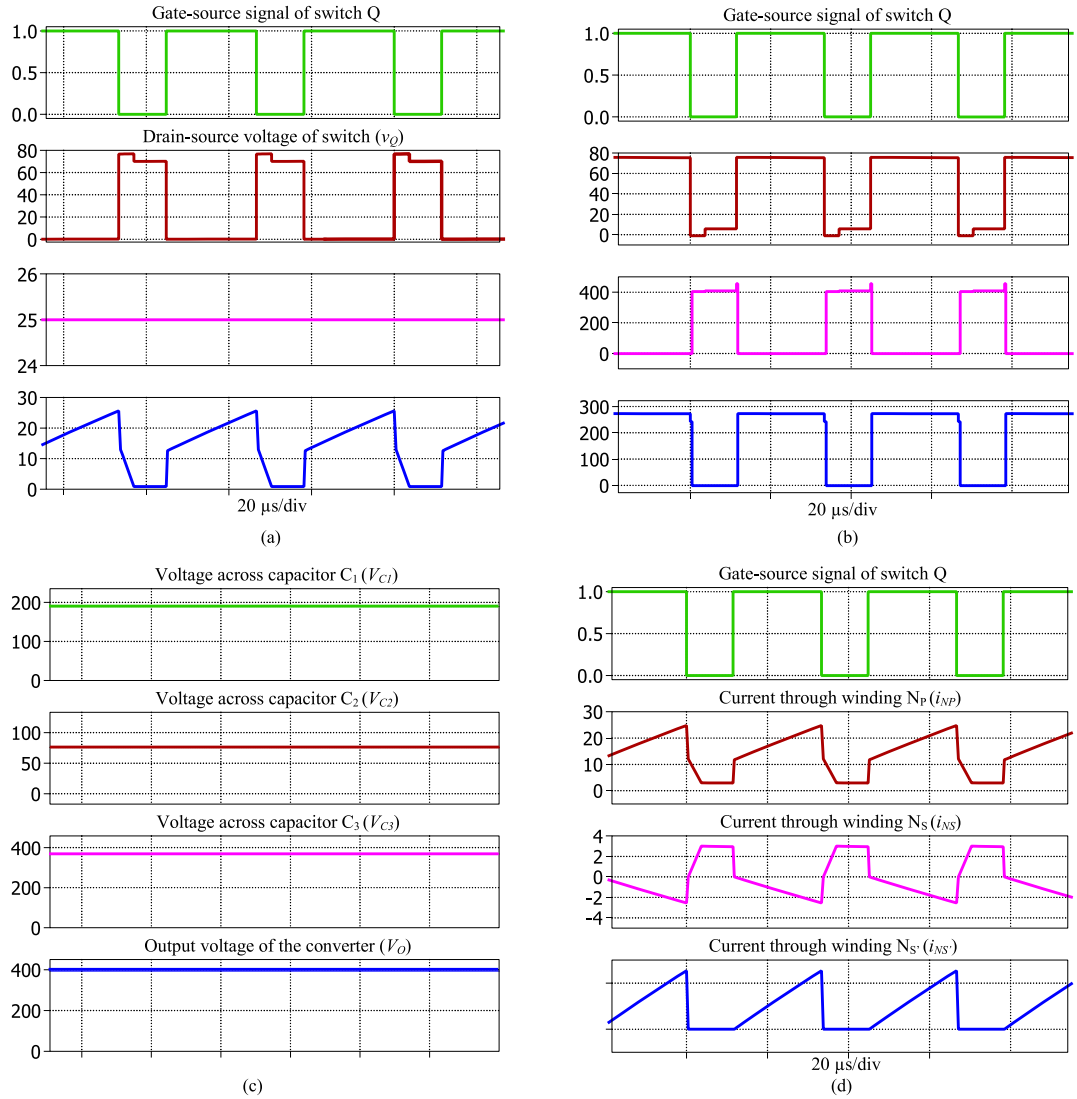


Fig. 13. Simulated waveforms of the proposed converter at $N = 4$, $m = 2$, $D = 0.65$, $V_{\mathrm{dc}} = 25$ V, and $f_s = 30$ kHz a full load: (a) input–output voltage current waveforms, and (b) switch Q and diode D_1 voltage and current waveforms.

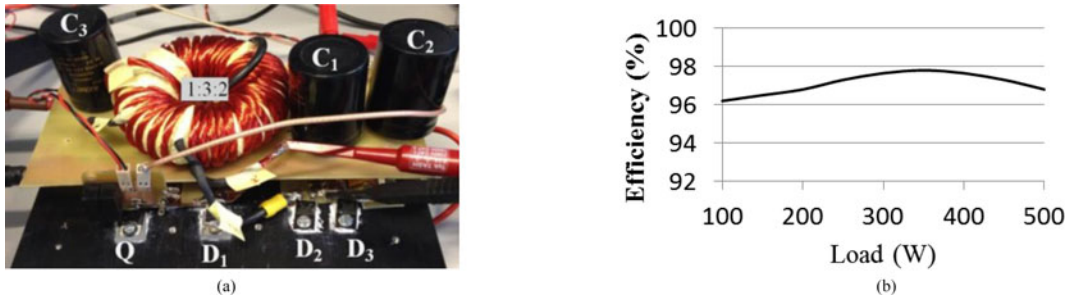


Fig. 14. (a) A 500-W experimental prototype of the proposed ultra-step-up dc–dc converter with (b) efficiency over a wide load range (at $V_{\rm dc} = 50$ V and $V_O = 400$ V).

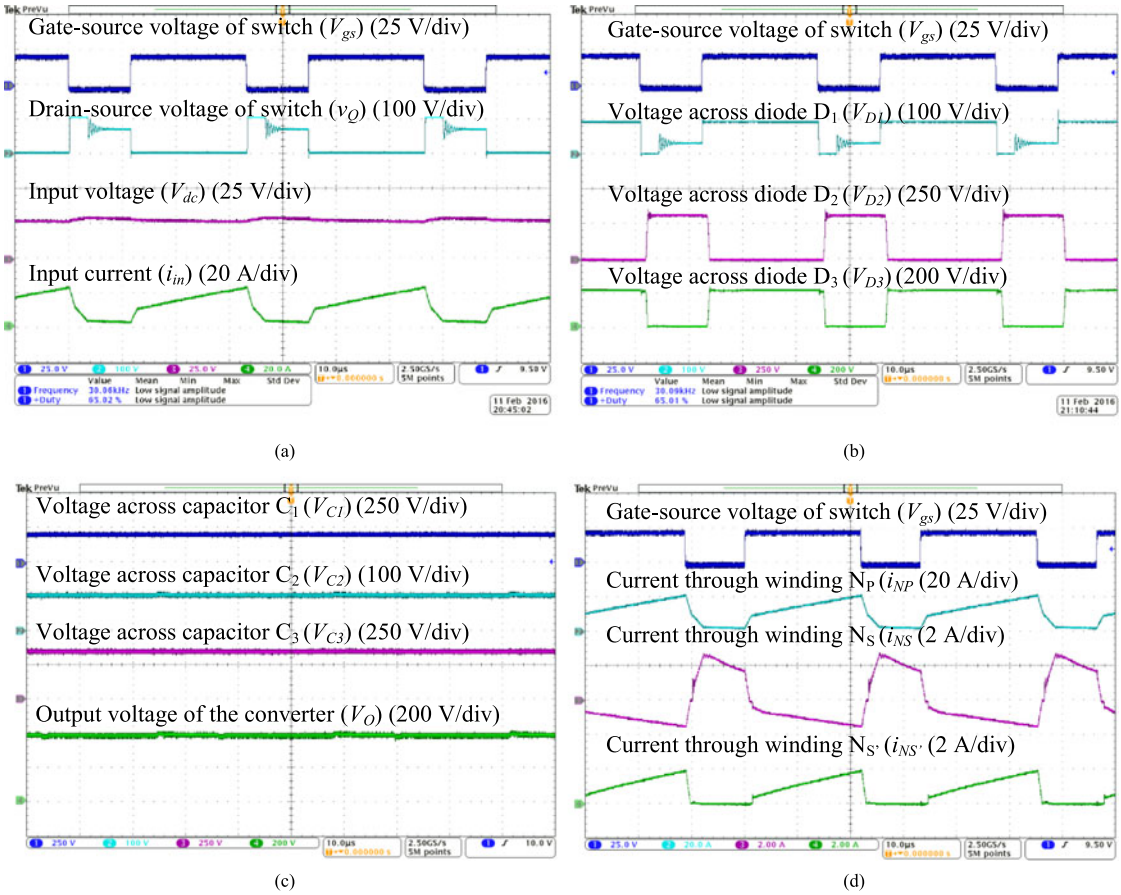


Fig. 15. Key experimental waveforms of the proposed dc–dc converter at $N = 4$, $m = 2$, $D = 0.65$, $V_{\rm dc} = 25$ V, and $f_s = 30$ kHz and 500 W load.

Usually aluminum electrolytic capacitors are used, whose ESR reduces with increasing capacitance. It may, therefore, help to have larger capacitances than those computed theoretically to keep low losses. Larger capacitances may also help to lengthen the holding time of the converter in cases of disturbances, which at times, may be necessary.

IV. Simulation and Experimental Results

Simulations were carried out in MATLAB-Simulink with PLECS toolboxes included to verify the performance of the proposed converter. The converter was simulated with $N = 4$, $m = 2$ ($N_P : N_S : N'_S = 1 : 3 : 2$), $D = 0.65$, and $f_s = 30$ kHz. With these conditions, the output voltage is boosted

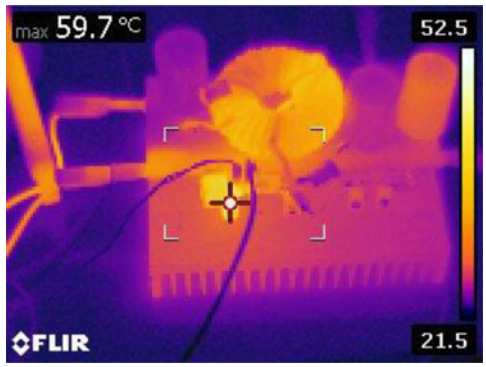


Fig. 16. Thermal image of the proposed dc–dc converter at a rated load of 500 W with $V_{\rm dc} = 25$ V and $V_O = 400$ V.

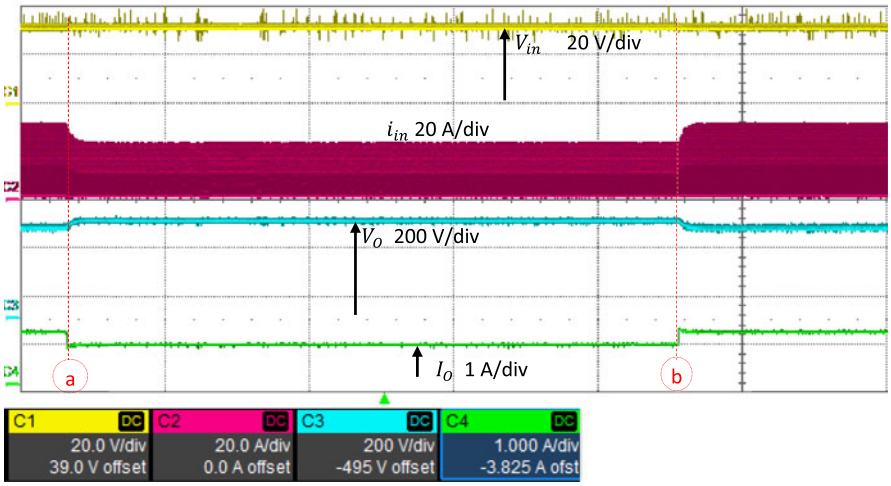


Fig. 17. Waveforms showing variation of load change from full load to half load and back to full load ($N = 4,\ m = 2, D = 0.6, V_{\rm dc} = 30$ V).

to $V_O = 398$ V for $V_{\rm dc} = 25$ V, which is consistent with (10) as shown in the fourth trace of Fig. 13(c). The drain source voltage of the switch is around 70 V as shown in the second trace of Fig. 13(a), which helps to select a low voltage and a low $R_{\rm DS-on}$ switch. Other simulated waveforms are also noted to be in agreement with the theoretical values derived in Section II. Performances expected from the converter are thus smoothly verified in simulations.

A 500-W experimental prototype as shown in Fig. 14(a) has been built in the laboratory to confirm the analysis and theory presented in Section II. Considering the size, loss, and ripple current as discussed in Section III-A, an integrated autotransformer-type coupled inductor was designed with 20:60:40 turns (11AWG wire on $N_{\rm p}$ and 18 AWG wire on N_S and N_S') on a C055863A2 MPP (molypermalloy powder). As the midpoint of the coupled inductor is tied directly to the switch Q and diode D_1, its coupling must be tightly ensured to minimize the leakage inductances seen at its windings. This can be done by following the winding design and style as used in [39]. The toroid core with distributed air gap used in the prototype improves coupling and reduces leakage inductances in the circuit [40].

Furthermore, a low voltage and low $R_{\rm DS-on}$ switch from NXP semiconductors PSMN5R6 (100 V, 100 A, 5.6 mΩ), diode D_1 43CTQ100 (100 V, 40 A), diodes D_2 and D_3 STTH20R04FP (400 V, 20 A), capacitors $C_1 - C_3$ (220 μF, 400 V) are used based on the design guidelines as discussed in Section III-A.

With these conditions and design, the output voltage was boosted to $V_O = 400$ V at $D = 0.65$ for an input voltage of $V_{\rm dc} = 25$ V, which is consistent with (10) as shown in the fourth trace of Fig. 15(c). The drain source voltage of the switch is around 90 V as shown in second trace of Fig. 15(a), which helps to select low voltage and a low $R_{\rm DS-on}$ switch. Other measured waveforms are also noted to be in good agreement with the simulation and the theoretical values derived in Section II. Also, the measured efficiency of the converter is above 96% and almost flat over a wide range of the load as shown in Fig. 14(b). Hence, the performances expected from the converter are thus smoothly verified.

For an overview of the converter loss distribution, a thermal image of the experimental prototype operating at rated 500 W in the steady state was captured and shown in Fig. 16. The high current and corresponding I^2R loss in the primary winding of the integrated coupled inductor and the switch contributes to the highest power loss among other components; however, the temperature remains stable after 60°C. All diodes and capacitors remain cool and do not even require a heat sink.

The converter response with the change in load is shown in Fig. 17. The load is changed from full load to 65% of the full load (at point a) and back to full load (at point b). The input current as well as the load current switches from full to 65% of the full and back again to full current corresponding to changes in load. The output voltage remains almost stable ($\Delta V_{\rm O}$ is $< 5\%$ of $V_{\rm O}$) with these load variation, which shows the robustness even under the open loop condition. The input voltage remains stable throughout the load changes.

Fig. 18 shows the frequency response (control-to-output notated as $G_{\rm vd} = \hat{v}_O/\hat{d}$) of the proposed dc–dc converter simulated in MATLAB. This corresponds well with the transfer function approximated below in Laplace domain as

$$G_{\rm vd}(s) = \frac{\widehat{v_0}}{\hat{d}} \approx \frac{2.24 \times 10^4 s^2 + 9.6 \times 10^5 s + 2.5 \times 10^9}{s^3 + 162.5 s^2 + 3.2 \times 10^5 s + 5 \times 10^6}. \tag{35}$$

The response shows that the converter is stable, as its gain crossover frequency is smaller than its phase crossover frequency. The responses show that the converter is stable, as its gain at the phase crossover frequency is smaller than 0 dB (i.e., with gain-margin of ≈ 20 dB), and its gain crossover frequency is smaller than its phase crossover frequency (with phase-margin of 70°). The responses have, however, been burdened by nonminimum-phase behavior, characterized by a phase range exceeding 90°. This needs to be considered while designing the closed loop control of the system. The same observation has also been observed with a general boost converter at a high duty cycle [38], which certainly is expected since they are all converters with boost ability.

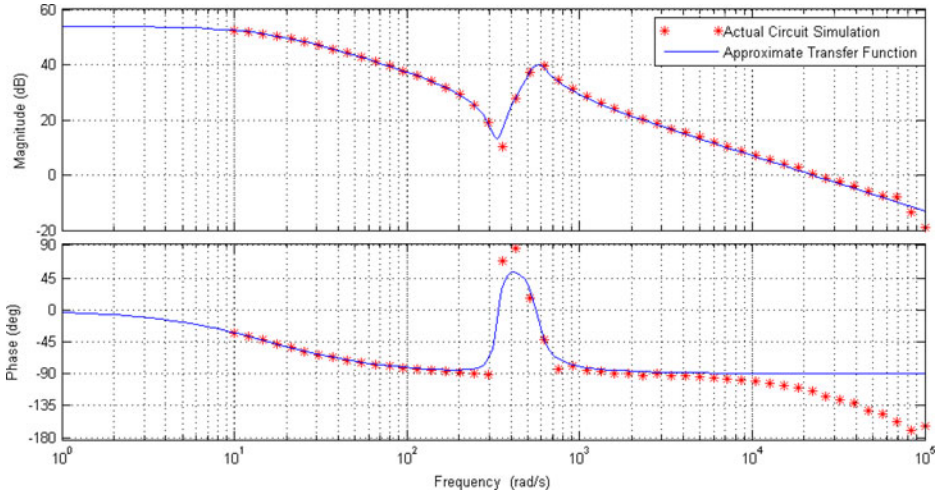


Fig. 18. Frequency responses (control-to-output, G_{vd}) plot of the converter.

V. Conclusion

A high step-up single-switch dc–dc converter with high voltage gain and reduced switch voltage stress is proposed in this paper using an integrated autotransformer and a coupled inductor. The converter was realized using low voltage and low $R_{\mathrm{DS-on}}$ switch, which helps to improve the efficiency. Experimental results have verified the principle of operation and confirmed the presented theoretical analysis. The measured efficiency of the converter over a wide range of load is above 96%, which is comparatively higher than the conventional converter at similar voltage gain and power level. These demonstrated performances clearly stand out the proposed topology as a competitive alternative for a practical application where a high voltage gain is demanded, such as for a fuel cells and high voltage LED lamps.

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