Control of Modular Multilevel Converter With Parallel Connectivity—Application to Battery Systems

Stefan M. Goetz, Zhongxi Li, Xinyu Liang, Chengduo Zhang, Srdjan M. Lukic*, and Angel V. Peterchev*

***Abstract*—This paper presents a multiobjective real-time controller for a modular multilevel converter capable of parallel module connectivity, the so-called modular multilevel series parallel converter (MMSPC). The MMSPC topology allows the batteries to be dynamically rewired in various series–parallel configurations, generating a wide range of output voltage levels. The novel control method parallelizes the modules to balance their voltages without the need for individual module voltage monitoring. Additionally, the controller optimizes across the large number of feasible system configurations to minimize switching and conduction losses. Finally, the controller efficiently encodes the system configuration with module interconnection states rather than the module switch states, which substantially simplifies control. Furthermore, this work experimentally validates the MMSPC topology and concept. In the prototype, the parallel mode reduced the system losses at 5 kW output power by 18% and 24% for load power factors of 1.0 and 0.8, respectively. Sensorless balancing via parallelization maintained well-matched module voltages (standard deviation = 0.045 V) over a 5-h battery discharge with highly variable load current. The reduced conduction losses and simple balancing capability of the MMSPC can enable new applications at medium and low voltages that benefit from its high-quality output, elimination of filtering magnetics, fast response, and modularity.**

***Index Terms*—Balancing, battery, modular multilevel converter (MMC), modular multilevel series parallel converter (MMSPC), switched-capacitor converter.**

I. Introduction

THE modular multilevel converter (MMC) has become common in high voltage and power applications due to several advantages [1]–[7]. The MMC splits the system voltage into a sum of lower voltages, each provided by a separate module. This enables the use of efficient and cost-effective low-voltage passive and active components in the modules. Moreover, the modules are identical, which simplifies design as well as manufacturing, and renders the converter easily scalable for various system voltage ratings. The output waveform is of exceptionally high quality due to the practicality of a large number of levels. For high availability of the system, redundancy modules are typically added which remain in bypass mode until they have to replace a failed module [2].

However, MMC has limitations that can present significant challenges in some applications. It essentially has two operating states: the series state, in which the module storage element is presented in series to the other modules, and the bypass state, in which current is directed around the storage element so that the module does not contribute to the total system voltage. Unfortunately, in bypass state the module introduces conduction loss due to the on resistance of the module switches. Thus, at low system voltages the large number of modules in bypass mode can reduce the efficiency of the converter. The presence of redundancy modules to increase reliability further aggravates this issue during normal operation [2], [8], [9]. The series connectivity of modules is particularly detrimental if the storage elements have high energy density but also high effective series resistance as in electrolytic capacitors or battery cells which have been proposed for grid storage applications with MMC technology [10]–[13].

Another disadvantage of MMC is the requirement to balance the individual module voltages [14]. The voltage distribution among the modules during operation depends on the modulation scheme, storage element losses, and the load profile. If a module storage element is overcharged, it as well as the electronics of that module could be damaged. If, on the other hand, the storage is discharged below a certain limit, the power supply of the module, which usually receives its power from the module capacitor, may turn OFF and render the module uncontrollable. In consequence, MMCs typically monitor the charge level of each module storage element to prevent a charge imbalance [15]. A scheduler decides which modules are active or bypassed, dependent on their individual voltage level and the direction of the power flow [1], [16]. Since this requires knowledge of each module's voltage at high speed, most systems implement fast voltage sensors at each storage element, which is typically a capacitor, and transfer all data to the central controller [17]. However, the requirement of a Galvanically isolated signal transmission to the controller, a high number of modules, and a low latency render monitoring expensive.

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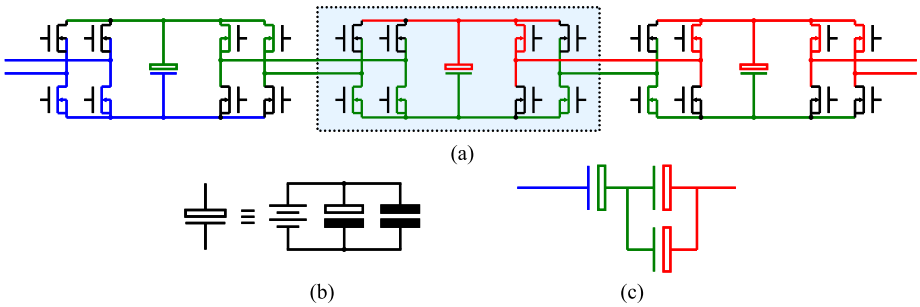


Fig. 1. Circuit topology of three neighboring MMSPC modules, illustrating a representative connection state. The color code indicates parts of the circuit that are connected together, resulting in the connection pattern of the simplified wiring diagram shown at the bottom. The storage element can be a capacitor, a battery, or a combination of both. The prototype in this paper uses a battery as the main storage element in parallel with filtering capacitors, consisting of a ceramic capacitor for fast and electrolytic capacitor for slower frequency components.

Numerous completely or partially sensorless strategies to avoid or reduce the effort for expensive monitoring have been proposed, but they typically either rely on stationary cyclic load conditions that would average out charge imbalance during unobserved shuffling of the capacitors or require a measurement of the current to estimate the charge inflow and outflow of each module [18]–[27]. For instance, a number of methods for rotating the modules within a power-line cycle have been proposed [20], [25]–[27]. Ängquist *et al*. suggested a sophisticated open-loop charge estimator for the module storages based on the measured phase current which is assumed to be sinusoidal with negligible distortion, transients, or offset [18], but this approach could be highly sensitive to accurate knowledge of parameters and drift [19]. The actual waveform of the load current can be used instead, in conjunction with estimates of the module capacitances [19]; however, the current integration necessary to estimate charge is sensitive to measurement offsets, which can destabilize the system over time.

Addressing these limitations of MMC, we recently proposed a novel topology that enables parallel connectivity between the modules, forming a modular multilevel series parallel converter (MMSPC; see Fig. 1) [28]. The MMSPC module is an extension of the MMC full-bridge module, which has four-quadrant capability. In contrast to other solutions that integrate parallel connectivity into the MMC [29]–[32], the MMSPC supports parallel connectivity across more than two modules and has a simple module structure. As in the conventional MMC, the operating voltage of each module component is the module voltage. An MMSPC module has twice as many switches, but in each state two switches in parallel share the load current: in bypass state both low- or high-side switches, in series state the adjacent low- or high-side switches, and in parallel state one low-side and one high-side switch. Thus, each switch has half the current rating compared to conventional MMC, and compared to MMC the total semiconductor switch area is the same [28]. The parallel module state confers the MMSPC properties that are analogous to switched-capacitor converters. It can reduce the converter source impedance by always utilizing the storage elements of all available modules. As well, parallelizing modules reduces the charge/discharge dynamics and enables simple sensorless module voltage balancing. Using these advantages, monitoring effort and control complexity can be reduced compared to MMC. Moreover, as the MMSPC incorporates all available modules at all times to achieve lowest source impedance—in series for high output voltages or in parallel for low output voltages—it enables unmatched efficiency over a wide range of modulation indices. In consequence, the modulation index of each individual module can be increased compared to conventional MMC with its amplitude-dependent use of modules, which deteriorates at low output levels and reactive load. Similarly, the parallel connectivity can make better use of redundancy modules to reduce the average load per module, whereas they even increased the losses in MMC. The same advantages over MMC can be achieved if the principles of the full-bridge MMSPC are applied to a half-bridge module in applications where four-quadrant module operation is not required. The advantages of the MMSPC could make it practical for combined battery energy storage and conversion as well as other applications extending to low- and medium voltages such as motor drives and integrated circuits.

Previously, we evaluated the MMSPC theoretically and predicted its characteristics [28]. In this paper, we propose a control that enables sensorless balancing and a tradeoff of multiple objectives in real time due to a rapid elimination of state alternatives. In contrast to our previous evaluation of capacitor-based MMSPCs, we describe the implementation of an energy storage system that incorporates batteries in the modules, while still providing flexible, high-quality output. We furthermore substantially simplify the MMSPC control by introducing an efficient new encoding of states that represents the module interconnections instead of the individual module switches. Based on this orthogonal state encoding, the MMSPC is controlled with a novel technique that optimizes various aspects of performance including switching and conduction losses as well as module balancing. The method translates objectives into constraints for the rapid elimination of a high number of suboptimal state alternatives. The elimination ultimately renders the predictive optimization method computationally manageable on available controller hardware. We show through analysis and experiments that the parallel state accomplishes balancing of the module voltages without any required sensing, and reduces the source impedance without affecting the switching losses, therefore

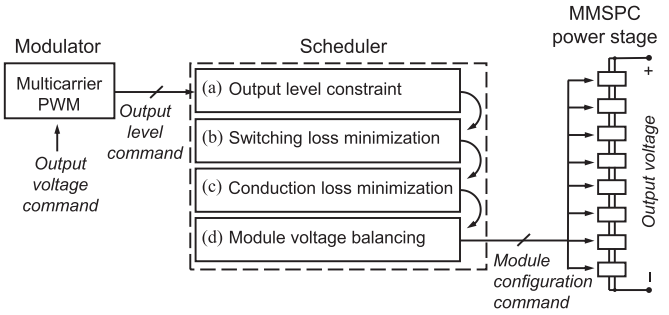


Fig. 2. Block diagram of the system control, incorporating a modulator and a scheduler that addresses four constraints or objectives. (a) Correct output level. (b) Low switching loss. (c) Low conduction loss. (d) Module balancing. In this implementation, the objectives are evaluated subsequently. The number of module configuration options remaining after each constraint/objective is fulfilled are illustrated in Fig. 4.

improving efficiency. In contrast to the MMSPC control approach proposed previously, which requires sensing of each module's voltage and the currents through each charge-storage element [28], monitoring these quantities is generally unnecessary with the method introduced here, making the MMSPC more practical for medium and low power applications.

II. Control Approach

A. Overview

Figure 2 summarizes the structure of the MMSPC controller which carries out several tasks. It ensures that the output voltage follows the specified reference and that the module voltages are balanced. Furthermore, it uses the additional degrees of freedom of the converter to optimize performance by keeping the conduction and switching losses low. These tasks are split between a modulator that determines the discrete output voltage level based on a reference signal and a scheduler that decides how the individual modules are connected to achieve that output. The scheduler is necessary since there are multiple ways to connect the modules that result in the same output voltage level.

Stable long-term operation requires that the scheduler ensures a balanced state with absolute certainty—no module may drift to overly high voltages or be depleted. In the proposed control approach, this requirement is achieved by parallelizing modules frequently enough so that the voltage levels of the energy storage elements equilibrate. This method is akin to capacitor parallelization in switched-capacitor converters. It does not need to keep track of the individual module voltages or charge inflows and outflows. It can ensure a balanced state by minimizing the time it takes an individual module to be parallelized with its neighbors. Since the scheduler balances the modules, the modulator can assume that the modules contribute approximately the same voltage step size to the output.

In addition to balancing, the scheduler minimizes the converter losses. The latter are dominated by switching and conduction loss, whereas parallelization losses are negligible if the modules are balanced, i.e., if the main objective of the scheduler is fulfilled [28]. The treatment of the control constraints and objectives is detailed in Section II-C.

B. Orthogonal Encoding of Interconnection States

The encoding of converter states has substantial influence on control complexity. In MMSPC, nine module states are necessary to encode directly the useful switch configurations of each module including the parallel state [28]. However, the number of converter states increases exponentially with the number of states per module, resulting in potentially high control complexity and computational burden. Furthermore, the feasible states of a module depend on the states of the neighboring modules. For instance, a parallel state of one module has to be matched with a parallel state of its neighbor for proper function. If across an interconnection one module is in series state and the adjacent module is in parallel state, then a short would occur. Therefore, the controller has to track module state interactions between modules to prevent invalid module state combinations, which complicates controller design.

Addressing this issue, instead of encoding the module switch states directly, we propose to encode the state of the interconnection between two adjacent modules. This reduces the number of states almost by half and simplifies the code book, which maps each useful interconnection state to a unique identifier. To provide all functionality of MMSPC, the code book requires only five states per interconnection site, illustrated in Fig. 3. The interconnection states include **s**+ (series connection of the energy storages of the two adjoining modules with positive polarity), **s–** (series connection of the energy storages of the two adjoining modules with negative polarity), **b** (bypass of at least one energy storage, i.e., no increase of the output voltage), **0** (all switches of the interconnection site are deactivated, only diodes are available), and **p** (parallel connection). Thus, the interconnection states are only one more (the parallel state) than the conventional MMC.

These five interconnection states are orthogonal, i.e., they do not directly interact with the states of other interconnections. Thus the state of one interconnection does not limit nor determine the state of any other interconnections. Consequently, using the predefined set of interconnection states simplifies communications and control, and ensures that an invalid interconnection state that may lead to a short is not encoded and therefore cannot occur in the controller commands. Furthermore, interconnection states **b** and **p** can be implemented with an alternative which is given by the inverse of each switch's state. The bypass current, for instance, can be conducted either on the high side or on the low side of the module. These alternatives are topologically equivalent and could be cycled in the control implementation in order to distribute the load among all switches, thus avoiding faster ageing of some switches.

C. Constraints and Objectives

1) Output Voltage Level: The foremost constraint of the scheduler is to produce an output voltage level matching the modulator command. For a converter with N modules and modulator command for an output level of m module steps, the scheduler should form m series-connected groups each comprising $n_1 \ \ldots \ n_{\mathrm{m}}$ parallel-connected modules, where $\sum_{i=1}^{m} n_i =$

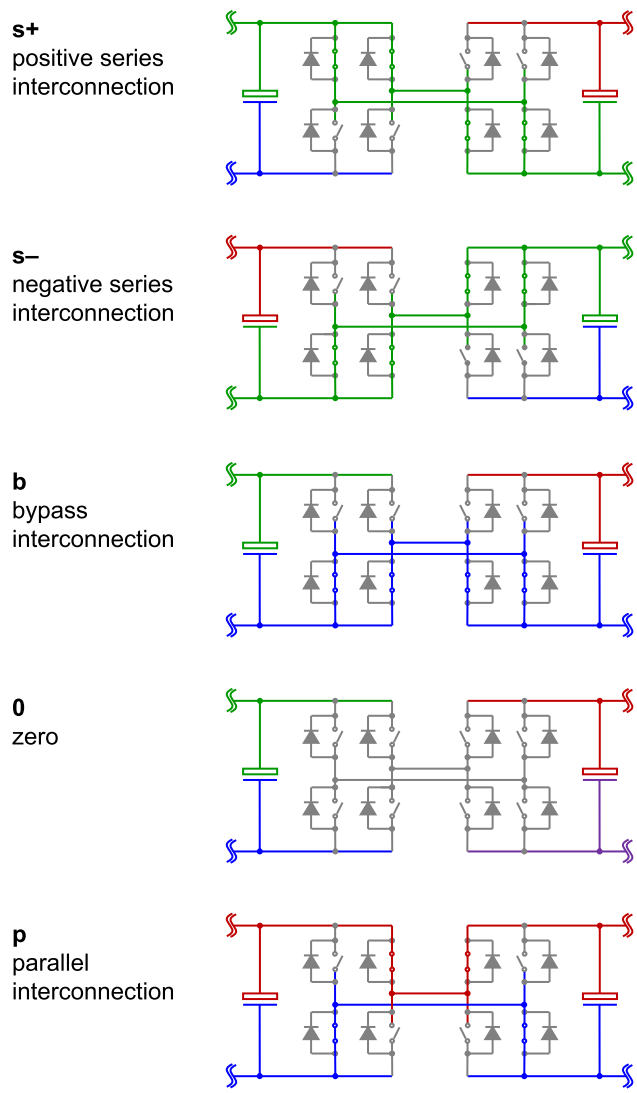


Fig. 3. Most important interconnection states of two neighboring MMSPC modules. The state of active semiconductors is represented with a simple switch. The color code indicates parts of the circuit that are connected together.

N. For this constraint, the number of options is $\binom{N}{m}$, which is less than both the total number of possible converter states, 5^N, as well as the total number of states excluding the trivial bypass and zero states, 3^N.

2) Switching Loss: One performance objective is to minimize switching loss which is proportional to the number of switches that have to be toggled for the transition from one system state to the next. Except for a voltage polarity change of an interconnection, i.e., a transition from a negative series connection (**s–**) to a positive series connection (**s**+) or vice versa, which toggles all eight switches, any other state transition affects four switches. Let the state of the *N*-module converter at time *t* be represented by the vector

$$v^t = (v_1^t, \ldots, v_N^t) \in \{\mathbf{s}+, \mathbf{s}-, \mathbf{p}, \mathbf{b}, \mathbf{0}\}^N \tag{1}$$

describing $N-1$ module interconnections plus one load connection. When module interconnection *j* is switched from state v_j^{t-1} to v_j^t, the number of toggled switches is

$$\delta_j^t = \begin{cases} 0 & \text{for } v_j^{t-1} = v_j^t \\ 8 & \text{for } v_j^{t-1} = \mathbf{s}-, v_j^t = \mathbf{s}+ \ \vee \ v_j^{t-1} = \mathbf{s}+, v_j^t = \mathbf{s}- \\ 4 & \text{otherwise.} \end{cases} \tag{2}$$

Thus, the total number of switch transitions is

$$\Delta^t = \sum_{j=1}^{N} \delta_j^t. \tag{3}$$

Since the current per toggled switch is approximately half of the module current (which equals the load current in this application), the switching loss is directly proportional to the number of toggled switches in the converter, for both the saturation and capacitive switching loss of typical field-effect transistors (FETs) and insulated-gate bipolar transistors

$$E_{\text{loss,sw}}^t = \Delta^t \cdot \left(\underbrace{\tfrac{1}{2} V_\text{m} I \cdot (t_\text{on} + t_\text{off})}_{\text{saturation loss}} + \underbrace{\tfrac{1}{2} V_\text{m}^2 \cdot (C_\text{gd} + C_\text{ds})}_{\text{capacitive loss}} \right) \tag{4}$$

where V_m is the module voltage, *I* is the load current, t_on and t_off are the switch turn-ON and turn-OFF times, and C_gd and C_ds are the gate–drain and drain–source capacitances, respectively. Therefore, to minimize switching loss the scheduler has to minimize the total number of switching transitions, Δ^t.

3) Conduction Loss and Source Impedance Minimization: Another objective is to minimize internal and conduction loss. For this objective, the converter should select a series–parallel configuration of its modules that results in the minimum overall source impedance for the specified output voltage. This condition is met when the number of parallel connected modules, n_i, is as equal as possible across the *m* series-connected module groups required for the specified output voltage. For example, a configuration with seven paralleled modules in series with a single module has approximately 129% higher impedance than two series-connected groups of four paralleled modules. Therefore, the optimum distribution $n_1 \ldots n_m$ among the *m* groups is

$$\min_{N = \sum_{i=1}^{m} n_i} \sum_{i=1}^{m} \frac{1}{n_i} \tag{5}$$

which is equivalent to minimizing the variance of n_i.

4) Parallelization Loss: Similar to switched-capacitor circuits, each parallel connection of two or more charge storages with unequal initial open-circuit voltage results in energy loss, which is independent from the resistance of the equalization loop in the first approximation. The loss associated with connecting in parallel two energy storage elements with unequal voltages follows

$$E_{\text{loss,par}} = \tfrac{1}{4} C_\text{m} \Delta V_\text{m}^2 \leq \tfrac{1}{4} C_\text{m} \left(\frac{I\tau}{C_\text{m}} \right)^2 \propto \frac{\tau^2}{C_\text{m}} \tag{6}$$

for a capacitance C_{m} per module, load current I, voltage difference ΔV_{m} before parallelization, and duration τ since the last parallelization of these modules [28]. This formula assumes a negligible inductance. Thus, this loss type falls with an increasing module capacitance, e.g., it will be low for batteries, and can be further reduced to any level by selecting a sufficiently short τ. For the presented prototype, τ keeps the loss below 0.1% of real output power and is overcompensated by the associated efficiency gain due to lower internal Ohmic losses with the parallel connectivity. Since the speed for building up voltage differences at constant module capacitance scales linearly with the load current, on which the associated balancing loss depends quadratically, balancing loss decreases at partial load [28]. As well, at partial load the efficiency gain due to lower source impedance in the parallel mode increases as more modules that are not required in series can be in parallel.

5) Balancing: With the objective of balancing the module voltages, the scheduler aims to have each module interconnection in the parallel state as often as possible and at least once within a specified maximum duration $\tau_{\max}$. The controller keeps track of the time, τ_j, since the last parallel state of each module interconnection. To ensure balancing, the controller can parallelize the modules with the longest duration since their last parallelization. Thus, the optimal converter state $\mathbf{v}^t$ in switching cycle t is

$$\min_{\mathbf{v}^t} \max\{\tau_1, ..., \tau_{N-1}\}. \tag{7}$$

This procedure is analogous to earliest-deadline-first scheduling in real-time computing.

If $\tau_j > \tau_{\max}$, the controller enforces parallelization independently of the loss objectives. This hard constraint guarantees that the module voltage stays within operating limits. The time-out parameter $\tau_{\max}$ should be considerably smaller than the time it takes to reach the under-voltage lockout, V_{lockout}, of a module

$$\tau_{\max} < \frac{(V_{\mathrm{m,nom}} - V_{\mathrm{lockout}})C_{\mathrm{m}}}{I} \tag{8}$$

where $V_{\mathrm{m,nom}}$ is the nominal module voltage and C_{m} is the module capacitance. While $\tau_{\max}$ could be adaptively adjusted to the load current I to minimize enforced parallelization, using the peak current rating is a simple compromise.

D. Concurrent Versus Consecutive Optimization

Implementing constraints is relatively straight forward and can be done in any order as it amounts to eliminating the configurations that do not meet the constraint. Optimizing performance objectives is more complicated as it involves searching through all configurations within the constraints to find an optimum. In principle, the controller could perform a concurrent optimization of all objectives; however, the large number of alternative configurations would require extensive computational effort. Therefore, we adopted an approach that addresses the objectives consecutively in a particular order. Furthermore, the objectives are applied in the form of constraints that rapidly eliminate alternatives so that only a minimum of explicit objective evaluations is necessary. This approach is well justified when there is a clear hierarchy in the relative magnitude or importance of the objectives' contribution to performance. It starts with the generation of a list of all module configurations that produce the output voltage specified by the modulator. To this list, it applies the other objectives and constraints in the order determined by the application and the specific converter's properties.

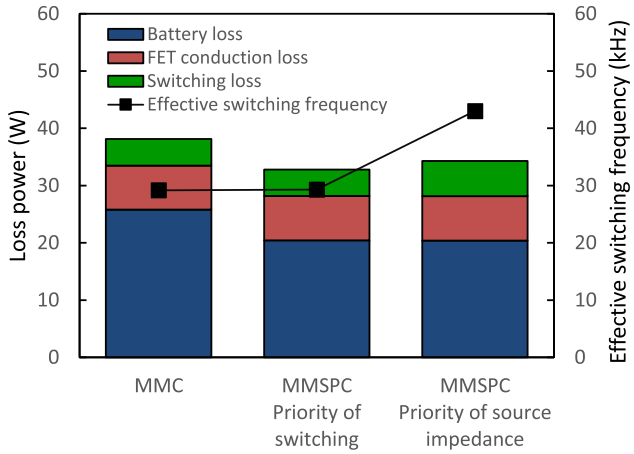


Fig. 4. Simulation results for the contribution of the three main loss mechanisms—battery loss, FET conduction loss, together subsumed as conduction loss, and switching loss—for three control schemes—MMC or MMSPC that prioritizes minimization of switching loss or source impedance.

For example, in the presented prototype switching loss minimization is a more important optimization target than module balancing due to the high capacity of the module energy storages and therefore slow unbalancing trend. The prototype has an average switching rate per module of more than 3 kHz while the ratio of the module energy storage capacity divided by the expected peak module current exceeds 4 min. Thus, due to the high switching rates and high module capacitance, the controller prioritizes reduction of switching loss over balancing. For low switching rates, the switching loss could become the last objective in the elimination process, prioritizing balancing and conduction loss.

III. Simulation

A. Simulation Model

We set up a simulation model to characterize the control strategy and to analyze properties that are not accessible in a hardware setup. The model was implemented in MATLAB/Simulink (The Mathworks, Inc., Natick, MA, USA). The model contains eight power modules, each implementing eight FETs (on-resistance $r_{\mathrm{ds,on}} = 4.8\ \mathrm{m}\Omega$), a capacitor for current commutation (1 mF with an equivalent series resistance of 10 mΩ), and a lead-acid battery. The latter was represented by the Tremblay–Dessaint lead-acid model with dedicated separate charge and discharge representations and a static series resistance of 30 mΩ [33]. The controller is implemented in MATLAB/Simulink as described above.

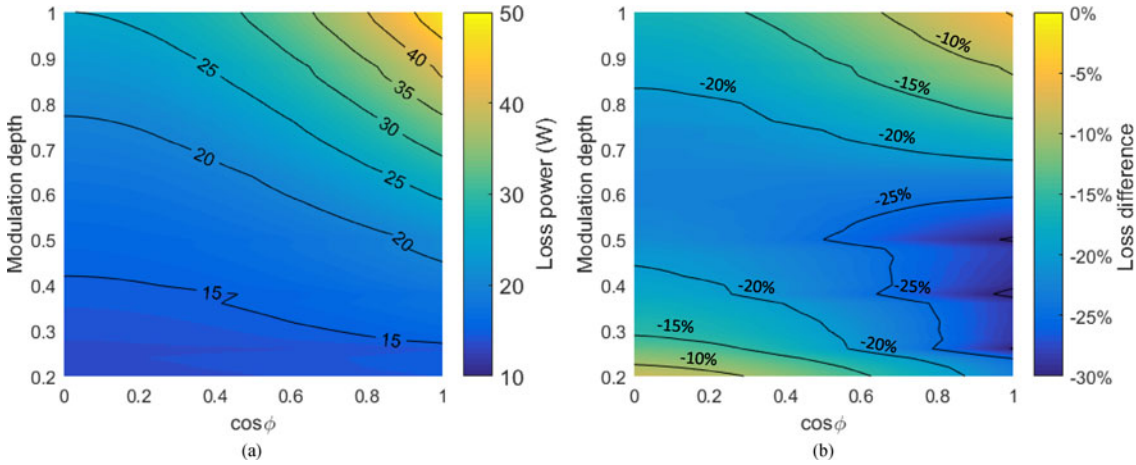


Fig. 5. (a) Power loss of the computational MMSPC model for power factors ranging from 0 to 1 and modulation depths from 20% up to 100%. (b) MMSPC loss relative to MMC provided by the parallel connectivity.

B. Results

We operated the model with three different controllers. Conventional MMC control without a parallel interconnection state served as the first controller and reference. The FETs of the parallel half bridges operate in parallel here so that the overall amount of silicon per module is equal to MMSPC. The second controller is the above-described MMSPC control method with priority of switching over conduction loss in the sequential state elimination. For a third controller, we interchanged the priorities so that conduction loss was optimized first. The output and thus the output quality was approximately equal for all three cases as the modulator is not part of the scheduler and is matched for all cases. As demonstrated in Fig. 4, the choice of the order of the objectives in the elimination process affects the overall performance. In the presented setup, prioritizing switching over source impedance minimization shows a 45% reduction in the overall switching rate compared to the inverse order shown in the third column in Fig. 4, while conduction loss is only affected to a small degree. For switching as the first objective in the elimination process, multiple switch transitions in one clock period are suppressed so that the overall switching corresponds to the clock rate of 30 kHz. Despite the substantial change of the cumulative switching rate, it only affects the overall loss mildly, reflecting the overall low switching rate for FETs. Since the MMSPC control strategy that prioritized switching over source impedance minimization performed the best, we used it in the subsequent simulation and experimental studies.

In all cases, MMSPC outperforms MMC. The main reason is the higher battery loss associated with the higher source impedance of MMC compared to MMSPC (see Fig. 4). The performance gain of MMSPC over MMC is further not surprising as MMSPC is an extension of MMC and the presented control automatically uses conventional MMC states when they show better outcomes in the optimization.

The higher efficiency compared to MMC can be observed throughout a wide range of output conditions as shown in Fig. 5. For increasing load, the quadratically increasing conduction loss dominates the overall loss power. Although the MMSPC increasingly uses the series states for high overall modulation indices, there is still a gain of more than 5% in efficiency compared to MMC at high output amplitudes and power factors. Highest gains arise at medium modulation indices.

Importantly, the switched-capacitor-like balancing mechanism across the modules depends on the voltage difference between module batteries. However, in case of fairly steady load conditions, the imbalance of the batteries' state of charge is monotonically linked to the differences in voltage as shown in Fig. 6(a). Furthermore, the driving force for balancing the modules increases at lower state of charge (SOC) as demonstrated by the increasing voltage difference towards the end of the discharging cycle. The balancing performance is largely constant for varying load current [see Fig. 6(b)]. As Fig. 6(c) demonstrates, an increase of the switch resistance has slightly negative impact on the balance as the balancing current has to pass through the switches.

IV. Experimental Results

A. Power Stage

A prototype MMSPC converter was implemented with eight modules. Each module's storage consists of a parallel arrangement of an absorbent-glass-mat lead-acid battery (nominal 12 V, 7 Ah, Enersys Genesis NP7-12, Reading, PA), low-cost aluminum electrolytic capacitors for sufficient capacitance to limit current ripple (1 mF, ZLH, Rubycon, Inc., Ina City, Japan), and low-impedance ceramic capacitors for high power density for current commutation during switching (200 μF, X7R, Taiyo Yuden Co. Ltd., Tokyo, Japan). The capacitors reduce switching ripple current on the batteries as well as the output and provide a low-impedance path for commutating the current from one switch to another during switching without stressing the batteries. The module switches are implemented with silicon FETs (on-resistance $r_{\mathrm{ds,on}} = 4.8$ mΩ, IRFP 4310, International Rec-

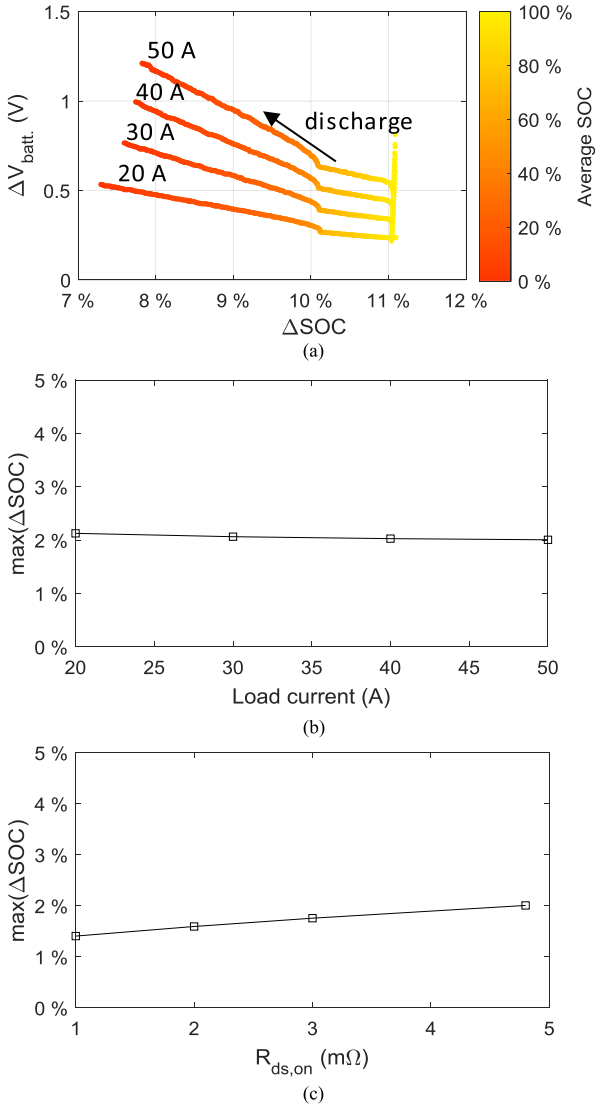


Fig. 6. (a) Relationship of SOC and voltage balance for four load conditions discharging the batteries from 100% to 0%. The color bar represents the SOC for the four full discharging cycles. (b) Maximum SOC imbalance over a full SOC cycle in dependence of the load current. (c) Maximum SOC imbalance in dependence of the transistor channel resistance at a load current of 50 A.

tifier, El Segundo, CA, USA). Together with the ceramic capacitors, Schottky diodes (forward voltage = 0.4 V, STPS8H100D, STMicroelectronics, Geneva, Switzerland) antiparallel with the FET switches provide sufficient snubbing of the switching transients with small loss due to their high turn-ON speed, low forward voltage, and negligible reverse recovery. With eight modules, the prototype has a maximum rms current rating of 200 A and a peak voltage of 104 V for an actual module voltage of 13 V.

Fast recordings were made with Tektronix DPO2024 oscilloscopes. Long-term recordings of the module battery voltages were performed with an eight-channel isolated Agilent 34972A data logger with a 34901A interface.

B. Controller

Based on the objectives and corresponding relationships described in Section II-C, the converter control architecture

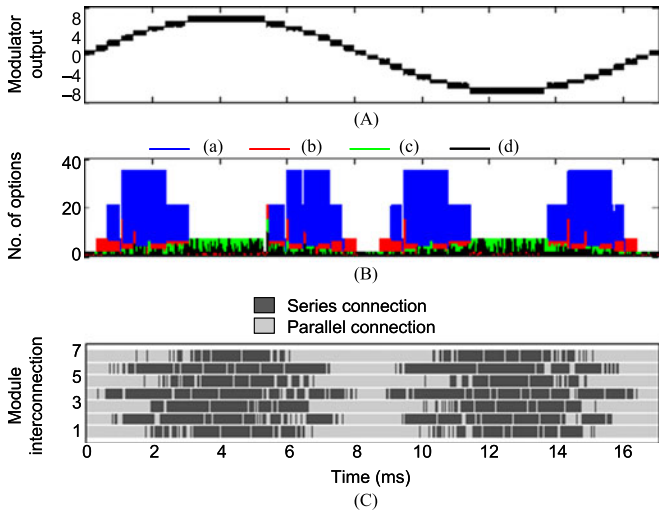


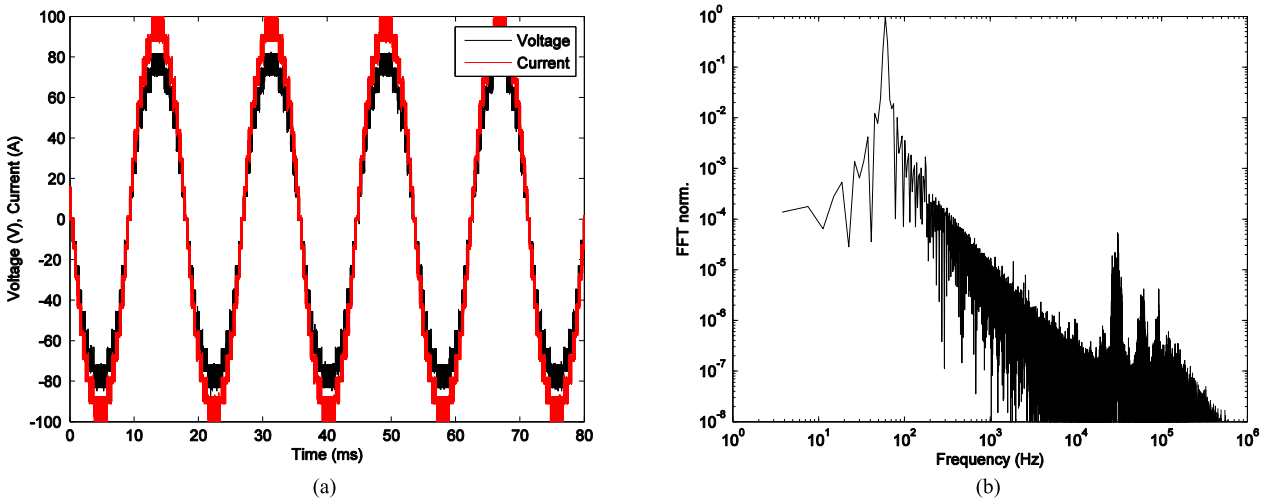
Fig. 7. Experimental demonstration of sensorless scheduler operation. (A) Modulator output going to scheduler. (B) Scheduler sequentially reduces the number of switch configuration options: (a) options generating the required output voltage; (b) options left after eliminating those that would cause high switching loss (large number of switch state transitions); (c) remaining alternatives with lowest conduction loss due to optimal use of parallel connections; and (d) final selection picked by randomization. (C) States of the seven module interconnections commanded by the scheduler.

outlined in Fig. 2 was implemented with a hardware-in-the-loop system (OP5607, OPAL-RT Technologies, Inc., Montreal, QC, Canada). All control routines were implemented in Matlab/Simulink (The Mathworks, Inc., Natick, MA, USA) and compiled for the OPAL-RT platform.

The modulator uses standard multicarrier pulse-width modulation (PWM). The switch update rate is 30 kHz, allowing a moderate average switching frequency per module of 3.75 kHz with appropriate module scheduling. The selected switching rate causes negligible switching loss with limited switching ripple on the charge storage elements. The scheduler carries out sequential optimization of the performance objectives. As described above, the procedure solves the computationally challenging multiobjective optimization problem by converting it into constraints that can be applied consecutively to eliminate alternatives. This decoupling into constraints efficiently eliminates many module interconnection options, which reach 32,768 for the experimental setup, to generate the required converter output.

The controller first selects module configurations that fulfill the quantized output voltage level command from the modulator. As described in Section II-C, the output voltage is almost exclusively determined by the number of series interconnections in a module branch, whereas parallel or bypass interconnections do not affect the voltage in the first approximation. Thus, in this first step, the scheduler distributes the required number of series interconnections by generating all possible permutations. All remaining interconnections in each alternative are set to be parallel.

In a second step, in order to keep switching loss low, the scheduler eliminates all alternatives that would require more than eight toggled switches relative to the interconnection states that were set in hardware at the previous clock step. The selection



(a) (b)

Fig. 8. (a) Measured sinusoidal output current and voltage with a frequency of 60 Hz and PWM at 30 kHz for a purely resistive load. (b) Fourier transform of the output voltage in (a).

of a limit of eight toggled switches is equivalent to allowing two interconnections to change between series and parallel/bypass state (see Section II-C). This metric can be rapidly evaluated by forming the difference of each option's state vector, $\mathbf{v}^{t,i}$, with the state vector set in hardware, $\mathbf{v}^{t-1}$, and summing the differences according to Eq. (3).

Third, those states are selected that would cause no more than 5% higher source impedance than the best available option [as quantified by Eq. (5)] to keep internal loss low but not eliminate all options for the next step. If the voltage is unchanged or changed by only a single module voltage level, this procedure cannot end with an empty set of states as the elimination procedure does not use absolute limits, but elimination criteria are set relative to the best among the alternative states. Thus, an elimination step leaves at least one option in the set.

In the final step, the scheduler randomly shuffles these options to select the final configuration in lieu of optimizing balancing, and completes the elimination procedure for selecting the next state configuration.

The above-mentioned parallelization time-out parameter to enforce the parallel state for interconnections is set to $\tau_{\max} = 1$ s. The overall elimination approach has low computational effort but is nevertheless sufficient to ensure long-term balancing even for the moderate switching rates of this prototype, as demonstrated in Section II-D.

Figure 7 illustrates the controller operation for sinewave output of the prototype converter according to the elimination approach from Fig. 2 [see Section II-C]. Out of 32,768 total alternatives, up to almost 40 different interconnection state combinations can generate the required output voltage provided by the modulator at each time as shown in Fig. 7(b) (see blue line). Except for a few, the number of options for the configuration of the module interconnections decreases by more than a factor of four after all alternatives that would require too many (more than eight) switches to be toggled are removed (see red line). These alternatives would cause high switching loss in transitioning from the current converter state. In a few situations, which can be identified as spikes of the red line, the switching loss of all alternatives is within the limits. The limitation of the number of toggled switches is responsible for the largest reduction of options here. The subsequent elimination of alternatives with high source impedance is comparably less limiting (see green line). As expected, the objective of reducing the source impedance becomes most relevant when the output voltage is low and the objective can eliminate alternatives that do not use the parallel mode efficiently. On the other hand, particularly during periods with high-voltage amplitudes, most modules are in series resulting in the scheduler being able to reduce the source impedance substantially in these intervals. The random selection of the actuated state from the remaining set of options is computationally fast and sufficient to ensure that any interconnection is frequently commanded to the parallel state for capacitive balancing as shown in Fig. 7(c).

An overall stricter limit for any objective could further reduce the remaining set of options at the price of less available alternatives for the subsequent steps to optimize the remaining objectives and thus the influence of later objectives.

C. Output Quality

Figure 8 shows the output of the system for a load of 3.8 kW at unity power factor. Switching causes low-amplitude harmonics at the modulation frequency and its overtones (30 kHz, 60 kHz, 90 kHz, etc.). Despite the low switching rate, the 17 voltage levels reduce the harmonics of the voltage to less than -86 dBc [see Fig. 8(b)], corresponding to harmonic distortion of only 4.9%. The dynamic bandwidth was tested in frequency sweeps (Fig. 9) demonstrating that the spurious-free dynamic range of the output voltage at 10 kHz is still high (28 dBc) with a low harmonic distortion ($<$16%).

D. Balancing

Figure 7(c) demonstrates that the controller as outlined in Section II and run on the OPAL-RT hardware parallelizes mod-

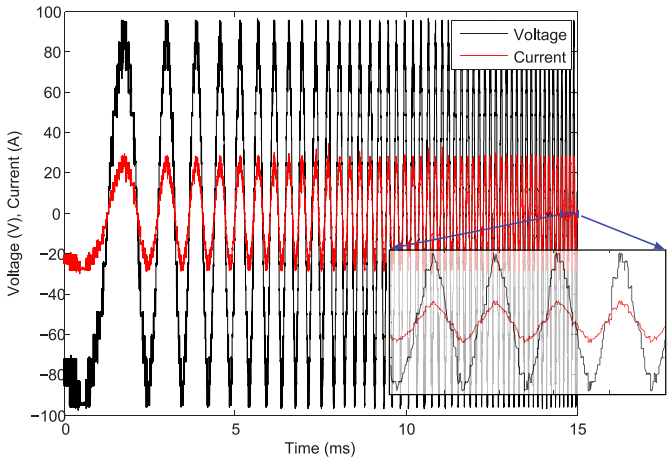


Fig. 9. Measured sinusoidal frequency sweep up to 10 kHz with the effective switching rate increased up to 300 kHz. The inset magnifies an interval of 500 μs duration at 10 kHz, where distortion becomes visible.

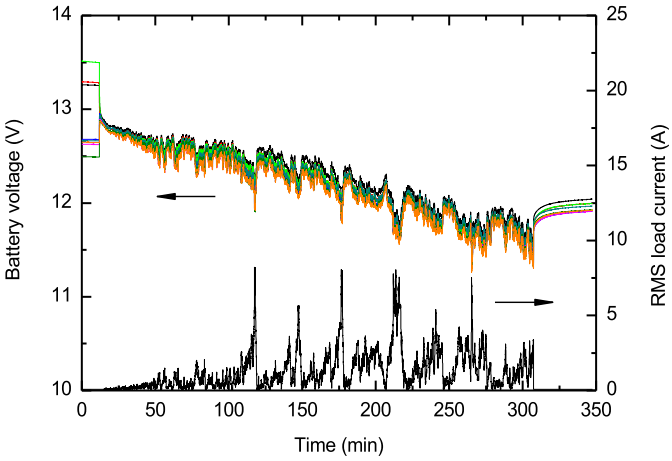


Fig. 10. Module balancing performance demonstrated with long-term measurement of the eight individual battery voltages (left y-axis) during ac operation with highly variable load (right y-axis). The initial module voltages are deliberately mismatched at Time = 0. Module balancing is turned on at Time = 10 min and turned off at Time = 310 min to observe the initial and final voltage mismatch.

ules frequently, promoting equilibration of the module voltages. The longest duration of a module interconnection site without parallelization is 2.95 ms (with an average of 1.62 ms). These values are much smaller than the 1 s time-out; therefore, parallelization is never forced by the controller but rather occurs as a result of the other objectives.

Figure 10 reveals that the combination of the controller and the topology can balance and keep balanced the module voltages. The batteries were discharged over 5 h with an average load at their recommended lifetime derating level. This level would be the reference for discharge cycles above peak load of up to 20 s in commercial applications of the batteries. The initial module voltages are deliberately varied beyond what would be encountered in normal operation to demonstrate the ability of the converter to balance even extreme mismatches. When balancing is turned ON, the measured voltages, which are detected at the batteries' terminals and thus behind the internal resistance and any *RC* time constants, converge almost instantaneously. The seeming immediate elimination of all differences is largely due to the batteries' internal resistances, filtering capacitors, and rapid interconnection shuffling relative to the slower sampling rate. Thus, the converged voltage amounts to the average of the initial battery voltages and not the rms value that would result from parallelization-based balancing, ruling out any energy loss high balancing currents would necessarily entail. The battery voltages can be seen in the initial and final segments of the plot in Fig. 10, which are recorded without balancing or load. After 5 h of operation, the standard deviation of the individual module voltages is reduced by a factor of eight (from 0.367 to 0.045 V), and the module voltage levels are no longer in the same order compared to the initial conditions. For the batteries in the prototype, the remaining imbalance corresponds to less than 1% of the state of charge. Thus, the module balancing appears to work well, even if the system starts with a substantial module voltage mismatch.

The balancing current flowing between modules connected in parallel is limited by the resistance of the FETs, $r_{\mathrm{ds,on}}$, the intrinsic resistance of the batteries, $r_{\mathrm{i,bat}}$, and the inductance of the loop between the modules, L_{balance}. For this prototype, $r_{\mathrm{ds,on}} \approx 4.8\ \mathrm{m\Omega}$ and $r_{\mathrm{i,bat}} \approx 23\ \mathrm{m\Omega}$, resulting in a total resistance around the balancing loop of $r_{\mathrm{balance}} = 4\,r_{\mathrm{ds,on}} + 2\,r_{\mathrm{i,bat}} \approx 65.2\ \mathrm{m\Omega}$. Thus, accounting solely for the loop resistance, the balancing currents are less than 2 A for representative steady-state module voltage difference of 0.1 V. The inductance of the equilibration loop further limits the current surge within the initial $L_{\mathrm{balance}}/r_{\mathrm{balance}} \approx 100\,\mu$s of parallelizing two modules.

Balancing by parallelization, however, has limitations for large load currents and/or high resistances of the switches and battery cells. The equalization process is intentionally over-damped, typically having a low quality factor $Q = \sqrt{L_{\mathrm{balance}}/C_{\mathrm{m}}}/r_{\mathrm{balance}} < 10^{-2} << 1$. The continuous charge equilibration is further counteracted by the load current, I_{load}, which draws charge from the modules unequally. Though the MMSPC outperforms the MMC in all situations, for a high ratio of interconnection resistance to battery equivalent series resistance, the load current may no longer distribute equally among the batteries in a parallel group of modules but primarily flow through the outmost modules. In the worst case, all current is drawn from the two outmost modules, corresponding to an upper limit for the module voltage change of

$$\frac{d}{dt}V_{\mathrm{m}} \le \underbrace{-\frac{\Delta V_{\mathrm{m}}}{2r_{\mathrm{balance}}C_m}\cdot\exp\left(-\frac{t}{2r_{\mathrm{balance}}C_{\mathrm{m}}}\right)}_{\text{Equilibration}} + \underbrace{\frac{I_{\mathrm{load}}}{2C_{\mathrm{m}}}}_{\text{Discharging}}$$
$$= \frac{1}{2C_{\mathrm{m}}}\left(-\frac{\Delta V_{\mathrm{m}}}{r_{\mathrm{balance}}}\cdot\exp\left(-\frac{t}{2r_{\mathrm{balance}}C_{\mathrm{m}}}\right) + I_{\mathrm{load}}\right). \quad (9)$$

If the load current exceeds the equalizing currents, the voltage difference ΔV_{m} in the first term of Eq. (9) will increase and balance the two terms. Thus, the modules converge to an average voltage difference, which in the worst case can reach

$$\Delta V_{\mathrm{m}} \le r_{\mathrm{balance}} I_{\mathrm{load}}. \quad (10)$$

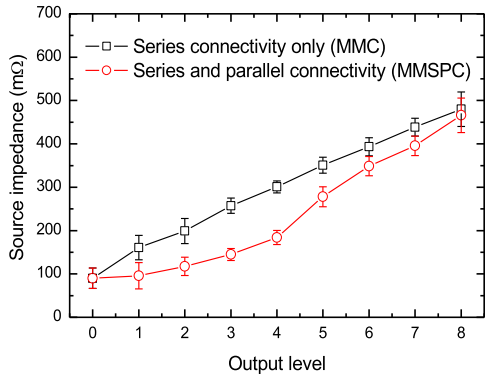


Fig. 11. Measured source impedance of the converter using either only series (as in MMC) or both series and parallel combinations of modules (enabled by MMSPC). The load is resistive. The measurements are for the available eight different output voltage levels of either polarity as well as zero output. The error bars indicate the 0.95% confidence intervals.

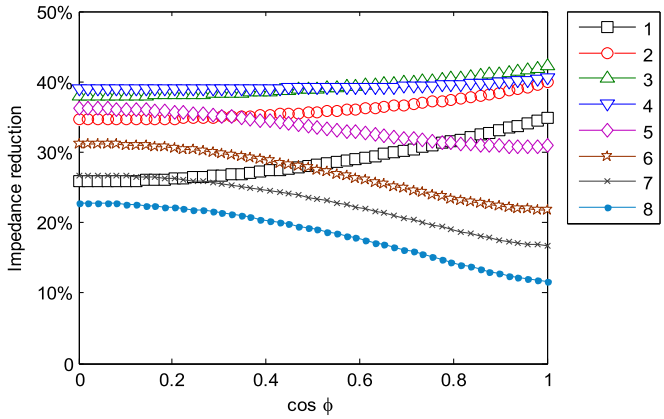


Fig. 12. Reduction of the average source impedance of the prototype controlled as MMPSC versus MMC for ac output with various amplitudes (denoted in the legend as multiples of the module voltage of 13 V) and power factors (cos φ).

Closed-loop control could remove this offset by systematically taking into account different discharge rates within a string of modules and rotate modules to equalize the average module current.

E. Source Impedance

To evaluate the reduction of the MMSPC source impedance with the use of parallel module connectivity, we compared the converter operation to that without parallel mode, emulating a conventional MMC under otherwise identical conditions. The source impedance was measured as a function of the output voltage level for each module configuration and for resistive loads of approximately 0.5, 1, 2, 5, 20, and 50 Ω. The impedance was estimated from measurements of the output voltage and current in steady state using a four-wire technique and analysis in Matlab and JMP (SAS Institute, Cary, NC, USA). Figure 11 shows the source impedance data of MMSPC versus MMC, both using full-bridge module topologies. For zero voltage and peak voltage output, both MMC and MMSPC use the same module configurations (all bypass and all series, respectively) and therefore have the same impedance. For the intermediate voltage levels (the dominant range for ac output) the MMSPC has up to 40% lower impedance than the MMC.

The reduced source impedance for each output level translates into a decrease of the average impedance for ac outputs, as illustrated in Fig. 12. This reduction depends on the amplitude of the ac output and the power factor. Under all ac output and load conditions, the source impedance of the MMSPC undercuts the one of the MMC. The relative advantage ranges from 12% for eight levels peak amplitude (104 V) to 43% for three levels (39 V), both for cos $\varphi = 1$. Generally, the largest reductions of the source impedance are achieved for low and medium ac voltage amplitudes. For output amplitudes up to four modules (52 V peak), the reduction in source impedance increases with increasing power factor, reflecting the higher difference in impedance for intermediate levels in Fig. 11. On the other hand, there is also a significant reduction of the average source impedance for high ac output amplitudes with low power factors. In this case the peak current is shifted to times when the voltage is relatively low and therefore more module interconnections are in the parallel state. This translates to a reduction in conduction losses. For instance, at peak ac output equal to the system maximum (104 V), the use of the parallel mode reduces the conduction loss by 18% for cos $\varphi = 1$ and by 24% for cos $\varphi = 0.8$ at equal apparent output power.

V. Conclusion

This paper demonstrated experimentally MMSPC—a novel MMC topology with the capability for parallel connectivity between modules. All advantages of the MMC persist in MMSPC, including modularity, exclusive use of low-voltage components, and a high-quality output waveform with low harmonic content over a wide frequency range.

Beyond the MMC capabilities, the MMSPC parallel state reduces the source impedance and hence conduction losses. The decrease in conduction loss depends on the specific implementation of the system and the load, and is larger for inductive loads. Thus, power flow compensatory facilities such as STATCOM, which is among the most common applications of MMCs, and battery energy storage, which may implement power-factor-compensation functionality, could benefit from the parallel connectivity.

As well, the parallel state can be used to transfer energy between different modules. While conventional balancing through appropriate module scheduling known from MMC is available further on, this switched-capacitor-type energy transfer enables a simple, sensorless control approach that balances the module voltages by parallelization. This is a substantial advantage over conventional MMCs, which require accurate, high-bandwidth monitoring of each module's voltage or current to ensure balancing. Besides balancing, the demonstrated control approach uses the large number of degrees of freedom of the MMSPC to optimize performance objectives including minimizing conduction and switching loss.

Collectively, these features of MMSPC and its control could enhance traditional applications of MMCs and enable novel applications at lower voltage levels such as the demonstrated modular battery system.

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REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. 2003 IEEE Bologna Conf. Power Tech.*, 2003, vol. 3.

[2] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.

[3] B. Gultekin and M. Ermis, "Cascaded multilevel converter-based transmission STATCOM: System design methodology and development of a 12 kV $\pm$ 12 MVAr power stage," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4930–4950, Nov. 2013.

[4] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[5] B. Sanzhong and S. Lukic, "Modular design of cascaded H-bridge for community energy storage systems by using secondary traction batteries," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2014, vol. 29, pp. 3297–3304.

[6] S. M. Goetz *et al.*, "Circuit topology and control principle for a first magnetic stimulator with fully controllable waveform," in *Proc. Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, 2012, pp. 4700–4703.

[7] A. V. Peterchev, Z.-D. Deng, and S. M. Goetz, "Advances in transcranial magnetic stimulation technology," in *Brain Stimulation: Methodologies and Interventions*, I. M. Reti, Ed. Hoboken, NJ, USA: Wiley, 2015.

[8] M. Malinowski *et al.*, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[9] G. T. Son *et al.*, "Design and control of a modular multilevel HVDC converter with redundant power modules for noninterruptible energy transfer," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1611–1619, Jul. 2012.

[10] M. Lomaskin, B. Sanzhong, and S. Lukic, "Current sharing control for cascaded H-bridge applied to secondary use batteries in Community Energy Storage systems," in *Proc. Int. Conf. Energy Convers. Congr. Expo.*, 2012, pp. 2107–2111.

[11] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 163–175, Jan. 2015.

[12] D. Hong, S. Bai, and S. M. Lukic, "Closed form expressions for minimizing total harmonic distortion in 3-phase multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5229–5241, Oct. 2014.

[13] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[14] G. P. Adam *et al.*, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *IET Power Electron.*, vol. 3, no. 5, pp. 702–715, 2010.

[15] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 298–306, Jan. 2011.

[16] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66–76, Jan. 2014.

[17] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *Proc. 2008 IEEE/PES Transmiss. Distrib. Conf. Expo.*, 2008.

[18] L. Ängquist *et al.*, "Open-loop control of modular multilevel converters using estimation of stored energy," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2516–2524, Nov./Dec. 2011.

[19] H. Nademi, A. Das, and L. E. Norum, "Modular multilevel converter with an adaptive observer of capacitor voltages," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 235–248, Jan. 2015.

[20] A. Elserougi *et al.*, "Investigation of sensorless capacitor voltage balancing technique for modular multilevel converters," in *Proc. 2014 IEEE 40th Annu. Ind. Electron. Soc.*, 2014, pp. 1569–1574.

[21] K. H. Ahmed and G. P. Adam, "New modified staircase modulation and capacitor balancing strategy of 21-level modular multilevel converter for HVDC transmission systems," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drives*, 2014.

[22] K. Ilves *et al.*, "Predictive sorting algorithm for modular multilevel converters minimizing the spread in the submodule capacitor voltages," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 440–449, Jan. 2015.

[23] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4568–4579, Sep. 2014.

[24] A. Ghazanfari and Y. I. Mohamed, "A hierarchical permutation-cyclic-coding strategy for balancing capacitor voltages in modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 576–588, Jun. 2016.

[25] F. Z. Peng, J. W. McKeever, and D. J. Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," *IEEE Trans. Ind. Appl.*, vol. 34, no. 6, pp. 1293–1298, Nov./Dec. 1998.

[26] F. Z. Peng, "Power line conditioner using cascade multilevel inverters for voltage regulation, reactive power correction, and harmonic filtering," *Lockheed Martin Energy Res. Corp.*, Bethesda, MD, USA, US 6075350 A, 2000.

[27] A. M. Massoud *et al.*, "Three-phase, three-wire, five-level cascaded shunt active filter for power conditioning, using two different space vector modulation techniques," *IEEE Trans. Power Del.*, vol. 22, no. 4, pp. 2349–2361, Oct. 2007.

[28] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel module connectivity: Topology and control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 203–215, Jan. 2015.

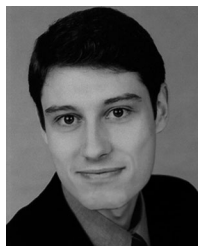
[29] K. Ilves *et al.*, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," in *Proc. IEEE 15th Eur. Conf. Power Electron. Appl.*, 2013.

[30] K. Ilves *et al.*, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3518–3527, Jul. 2015.

[31] S. Ramkumar *et al.*, "A new series parallel switched multilevel dc-link inverter topology," *Int. J. Electr. Power Energy Syst.*, vol. 36, no. 1, pp. 93–99, 2012.

[32] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel dc voltage sources," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2643–2650, Aug. 2010.

[33] O. Tremblay and L.-A. Dessaint, "Experimental validation of a battery dynamic model for EV applications," *World Elect. Veh. J.*, vol. 3, no. 1, pp. 1–10, 2009.



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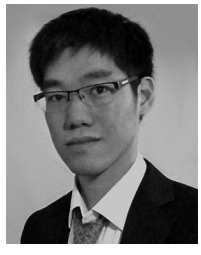

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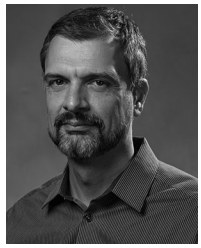

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