Confined Band Variable Switching Frequency Pulse Width Modulation (CB-VSF PWM) for a Single-Phase Inverter With an *LCL* Filter

Hussain A. Attia, Tan Kheng Suan Freddy, Hang Seng Che, *Member, IEEE*, Wooi Ping Hew, *Member, IEEE*, and Ahmad Elkhateb, *Member, IEEE*

***Abstract*—Variable switching frequency pulse width modulation (VSF PWM) has been proposed in the past to optimize the total harmonic distortion (THD) performance and switching losses of an inverter. Nevertheless, such VSF PWMs give rise to switching harmonics which vary across a wide frequency spectrum, where the lower frequencies could resonate with the filter while the upper frequency could exceed the maximum switching frequency. This complicates VSF PWM design, restricting their practical uses. In this paper, a confined band VSF PWM (CB-VSF PWM) for a single-phase inverter with an *LCL* filter is presented. By confining the switching frequencies within a practical band, the design of the filter becomes easier while maintaining low current THD with low switching losses. The choices of the upper and lower bands of the proposed VSF are defined and the design criterion is introduced. It is found that the proposed method allows reduction in switching losses as well as reduction in current THD when the effect of the *LCL* filter is taken into consideration. The performance analysis is validated through simulation and experimental results in a 1 kW inverter.**

***Index Terms*—Confined band (CB), switching losses, variable switching frequency pulse width modulation (VSF PWM).**

I. Introduction

RENEWABLE energy has been identified as a potential solution to mitigate climate change. As more renewable energy systems are connected to a utility grid, more stringent requirements on inverters have been introduced. Modern inverters require not only low current total harmonic distortion (THD), but also low losses for better efficiency [1], [2].

The choice of pulse width modulation (PWM) strategy has profound impacts on the THD and switching losses of an inverter [3]. Constant switching frequency PWM (CSF PWM) has been widely implemented in a single-phase inverter due to simplicity. Nevertheless, the choice of switching frequency in CSF PWM is inherently a tradeoff between efficiency and THD. Higher switching frequency will no doubt improve the THD and increase power density by reducing the size of inductors and capacitors. However, this comes at the cost of increased switching losses, which reduces the overall inverter efficiency. Instead of fixing the switching frequency, variable switching frequency PWM (VSF PWM) has been proposed [4]–[10], where switching frequency in one fundamental cycle is varied to provide more degrees of freedom for performance improvement.

Various VSF PWM methods have been reported recently, such as the random PWM (RPWM) [4], [5] where the harmonic spectrum is distributed over a wide range of frequency by the randomizing switching period. It was reported that RPWM can effectively suppress electromagnetic interference noise in the converter system. Optimal VSF PWM schemes based on the current ripple analysis were proposed to minimize the switching loss while meeting the required output current THD in single-phase [7], [8] and three-phase [9], [10] inverters.

Despite the advantages claimed, the variable frequency in these VSF PWMs poses some challenges that restrict their practical uses. This is mainly due to the fact that existing VSF PWM schemes do not explicitly control their frequency band. Such unconfined switching frequency band have two implications: the lower frequency components could resonate the filter (particularly the *LCL* filter [11]–[13]) while the upper frequency components could exceed the maximum switching frequency, which can exceed the practical limits of the hardware (gate drive and switches), or cause current waveform distortion due to pulse dropping.

In this paper, a confined band VSF PWM (CB-VSF PWM) for a single-phase inverter with the *LCL* filter is presented. By confining the switching frequencies within a practical band, the design of the filter becomes easier while maintaining low current THD with low switching losses. The choices of the upper and lower bands of the proposed CB-VSF PWM are defined and the design criteria of which are introduced. It is found that the proposed method allows reduction in switching losses as well as reduction in current THD when the effect of the *LCL* filter is taken into consideration. The performance analysis is validated though simulation and experimental results in a 1 kW inverter.

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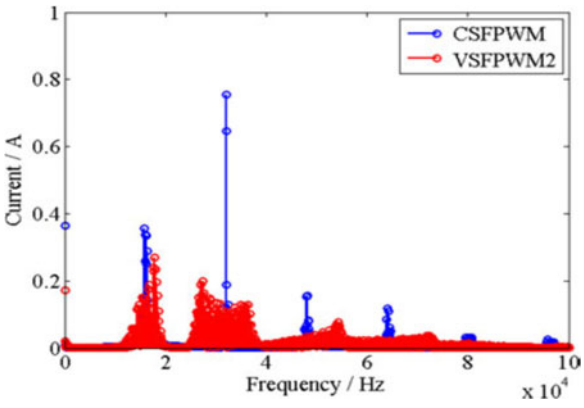

Fig. 1. Harmonic spectrum of current for VSF PWM [9].

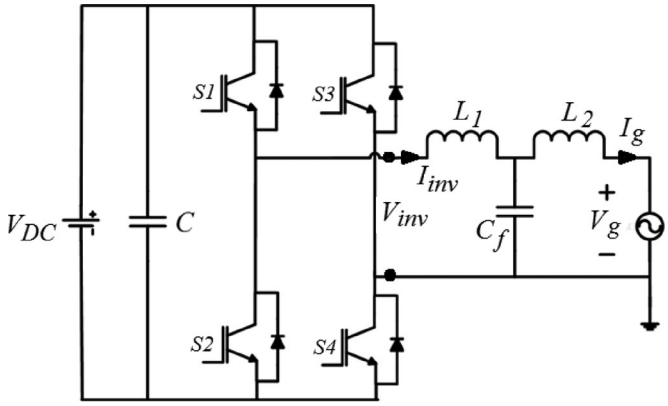

Fig. 2. Single-phase full-bridge inverter with an *LCL* filter.

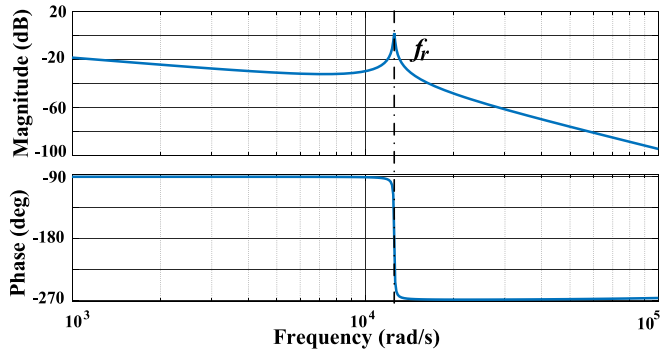

Fig. 3. Bode plots of an *LCL* filter.

The rest of this paper is as follows: operating principle of the proposed CB-VSF PWM and the design procedure of the CB of the proposed CB-VSF PWM are explained in Section II. The current ripple and switching losses analysis based on simulation studies are presented in Section III. Experimental results and related comparisons are presented in Section IV. Finally, the findings summary is included in conclusion in Section V.

II. Proposed CB-VSF PWM Scheme

Fig. 1 illustrates the harmonic spectrum of output current for a typical VSF PWM scheme [7], where the harmonics spectrum is distributed across a wide frequency range. There is a risk to excite the resonance of the *LCL* filter if the frequency band is not confined within a proper region. Nevertheless, existing VSF PWM schemes give little consideration on the frequency spectrum. In this paper, a CB-VSF PWM is proposed, where its frequency spectrum is confined within a band, which is part of the design criteria.

A. Frequency Band

First, the boundaries of frequency band for the proposed CB-VSF PWM are identified as

$$f_{\max} = f_C \tag{1}$$

$$f_{\min} = B \cdot f_C \; B \in [0,1] \tag{2}$$

where f_C represents the CSF, $f_{\max}$ and $f_{\min}$ represent the maximum and the minimum frequencies of the proposed CB-VSF PWM, respectively; B is the constant parameter that determines $f_{\min}$. Here, the maximum frequency is set as f_C, and the frequency range is controlled through B. When $B = 1$, the characteristic of the scheme becomes CSF PWM.

Reducing $f_{\min}$ undoubtedly reduces the switching losses. Nonetheless, $f_{\min}$ should be confined so that it does not resonate with the filter. Fig. 2 shows a full-bridge inverter with an *LCL* filter which is well-known to be more superior to the conventional *L* filter for the attenuation of high-frequency harmonic. The transfer function of the *LCL* filter is expressed as [11]–[13]

$$G(s) = \frac{1}{L_1 L_2 C_f s^3 + (L_1 + L_2)s}. \tag{3}$$

Fig. 3 presents the frequency response of the *LCL* filter. As shown in Fig. 3, there is a resonance peak with the *LCL* filter with a resonant frequency f_r given by

$$f_r = \frac{1}{2\pi\sqrt{\left(\frac{L_1 L_2}{L_1 + L_2}\right) C_f}}. \tag{4}$$

To avoid resonance and for effective suppression of switching frequency harmonic components, f_r is always constrained within $10 f_g < f_r < 0.5 f_s$ [11], where f_g is the grid frequency (50/60 Hz), and f_s is the switching frequency. Since unipolar sinusoidal pulse width modulation (SPWM) is implemented, the effective switching frequency will be $2f_s$. Therefore, to avoid resonance, $2f_s > 2f_r$. In other words, $f_s > f_r$ for unipolar SPWM. For the VSF PWM scheme, switching frequency varies from $f_{\min}$ to $f_{\max}$. As a result, $f_{\min} > f_r$ for CB-VSF PWM.

On the other hand, the upper frequency $f_{\max}$ is dependent on the dead time. Dead time is important to make sure the upper (lower) switch is fully OFF before the lower (upper) switch is ON, to avoid shoot through effect. For a given dead time, there is a maximum limit to the switching frequency to avoid pulse

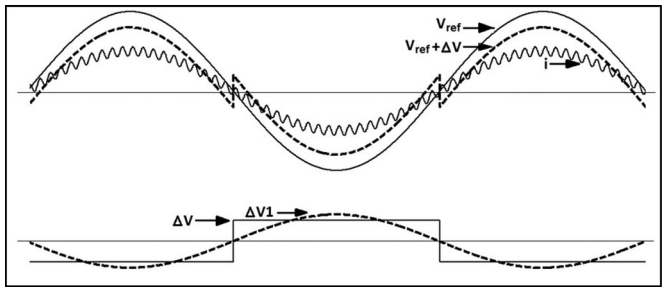

Fig. 4. Dead-time effect of output voltage.

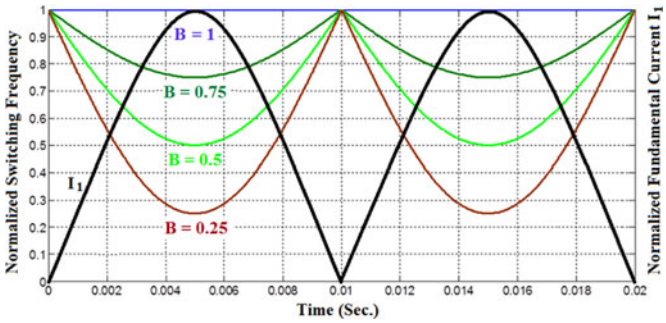

Fig. 5. Behavior of proposed CB-VSFPWM for different *B* values.

dropping which distorts the output voltages and currents. In other words, maximum allowable switching frequency is dead time dependent, which can be calculated as [14], [15]

$$f_{\max} < \frac{1-m}{2T_d} \tag{5}$$

where m and T_d denote the modulation index and the dead time, respectively.

The VSF PWM method proposed in [7] varies the switching frequency based on the current ripple. As a result, the frequency band is uncontrolled which can be as high as few times the switching frequency of a CSF PWM. Such design could exceed the maximum switching frequency limit which may result in current waveform distortion due to pulse dropping.

Based on the analysis mentioned above, the design procedures for the frequency band of the proposed CB-VSF PWM are

1) The lower frequency band (effective switching frequency) should always be greater than the resonant frequency of the *LCL* filter, so $f_{\min} > f_r$.
2) The upper frequency band, $f_{\max}$ shall comply with (5).

B. Switching Loss

Having addressed the confined frequency bands, a simple CB-VSF PWM is proposed in this section based on the switching losses analysis.

Power (P) is defined as energy (E) per unit time. Therefore, switching losses over one PWM cycle are calculated by [18]

$$P_{\text{sw}} = \frac{E}{T_s} = E \cdot f_s \tag{6}$$

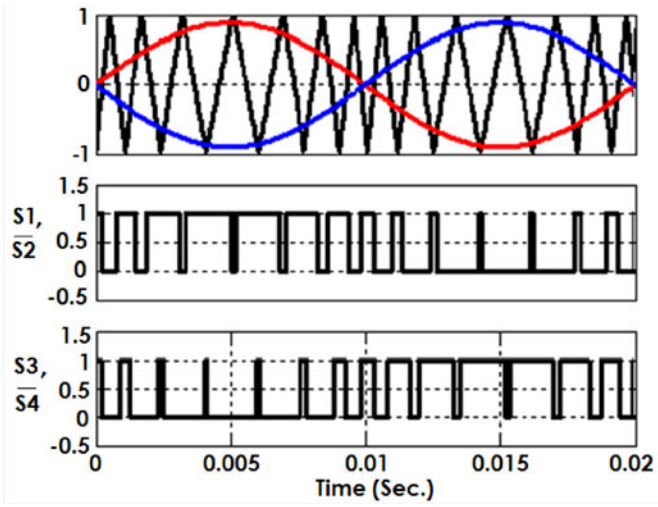

Fig. 6. Proposed CB-VSF PWM scheme.

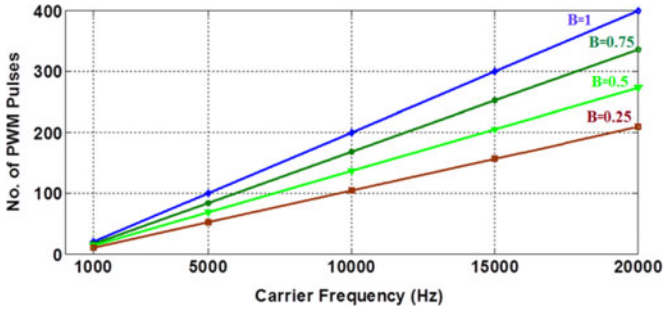

Fig. 7. Total number of pulses per reference cycle of the discussed PWM technique.

where P_{sw} is switching losses, T_s is the switching period, and f_s is the switching frequency.

For a sinusoidal current, the energy dissipated in the semiconductor can be derived as

$$E = E_{\max} \sin \omega t \tag{7}$$

where ω denotes the reference frequency in rad/s. $E_{\max}$ is the maximum switching energy which occurs at peak of the instantaneous current ($\omega t = 90°$).

According to (6) and (7), the switching losses of semiconductor devices are proportional to the magnitude of instantaneous current and the switching frequency. The higher the switching frequency and the magnitude of the current, the higher the switching losses, and vice versa.

C. Harmonic Distortion

Fig. 4 shows the effect of dead time on inverter output voltage. V_{ref} is the fundamental output voltage. Since the dead time increases (decreases) the inverter output voltage for the negative (positive) half-cycle of the current, the average voltage deviation over a cycle can be represented by Fig. 4 as the square wave ΔV. Besides the fundamental and switching frequency components, the inverter output voltage contains harmonics of the square

TABLE I
TOTAL NUMBER OF PWM PULSES PER REFERENCE CYCLE OF DISCUSSED PWM TECHNIQUES

	N_{PWM}			
fc (kHz)	*CSF (B = 1)*	*CB-VSF (B = 0.75)*	*CB-VSF (B = 0.50)*	*CB-VSF (B = 0.25)*
5	100	84	68	52
10	200	168	136	105
20	400	336	273	209

TABLE II
INVERTER SPECIFICATIONS

Parameters	Value
Input dc link voltage, V_{dc}	370 V
Rated power	1 kW
Constant switching frequency, f_c	10 kHz ($B = 1.0$)
	7.5–10 kHz ($B = 0.75$)
CB-VSF carrier range, $f_{\mathrm{CB-VSF}}$	5–10 kHz ($B = 0.5$)
	2.5–10 kHz ($B = 0.25$)
Dead time, T_d	2.5 μs
DC-link capacitors	2200 μF, 400 V
IGBT with ultrafast soft recovery diode	IRG4PH50KDPbF [20]
	$V_{\mathrm{CES}} = 1200$ V, $I_C = 24$ A
Load resistor	40 Ω
Modulation Index, *m*	0.8
LCL filter: L_1, C_f, L_2	4 mH, 2 μF, 1 mH
Resonance frequency, f_r	4 kHz

wave. The magnitude of which can be calculated as [19]

$$V_n = \frac{1}{n}\Delta V_1 \; n = 3, 5, 7.... \tag{8}$$

where ΔV_1 is the amplitude of fundamental component of square wave which can be calculated as

$$\Delta V_1 = \frac{4}{\pi}\Delta V = \frac{4}{\pi}\left(\frac{N_{\mathrm{PWM}} T_d}{T} V_{\mathrm{dc}}\right) \tag{9}$$

where N_{PWM}, T, and V_{dc} are the number of pulses per cycle, the time per cycle, and the dc-link voltage, respectively.

According to (8) and (9), harmonic distortion incurred by the dead-time effect is proportional to number of pulses per cycle. In other words, increasing the switching frequency will increase the low-order harmonic components.

D. Proposed CB-VSF

Based on the analysis, a CB-VSF PWM scheme is proposed here such that the switching frequency is varied within a predefined frequency band, and can be calculated as

$$f_{\mathrm{CB-VSF}} = fc \cdot \{1 - [(1 - B) \cdot \mathrm{abs}(\sin(\omega t))]\}. \tag{10}$$

The characteristic of (10) is presented in Fig. 5. It is noticed that $f_{\mathrm{CB-VSF}}$ has been selected such that the switching frequency reaches its minimum at the points with maximum voltage amplitude. In unity power factor operation, the switching loss reduction is achieved via the reduction of total number of pulses. The switching loss is further reduced as the reduction of number of pulses occurs at the current with higher magnitude. For nonunity power factor operation, the peak current magnitude will occur at positions phase shifted from those under unity power factor operation. Under such scenarios, the switching loss can be minimized by varying the switching frequency with the current amplitude, similar to that in [7]. Since the operating principals are essentially same as unity power factor, the subsequent discussions and results are based only on unity power factor operation for brevity.

According to (10), f_{min} (minimum frequency band) of (2) can be calculated as

$$f_{\mathrm{min}} = f_c[1 - (1 - B)] = B \cdot f_C. \tag{11}$$

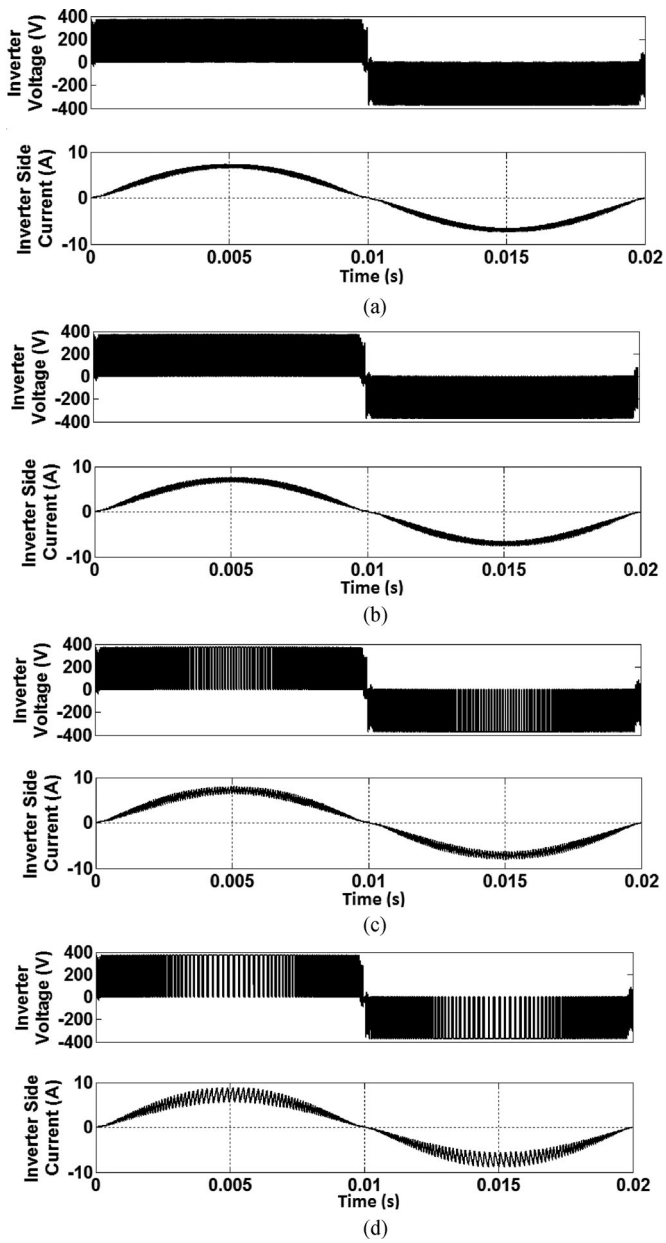

Fig. 8. Simulated output voltage (top) and output current (bottom): (a) CSF PWM, $f_C = 10$ kHz, (b) CB-VSF PWM, $f_{\mathrm{CB-VSF}} = 7.5$–10 kHz, (c) CB-VSF PWM, $f_{\mathrm{CB-VSF}} = 5$–10 kHz, and (d) CB-VSFPWM, $f_{\mathrm{CB-VSF}} = 2.5$–10 kHz.

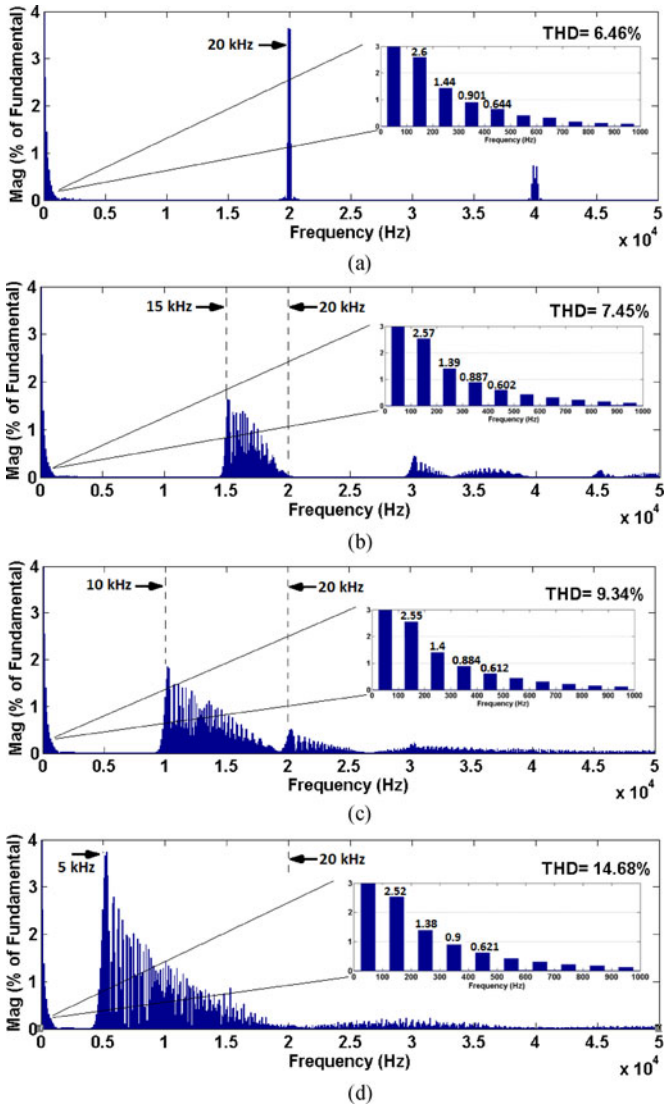

Fig. 9. Harmonic spectrum of output current (inverter side) before the *LCL* filter: (a) CSF PWM, $f_{C=}10\,\text{kHz}$, (b) CB-VSF PWM, $f_{\text{CB}-\text{VSF}} = 7.5$–$10\,\text{kHz}$, (c) CB-VSF PWM, $f_{\text{CB}-\text{VSF}} = 5$–$10\,\text{kHz}$, and (d) CB-VSFPWM, $f_{\text{CB}-\text{VSF}} = 2.5$–$10\,\text{kHz}$.

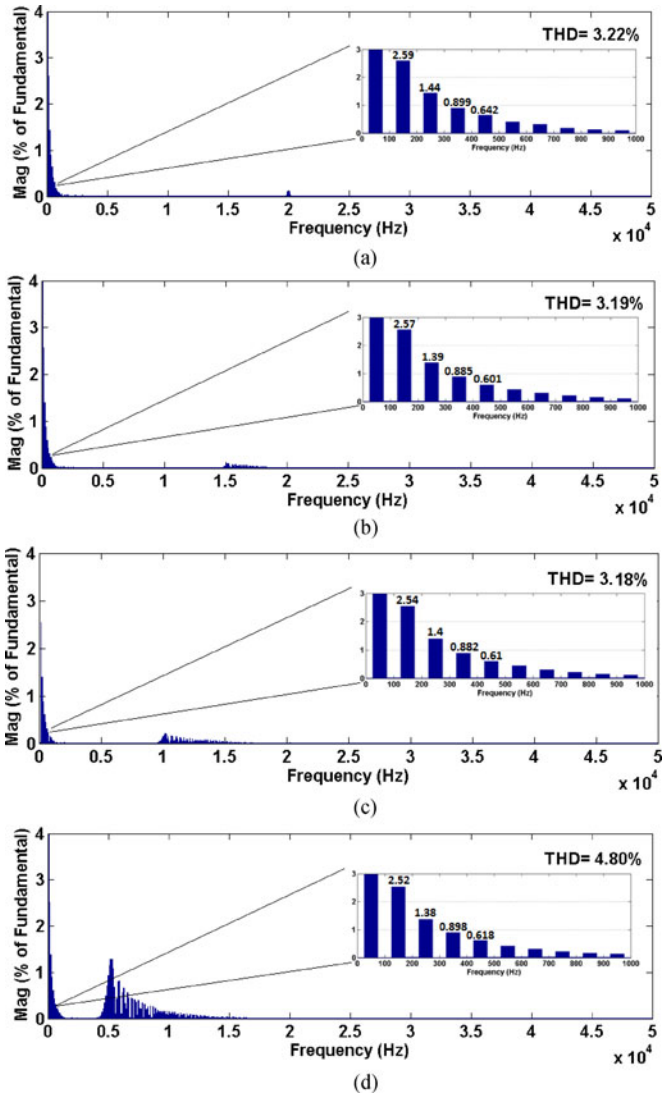

Fig. 10. Harmonic spectrum of output current (load side) after the *LCL* filter: (a) CSF PWM, $f_{C=}10\,\text{kHz}$, (b) CB-VSF PWM, $f_{\text{CB}-\text{VSF}} = 7.5$–$10\,\text{kHz}$, (c) CB-VSF PWM, $f_{\text{CB}-\text{VSF}} = 5$–$10\,\text{kHz}$, and (d) CB-VSFPWM, $f_{\text{CB}-\text{VSF}} = 2.5$–$10\,\text{kHz}$.

Equation (11) matches (2). The frequency range of VSF is $B \cdot f_C < f_{\text{CB}-\text{VSF}} < f_C$, which indicates that the parameter B is an important key factor that determines the frequency range of the proposed CB-VSF PWM. Minimizing B will reduce the number PWM pulses within one fundamental cycle, and thus lowering the switching losses as well as low-order harmonic. When $B = 1.0$, $f_{\text{CB}-\text{VSF}} = f_C$ according to (10), the behavior of the switching scheme becomes similar to that of CSF. When $B < 1.0$, the rate of change of PWM pulses or switching frequency varies throughout the reference cycle. The proposed CB-VSF PWM scheme is shown in Fig. 6.

For the CSF technique, the number of PWM pulses per reference cycle $N_{\text{PWM\_CSF}}$ is the ratio of CSF to reference frequency [16]:

$$N_{\text{PWM\_CSF}} = f_C / f \tag{12}$$

where f is the reference frequency (50 Hz).

On the other hand, total number of PWM pulses per reference cycle for proposed CB-VSF PWM $N_{\text{PWM\_CB}-\text{VSF}}$ is not that straightforward. It is determined by the covered area under the curve of Fig. 5. In other words, $N_{\text{PWM\_CB}-\text{VSF}}$ can be calculated by taking the integration of (10) over a reference period as

$$N_{\text{PWM\_CB}-\text{VSF}} = \frac{N_{\text{PWM\_CSF}}}{2\pi} \int_0^{2\pi} \{1 - [(1-B) * \text{abs}(\sin(\omega t))]\} d\omega t. \tag{13}$$

Fig. 7 shows the total number of pulses for conventional PWM and proposed CB-VSF PWM methods. The number of pulses is calculated according to (13) and listed in Table I. As expected, the total number of PWM pulses in CB-VSF PWM reduces as

TABLE III
IGBT DEVICE PARAMETERS FOR LOSS SIMULATION [22]

Parameters	Value
Device : IGBT	IXGH40N60C2
Frequency	50 Hz
Saturation voltage, $V_{\mathrm{CE(SAT)}}$	<1.7 V
Forward voltage, V_F	2.7 V
Junction temperature, $T_{j(\max)}$	150 °C
Turn-on energy losses, E_{ON} @ $V_{\mathrm{dc}} = 400$ V	0.3 mJ
Turn-off energy losses, E_{OFF} @ $V_{\mathrm{dc}} = 400$V	0.5 mJ
Pcond_Q calibration factor	1
Psw_Q calibration factor	1
Pcond_D calibration factor	1
Psw_D calibration factor	1

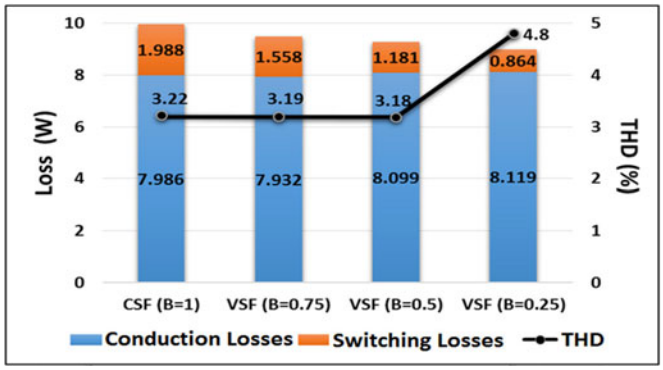

Fig. 11. Comparison of switching loss and THD.

compared to conventional CSF PWM, with a greater reduction with a lower value of *B*.

III. SIMULATION RESULTS

Simulation is carried out via MATLAB/Simulink to investigate the operation and overall performance of the discussed PWM techniques. The discussed PWM methods are implemented in a single-phase full-bridge inverter with the *LCL* filter as shown in Fig. 2. All the simulations are carried out based on the same parameters as listed in Table II. A conventional 10 kHz unipolar CSF PWM is used as the baseline for comparison. An *LCL* filter is hence designed based on the standard method [11] for CSF PWM. Based on the parameters chosen, $f_r = 4\,\mathrm{kHz}$ and $f_{\max} = 40\,\mathrm{kHz}$ according to (4) and (5), respectively. For the proposed CB-VSF PWM method, three frequency ranges are investigated, i.e., 2.5–10, 5–10, and 7.5–10 kHz, and are compared with conventional CSF PWM ($f_c = 10$ kHz). It is worth noting that since unipolar PWM is implemented, it carries double effective switching frequency characteristic.

The output voltage and output current (inverter side) before the *LCL* filter are presented in Fig. 8. As expected, when $f_{\mathrm{CB-VSF}}$ of proposed CB-VSF PWM is reduced, the current ripple is relatively larger as indicated in Fig. 8(b)–(d). Nevertheless, the high-frequency current ripple will be eliminated with the *LCL* filter. Higher quality (lower THD) output voltage and current will be obtained on the load side.

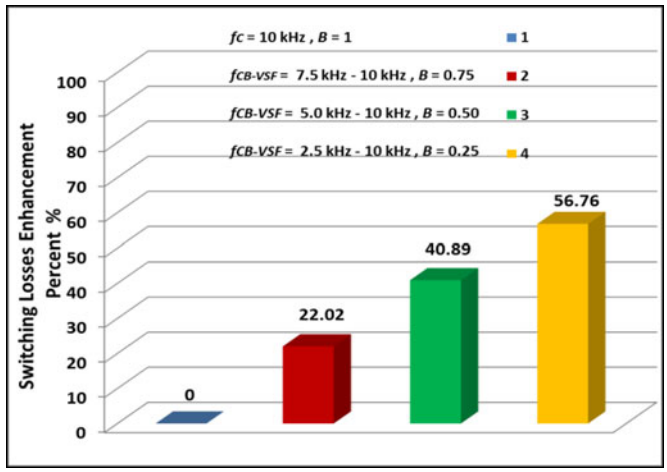

Fig. 12. Switching losses enhancements of discussed PWM methods.

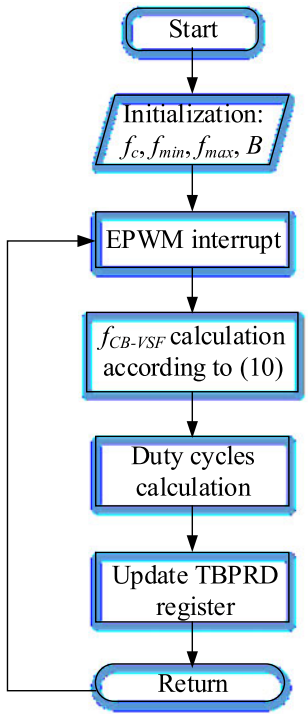

Fig. 13. Flow chart of the process sequency of loading the desired data to the ePWM block.

The ripple analysis is further investigated by applying fast Fourier transform to obtain the current harmonic spectrum, as presented in Fig. 9. For the conventional CSF PWM method, the harmonic component falls around the switching frequency as shown in Fig. 9(a). The large energy component at switching frequency produces undesirable acoustic noise in the filter inductor. This issue is mitigated with proposed CB-VSF PWM. As presented in Fig. 9(b)–(d), in the spectrum, harmonics components are distributed across a wide frequency range. Furthermore, the magnitude of individual harmonic is lower than that of the CSF PWM technique. It is worth noting that the frequency range of the harmonic spectrum for proposed

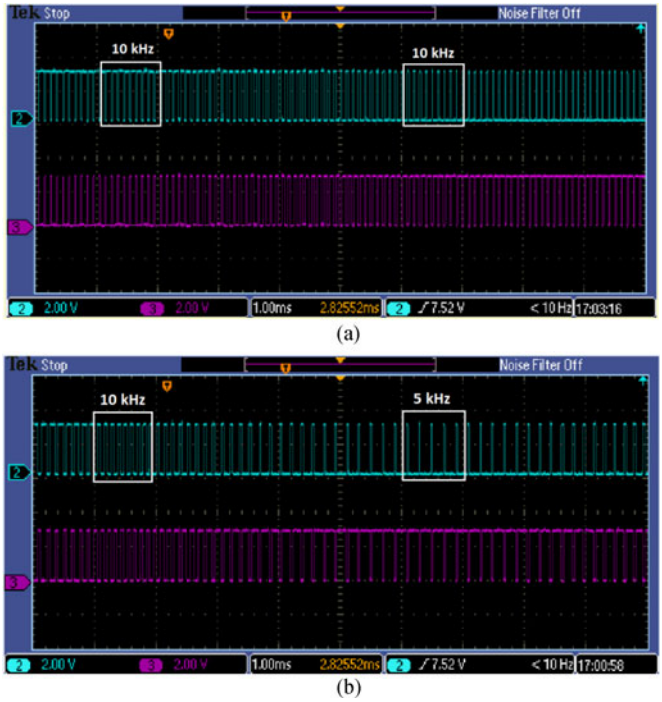

Fig. 14. PWM pulses for (a) constant switching frequency at $f_c = 10\,\text{kHz}$ and (b) proposed CB-VSFPWM technique at $f_{\text{CBVSF}} = 5.0\text{–}10\,\text{kHz}$.

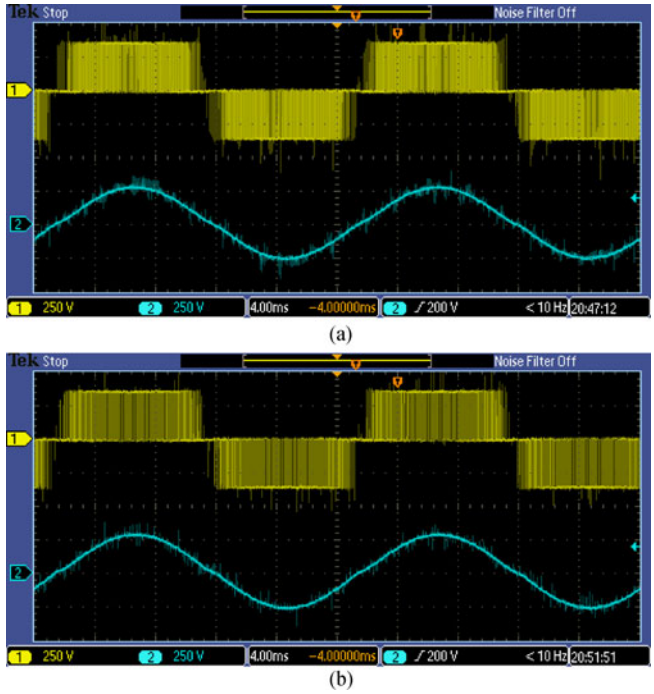

Fig. 15. Inverter voltage (top) and load voltage (bottom) waveforms: (a) conventional CSF PWM technique at $f_c = 10\,\text{kHz}$, and (b) proposed CB-VSFPWM techniques at $f_{\text{CBVSF}} = 5\text{–}10\,\text{kHz}$.

CB-VSF PWM methods can be predicted since a confined frequency band is used. As shown in Fig. 9(b)–(d), the spectrum falls within the frequency bands. Reducing the effective switching frequency will increase current ripples which degrade THD performance. Nonetheless, the current ripples are dominated by the high-switching frequency harmonic components which can be easily attenuated with the proper design of the *LCL* filter for the corresponding frequency bands, as will be shown in Fig. 10.

Fig. 10 shows the harmonic spectrum of the output current (load side) after the *LCL* filter. Based on the simulation results, it is found that the THDs for CB-VSF (7.5–10 and 5–10 kHz) are slightly lower than that of the CSF-PWM. It can be noticed that the high-frequency harmonic is well eliminated for all the discussed PWM techniques, leaving the low-order harmonic components (which cannot be filtered with the *LCL* filter). These low-order harmonic components are generated by dead-time effect as proven in (9). Since the proposed CB-VSF PWM scheme has lower effective switching frequency, the impact of dead time is lower compared to the CSF-PWM scheme. This phenomenon is clearly observed in the microscopic harmonic spectrum in Fig. 10, which shows the reduced magnitude of the low-order harmonic components in proposed CB-VSF PWM as the effective switching frequency is reduced. Furthermore, the fundamental components are higher in the proposed PWM method and this explains why the current THD (after filter) is reducing even though the effective switching frequency is lower. Nevertheless, as $f_{\min}$ (effective switching frequency $= 5$ kHz) is approaching f_r (4 kHz) of the *LCL* filter, the attenuation of the high-frequency components becomes difficult as shown in Fig. 10(d). Therefore, to avoid resonance and for better attenuation $f_{\min} > f_r$, which has been discussed in Section II. By confining the switching frequencies within a practical band, *LCL* filter design becomes easier and practical to eliminate the harmonic spectrum of the proposed CB-VSF PWM scheme.

The loss analysis is simulated via thermal module in Powersim (PSIM). The simulated device parameters are listed in Table III. Fig. 11 presents the losses and THD results for the discussed PWM techniques. As expected, the conduction losses for both conventional CSF PWM and proposed CB-VSF PWM are almost similar as the same quantity of semiconductors are employed. On the other hand, the proposed CB-VSF PWM methods show improvement with regard to switching losses. The results prove the theoretical analysis of Section III. With reduced number of pulses, the switching losses are undoubtedly reduced in the proposed PWM. The losses are reduced further because the proposed CB-VSF PWM yields lower carrier frequency when the magnitude of the current is large; higher carrier frequency when the magnitude of the current is small. Contrary to common expectation that the reduction in switching frequency will reduce switching losses at the expense of current THD, the proposed CB-VSF PWM not only reduces the switching loss, but lowers the current THD at the same time. With the proposed PWM, the reduced number of pulses minimizes the dead-time effect as explained earlier. It is worth noting that the THD increases significantly when $f_{\min}$ is lower than f_r. As $f_{\min}$ (effective switching frequency $= 5$ kHz) is approaching f_r (4 kHz) of the *LCL* filter, the attenuation of the high-frequency components becomes difficult. The enhancement of the switching losses with respect to that of the conventional CSF PWM

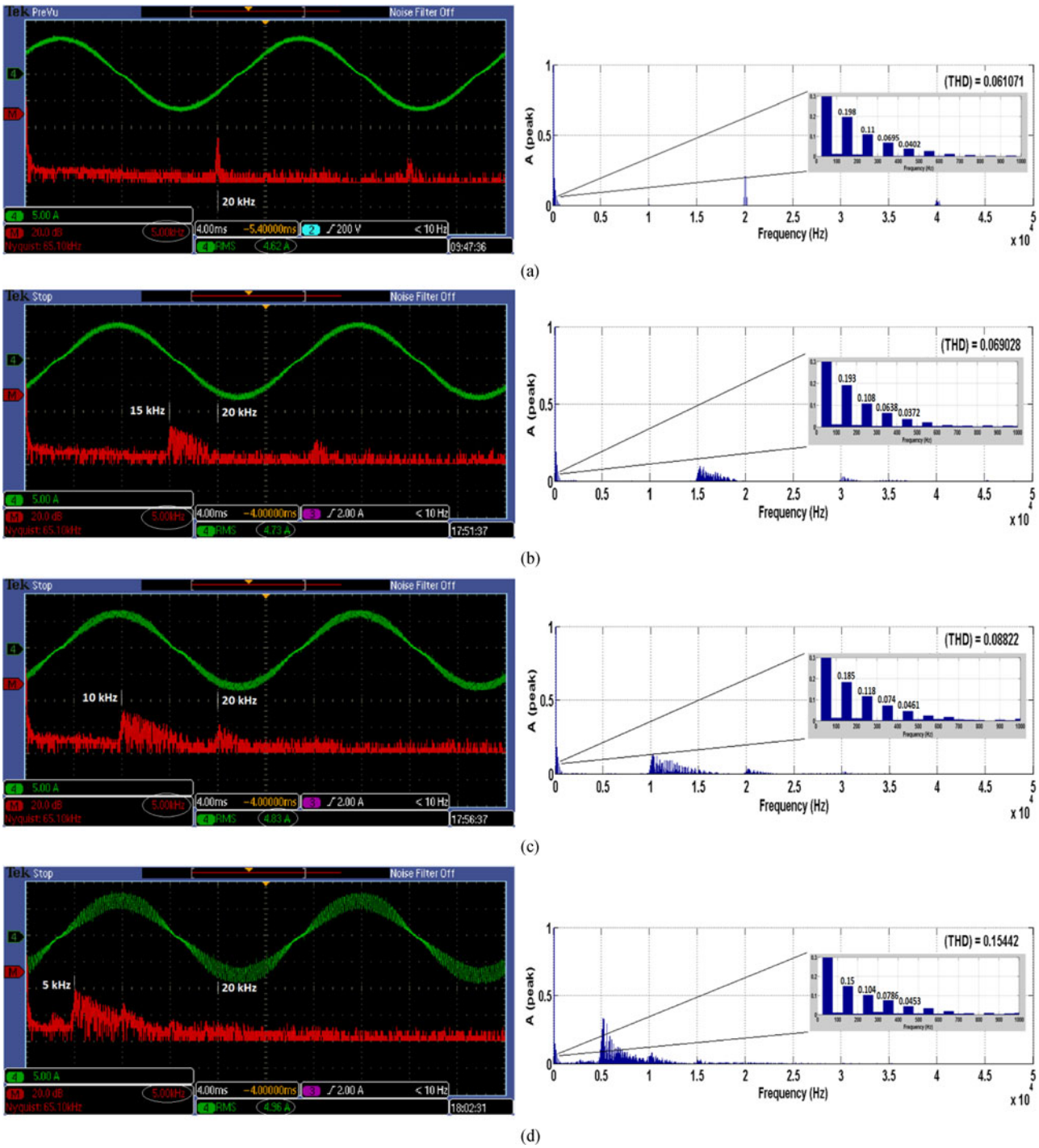

Fig. 16. Harmonics distribution of load currents (inverter side): (a) conventional CSF PWM at $f_c = 10\,\text{kHz}$, (b) proposed CB-VSFPWM at $f_{\text{CBVSF}} = 7.5\text{–}10\,\text{kHz}$, (c) proposed CB-VSFPWM at $f_{\text{CBVSF}} = 5\text{–}10\,\text{kHz}$, and (d) proposed CB-VSFPWM at $f_{\text{CBVSF}} = 2.5\text{–}10\,\text{kHz}$.

method is shown in Fig. 12, the switching loss enhancement, $P_{\text{SW\_enhancement}}\,\%$ is calculated via

$$P_{\text{SW\_enhancement}}\% = \frac{(P_{\text{SW\_CSF}} - P_{\text{SW\_CB-VSF}})}{P_{\text{SW\_CSF}}} * 100\% \tag{14}$$

where $P_{\text{SW\_CSF}}$ and $P_{\text{SW\_CB-VSF}}$ are switching losses of conventional CSF PWM and CB-VSF PWM, respectively.

IV. Experimental Results

In order to verify the theoretical simulation results, the experimental test is carried out based on the simulation parameters as listed in Table II. The proposed CB-VSF PWM schemes (i.e., 2.5–10, 5–10, and 7.5–10 kHz) are investigated here and compared with CSF PWM ($f_c = 10\,\text{kHz}$). All the algorithms are implemented in TMS 320F28335 DSP.

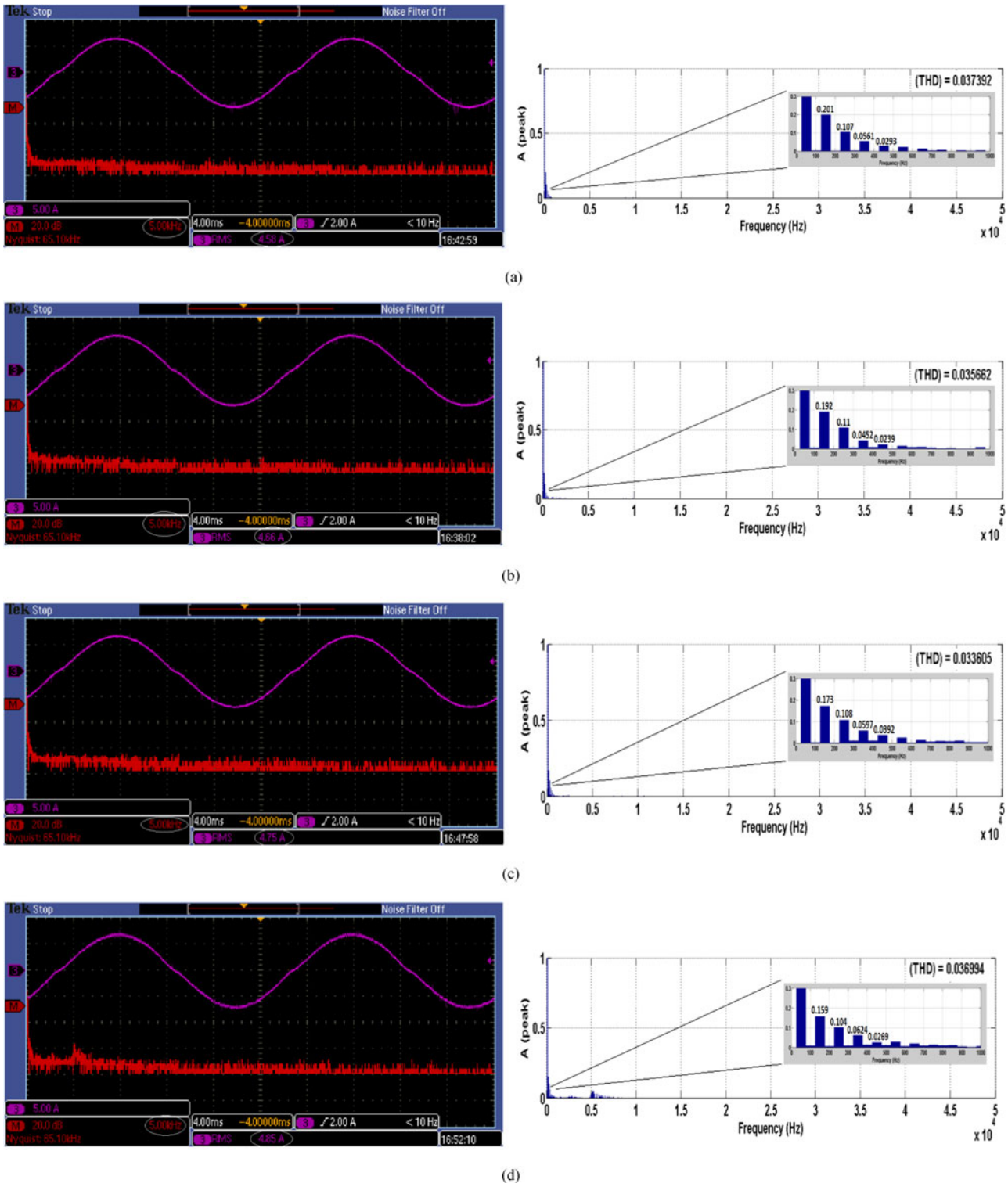

Fig. 17. Harmonics distribution of load currents (load side): (a) conventional CSF PWM at $f_c = 10\,\text{kHz}$, (b) proposed CB-VSFPWM at $f_{\text{CBVSF}} = 7.5$–$10\,\text{kHz}$, (c) proposed CB-VSFPWM at $f_{\text{CBVSF}} = 5$–$10\,\text{kHz}$, and (d) proposed CB-VSFPWM at $f_{\text{CBVSF}} = 2.5$–$10\,\text{kHz}$.

The proposed CB-VSF PWM is implemented based on (10). According to (10), the desired variable frequency will be calculated and updated from time to time. Based on the calculated frequency, the corresponding values will be loaded into the period register of DSP, i.e., time-base period register (TBPRD) for TMS320F28335 DSP, which defines the carrier frequency. In other words, the carrier frequency is update continuously. Fig. 13 shows the flow chart of the process sequency in which the steps start by entering the desired parameters and end by the suitable loaded data to the enhanced

pulse width modulator (ePWM) block of the implemented DSP.

Fig. 14 shows switching pattern and the PWM pulses for both the conventional CSF PWM and the proposed CB-VSF PWM methods. The significant reduction of the number of pulses is noticed in CB-VSF PWM as shown in Fig. 14(b). The inverter voltage and load voltage profile are presented in Fig. 15. One can observe the difference in the shape of different PWM schemes.

Fig. 16 shows the harmonics distribution of the load currents (inverter side) before the *LCL* filter. The harmonics distribution of the conventional CSF PWM is shown in Fig. 16(a). It is noticeable that the harmonic components with high magnitude appear at f_C (10 kHz) and at the multiples of f_C. Fig. 16(b)–(d) illustrates the harmonics spectrum of proposed CB-VSF PWM schemes. As expected, the spectrum is distributed across a wide frequency range. Similar to that of the simulation results, the spectrum falls within the specified frequency bands. By confining the switching frequencies within a practical band, *LCL* filter design becomes easier and practical to eliminate the harmonic spectrum of the proposed CB-VSF PWM scheme.

The harmonic spectrum of the load current (after the *LCL* filter) is presented in Fig. 17. It is indisputable that the *LCL* filter has effectively attenuated the high-frequency harmonic components in the current. However, the low-order harmonic components, which are mainly due to the dead-time effect, cannot be filtered with the *LCL* filter. According to (9), the dead-time effect is proportional to switching frequency. As noticed in the microscopic view of harmonic spectrum of Fig. 17, the magnitude of the low-order harmonic components is smaller with the reducing effective switching frequency. This explains why the current THD (after filter) is reducing in the proposed PWM scheme. Nonetheless, as $f_{\min}$ (effective frequency = 5 kHz) that is approaching f_r (4 kHz) of the *LCL* filter, the attenuation of the high-frequency components becomes difficult. Switching-frequency components are observed in Fig. 17(d). Therefore, to avoid resonance and for better attenuation, $f_{\min}$ of the proposed CB-VSF PWM should always be greater than the resonant frequency of the *LCL* filter, i.e., $f_{\min} > f_r$, which has been discussed in Section II.

In this study, the efficiency is measured via the dc input power and output power [23]–[26]. These powers are measured based on CEC [23], i.e., at 10%, 20%, 30%, 50%, 75%, and 100% of rated power. Then, efficiency is calculated as

$$\eta_{\mathrm{CEC}} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%}. \quad (15)$$

Fig. 18 shows the measured efficiency for different PWM techniques, the calculated Californian efficiency for f_C = 10 kHz, f_{CBVSF} = 7.5–10 kHz, f_{CBVSF} = 5–10 kHz, and f_{CBVSF} = 2.5–10 kHz are 92.89%, 93.47%, 93.98%, and 94.29%, respectively. The result proves the theoretical analysis and simulation investigation. With reduced number of pulses, the switching loss undoubtedly reduces in the proposed technique. This fact reflects positively on inverter efficiency. The loss is reduced further because the proposed CB-VSF PWM yields higher carrier frequency when the magnitude of the current is small; lower carrier frequency when the magnitude of the current is large. The increase of the load current also reflects the increase of the efficiency as shown in Fig. 18. The experimental performance comparisons for the discussed PWM methods are summarized in Table IV.

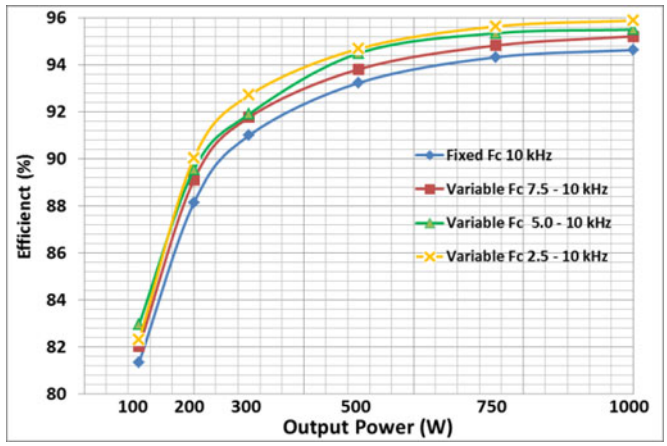

Fig. 18. Measured efficiency for different loads of the conventional and the proposed PWM technique based inverter.

TABLE IV
PERFORMANCE COMPARISONS FOR VARIOUS PWM METHODS

	Conventional CSF PWM, 10 kHz	Proposed CB-VSFPWM, 7.5–10 kHz	Proposed CB-VSFPWM, 5.0–10 kHz	Proposed CB-VSFPWM, 2.5–10 kHz
load current (A)	4.58	4.66	4.75	4.85
Californian eff. (%)	92.89	93.47	93.98	94.29
THD after *LCL* filter (%)	3.739	3.566	3.605	3.699

In addition to conventional CSF PWM, the performance of another VSF PWM, i.e., the RPWM (implemented based on [5]), is compared here with proposed CB-VSF PWM (5–10 kHz). Based on [5], the switching frequency and period of the RPWM are given by

$$f_s = f_{\mathrm{so}} + \Delta \cdot R \quad (16)$$

$$0.75T_{\mathrm{samp}} < T_s < 1.5T_{\mathrm{samp}} \quad (17)$$

where f_{so} is the average switching frequency, Δf_s is switching frequency random range [(0.67 f_s to 1.33 f_s according to (17)], R is random number in the range [–1, +1], and T_{samp} represents the sampling time which is reciprocal of switching frequency f_s. It is clearly seen in Fig. 19 that the PWM pulses, voltage, and harmonic spectrum are randomly distributed. The magnitude of the low-order harmonics and the current THD are higher as compared to proposed CB-VSF PWM. To further investigate the proposed PWM, m is increased to 0.9. Thus, the maximum allowable switching frequency $f_{\max}$ becomes 17 kHz according to (5). Since unipolar PWM is used, the actual switching frequency of RPWM is 13.3–26.7 kHz (37.5–75 μs) while 10–17 kHz (50–100 μs) in the proposed CB-VSF PWM. Pulse dropping effect is observed in RPWM. As shown in Fig. 20(a),

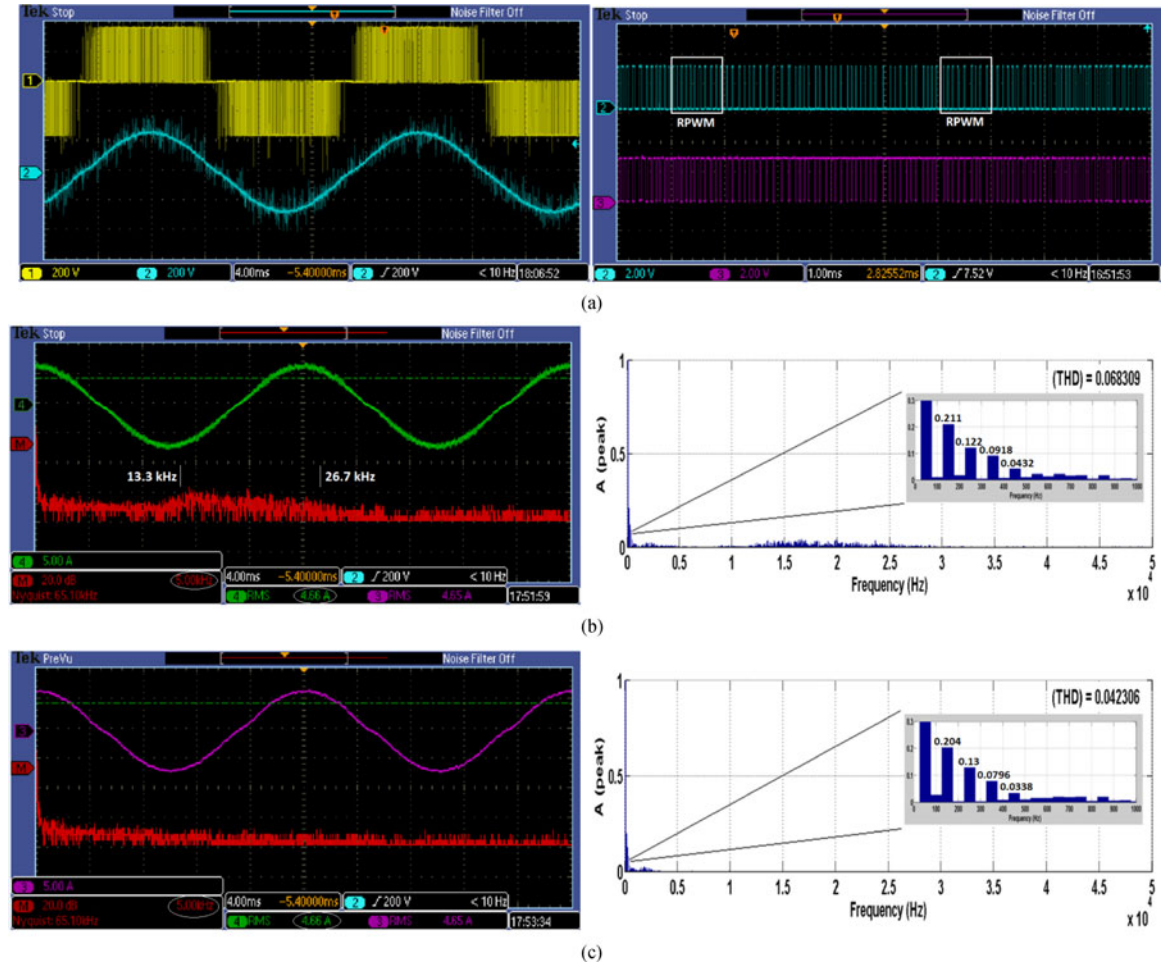

Fig. 19. Random PWM [5] at $m = 0.8$: (a) PWM pulses, (b) inverter voltage (top) and load voltage (bottom), (c) harmonics distribution of load currents (inverter side), and (d) harmonics distribution of load currents (load side).

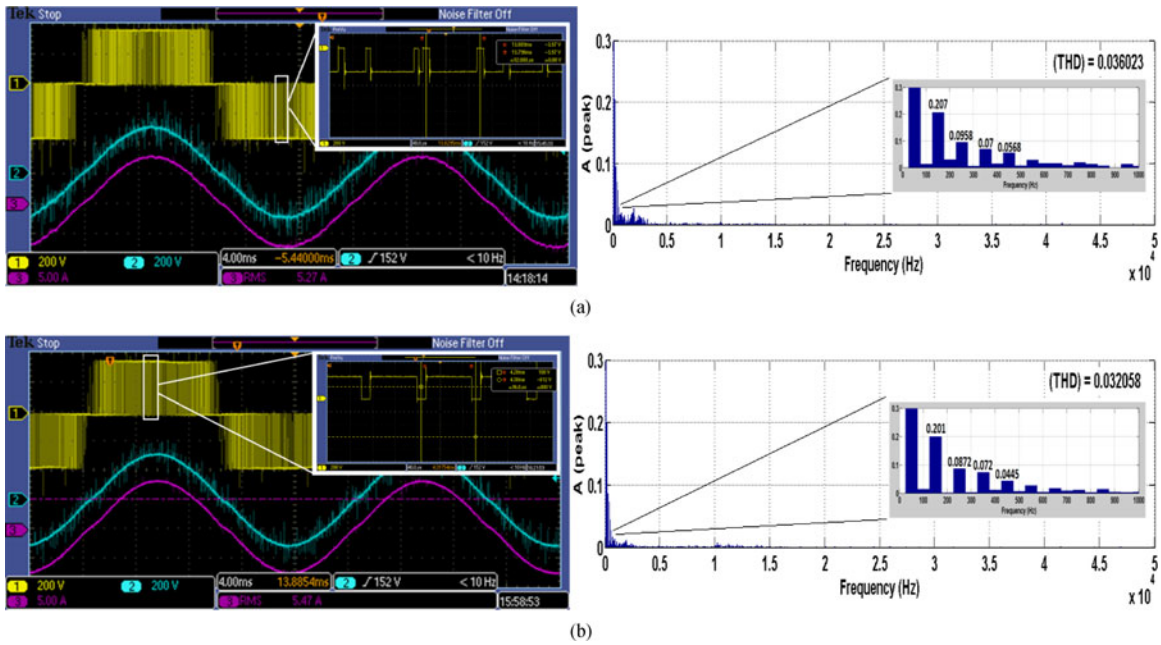

Fig. 20. Inverter voltage (Ch 1: yellow trace) with zoomed-in view for pulse drop demonstration, load voltage (Ch 2: cyan trace), and load current (Ch 3: pink trace) with harmonics spectrum of the load currents (load side) at $m = 0.9$: (a) random PWM [5] and (b) CB-VSF PWM at 5–10 kHz.

the random period reaches up to 92.8 μs which is more than the designed period (75 μs).

V. Conclusion

In this study, a CB-VSF PWM is proposed by comparing a sinusoidal modulation signal with CB variable triangular carrier based on a unipolar technique. To achieve effective reduction in switching losses, the CB-VSF PWM is designed in such a way that the carrier frequency is higher when the magnitude of the fundamental current is small (the ripple is large); and carrier frequency is lower when the magnitude of the current is large (ripple is small). Contrary to common expectation that the reduction in switching frequency will reduce switching losses at the expense of current THD, the proposed switching scheme not only reduces the switching loss, but lowers the current THD at the same time. This is mainly because of the reduced dead-time effect and increased fundamental component in the proposed CB-VSF PWM technique.

By having the VSF confined within a frequency band, the proposed technique preserves the advantages of VSF PWM while avoiding the negative effects of *LCL* filter resonance and overly high switching frequency. All the theoretical discussions are validated through simulation and experimental results in a 1 kW inverter, which confirms the superior performance of the proposed CB-VSF-PWM technique. It is hoped that the findings in this paper will find new practical uses for VSF PWM in high efficiency and low THD applications.

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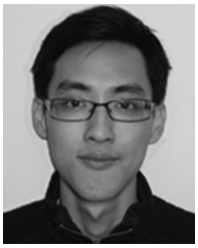

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