

# An Asymmetric Three-Level Neutral Point Diode Clamped Converter for Switched Reluctance Motor Drives

Fei Peng, *Member, IEEE*, Jin Ye, *Senior Member, IEEE*, and Ali Emadi, *Fellow, IEEE*

**Abstract**—An asymmetric three-level neutral point diode clamped converter for switched reluctance motor drives is proposed in this paper. The modulation method, the dc-link voltage balancing algorithm, and the current control scheme of this converter are presented. The proposed three-level converter is compared with the conventional two-level asymmetric half-bridge converter in terms of cost, current ripple, noise, and power losses. Compared to the conventional two-level converter, the proposed three-level converter has much lower current ripple, lower noise, and higher efficiency. The effectiveness of the proposed converter is verified by both simulation and experimental results.

**Index Terms**—Current control, pulse width modulation (PWM), switched reluctance motor (SRM), three-level converter.

## I. INTRODUCTION

SWITCHED reluctance motor (SRM) is an attractive alternative to induction and permanent magnet motors due to its simple rugged structure and low cost [1]–[3]. In general, an SRM is driven by the asymmetric half-bridge converter with the current hysteresis controller, as shown in Fig. 1. Under the same voltage rating, the winding inductance (both the aligned and unaligned inductance) decreases to obtain the larger phase current as the power rating of SRM increases. With lower inductance, either the switching frequency increases to keep the same current ripple or the current hysteresis band is increased to maintain the same switching frequency. The increase of the switching frequency or current ripple introduces higher switching losses of power devices, iron losses, as well as higher winding losses due to the skin and proximity effects. Also, it brings challenges

Manuscript received June 16, 2016; revised October 9, 2016; accepted December 11, 2016. Date of publication December 20, 2016; date of current version June 23, 2017. This paper was presented at the *2015 IEEE Transportation Electrification Conference and Expo*, Dearborn, MI, USA, June 2015. However, this paper is significantly improved compared with the conference version of the paper. This work was supported by the Canada Excellence Research Chairs Program and the Natural Sciences and Engineering Research Council of Canada Discovery Grants Program. Recommended for publication by Associate Editor J. R. Espinoza.

F. Peng is with the School of Electrical Engineering, Southeast University, Nanjing, Jiangsu 210018, China (e-mail: pengf6@mcmaster.ca).

J. Ye is with the School of Engineering, San Francisco State University, San Francisco, CA 94132 USA (e-mail: jinye@sfsu.edu).

A. Emadi is with the Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON L8S 4L8 Canada (e-mail: emadi@mcmaster.ca).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2016.2642339

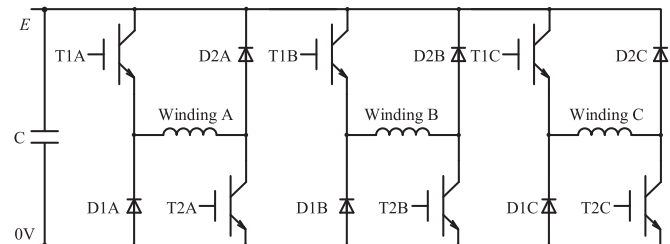


Fig. 1. Conventional asymmetric half bridge for three-phase SRM drives.

in the design of the winding insulation and increases the electromagnetic interference (EMI) issues [4]–[6]. Therefore, the asymmetric half bridge is not a promising topology for high power SRMs with very low inductance.

As compared to conventional two-level converters, multilevel converters have several advantages, such as the lower magnitude of current ripple, lower power losses at high switching frequency, lower common-mode voltage, and lower EMI [7]. Due to these advantages, multilevel converters have gained popularity in medium-voltage applications. Several multilevel converter topologies have been reported, including cascaded H-Bridge converters, neutral point diode clamped (NPC) multilevel converters, flying capacitor multilevel converters, generalized multilevel converters, mixed-level hybrid multilevel converters, etc. Their operational principles, modulation methods, and application fields are investigated in [7]. Although, multilevel converters are mainly used in high-power medium-voltage applications, they also present system-level benefits in low-voltage applications [8]. Cascaded H-Bridge converters need extra independent dc sources, and flying capacitor converters need considerable amount of voltage sensors. Therefore, considering the critical cost requirement in low-voltage applications, the NPC multilevel topology is the most attractive candidate for three-level converters [9].

In [8], an NPC three-level converter with IGBTs is compared with conventional two-level converters in terms of power losses, loss distribution among semiconductors, common-mode voltage, reliability, and cost. The comparison results show that the three-level converter has much less total losses when the switching frequency is above 4000 Hz. Also, three-level converters present lower common-mode voltage and lower cost although more power devices are required. In [10], the possibility

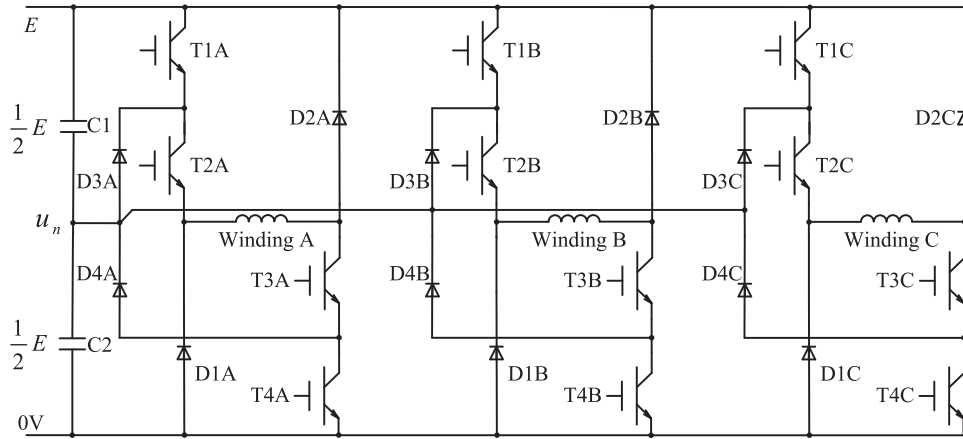


Fig. 2. Proposed asymmetric NPC three-level converter for three-phase SRM drives.

of using MOSFETs in a NPC three-level converter is investigated and a special gate driver circuit is proposed to reduce the cost. In [11], a quasi-three-level converter for SRM drives is proposed to reduce the rising and falling time of the phase current. In [12], a special multilevel converter for four-phase SRM drives is proposed. In order to increase or decrease the phase current rapidly, phase windings are magnetized or demagnetized using the boosting voltage. However, the boosting voltage cannot be controlled directly and it varies with the phase current, rotor speed, winding inductance, and the electrical parameters of power devices. In [13], a family of asymmetric multilevel converters for SRM are presented, including the cascaded asymmetric H-bridge converter, the flying capacitor multilevel asymmetric converter, and the NPC multilevel asymmetric converter. In [14], an asymmetric NPC five-level converter and an asymmetric modular five-level converter are proposed for SRM drives. However, since the current hysteresis controller is adopted, only one voltage level is applied on the motor winding. Therefore, it does not take the advantages of multilevel converters.

In this paper, a novel asymmetric three-level NPC converter for SRM drives is proposed. The operational modes of this converter are analyzed in details. The pulse width modulation (PWM) method, dc-link voltage balancing algorithm, and the current control method of this converter are presented. The proposed converter is compared with the conventional two-level asymmetric half-bridge converter in terms of cost, current ripple noise, and power losses. It is shown that the cost of the proposed converter is similar to the conventional two-level converter. In addition, the proposed converter reduces current ripple as well as switching losses significantly. Moreover, with the proposed current control method, the dynamic response of the proposed converter is almost as fast as that of the current hysteresis regulation.

## II. OPERATIONAL PRINCIPLE OF THE PROPOSED ASYMMETRIC NPC THREE-LEVEL CONVERTER

The proposed NPC three-level converter for three-phase SRM drives is shown in Fig. 2. The required blocking voltages of the main switches (T1X, T2X, T3X, and T4X, X=A, B, or C)

and clamping diodes (D3X, D4X) are half of the dc-link voltage ( $E/2$ ). The required blocking voltages of D1X and D2X are full of the dc-link voltage  $E$ . There are nine operational modes for each phase leg, which are illustrated in Fig. 3. For simplicity, all the power devices of the topology are assumed to be ideal devices. The possible modes of the four switches in one phase is illustrated in Table I. The phase voltage  $u_w$  and the neutral point potential  $u_n$  under different modes are also listed in Table I. The ON and OFF states of the switches are denoted as 1 and 0, respectively.  $\uparrow$  represents the increase of potential,  $\downarrow$  represents the decrease of potential, and  $\times$  represents no changes. There are five voltages for each phase. Different modes produce the same voltage with different behaviors of the neutral point potential. In order to determine which mode should be applied, the modulation scheme has to be developed. The detailed operational modes are explained as follows.

*Mode 1 [Fig. 3(a)]:* All the switches are ON. The dc-link voltage  $E$  is applied to the phase winding and the load current flows through T1, T2, T3, and T4. The diodes D1, D2, D3, and D4 are blocked. No current flows into the neutral point. Therefore, the neutral point potential is unchanged in this mode. The phase voltage is  $E$ .

*Mode 2 [Fig. 3(b)]:* T1, T2, and T3 are ON. T4 is OFF. Diodes D1, D2, and D3 are blocked. The load current flows through T1, T2, T3, and D4. Current flows into the neutral point. Therefore, the neutral point potential increases in this mode. The phase voltage is around  $0.5E$ .

*Mode 3 [Fig. 3(c)]:* T1 and T2 are ON. T3 and T4 are OFF. Load current flows through T1, T2, and the freewheeling diode D2. Diodes D1, D3, and D4 are blocked. No current is injected into the neutral point. Therefore, the neutral point potential is unchanged in this mode. The phase voltage is 0.

*Mode 4 [Fig. 3(d)]:* T1 is OFF. T2, T3, and T4 are ON. D1, D2, and D4 are blocked. Current flows through D3, T2, T3, and T4. The neutral point potential decreases in this mode because the current flows out from the neutral point. The phase voltage is around  $0.5E$ .

*Mode 5 [Fig. 3(e)]:* T1 and T4 are OFF. T2 and T3 are turned ON. Current flows through T2, T3, D3, and D4. Diodes D1 and D2 are blocked. No current is injected into the neutral point.

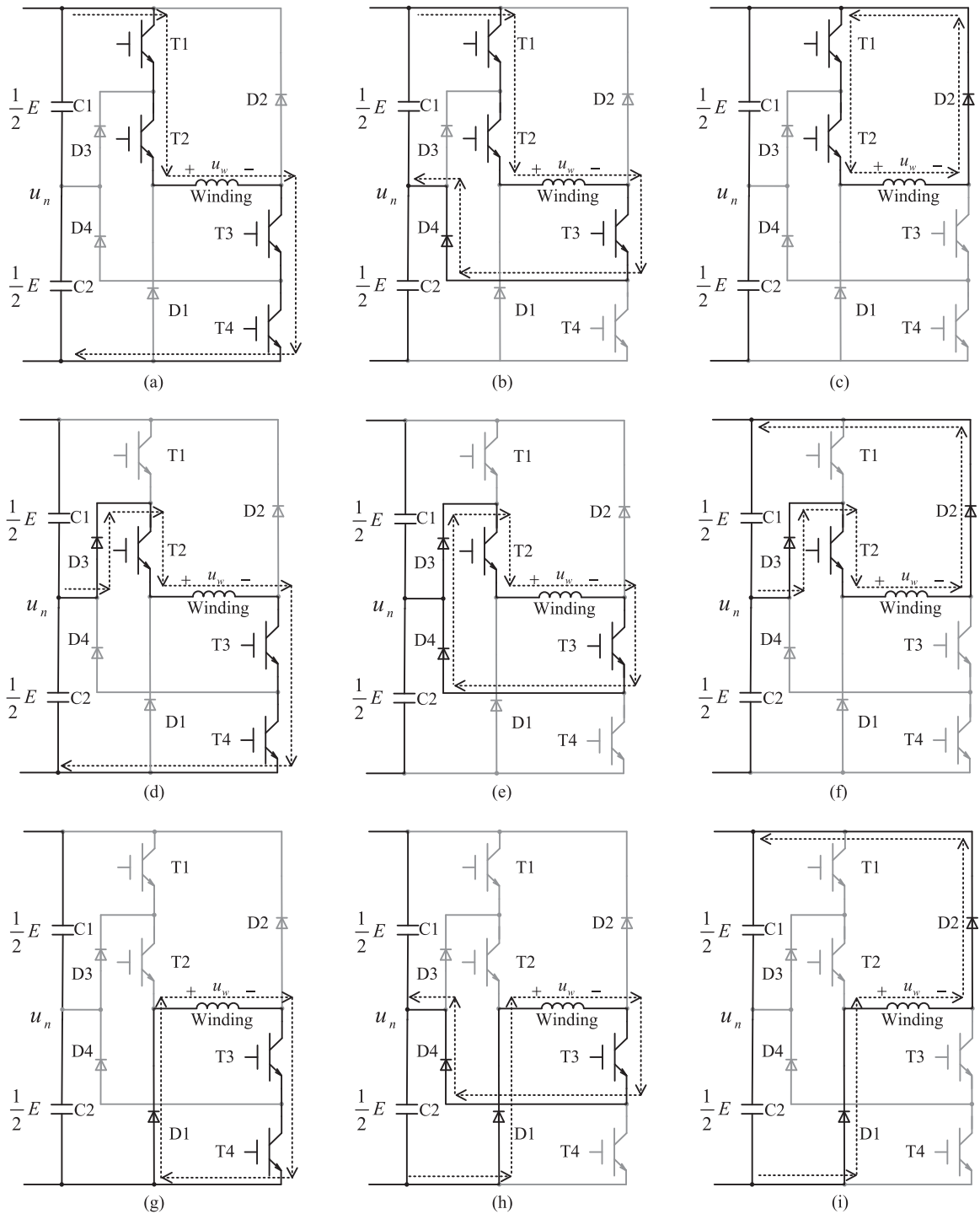


Fig. 3. Operational modes of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9.

Therefore, the neutral point potential is unchanged in this mode. The phase voltage is 0.

*Mode 6 [Fig. 3(f)]:* T1, T3, and T4 are OFF. T2 is ON. Current flows through D3, T2, and D2. Diodes D1 and D4 are blocked. Current flows out from the neutral point. Therefore, the neutral point potential decreases in this mode. The phase voltage is around  $-0.5E$ .

*Mode 7 [Fig. 3(g)]:* T1 and T2 are OFF. T3 and T4 are ON. Current flows through T3, T4, and the freewheeling diode D1. Diodes D2, D3, and D4 are blocked. No current is injected into the neutral point. Therefore, the neutral point potential is unchanged in this mode. The phase voltage is 0.

*Mode 8 [Fig. 3(h)]:* T1, T2, and T4 are OFF. T3 is ON. Current flows through D1, T3, and D4. Diodes D2 and D3 are blocked.

TABLE I  
 POSSIBLE MODES OF THE FOUR SWITCHES IN ONE PHASE

Mode number	T1	T2	T3	T4	$u_w$	$u_n$
1	1	1	1	1	$E$	$\times$
2	1	1	1	0	$0.5E$	$\uparrow$
3	1	1	0	0	0	$\times$
4	0	1	1	1	$0.5E$	$\downarrow$
5	0	1	1	0	0	$\times$
6	0	1	0	0	$-0.5E$	$\downarrow$
7	0	0	1	1	0	$\times$
8	0	0	1	0	$-0.5E$	$\uparrow$
9	0	0	0	0	$-E$	$\times$

Current is injected into the neutral point. Therefore, the neutral point potential increases in this mode. The phase voltage is around  $-0.5E$ .

*Mode 9 [Fig. 3(i)]:* All the switches are OFF. Current flows through the freewheeling diodes D1 and D2. Diodes D3 and D4 are blocked. No current is injected into the neutral point. Therefore, the neutral point potential is unchanged in this mode. The phase voltage is 0.

### III. COST COMPARISON BETWEEN THE TWO-LEVEL AND THE PROPOSED NPC THREE-LEVEL CONVERTER FOR SRM

The volt-ampere (VA) rating is often adopted to evaluate the costs of the converters for SRM drives [15]. The blocking voltage of the switches in the proposed topology is half of that in conventional two-level converter. Although the number of switches in the proposed converter is doubled, the total voltage ratings of switches are the same for these two converters. In addition, the current ratings of switches in both of the converters are the same. Therefore, the total VA rating of switches in the proposed converter remains the same as that of the conventional two-level converter. This indicates the cost on switches of the proposed converter is almost the same as that of the conventional two-level converter.

The diodes D1X and D2X in Fig. 2 need to block the full voltage as they do in the conventional two-level asymmetric half-bridge converter. However, different from a conventional two-level converter, D1X and D2X are only used when the phase winding needs to cut off when the current in the phase winding need to flow back to the dc link. Therefore, D1X and D2X could be selected according to the peak repetitive forward current  $I_{FRM}$  instead of average forward current  $I_F$ . In this comparison, the current rating  $I_F$  of the diodes D1X and D2X is selected as half of that in the conventional two-level converter. However, diodes D3X and D4X have to provide the free-wheeling current path for the proposed converter, which increases the VA rating of the proposed topology.

Table II gives the comparison of the VA ratings of switching devices and diodes between the proposed three-level converter and the conventional two-level converter.  $I$  is the rated phase current. It is shown that their total VA ratings on both switching devices and diodes are the same. This indicates that the cost of power devices in the proposed converter is almost the same as those is in the conventional two-level converter.

 TABLE II  
 VA RATINGS COMPARISON

	Two-level			Three-level		
	rating	amount	total	rating	amount	total
Switches	$E \times I$	6	$6E \times I$	$0.5E \times I$	12	$6E \times I$
Switches Total			$6E \times I$			$6E \times I$
D1X,D2X	$E \times I$	6	$6E \times I$	$E \times 0.5I$	6	$3E \times I$
D3X,D4X	$E \times I$	0	0	$0.5E \times I$	6	$3E \times I$
Diodes Total			$6E \times I$			$6E \times I$

The proposed converter needs two dc bus capacitors. The capacitance of each capacitor has to be doubled to maintain the same voltage ripple on the dc link. However, compared to two-level converter, the capacitor voltage rating is divided in half. Therefore, total energy storage of dc capacitors is the same and the cost on capacitors for the proposed converter is not increased.

Although the proposed converter increases the cost because of more gate drivers and an additional voltage sensor to control the neutral point potential, the cost of passive components such as EMI filters can be reduced. Therefore, the costs of the two-level converter and proposed three-level converter would be similar.

### IV. MODULATION METHOD OF THE PROPOSED CONVERTER

Two-phase voltages are used by the conventional current hysteresis control for SRM. However, there are five-phase voltages in the proposed NPC three-level converter:  $-E$ ,  $-0.5E$ ,  $0$ ,  $0.5E$ , and  $E$ . Therefore, the current hysteresis control is not suitable for the NPC three-level converters, and a PWM method should be developed.

#### A. Basic Modulation Method

The basic modulation method for the NPC three-level converter is shown in Fig. 4. As is shown, four space sections are formed by five-phase voltages, and a triangle carrier waveform is applied for each space section. There is  $T/2$  shift between these triangle waveforms, where  $T$  is the switching period. The reference voltage  $u_{ref}$  provided by the current controller is located in one of the sections. If  $u_{ref}$  is higher than the carrier waveform, the top voltage of this section is applied. If  $u_{ref}$  is lower than the carrier waveform, the bottom voltage of this section is applied. The shifted carrier waveforms provide minimum switching actions when  $u_{ref}$  is both positive and negative.

After selecting the output voltage, the corresponding switching mode has to be determined. As shown in Table I, two modes (mode 6 and mode 8) can produce  $-0.5E$  and two modes (mode 2 and mode 4) can produce  $0.5E$ . Mode 8 and mode 2 increase the neutral point potential  $u_n$ . Mode 6 and mode 4 decrease  $u_n$ . There are three modes (mode 3, mode 5, and mode 7) which can produce 0 V, and these three modes do not have impact on the neutral point potential. However, compared to the other modes, mode 5 needs the least switching actions to switch to other nonzero voltages. Therefore, mode 5 is selected to produce voltage 0. As a summary, if the voltage is selected as  $-E$ ,  $0$ , and

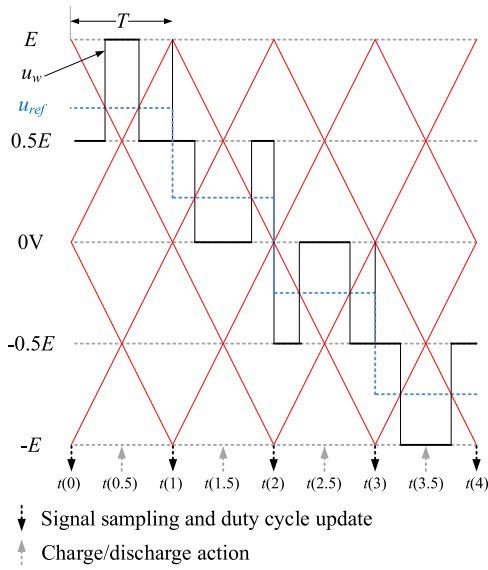


Fig. 4. Basic modulation method of the proposed NPC three-level converter.

TABLE III  
METHOD OF SELECTING THE SWITCHING MODES

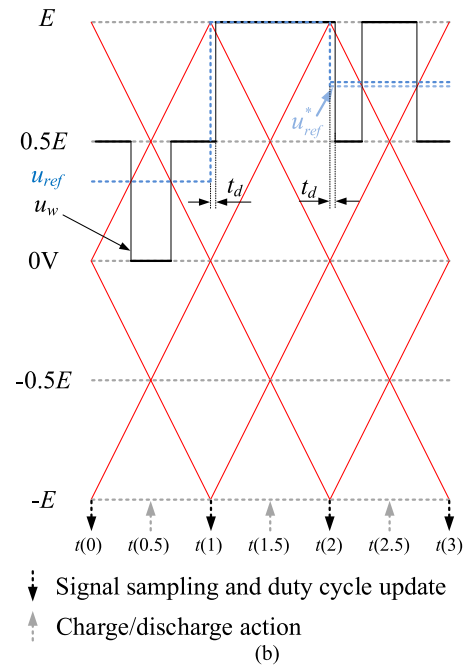
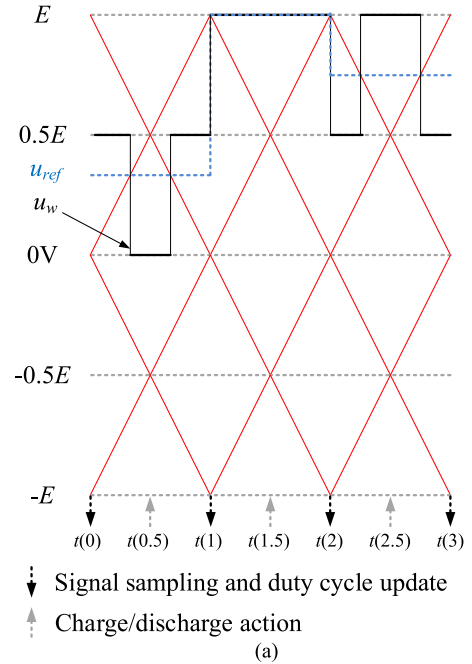
Mode	Voltage				
	$-E$	$-0.5E$	$0$	$0.5E$	$E$
$u_n > 0.5E$	9	6	5	4	1
$u_n < 0.5E$	9	8	5	2	1

$E$ , modes 9, 5, and 1 should be selected correspondingly. If the output voltage is selected as  $-0.5E$ , and the neutral point potential is below  $0.5E$ , mode 8 should be selected to increase the neutral point potential; otherwise, mode 6 should be selected to reduce the neutral point potential. Similarly, if the output voltage is selected as  $0.5E$ , and the neutral point is below  $0.5E$ , mode 2 should be selected, otherwise mode 4 should be selected. By using this algorithm, the neutral point potential can be balanced around  $0.5E$ . Table III describes the method of selecting the switching modes.

For the digital implementation of the modulation method, switching action should be avoided when signals being sampled—such as current, voltage, and position. Therefore, as shown in Fig. 4, signals are sampled at  $t(k)$ ,  $k = 0, 1, 2, \dots$ . The duty ratio is also updated at this time. Since charging or discharging the neutral point will lead to switching actions, in order not to introduce noise to the signals sampled,  $u_n$  is sampled at  $t(k + 0.5)$ ,  $k = 0, 1, 2, \dots$ . Therefore, the charge or discharge action is also updated at this time.

### B. Modified Modulation Method for Special Cases

There are several special cases in which the switching action and signal sampling happen simultaneously. The modulation method should be modified to avoid introducing noise to the sampled signals.

Fig. 5. Basic modulation method (a) and the modified modulation method (b) when  $u_{ref} = E$ .

1)  $u_{ref} = E$  or  $u_{ref} = -E$ : As shown in Fig. 5(a), if  $u_{ref} = E$  at  $t(1)$ , the switching action and signal sampling are simultaneous at both  $t(1)$  and  $t(2)$ . To prevent the switching action from interfering the signal sampling process, a short delay of  $t_d$  is inserted as shown in Fig. 5(b). Since  $t_d$  is inserted, to keep the same average output voltage of the interval  $t(2)$  to  $t(3)$ , the  $u_{ref}$  at  $t(2)$  should be modified as

$$u_{ref}^* = u_{ref} - \frac{t_d}{T} E \quad (1)$$

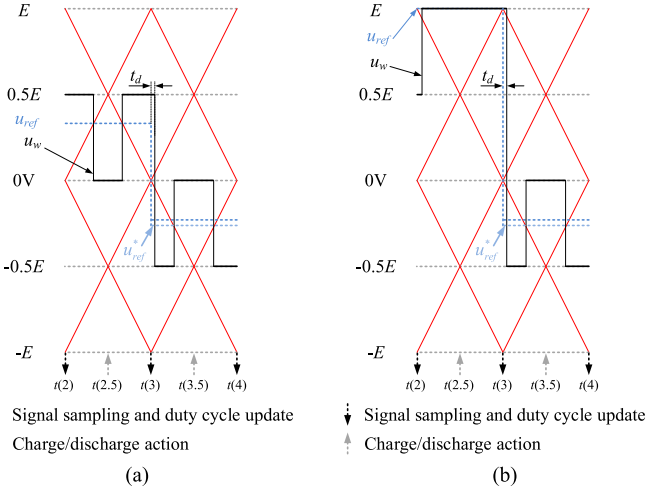


Fig. 6. Modified modulation method when  $u_{\text{ref}}$  crosses zero from position to negative.

where  $u_{\text{ref}}^*$  is the new voltage reference,  $T$  is the PWM period.

The same delay strategy is applied to the case when  $u_{\text{ref}} = -E$ , and  $u_{\text{ref}}$  at  $t(2)$  should be modified as

$$u_{\text{ref}}^* = u_{\text{ref}} + \frac{t_d}{T} E. \quad (2)$$

2) *Zero Cross*: If  $u_{\text{ref}}$  crosses zero, switching action and signal sampling are also simultaneous as shown at  $t(3)$  in Fig. 4. Also a short delay of  $t_d$  should be inserted to prevent this.

There are two cases when  $u_{\text{ref}}$  crosses zeros from position to negative, as shown in Fig. 6. Before  $u_{\text{ref}}$  crosses zero, it could be  $u_{\text{ref}} \in (0, E)$  or  $u_{\text{ref}} = E$ . Fig. 6(a) shows the modified modulation method of the first case ( $u_{\text{ref}} \in (0, E)$ ), and  $u_{\text{ref}}$  at  $t(3)$  should be modified as

$$u_{\text{ref}}^* = u_{\text{ref}} - 2\frac{t_d}{T} E. \quad (3)$$

Fig. 6(b) shows the modified modulation method of the second case ( $u_{\text{ref}} = E$ ), and  $u_{\text{ref}}$  at  $t(3)$  should be modified as

$$u_{\text{ref}}^* = u_{\text{ref}} - 3\frac{t_d}{T} E. \quad (4)$$

The same delay strategy is applied when  $u_{\text{ref}}$  crosses zero from negative to positive. If  $u_{\text{ref}} \in (-E, 0)$  before crossing zero, after inserting  $t_d$ ,  $u_{\text{ref}}$  at  $t(3)$  should be modified as

$$u_{\text{ref}}^* = u_{\text{ref}} + 2\frac{t_d}{T} E. \quad (5)$$

If  $u_{\text{ref}} = -E$  before crossing zero,  $u_{\text{ref}}$  at  $t(3)$  should be modified as

$$u_{\text{ref}}^* = u_{\text{ref}} + 3\frac{t_d}{T} E. \quad (6)$$

3) *Phase Turning on*: When one phase is turned ON, the switching action is simultaneous with the sampling process, as shown in Fig. 7(a). To avoid the interference in both cases, a short delay of  $t_d$  at  $t(1)$  is inserted as shown in Fig. 7(a) and (b).  $u_{\text{ref}}$  at  $t(3)$  while turning ON should be modified as

$$u_{\text{ref}}^* = u_{\text{ref}} + \frac{t_d}{T} E. \quad (7)$$

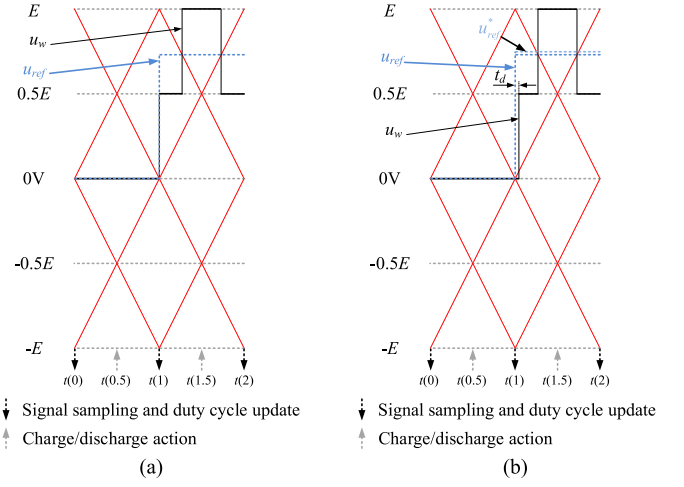


Fig. 7. Basic modulation method when one phase is turned ON (a) and the modified modulation method (b).

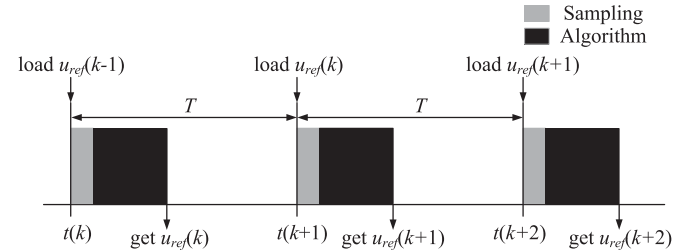


Fig. 8. Unit sampling time delay of the digital PWM generator.

## V. CONTROL SCHEME OF THE PROPOSED CONVERTER

To precisely control the phase current of SRM, a current controller is needed to generate the reference voltage for the modulator. Neglecting the magnetic mutual coupling between phases, the phase voltage equation of SRM can be obtained as

$$u = Ri + \frac{d\psi(\theta, i)}{dt} \quad (8)$$

where  $u$  is the phase voltage,  $R$  is the winding resistance,  $i$  is the phase current,  $\theta$  is the rotor position, and  $\psi$  is the flux linkage profile, which is a function of  $i$  and  $\theta$ .  $\psi(\theta, i)$  of the studied SRM of this paper is shown in Fig 10.

When the SRM is digitally controlled, (8) has to be digitalized as

$$u(k) = R \cdot i(k) + \frac{\psi(k+1) - \psi(k)}{T_s} \quad (9)$$

where  $T_s$  is the sampling period. When implemented in digital signal processor (DSP) or microcontroller unit (MCU), there is one sampling time delay of the digital PWM generator. As shown in Fig. 8, it takes time for the signal sampling and the control algorithm execution. At  $t(k)$ ,  $u_{\text{ref}}(k)$  cannot be obtained immediately and then feed into the PWM generator. It is  $u_{\text{ref}}(k-1)$  that is loaded into the PWM generator.  $u_{\text{ref}}(k)$  is obtained at the time later than  $t(k)$  and is loaded into the PWM generator at  $t(k+1)$ . This caused the unit sampling time delay

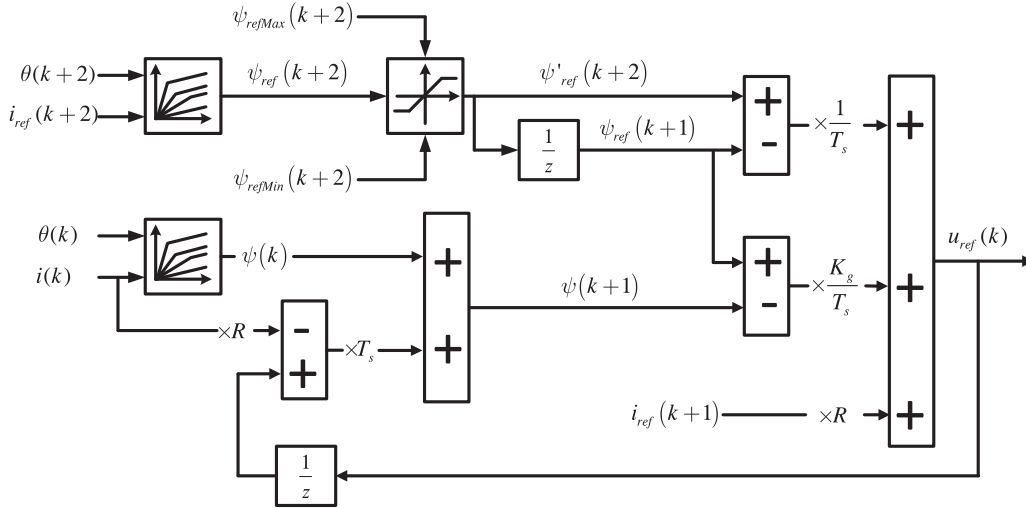


Fig. 9. Diagram of the current controller.

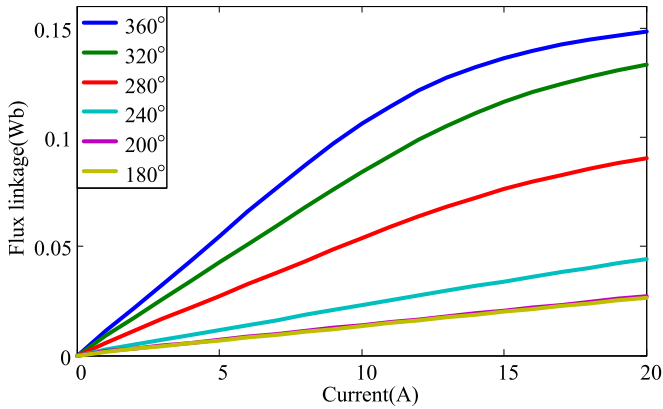


Fig. 10. Flux profile of the test SRM.

in the control loop. Considering this delay,  $\psi(k+2)$  instead of  $\psi(k+1)$  is controlled by adjusting  $u_{\text{ref}}(k)$ .

According to (9) and the unit sampling time delay of  $u_{\text{ref}}$  update. The flux linkage at  $t(k+1)$  is derived as

$$\psi(k+1) = [u_{\text{ref}}(k-1) - R \cdot i(k)] T_s + \psi(k) \quad (10)$$

where  $\psi(k)$  is the flux linkage at  $t(k)$  and is expressed as  $\psi(k) = \psi(\theta(k), i(k))$ . Since  $\theta(k)$  and  $i(k)$  are known at  $t(k)$ ,  $\psi(k)$  could be obtained.

Then, a current controller could be derived as (11) according to [16]

$$u_{\text{ref}}(k) = R \cdot i_{\text{ref}}(k+1) + \frac{\psi_{\text{ref}}(k+2) - \psi_{\text{ref}}(k+1)}{T_s} + K_g \frac{\psi_{\text{ref}}(k+1) - \psi(k+1)}{T_s} \quad (11)$$

where  $\psi_{\text{ref}}(k+1)$  and  $\psi_{\text{ref}}(k+2)$  are the reference flux linkage at  $t(k+1)$  and  $t(k+2)$ , respectively,  $K_g$  is the gain of the controller.  $\theta(k+2)$  and  $\theta(k+1)$  are needed to calculate the reference flux linkage and could be obtained by  $\theta(k+1) =$

$\theta(k) + \omega T_s$ ,  $\theta(k+2) = \theta(k+1) + \omega T_s$  respectively, where  $\omega$  is the angular speed.

Substituting (11) into (9), the error dynamic could be obtained

$$e(k+1) = e(k) - K_g e(k) - R e_i(k) T_s \quad (12)$$

where  $e(k) = \psi_{\text{ref}}(k) - \psi(k)$  is the flux control error  $e_i(k) = i_{\text{ref}}(k) - i(k)$  is the current control error. According to Fig. 10, for a certain position  $\theta$ ,  $\psi$  is a monotone increasing function of  $i$ , therefore  $e_i(k)$  can be expressed as  $e_i(k) = k_i \cdot e(k)$ , where  $k_i$  is a positive number. If a Lyapunov function is selected as

$$V(k) = e^2(k). \quad (13)$$

Then, the increment of the Lyapunov function is

$$\begin{aligned} \Delta V(k) &= V(k+1) - V(k) \\ &= -(K_g + k_i \cdot R \cdot T_s) (2 - K_g - k_i \cdot R \cdot T_s) e^2(k) \end{aligned} \quad (14)$$

which indicates that if  $0 < K_g + k_i \cdot R \cdot T_s < 2$ , then the system is stable with the current controller shown in (11).

In practice, the calculated  $u_{\text{ref}}(k)$  cannot exceed the dc bus voltage  $E$ . In order to prevent  $u_{\text{ref}}(k)$  from exceeding its physical limit, the flux reference limiter for the flux reference at  $t(k+2)$  is required. The flux reference limiter is derived as (16). By substituting  $E$  and  $-E$  into the  $u_{\text{ref}}(k)$  at (11), the upper limiter and lower limiter of the flux reference at  $t(k+2)$  are derived as

$$\begin{aligned} \psi_{\text{refMax}}(k+2) &= \psi_{\text{ref}}(k+1) \\ &+ \left[ E - K_g \frac{\psi_{\text{ref}}(k+1) - \psi(k+1)}{T_s} - R \cdot i(k+1) \right] T_s \\ \psi_{\text{refMin}}(k+2) &= \psi_{\text{ref}}(k+1) \\ &+ \left[ -E - K_g \frac{\psi_{\text{ref}}(k+1) - \psi(k+1)}{T_s} - R \cdot i(k+1) \right] T_s \end{aligned} \quad (15)$$

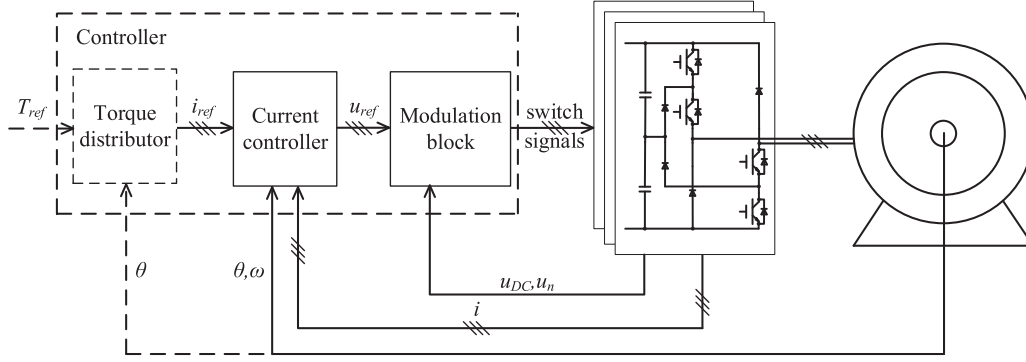


Fig. 11. Control diagram of the NPC three-level converter for SRM drives.

where  $\psi_{\text{refMax}}(k+2)$  and  $\psi_{\text{refMin}}(k+2)$  are the upper and lower limiter of the flux reference at  $t(k+2)$ , respectively. The behavior of the limiter can be described as

$$\begin{aligned} \psi'_{\text{ref}}(k+2) &= \psi_{\text{refMax}}(k+2), u_{\text{ref}}(k) > E \\ \psi'_{\text{ref}}(k+2) &= \psi_{\text{ref}}(k+2), u_{\text{ref}}(k) \in [-E, E] \\ \psi'_{\text{ref}}(k+2) &= \psi_{\text{refMin}}(k+2), u_{\text{ref}}(k) < -E \end{aligned} \quad (16)$$

where  $\psi'_{\text{ref}}(k+2)$  is the adjusted reference flux linkage of  $\psi_{\text{ref}}(k+2)$ .

The entire current control algorithm is described in Fig. 9.

## VI. SIMULATION RESULTS

The proposed converter is simulated in MATLAB/SIMULINK to verify both its effectiveness and power losses. The control diagram of the proposed converter for SRM drives is shown in Fig. 11.

In this simulation, flat top current control for SRM is applied with the proposed current control algorithm and the PWM method. The current reference is 10 A. The torque distributor is not used in the simulation.  $u_{\text{DC}}$  and  $u_n$  are the dc-link voltage and the neutral point potential, respectively. A 12/8, 2 kW, 6000 r/min three-phase SRM is modeled and tested in the simulation. Its flux profile is shown in Fig. 10. The dc-link voltage  $E$  is 300 V. For comparison, the two-level asymmetric half-bridge converter with soft-chopping PWM control is also simulated. The current controller is the same as that of the three-level converter.

Three cases are studied in this simulation. First, the two-level converter and the proposed three-level converter are simulated with the switching frequency of 10 kHz. After that the switching frequency of the proposed three-level converter is increased to 20 kHz.

### A. Current Ripple

The phase current and voltage waveforms obtained by the conventional two-level converter with switching frequency of 10 kHz at 1000, 2000, 4000, and 6000 r/min are shown in Fig. 12. Fig. 13 shows the phase current and voltage waveforms of the three-level converter with switching frequency of 10 kHz. Fig. 14 shows phase current and voltage waveforms of the three-level converter with switching frequency of 20 kHz.

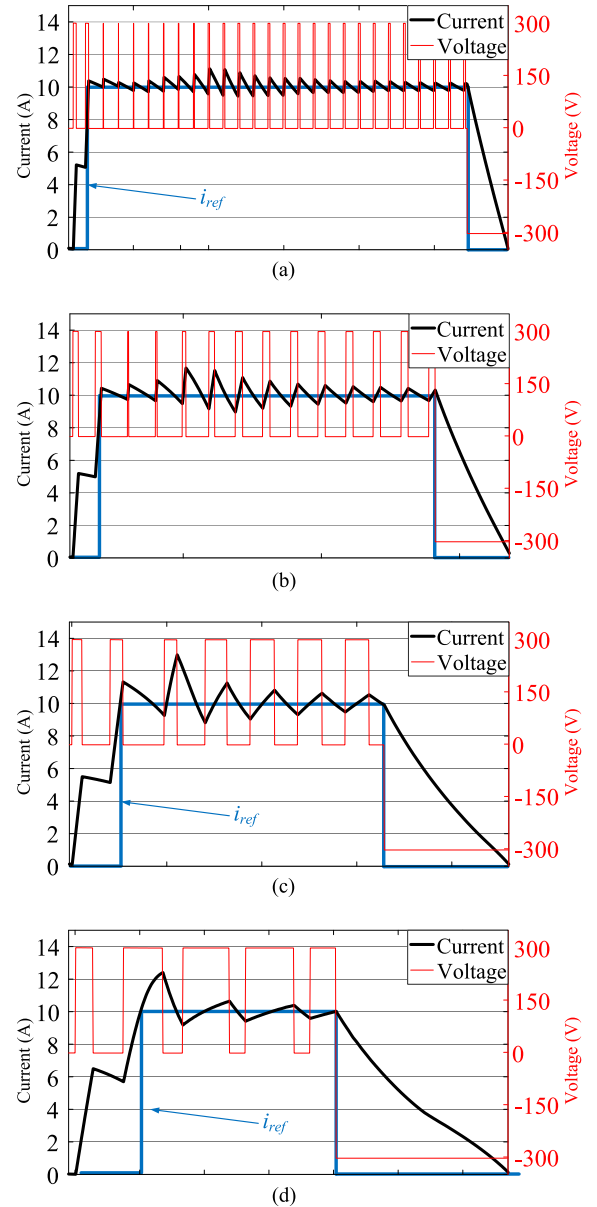


Fig. 12. Phase current (black), voltage (red), current reference (blue) of SRM driven by the two-level converter with 10-kHz switching frequency. (a) Voltage, current, and current reference at 1000 r/min. (b) Voltage, current, and current reference at 2000 r/min. (c) Voltage, current, and current reference at 4000 r/min. (d) Voltage, current, and current reference at 6000 r/min.

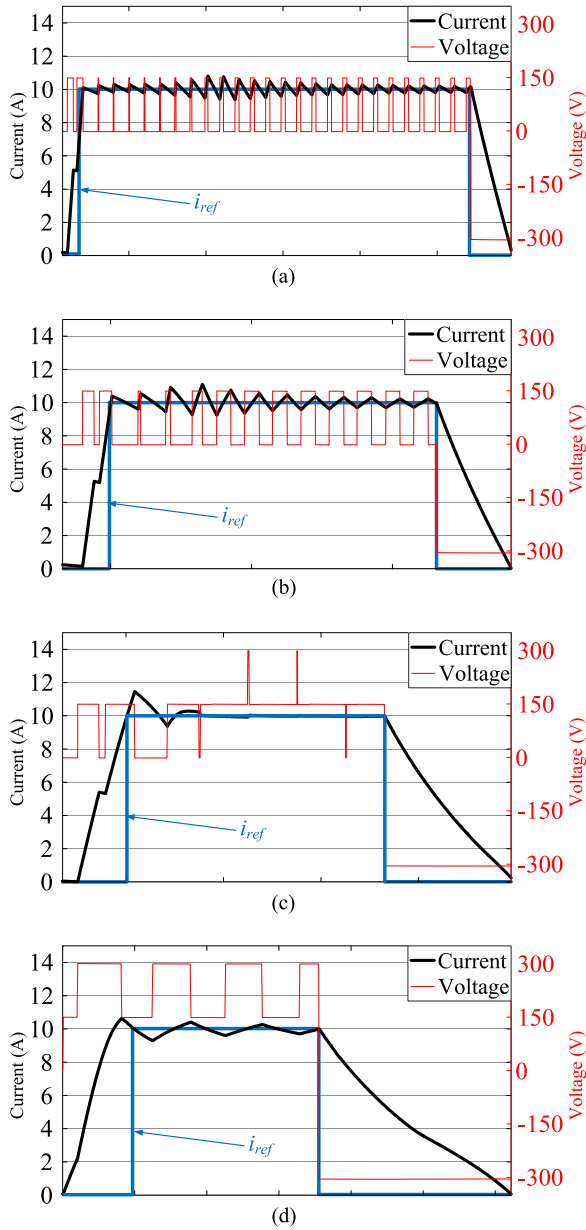


Fig. 13. Phase current (black), voltage (red), current reference (blue) of SRM driven by the proposed three-level NPC converter with 10-kHz switching frequency. (a) Voltage, current, and current reference at 1000 r/min. (b) Voltage, current, and current reference at 2000 r/min. (c) Voltage, current, and current reference at 4000 r/min. (d) Voltage, current, and current reference at 6000 r/min.

It is shown that, compared to the two-level converter, the peak-to-peak values of the current ripple of the proposed three-level converter are reduced. Fig. 15 shows the normalized current ripples of the three cases at different speeds. It is shown that the current ripples of the three-level converter with switching frequency of 20 kHz are reduced by more than half compared to the two-level converter.

### B. Power Losses

To compare the power losses of the proposed converter with the two-level converter, power devices for these converters are

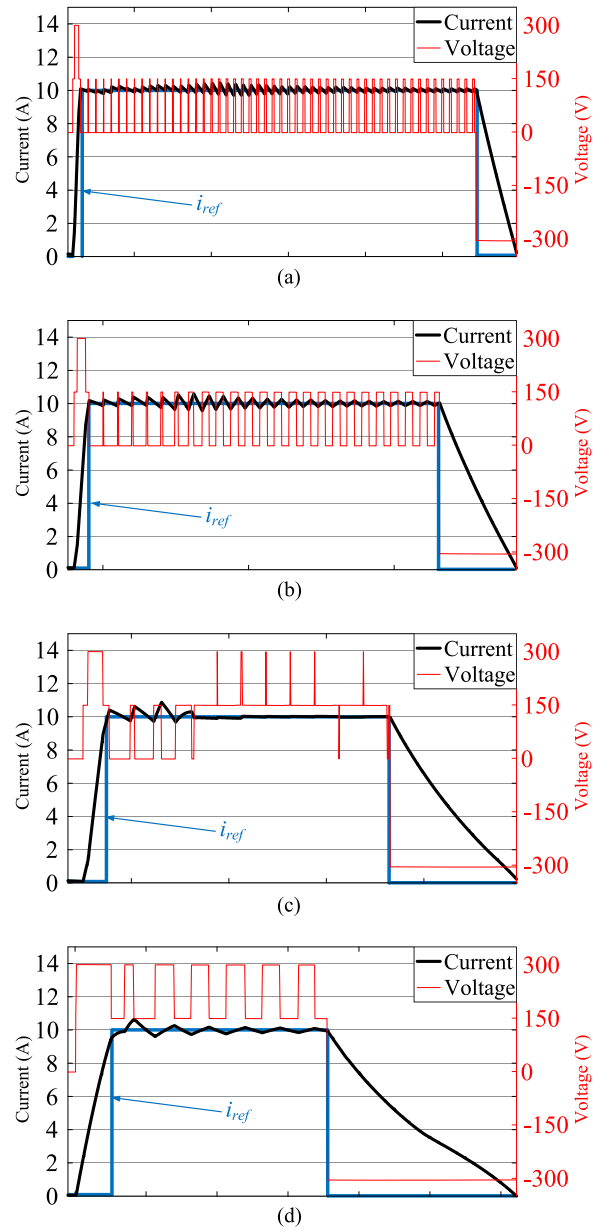


Fig. 14. Phase current (black), voltage (red), current reference (blue) of SRM driven by the proposed three-level NPC converter with 20-kHz switching frequency. (a) Voltage, current, and current reference at 1000 r/min. (b) Voltage, current, and current reference at 2000 r/min. (c) Voltage, current, and current reference at 4000 r/min. (d) Voltage, current, and current reference at 6000 r/min.

selected first. MOSFETs are selected as the switching device. The main parameters of the selected MOSFETs and diodes are obtained from their datasheets and are listed in Tables IV and V.

It can be seen that as the decreasing of the voltage rating, the  $R_{DS(on)}$  of the MOSFETs and  $V_F$  of the diodes both decrease. Although more devices are needed in the proposed NPC three-level converter, the total conduction losses will not increase. Since the switching speed of MOSFETs with lower voltage rating is much faster than that of higher voltage rating MOSFETs, the switching losses can be reduced. Moreover, as Q3X and Q4X only need to block half of the dc-link voltage, Schottky diodes with very low reverse recovery loss are available. Therefore, the

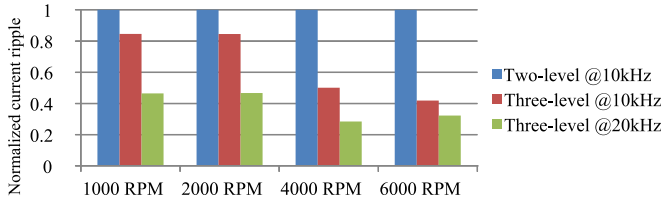


Fig. 15. Current ripple comparison of the three simulated cases.

 TABLE IV  
 MAIN PARAMETERS OF MOSFETS

	Two-level converter IPW60R041C6 at 10 A	Three-level converter IPP200N25N3 at 10 A
$V_{DS}$	650 V	250 V
$I_D$ at 100 °C	49 A	46 A
$R_{DS(on)}$	0.037 $\Omega$	0.017 $\Omega$
$V_{GS(th)}$	3 V	3 V
$Q_{sw}$	160 nC	13 nC
$V_{plateau}$	5.4 V	4.2 V

 TABLE V  
 MAIN PARAMETERS OF DIODES

	Two-level converter	Three-level converter	
	STTH50W06S at 10 A	MBR40250 at 10 A	BYC20X-600P at 10 A
$V_F$	1.7 V	0.75 V	2.3 V
$t_{rr}$	34 ns	35 ns	35 ns
$Q_{rr}$	850 nC	0	220 nC

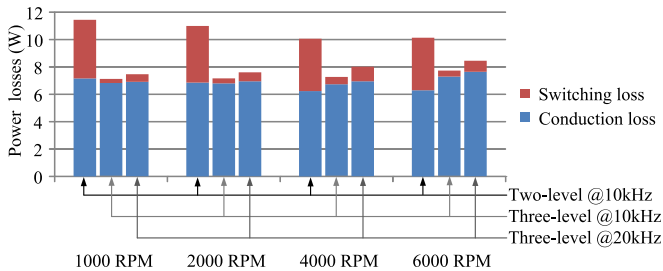


Fig. 16. Power losses comparison of the three simulated cases in one phase.

power losses of the proposed converter can be lower than that of the two-level converter.

Based on the parameters shown in Tables IV and V, the conduction and switching losses of the two-level and the three-level converters are estimated. Gate resistors are selected to keep the  $dv/dt$  below 4 kV/ $\mu$ s for the safe operation. The  $di/dt$  is also limited under 300 A/ $\mu$ s by the gate resistors. The loss estimation method is taken from [17]. The energy dissipation caused by reverse recovery of diodes per switching action is estimated by  $W_{RR} = Q_{RR} \times V_{IN}$ , where  $V_{IN}$  is the voltage across the diode before switching actions.

In the simulations, for similarity, the current and voltage waveforms of the MOSFETs and diodes in phase A are recorded and analyzed. The results of other phases are the same. Fig. 16 shows the calculated power losses of phase A, including the

 TABLE VI  
 COMPREHENSIVE COMPARISON OF TWO-LEVEL AND PROPOSED THREE-LEVEL CONVERTERS

Items	Two-level converter	Three-level converter
Switching frequency	low	high
Current ripple	high	low
Switching loss	high	low
Acoustic noise	high	low
Cost on switches	similar	similar
Cost on diodes	similar	similar
Cost on dc capacitors	similar	similar
Cost on EMI filter	high	low
Cost on gate drivers	low	high
DC voltage sensors	1	2
Control complexity	low	high

conduction loss and switching loss of the three cases at different speeds. It is shown that the conduction loss of the two-level converter and the proposed three-level converter are similar. However, the switching loss of the three-level converter is significantly reduced. In spite of minor increase in switching loss at the switching frequency of 20 kHz, the total losses are still significantly reduced compared to the two-level converter. Moreover, since there are only few sampling steps at each electric period when rotor speed is high, increased switching and sampling frequency will help increase control accuracy.

Therefore, the proposed three-level converter is capable to operate at higher switching frequency than the conventional two-level converter, which will lead to much better current waveform, lower acoustic noise, lower iron losses, and lower ac copper losses.

### C. Comprehensive Comparison

Based on the analysis and results above, a comprehensive comparison of the proposed three-level converter and the conventional two-level converter is summarized in Table VI. It is shown that with increased control complexity, the three-level converter is able to reduce current ripple and switching loss even though it works at high switching frequency. The cost of switches, diodes, and dc-link capacitors will not increase. The cost of EMI filters will be reduced because of smaller voltage pulses. Although an additional voltage sensor and more gate drivers are required, the cost of them are relatively low compared to that of the switches, diodes, and dc capacitors in high power high performance drive systems.

## VII. EXPERIMENTAL RESULTS

Experiments are conducted to verify the effectiveness of the proposed three-level converter. Fig. 17 shows the diagram of the experimental setup. The proposed three-level converter is controlled by a control board with DSP and field programmable gate array (FPGA). The modulation method is programmed in FPGA while the current control algorithm runs in DSP. The shaft of the SRM is connected to a brushless dc (BLDC) machine. The BLDC is connected to a diode rectifier. The output of the rectifier is connected to a dc/dc converter. The dc/dc con-

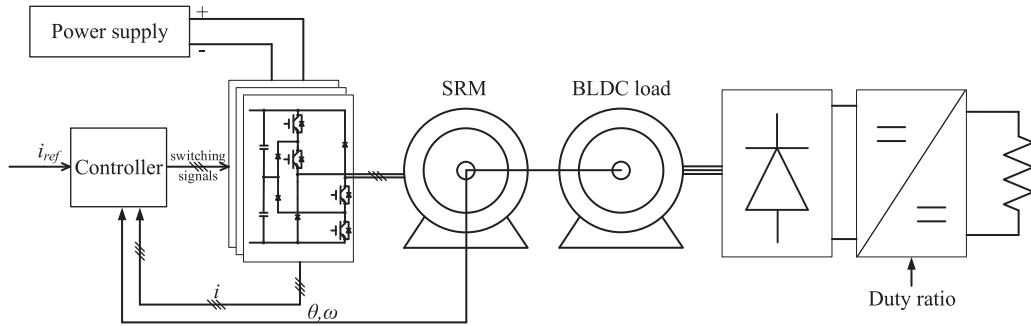
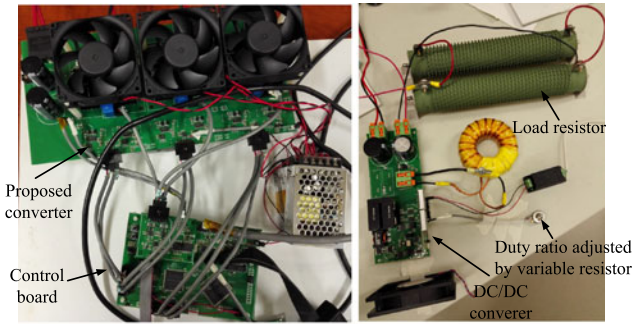
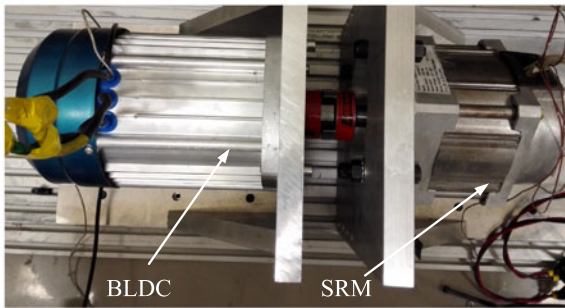


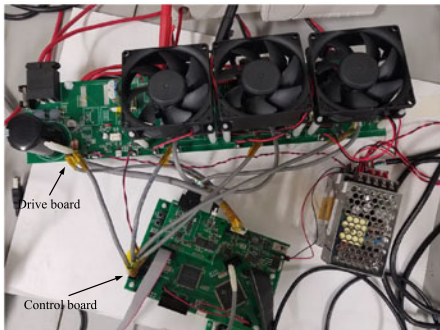
Fig. 17. Experimental diagram of the NPC three-level converter for SRM drives.



(a)



(b)



(c)

Fig. 18. Experimental setup. (a) The proposed three-level converter, the control board, DC/DC converter and the load resistor. (b) The tested SRM and the load BLDC. (c) The tested two-level converter.

verter is connected to a load resistor. By tuning the duty ratio of the dc/dc converter, the load torque of the SRM could be adjusted. Fig. 18(a) shows the proposed three-level asymmetric half-bridge converter for SRM, the control board, the dc/dc con-

TABLE VII  
PARAMETERS OF THE EXPERIMENTAL PLANT

Symbol	Parameter	value
$R_w$	SRM winding resistance	0.3 $\Omega$
$f_s$	Switching frequency	20 kHz
$T_s$	Sampling period	0.00005 s
$U_{DC}$	DC bus voltage	300 V
$K_g$	Control gain	0.2

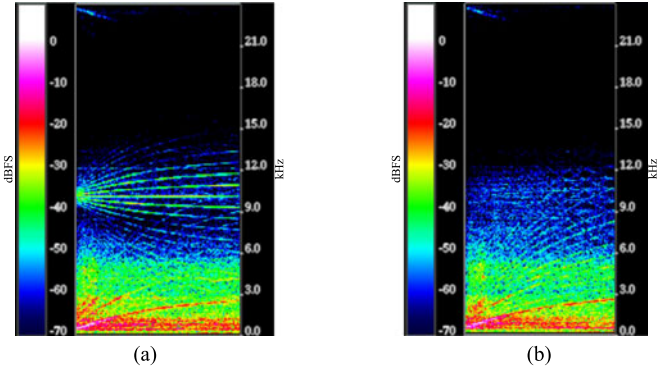


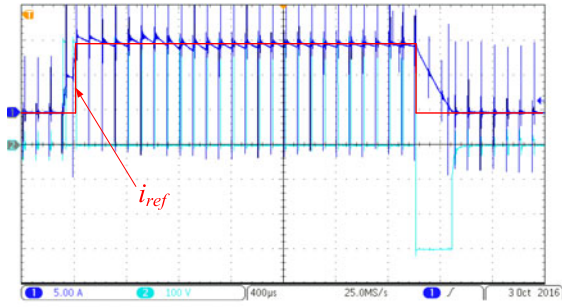
Fig. 19. Acoustic noise compare between the three-level (a) and the two-level (b) converters. (a) Acoustic noise of two-level converter. (b) Acoustic noise of three-level converter.

verter, and the load resistor. Fig. 18(b) shows the studied SRM and the BLDC load. For comparison, a two-level converter with PWM control is also tested. Fig. 18(c) shows the test two-level converter.

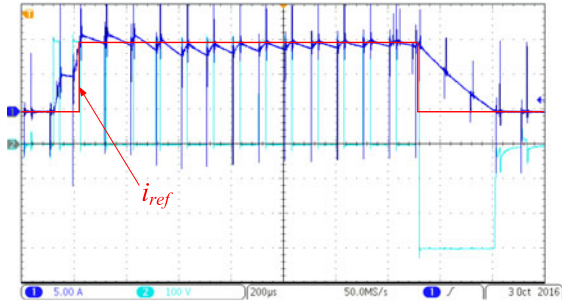
The flux linkage profile of the studied SRM is shown in Fig. 10. Parameters of the controller for this experiment is shown in Table VII.

First, flat-top current control is applied. A reference current of 10 A is given to the current controller. The SRM is controlled to run at 1000, 2000, 4000, and 6000 r/min, respectively. The turn on angle is  $192^\circ$  and the turn-OFF angle is  $320^\circ$ .

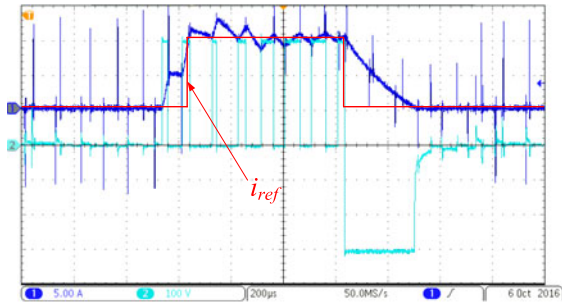
Figs. 20 and 21 show the current and voltage waveforms as well as the current reference of the two-level converter and three-level converter, respectively. It is shown that the current ripple of the three-level converter is significantly reduced compared to the two-level converter, when voltage demand of the three-level converter is low, the phase winding voltage switches



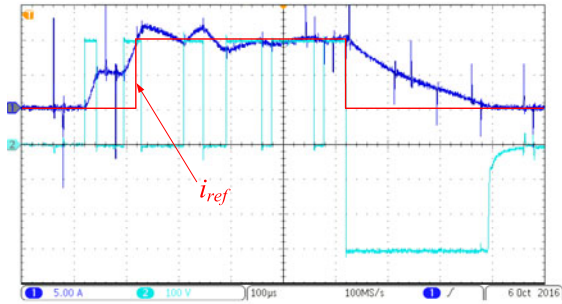
(a)



(b)



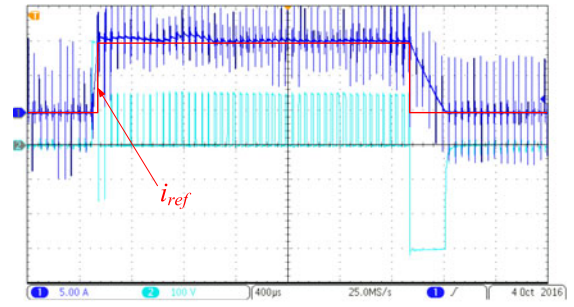
(c)



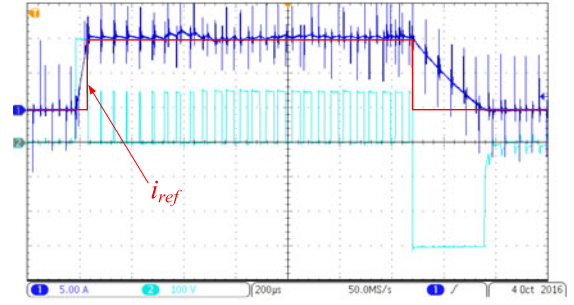
(d)

Fig. 20. Experimental Phase current (CH1), voltage (CH2), current reference (red line) of the SRM driven by the two-level converter with 10-kHz switching frequency. (a) Voltage, current, and current reference at 1000 r/min. (b) Voltage, current, and current reference at 2000 r/min. (c) Voltage, current, and current reference at 4000 r/min. (d) Voltage, current, and current reference at 6000 r/min.

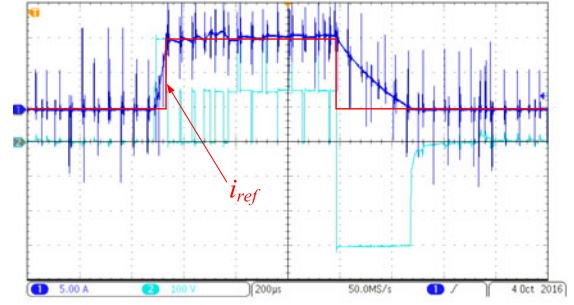
between 0 and  $0.5E$  instead of  $E$ , which significantly reduces the current ripple. When the phase is turned OFF,  $-E$  is applied on the winding and therefore the phase winding is demagnetized fast. The amplitude of voltage pulses are almost the same, which indicates that the neutral point is well balanced.



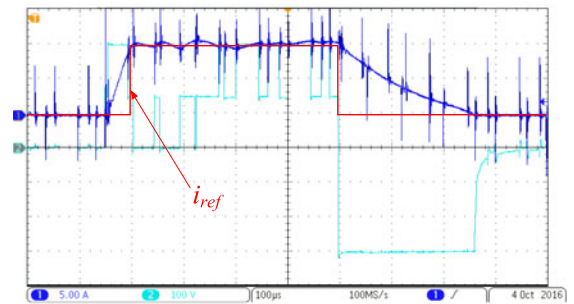
(a)



(b)



(c)



(d)

Fig. 21. Experimental phase current (CH1), voltage (CH2), current reference (red line) of the SRM driven by the proposed three-level NPC converter with 20-kHz switching frequency. (a) Voltage, current, and current reference at 1000 r/min. (b) Voltage, current, and current reference at 2000 r/min. (c) Voltage, current, and current reference at 4000 r/min. (d) Voltage, current, and current reference at 6000 r/min.

The experimental comparison results validate the simulation results.

The shaft of the SRM is disconnected with the load to isolate the noise of the load machine. The rotor speed is accelerated from 0 to 6000 r/min. Since the inertia of the rotor is low, a

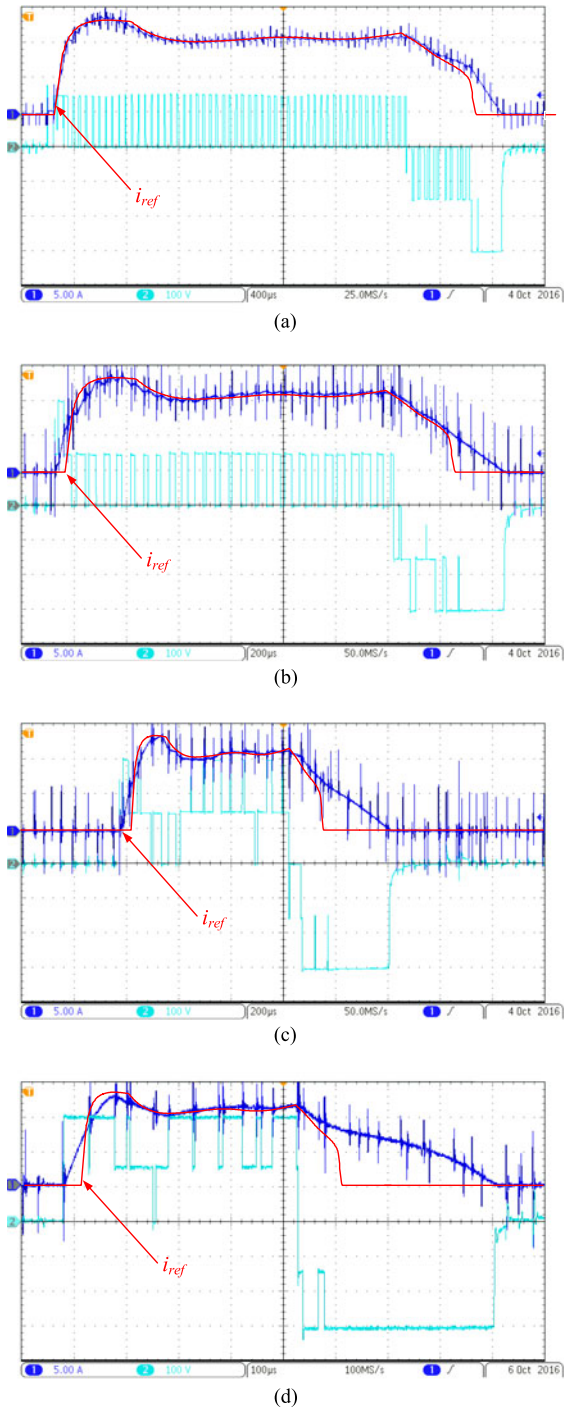


Fig. 22. Experimental phase current (CH1), voltage (CH2), current reference (red line) of the SRM driven by the proposed three-level NPC converter with torque sharing control and  $2.0 \text{ N} \cdot \text{m}$  torque output. (a) Voltage, current, and current reference at 1000 r/min. (b) Voltage, current, and current reference at 2000 r/min. (c) Voltage, current, and current reference at 4000 r/min. (d) Voltage, current, and current reference at 6000 r/min.

ramp-up current reference instead of the constant current reference is applied to lengthen the accelerating period. Acoustic noise is measured 1 m away from the SRM under test. Since the microphone is not calibrated, the noise is measured in the dBFS manner.

The measured noise driven by the two-level converter and the proposed three-level converter are shown in Fig. 19(a) and (b), respectively. It is shown that the mechanical noises at low frequency are very similar. The noise around the switching frequency of the two-level converter is higher. Since the phase current of SRM is discontinuous, the frequencies of noise are not fixed at 10 kHz but varies with speed. With the proposed three-level converter, the noises around the switching frequency are significantly reduced.

Finally, the converter is tested under the torque sharing control [18]–[20]. A reference torque of  $2.0 \text{ N} \cdot \text{m}$  is given to a linear torque distributor and Fig. 22 shows the current and voltage waveforms at 1000, 2000, 4000, and 6000 r/min, respectively.

It is shown that the current ripple with the proposed converter is still small. Even though  $i_{\text{ref}}$  is very nonlinear, the proposed converter with PWM current controller is effective at tracking  $i_{\text{ref}}$  at different speeds.

In the experiments, there is some difference between  $i_{\text{ref}}$  and the real current. This may be caused by the model mismatch. A better current controller is able to solve this problem [21].

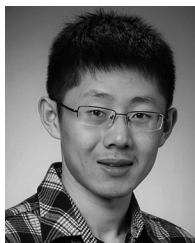
## VIII. CONCLUSION

In this paper, a NPC three-level converter for SRM drives is proposed. The PWM modulation method, the dc voltage balancing algorithm, and the current control method are presented. The proposed converter is compared with the conventional two-level converter in terms of cost, current ripple, noise, and power losses. It indicates that the costs of these two converters are similar but the current ripple, noise, and losses of the proposed converter is greatly reduced. The simulation and experimental results show that the proposed three-level converter is very promising in the low-voltage and high-power SRM drives.

## REFERENCES

- [1] A. Emadi, *Energy-Efficient Electric Motors: Selection and Applications*. New York, NY, USA: Marcel Dekker, Sep. 2004.
- [2] "Switched Reluctance Motor Drives," in *Electric Vehicle Machines and Drives*. Singapore: Wiley, May 2015, pp. 108–146.
- [3] K. M. Rahman, B. Fahimi, G. Suresh, A. V. Rajarathnam, and M. Ehsani, "Advantages of switched reluctance motor applications to EV and HEV: Design and control issues," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 111–121, Jan. 2000.
- [4] T. Lipo, "Improvements in EMC performance of inverter-fed motor drives," *IEEE Trans. Ind. Appl.*, vol. 31, no. 6, pp. 1247–1256, 1995.
- [5] N. Aoki, K. Satoh, and A. Nabae, "Damping circuit to suppress motor terminal overvoltage and ringing in PWM inverter-fed AC motor drive systems with long motor leads," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1014–1020, Sep. 1999.
- [6] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan. 1999.
- [7] J. Rodriguez, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [8] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 855–865, May 2005.
- [9] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [10] B. Welchko, M. Beltrao de Rossiter Correia, and T. Lipo, "A three-level MOSFET inverter for low-power drives," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 669–674, Jun. 2004.

- [11] K. Tomczewski and K. Wrobel, "Quasi-three-level converter for switched reluctance motor drives reducing current rising and falling times," *Power Electron., IET*, vol. 5, no. 7, pp. 1049–1057, Aug. 2012.
- [12] D.-H. Lee, H. Wang, and J.-W. Ahn, "An advanced multi-level converter for four-phase SRM drive," in *Proc. 2008 IEEE Power Electron. Spec. Conf.* Jun. 2008, pp. 2050–2056.
- [13] S. Watkins, "Multilevel asymmetric power converters for switched reluctance machines," in *Proc. Int. Conf. Power Electron. Mach. Drives*, vol. 2002, Jun. 2002, pp. 195–200.
- [14] D. Patil, S. Wang, and L. Gu, "Multilevel converter topologies for high-power high-speed switched reluctance motor: Performance comparison," in *Proc. 2016 IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2016, pp. 2889–2896.
- [15] K. Ha, C. Lee, J. Kim, R. Krishnan, and S.-G. Oh, "Design and development of low-cost and high-efficiency variable-speed drive system with switched reluctance motor," *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 703–713, May 2007.
- [16] Y.-R. Mohamed and E. El-Saadany, "Robust high bandwidth discrete-time predictive current control with predictive internal model: A unified approach for voltage-source PWM converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 126–136, Jan. 2008.
- [17] J. Depew, "AN1471—Efficiency analysis of a synchronous buck converter using microsoft office Excel-based loss calculator," pp. 1–14, 2012.
- [18] D. H. Lee, J. Liang, Z. G. Lee, and J. W. Ahn, "A simple nonlinear logical torque sharing function for low-torque ripple SR drive," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3021–3028, Aug. 2009.
- [19] X. D. Xue, K. W. E. Cheng, and S. L. Ho, "Optimization and evaluation of Torque-Sharing functions for torque ripple minimization in switched reluctance motor drives," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2076–2090, Sep. 2009.
- [20] J. Ye, B. Bilgin, and A. Emadi, "An offline torque sharing function for torque ripple reduction in switched reluctance motor drives," *IEEE Trans. Energy Convers.*, vol. 30, no. 2, pp. 726–735, Jun. 2015.
- [21] F. Peng, J. Ye, and A. Emadi, "A digital PWM current controller for switched reluctance motor drives," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7087–7098, Dec. 2015.



**Fei Peng** (S'15–M'16) received the B.S. and M.S. degrees in electrical engineering from Southeast University, Nanjing, China, in 2010 and 2012, respectively. He received the Ph.D. degree from McMaster University, Hamilton, ON, Canada, in 2016.

After receiving the Ph.D. degree, he worked as a Postdoctoral Fellow at the McMaster Institute for Automotive Research and Technology (MacAUTO), McMaster University. In December 2016, he joined the School of Electrical Engineering, Southeast University, as an Assistant Professor. His research inter-

ests include optimal design and control of power converters, modeling, and digital control of motor drives.



**Jin Ye** (S'13–M'14–SM'16) received the B.S. and M.S. degrees in electrical engineering from Xian Jiaotong University, Xian, China, in 2008 and 2011, respectively. She received the Ph.D. degree in electrical engineering from McMaster University, Hamilton, ON, Canada, in 2014. After Ph.D. degree, she worked as a Postdoctoral Research Associate at the McMaster Institute for Automotive Research and Technology, McMaster University, Hamilton.

She is currently an Assistant Professor of electrical engineering at San Francisco State University.

Her main research areas include power electronics, electric motor drives, renewable energy conversion and electrified transportation.



**Ali Emadi** (S'98–M'00–SM'03–F'13) received the B.S. and M.S. degrees in electrical engineering with highest distinction from Sharif University of Technology, Tehran, Iran, in 1995 and 1997, respectively, and the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2000.

He is the Canada Excellence Research Chair in Hybrid Powertrain at McMaster University in Hamilton, ON, Canada. Before joining McMaster University, he was the Harris Perlstein Endowed

Chair Professor of Engineering and the Director of the Electric Power and Power Electronics Center and Grainger Laboratories at Illinois Institute of Technology (IIT) in Chicago, IL, USA, where he established research and teaching facilities as well as courses in power electronics, motor drives, and vehicular power systems. He was the Founder, Chairman, and the President of Hybrid Electric Vehicle Technologies, Inc.—A university spin-off company of IIT.

Dr. Emadi received numerous awards and recognitions. He was the Advisor for the Formula Hybrid Teams at IIT and McMaster University, which received the GM Best Engineered Hybrid System Award at the 2010, 2013, and 2015 competitions. He is the principal author/coauthor of more than 350 journal and conference papers as well as several books including *Vehicular Electric Power Systems* (2003), *Energy Efficient Electric Motors* (2004), *Uninterruptible Power Supplies and Active Filters* (2004), *Modern Electric, Hybrid Electric, and Fuel Cell Vehicles* (2nd ed., 2009), and *Integrated Power Electronic Converters and Digital Control* (2009). He is also the editor of the *Handbook of Automotive Power Electronics and Motor Drives* (2005) and *Advanced Electric Drive Vehicles* (2014). He was the Inaugural General Chair of the 2012 IEEE Transportation Electrification Conference and Expo and has chaired several IEEE and SAE conferences in the areas of vehicle power and propulsion. He is the founding Editor-in-Chief of the IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION.