Active Suppression of Selected DC Bus Harmonics for Dual Active Bridge DC–DC Converters

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***Abstract*—AC coupled dual active bridge (DAB) dc–dc converters typically use phase shifted square wave (PSSW) modulation to manage the power flow between two dc sources. With this scheme, the current flowing between the converter bridges injects high-magnitude current harmonics into each dc port at multiples of the primary switching frequency, which can excite resonances in the LC circuits created by parasitic second-order impedances such as wiring inductances in the dc-link connections. This can cause substantial dc bus voltage and current oscillations, particularly with the higher switching frequencies that are used with wide bandgap devices, leading to excessive electromagnetic interference, significant filter stress, and eventual component operational failure. Conventionally, a relatively large dc bus filter capacitor (or inductor) helps to suppress these dc bus harmonic dynamics. However, the use of adaptive three-level modulation for a single phase DAB provides a much greater solution space to achieve a desired power transfer condition, with the three PSSW control angles that are available. This paper now explores the additional use of these angles to selectively suppress particular dc bus current harmonics across the entire operating range of the converter and thus allow the size of the DAB dc bus bridge capacitors to be minimized. This new active harmonic suppression (AHS) strategy is validated by theory, simulation, and matching experimental results.**

***Index Terms*—DC–DC power conversion, frequency domain analysis, harmonic analysis, HF transformers, modulation.**

I. Introduction

THE dual active bridge (DAB) dc–dc converter [2] is a very promising topology for bidirectional dc–dc applications with its inherent zero voltage switching (ZVS) soft switching capability that allows for high-efficiency operation [3]. To date, most research investigations into this topology have concentrated on design and operating techniques for the ac-link. In particular this includes the progression from conventional two-level to adaptive three-level phase shifted square wave (PSSW) modulation [4]–[10] and optimization of the magnetic components [11]–[14] to achieve wide range ZVS soft switching operation and reduce the circulating currents. However, unlike conventional dc–ac inverters [15] that use a high switching frequency to generate a low fundamental frequency output waveform, the PSSW modulation strategy of a DAB generates substantial harmonics at integer multiples of the (typically) high fundamental switching frequency. These harmonics reflect back into the dc buses on either side of the DAB, and must be absorbed by both the dc bus capacitors and any associated external elements such as a source battery. The capacitors form high Q resonant circuits with the parasitic inductances of the various conductors that connect between the DAB components, which can be excited by the high frequency current harmonics created by the PSSW modulation process under particular practical design conditions. The outcome can be substantial voltage and/or current oscillations on the dc buses, particularly when higher switching frequency, wider band-gap devices such as silicon-carbide or gallium-nitride devices are used. Conventionally, the relatively large dc bus filter capacitor (or inductor) that is normally used in a DAB helps to suppress these oscillations by creating a reasonably low filter cutoff frequency. However, this is not necessarily adequate or effective for many design applications. To date, a comprehensive analysis of the hazard, the characteristic dc bus harmonics that create the problem, and design and operational strategies for the DAB and its filter components to overcome potential difficulties, is yet to be found in the literature.

This paper now presents an active harmonic suppression (AHS) technique to address this resonance hazard for single-phase DAB converters. After identifying the practical issues in the dc bus filter design that can lead to harmonic problems, the work analytically derives the magnitude and frequency of the dc bus harmonic current components for any dc–dc bus voltage ratio and power transfer conditions using harmonic decomposition of the bridge output voltages. The analysis is then used to identify how adaptive three-level modulation can be used to actively shape the dc bus current to selectively suppress the particular harmonic components that can cause critical frequency resonance dc bus oscillations at either converter dc output. This allows the filter capacitor size to be set to the minimum value required to support the bridge switching transitions, with low-order modulation harmonics absorbed by the terminating impedance (e.g., a battery or an external bulk capacitive element) without creating a resonance hazard. The proposed design and control strategy has been verified using examples where the parasitic dc bus impedances and the minimized filter capacitor are characterized to highlight a dc bus

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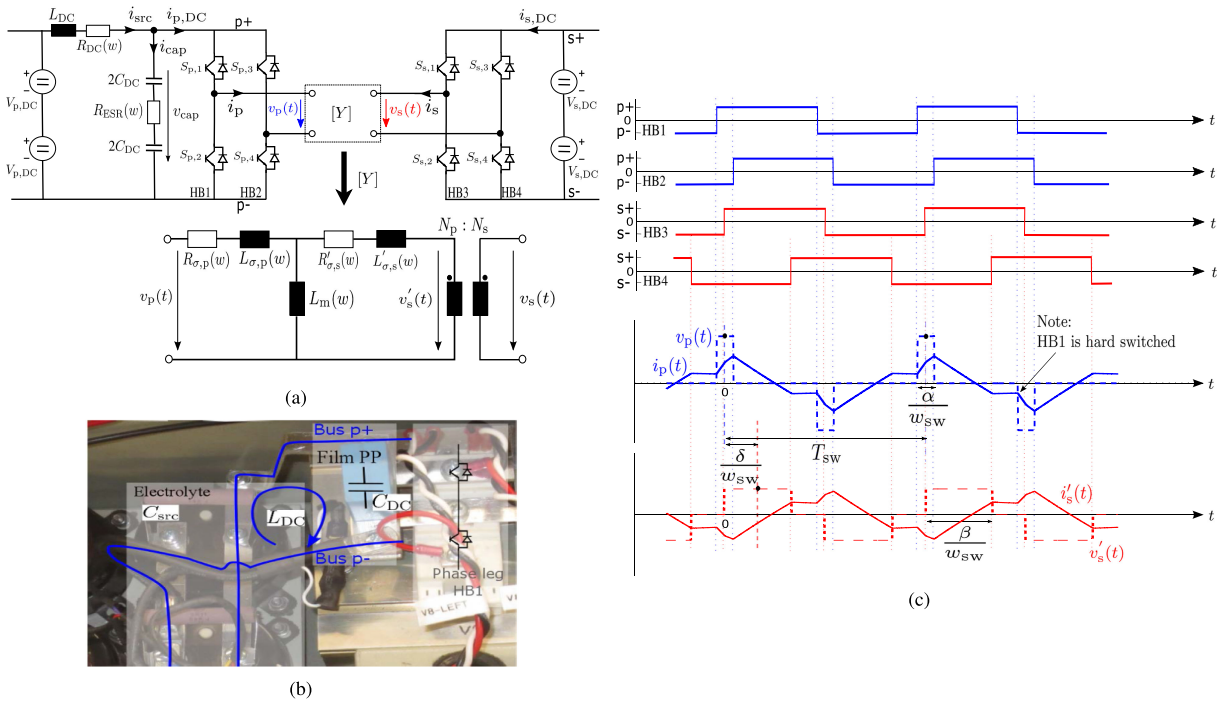

Fig. 1. Single-phase DAB including lumped parasitic dc bus impedance. (a) Topology and HF transformer impedance. (b) Experimental dc bus filter arrangement. (c) Phase leg switched voltages and bridge output currents.

resonance oscillation, which is then eliminated using AHS. Simulation and experimental waveforms are presented to confirm this analysis.

II. Interaction Between the DC Bus Bridge Filter Capacitor and the Parasitic Resonant Circuit

Fig. 1(a) shows the topology of a single-phase DAB, where the two bridges are linked by a generic admittance matrix $[Y]$. The typical dc bus arrangement for this topology has high-frequency dc bus capacitor/s with a finite capacitance $C_{\rm DC}$ and ESR resistance $R_{\rm ESR}$ that are located in close proximity to the bridge semiconductor devices, e.g., ceramic capacitors or film polypropylene (PP) capacitors, to buffer the energy required to support the switching transitions and minimize the parasitic commutation inductance (neglected in the context of this paper). A certain distance away, the primary energy source, e.g., electrolyte bulk capacitors or a storage battery, connects to the inner dc bus via a (short) conductor and/or an external discrete choke. This creates a parasitic impedance $L_{\rm DC}/R_{\rm DC}$ that forms a resonant circuit with the inner dc bus capacitance $C_{\rm DC}$, as shown in Fig. 1(a).

Fig. 1(b) shows a typical physical arrangement for such a bridge, where the parasitic inductance $L_{\rm DC}$ created by the wiring connection from the bulk dc electrolytic capacitors (2x Kendeil KO1450222, paralleled) via the dc bus capacitor (1x Kemet 463R4100) to the dc tabs of the phase leg module can be clearly seen.

Fig. 1(c) shows the three-level PSSW strategy that is used to modulate the DAB, where each phase leg is switched with a square wave, the primary and secondary bridge phase leg square waves are displaced by α and β, respectively, to produce reduced magnitude bridge output voltages, and the two bridge output voltages are displaced by δ to control the power flow (δ: load angle).

From Fig. 1(a), it can be seen that the dc bus current harmonics will share between the high frequency bus capacitor branch $R_{\rm ESR}/C_{\rm DC}$ and the parasitic inductance connection $R_{\rm DC}/L_{\rm DC}$ to the external source, according to Kirchoff's current law. Hence, the harmonic currents that flow into the external source from dc bus harmonics injected into the dc bus by the phase leg, are given by (for an ideal external voltage source with $C_{\rm src} \to \infty$)

$$I^k_{\rm src}\angle\theta^k_{\rm src} = G^k_{\rm tf,src}\angle\theta^k_{\rm tf,src}\cdot I^k_{\rm p,DC}\angle\theta^k_{\rm p,DC}$$

where

$$G^k_{\rm tf,src}\angle\theta^k_{\rm tf,src} = \frac{1+jkw_{\rm sw}R^k_{\rm ESR}C_{\rm DC}}{1-(kw_{\rm sw})^2L_{\rm DC}C_{\rm DC}+jkw_{\rm sw}C_{\rm DC}(R^k_{\rm DC}+R^k_{\rm ESR})}. \quad (1)$$

The high-frequency bus capacitor current harmonics can similarly be determined as

$$I^k_{\rm cap}\angle\theta^k_{\rm cap} = G^k_{\rm tf,cap}\angle\theta^k_{\rm tf,cap}\cdot I^k_{\rm p,dc}\angle\theta^k_{\rm p,dc}$$

where

$$G^k_{\rm tf,cap}\angle\theta^k_{\rm tf,cap} = \frac{-(kw_{\rm sw})^2L_{\rm DC}C_{\rm DC}+jkw_{\rm sw}R^k_{\rm DC}C_{\rm DC}}{1-(kw_{\rm sw})^2L_{\rm DC}C_{\rm DC}+jkw_{\rm sw}C_{\rm DC}(R^k_{\rm DC}+R^k_{\rm ESR})}. \quad (2)$$

The second-order denominator of (1) and (2) clearly identifies an oscillation hazard if the resonant frequency of the dc side impedance is close to a dc bus current harmonic component of significant magnitude. Note that, the parasitic inductance in $L_{\rm DC}$

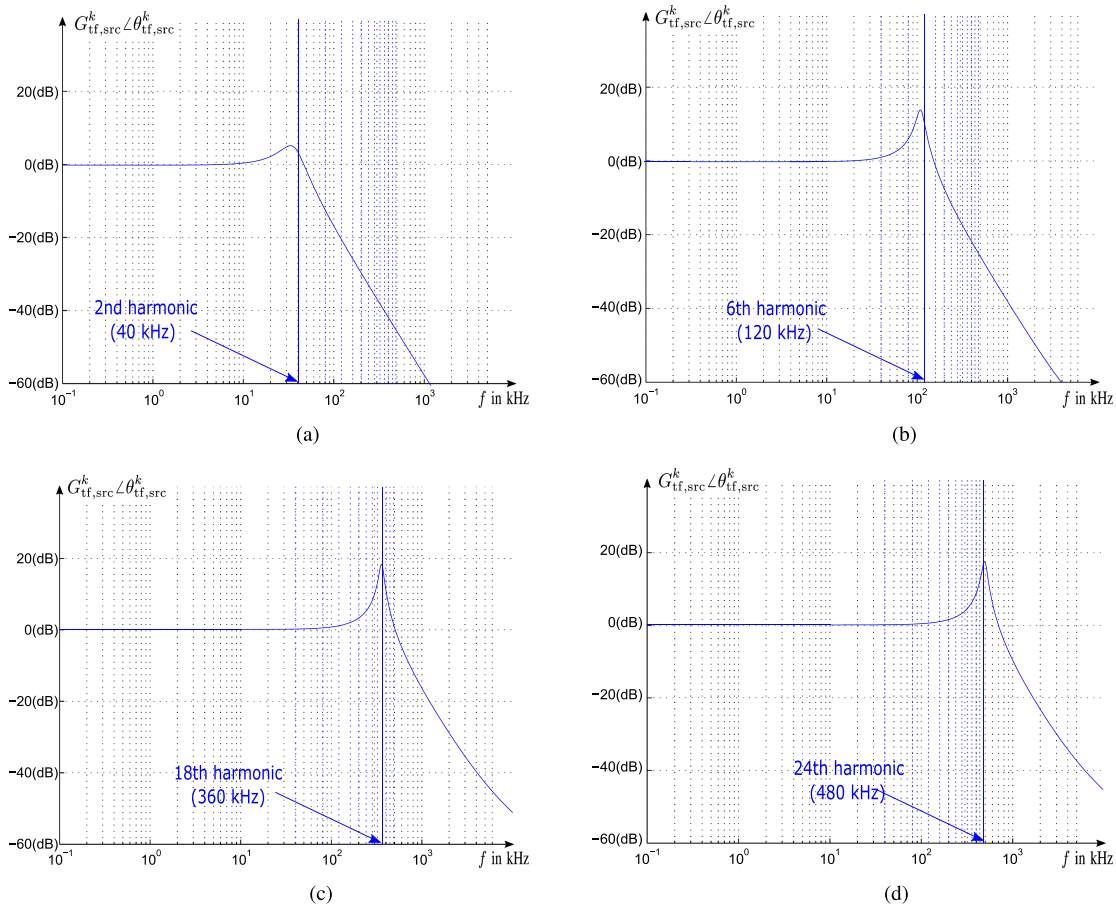

Fig. 2. Bode plot of primary dc bus transfer function for a variable dc bus capacitance ($L_{\mathrm{DC}} = 200$ nH). (a) $\mathrm{C_{DC}} = 100\ \mu$F, $\mathrm{R_{ESR}} = 0.3\ \mathrm{m\Omega}$. (b) $\mathrm{C_{DC}} = 10\ \mu$F, $\mathrm{R_{ESR}} = 3\ \mathrm{m\Omega}$. (c) $\mathrm{C_{DC}} = 1\ \mu$F, $\mathrm{R_{ESR}} = 30\ \mathrm{m\Omega}$. (d) $\mathrm{C_{DC}} = 0.5\ \mu$F, $\mathrm{R_{ESR}} = 60\ \mathrm{m\Omega}$.

TABLE I
EXPERIMENTAL SYSTEM AND OPERATING CONDITIONS

Parameter		Value
Primary bridge ..		
..dc bus inductance (parasitic)	L_{DC}	200 nH
..dc bus capacitance	C_{DC}	TBD
..bulk source capacitance	C_{src}	4.4 mF
ac-link coupled inductor	L	103 μH
	R	0.4 Ω
Primary dc bus voltage	$2\,V_{\mathrm{p,DC}}$	50 V
Dc–dc bus voltage ratio	d	0.8
Switching frequency	f_{sw}	20 kHz

as well as any passive damping caused by the parasitic resistance R_{DC} may be difficult to determine at the design stage, and hence identifying a dc bus resonant frequency ($f_{\mathrm{DC,res}}$) hazard before experimental testing can be very challenging.

Fig. 2 presents Bode plots for the dc filter frequency characteristic $G^k_{\mathrm{tf,src}}\angle\theta^k_{\mathrm{tf,src}}$ of the exemplar physical bridge used in this paper (parameters listed in Table I), for increasing values of dc bus bridge capacitance and a constant parasitic dc bus inductance of 200 nH connecting to the external power source. The damping resistances R_{DC} and R_{ESR} were estimated by developing a PLECS simulation [16] that matched the experimental response for a 1μF bus capacitor, as shown later in Figs. 5 and 6, with (frequency independent) values of $R^k_{\mathrm{DC}} = R_{\mathrm{DC}} = 25\ \mathrm{m\Omega}$ and $R^k_{\mathrm{ESR}}(1\mu\mathrm{F}) = R_{\mathrm{ESR}}(1\mu\mathrm{F}) = 30\ \mathrm{m\Omega}$. Note that, R_{ESR} is reduced linearly inverse to C_{DC} as can typically be observed in practice [17].

The enhanced vertical lines in these plots show the locations of the even integer harmonics of the fundamental PSSW switching frequency (20 kHz), as will be analytically determined in the following section. Note that these dc side current harmonics are all even (e.g., 40, 80, 120 kHz, etc.) because the rectification action of each H-bridge causes a fundamental frequency shift from the odd PSSW ac side current harmonics (e.g., 20, 60, 100 kHz, etc.). In principle, the effect of any critical dc bus resonance that may occur can be suppressed by one of the two following approaches:

1) Passive Damping: The bridge capacitor value C_{DC} is selected as large as is required to suppress all relevant dc bus harmonic frequencies. For example, for the reference bridge impedance parameters and operating conditions shown in Table I, C_{DC} has to be at least 100 μF, as shown in Fig. 2(a). This may not only be difficult to physically achieve without creating a further parasitic inductive connection, but also means that the second harmonic dc bus current component will still flow (almost) one-to-one to the terminating source supply (for $C_{\mathrm{DC}} = 100\ \mu$F). Alternatively, a separate discrete dc bus filter inductor can be

added to reduce the resonant cutoff frequency of the parasitic LC resonant circuit, which can be useful to reduce the total filter volume if the injected bridge dc harmonic magnitudes are low relative to the dc bus voltage (as happens in higher voltage lower current applications). In any case, passive damping is a relatively ad hoc approach that is difficult to design, and may not be effective in many applications.

2) AHS: If $C_{\rm DC}$ is set to significantly less than 100 μF, the parasitic dc bus resonance will inevitably be excited by one of the injected dc bus current harmonics. For $C_{\rm DC} = 10$ μF, the rather significant sixth dc bus harmonic is likely to cause substantial dc bus oscillations, as indicated by Fig. 2(b). Unfortunately, since this harmonic multiple is a convolution product of two low-order ac-link current harmonic components, which contribute significantly to the zero-order dc bus harmonic and thus the fundamental power transfer, it is difficult to suppress using AHS. Reducing $C_{\rm DC}$ further to 1 μF causes a resonance at the less significant 18th harmonic frequency, as shown in Fig. 2(c), which is easier to suppress using AHS as will be presented later. As the dc bus capacitance is reduced further, i.e., $C_{\rm DC} = 0.5$ μF in Fig. 2(d), the parasitic resonant frequency becomes higher and higher, and hence is less likely to be influenced by dc bus harmonics injected from the DAB switching process. However, a certain minimum bridge capacitance is always required to buffer energy for the bridge switching transitions, which limits the minimum size dc bus capacitance that is feasible. For the AHS approach, the lower-order dc bus current harmonics (below the parasitic resonance cutoff frequency) created by the PSSW modulation process will be absorbed by the external source (e.g., a battery [18], [19]).

III. Determination of DC Bus Harmonics in Single-Phase DAB

The dc bus harmonic current components for any arbitrary operating condition and DAB ac coupling impedance will now be determined using harmonic decomposition analysis of the PSSW switching pattern, as a precursor to selectively suppressing a particular dc bus harmonic using AHS in the following Section.

A. Frequency Domain Analysis of DC Bus Current Harmonics

In general terms, the primary-side DAB ac-link current shown in Fig. 1(b) can be expressed as a sum of harmonic sinusoids, viz

$$i_{\rm p}(w_{\rm sw}t) = \sum_{n=1}^{\infty} i_{\rm p}^{m}(w_{\rm sw}t) = \sum_{n=1}^{\infty} I_{\rm p}^{m}\sin(mw_{\rm sw}t + \theta_{\rm p}^{m}). \quad (3)$$

The magnitude and phase angle of each of these harmonic components can be found by applying two-port network analysis assuming negligible ripple in the dc bus voltage. The relationship between the ac-link currents and the DAB switched bridge output voltages can thus be recalled from [4] for each harmonic component using ac phasor theory as

$$\begin{bmatrix} I_{\rm p}^{m}\angle\theta_{\rm p}^{m} \\ I_{\rm s}^{m}\angle\theta_{\rm s}^{m} \end{bmatrix} = \frac{4V_{\rm p,DC}}{\pi m}\begin{bmatrix} Y_{\rm p,p}^{m}\angle\gamma_{\rm p,p}^{m} & Y_{\rm p,s}^{m}\angle\gamma_{\rm p,s}^{m} \\ Y_{\rm s,p}^{m}\angle\gamma_{\rm s,p}^{m} & Y_{\rm s,s}^{m}\angle\gamma_{\rm s,s}^{m} \end{bmatrix} \times \begin{bmatrix} 1\angle\{m[\alpha/2]\} - 1\angle\{m[-\alpha/2]\} \\ d\angle\{m[\beta/2-\delta]\} - d\angle\{m[-\beta/2-\delta]\} \end{bmatrix} \quad (4)$$

where d is the dc–dc bus voltage ratio (incl. the transformer turns ratio $N_{\rm p}/N_{\rm s}$) and $m = [2n-1]$ with $n = 1, 2, \ldots N$.

The primary bridge switching functions "crop" the harmonic ac-link currents described by (3) into discontinuous segments on the dc bus, as shown in Fig. 3, for the first and third ac harmonic current components. These segments can then be expressed as another set of harmonic components using a Fourier series, giving a resulting dc bus current in harmonic form of

$$i_{\rm p,DC} = \sum_{k=0}^{\infty} i_{\rm p,DC}^{k}(w_{\rm sw}t) = \frac{a_{\rm p}^{0}}{2} + \sum_{k=1}^{\infty}\left\{ \begin{array}{l} a_{\rm p}^{k}\cos(kw_{\rm sw}t) \\ +\, b_{\rm p}^{k}\sin(kw_{\rm sw}t) \end{array} \right\}. \quad (5)$$

From Fig. 3 it can be seen that a positive dc bus current component only flows during the period $-\alpha/2 \le wt \le \alpha/2$ through switches $S_{\rm p,1}$ and $S_{\rm p,4}$, while a negative dc bus current component only flows during the period $\pi - \alpha/2 \le wt \le \pi + \alpha/2$ through switches $S_{\rm p,2}$ and $S_{\rm p,3}$. Using these limits, the harmonic coefficients of (5) can be determined by a Fourier

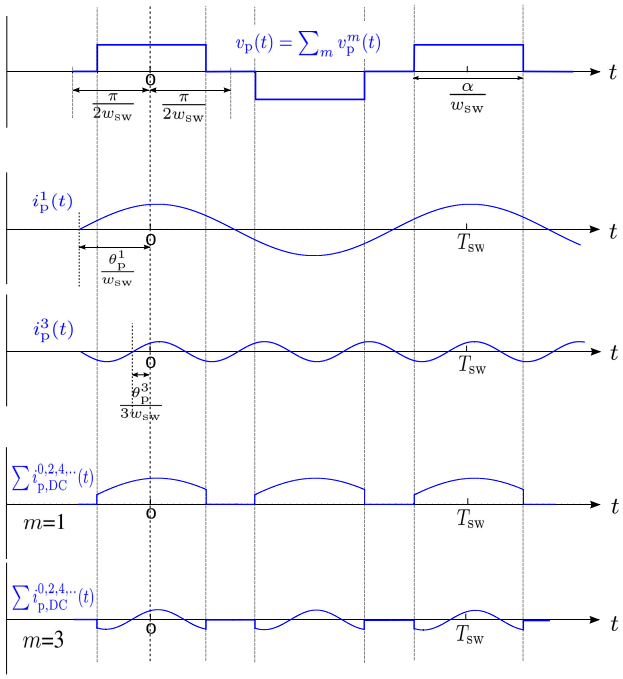

Fig. 3. Translation from ac-link into dc bus current harmonics in time domain.

integral of the form

$$I^k_{\mathrm{p,DC}}\angle\theta^k_{\mathrm{p,DC}} = \underline{c}^k_{\mathrm{p}} = a^k_{\mathrm{p}} + jb^k_{\mathrm{p}} = \frac{1}{\pi}\left\{\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} i_{\mathrm{p}}(w_{\mathrm{sw}}t)e^{jk\omega_{\mathrm{sw}}t}d(\omega_{\mathrm{sw}}t) - \int_{\pi-\frac{\alpha}{2}}^{\pi+\frac{\alpha}{2}} i_{\mathrm{p}}(w_{\mathrm{sw}}t)e^{jk\omega_{\mathrm{sw}}t}d(\omega_{\mathrm{sw}}t)\right\}. \quad (6)$$

Substituting (3) into (6) gives

$$\underline{c}^k_{\mathrm{p}} = \frac{1}{\pi}\left\{\begin{array}{l}\displaystyle\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}}\sum_{n=1}^{\infty} I^m_{\mathrm{p}}\sin(mw_{\mathrm{sw}}t+\theta^m_{\mathrm{p}})e^{jk\omega_{\mathrm{sw}}t}d(\omega_{\mathrm{sw}}t) \\ \displaystyle -\int_{\pi-\frac{\alpha}{2}}^{\pi+\frac{\alpha}{2}}\sum_{n=1}^{\infty} I^m_{\mathrm{p}}\sin(mw_{\mathrm{sw}}t+\theta^m_{\mathrm{p}})e^{jk\omega_{\mathrm{sw}}t}d(\omega_{\mathrm{sw}}t)\end{array}\right\} \quad (7)$$

which can be rearranged as

$$\underline{c}^k_{\mathrm{p}} = \frac{1}{\pi}\sum_{n=1}^{\infty} I^m_{\mathrm{p}} \left\{\begin{array}{l}\displaystyle\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}}\sin(mw_{\mathrm{sw}}t+\theta^m_{\mathrm{p}})e^{jk\omega_{\mathrm{sw}}t}d(\omega_{\mathrm{sw}}t) \\ \displaystyle -\int_{\pi-\frac{\alpha}{2}}^{\pi+\frac{\alpha}{2}}\sin(mw_{\mathrm{sw}}t+\theta^m_{\mathrm{p}})e^{jk\omega_{\mathrm{sw}}t}d(\omega_{\mathrm{sw}}t)\end{array}\right\}. \quad (8)$$

Using the relationship

$$\sin\Delta = \frac{e^{j\Delta}-e^{-j\Delta}}{2j}, \quad (9)$$

Eqn. (6) can be solved as

$$\underline{c}^{k(\mathrm{odd})}_{\mathrm{p}} = 0$$

$$\underline{c}^{k(\mathrm{even})}_{\mathrm{p}} = \frac{1}{\pi}\sum_{n=1}^{\infty} I^m_{\mathrm{p}} \left\{\begin{array}{l}\displaystyle\frac{[k-m](e^{j[k+m]\frac{\alpha}{2}}-e^{-j[k+m]\frac{\alpha}{2}})e^{j\theta^m_{\mathrm{p}}}}{-[k^2-m^2]} + \\ \displaystyle\frac{[k+m](e^{j[k-m]\frac{\alpha}{2}}-e^{-j[k-m]\frac{\alpha}{2}})e^{-j\theta^m_{\mathrm{p}}}}{-[k^2-m^2]}\end{array}\right\}. \quad (10)$$

This reduces, for even k, to

$$a^k_{\mathrm{p}} = \frac{4}{\pi}\sum_{n=1}^{\infty} I^m_{\mathrm{p}}\frac{\sin(\theta^m_{\mathrm{p}})}{(k^2-m^2)}\begin{pmatrix} k\sin(\frac{k\alpha}{2})\cos(\frac{m\alpha}{2}) \\ -m\cos(\frac{k\alpha}{2})\sin(\frac{m\alpha}{2})\end{pmatrix} \quad (11a)$$

$$b^k_{\mathrm{p}} = \frac{4}{\pi}\sum_{n=1}^{\infty} I^m_{\mathrm{p}}\frac{\cos(\theta^m_{\mathrm{p}})}{(k^2-m^2)}\begin{pmatrix} m\sin(\frac{k\alpha}{2})\cos(\frac{m\alpha}{2}) \\ -k\cos(\frac{k\alpha}{2})\sin(\frac{m\alpha}{2})\end{pmatrix}. \quad (11b)$$

Eqn. (11) defines the coefficients of each of the harmonic components of the dc bus current that flows between the dc bus capacitors and the primary-side single-phase bridge. From (10), it can also be concluded that the dc bus current contains only even harmonic multiples of the switching frequency, as could be expected since the odd switching harmonics of the modulation process convolve with the odd ac-link current harmonics to produce only even dc bus harmonic components. The zero-order dc bus harmonic ($k = 0$) is determined to be

$$i^0_{\mathrm{p,DC}} = \frac{a^0_{\mathrm{p}}}{2} = \frac{2}{\pi}\sum_{n=1}^{\infty} I^m_{\mathrm{p}}\frac{\sin(\theta^m_{\mathrm{p}})}{m}\sin\left(\frac{m\alpha}{2}\right) \quad (12)$$

where I^m_{p} and θ^m_{p} are defined by (4) and vary depending on the values of α, β, and δ.

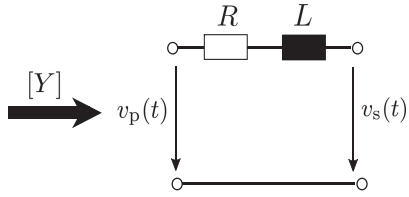

Fig. 4. Simplified RL impedance network.

B. Simulation and Experimental Verification of DC Bus Oscillations

To illustrate the potential dc resonance hazard for a DAB converter, the dc bus capacitors for both the primary and secondary side bridge of the exemplar DAB converter with parameters as listed in Table I, were set to $C_{\mathrm{DC}} = 1\ \mu$F. The ac-link coupling impedance network was simplified to an RL coupled inductor component, as shown in Fig. 4 (i.e., single ac-link current path and "unity transformer turns ratio"), whereby the matrix elements of $[Y]$ for the two-port analysis in (4) become

$$Y^m_{\mathrm{p,p}}\angle\gamma^m_{\mathrm{p,p}} = Y^m_{\mathrm{s,s}}\angle\gamma^m_{\mathrm{s,s}} = -Y^m_{\mathrm{p,s}}\angle\gamma^m_{\mathrm{p,s}} = -Y^m_{\mathrm{s,p}}\angle\gamma^m_{\mathrm{s,p}} = \frac{1}{R+jmw_{\mathrm{sw}}L}. \quad (13)$$

Fig. 5(a) and (b) (OP1), and Fig. 6(a) and (b) (OP3), illustrate the dc bus oscillation that occurs (both in simulation and in matching experimental conditions) for this converter under two exemplar operating conditions, where a significant 18th harmonic resonance current (dominant: $f_{\mathrm{DC,res}} = 360$ kHz) is measured in the dc bus current that flows back into the external source. The phase angle drift of the source current harmonic frequencies causes the ring to decay within a half primary switching cycle. It is commented that this oscillation becomes more severe as the output current magnitude increases in relation to the dc bus voltage, as noted earlier. Note also that the results from simulation and experiment slightly differ due to frequency dependencies, the actual IGBT voltage drop, and some dc bus voltage oscillation across the secondary bridge output voltage.

Figs. 5(c) and Fig. 6(c) show the theoretical value of the harmonic components of the injected dc bus current $i_{\mathrm{p,DC}}$ using (11), compared against a fast Fourier transform of the measured experimental waveforms as well as sketched source current harmonic magnitudes derived from Fig. 2(c). From (11), it can be seen that the magnitudes of each of the dc bus reflected

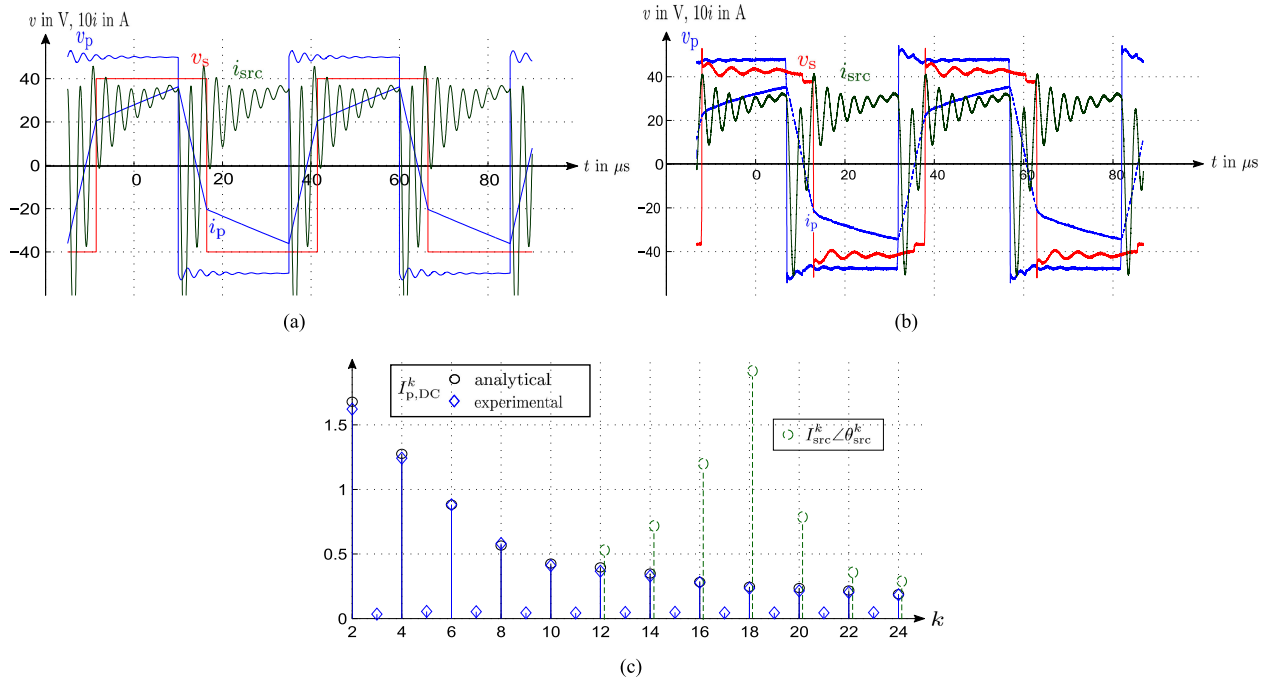

Fig. 5. Standard two-level PSSW @ 1.9 A (OP1: $\alpha = \pi$, $\delta = 0.81$). (a) Simulation. (b) Experiment. (c) Fourier spectrum of $i_{\mathrm{p,DC}}$.

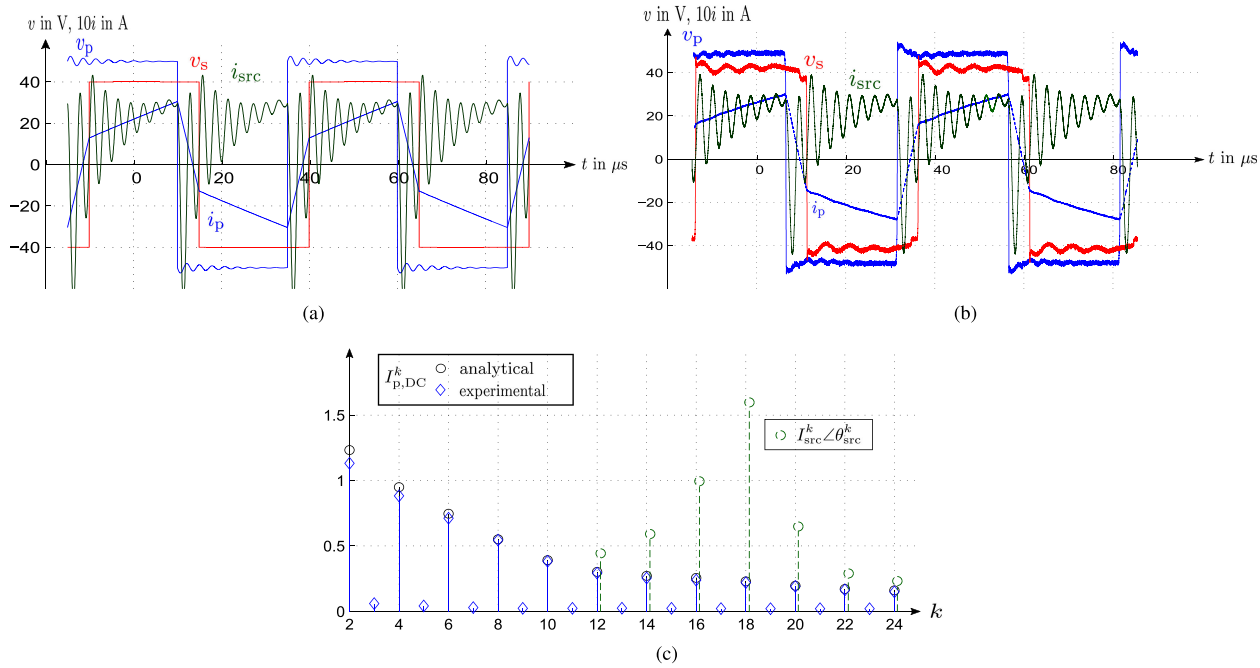

Fig. 6. Standard two-level PSSW @ 1.6 A (OP3: $\alpha = \pi$, $\delta = 0.62$). (a) Simulation. (b) Experiment. (c) Fourier spectrum of $i_{\mathrm{p,DC}}$.

harmonics vary as the primary bridge duty cycle α changes. Hence the influence of any one harmonic can be minimized by appropriately selecting the value for the primary bridge duty cycle α. However, if the secondary bridge is switched using two-level PSSW modulation ($\beta = \pi$), both α and δ must then be simultaneously varied if a constant power flow, i.e., zero-order dc current harmonic in (12), is to be maintained as the influence of the selected harmonic is minimized.

IV. Active Suppression of Selected Primary DC Bus Harmonic

Selective AHS will now be used to suppress the critical dc bus current oscillation around the dominant 18th harmonic. Fig. 7(a) shows the magnitude of this 18th harmonic current component $I^{18}_{\mathrm{p,DC}}$ as α and δ vary, while β is kept constant at $\beta = \pi$, for average dc bus currents of 1.6 and 1.9 A feeding into the DAB (determined for $N = 30$). Note that, ZVS operation is

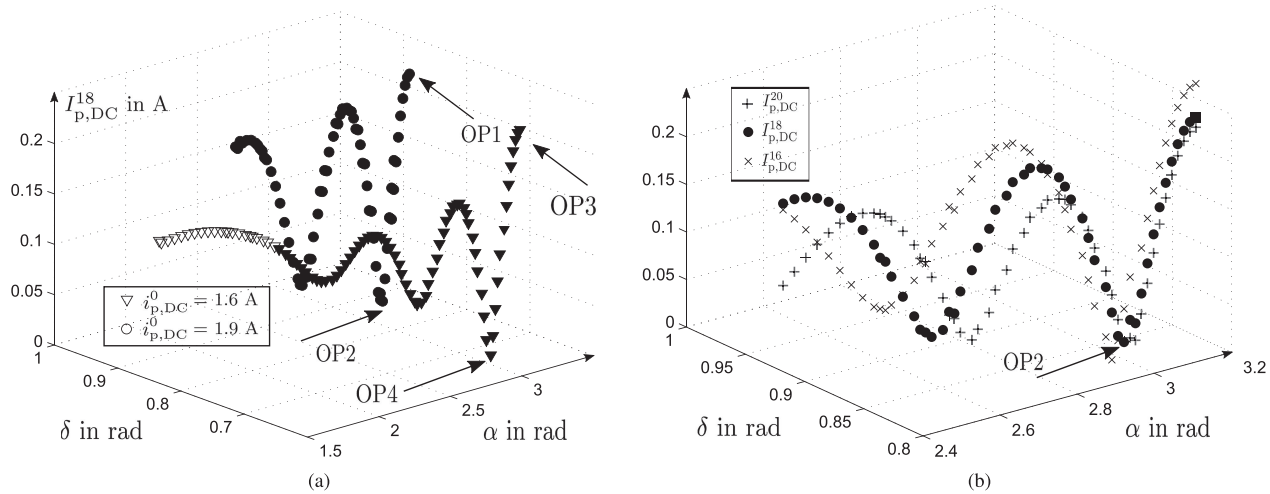

Fig. 7. Manipulation of dc bus harmonics using adaptive three-level modulation ($\beta = \pi$). (a) 18th dc bus harmonic for two different power levels. (b) 16th, 18th, 20th dc bus harmonic @ 1.9 A.

maintained for all operating conditions in accordance with the principles of [4], indicated as solid filled symbols in this figure. From this figure, it can be seen that for $\alpha = 2.95$ (radians) the $18\mathrm{th}$ dc bus current harmonic component is heavily suppressed. This suggests that if the DAB is always operated with this value for α as the power magnitude varies between these two reference power levels, the unacceptable $18\mathrm{th}$ harmonic resonance in the dc bus current should be significantly reduced.

As a practical aspect it is noted here that PP film capacitors are typically available with a positive/negative tolerance of $5 - 10\%$ [17]. Similar deviations can be expected for the parasitic dc bus inductance (e.g., a battery cable). A relative component tolerance in either C_{DC} (tol_C) and/or L_{DC} (tol_L) causes a relative change in resonance frequency ($tol_{f_{\mathrm{res}}}$) of $tol_{f_{\mathrm{res}}} = \frac{1}{\sqrt{(1+tol_C)(1+tol_L)}} - 1$. For the worst case condition, i.e., a maximum deviation of $10\,\%$ at the same negative (positive) polarity, $tol_{f_{\mathrm{res}}}$ becomes +9% (-11%). Hence, for the application example in this paper, the primary dc bus resonance peak would be located anywhere between the $16\mathrm{th}$ and the $20\mathrm{th}$ harmonic. Fig. 7(b) then shows how the magnitude of the neighboring dc bus harmonics ($16\mathrm{th}$, $20\mathrm{th}$) varies as α and δ vary. It can be observed that while their minimums are located slightly apart from OP2, their magnitudes are however still largely suppressed for this operating condition. Hence, the AHS technique retains its suppressing capability to a large extent despite practical component tolerance variations (or low Q filter resonant circuits).

Fig. 8 shows the PSSW modulation angles to minimize the magnitude of this particular harmonic for the entire power range of the exemplar DAB converter. Note that for small load angles (i.e., partial load conditions), α needs to be reduced to maintain ZVS soft switching operation of all DAB phase legs at the given dc–dc bus voltage ratio d of 0.8.

A. Large Load Angle δ

The experimental single phase DAB system is now used to verify this concept and to show how the harmonic components

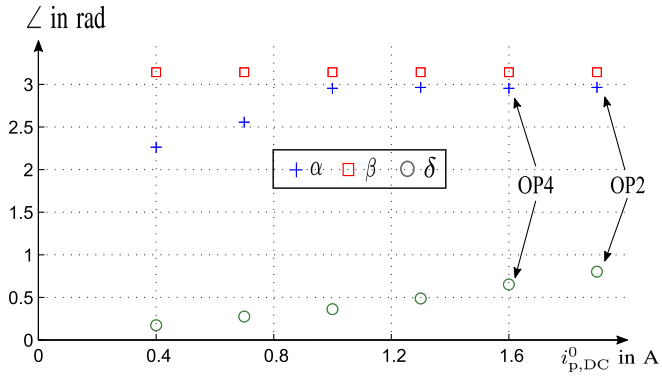

Fig. 8. PSSW modulation angles to minimize the impact of $18\mathrm{th}$ dc bus harmonic while maintaining ZVS.

that excite the characteristic dc bus resonant frequency can be actively suppressed using adaptive three-level modulation while still maintaining constant power transfer. Fig. 9(a) and (b) (OP2), and Fig. 10(a) and (b) (OP4), provide simulation and experimental confirmation of this result. The elimination of the $18\mathrm{th}$ component is also shown in the harmonic spectrum of Figs. 9(c) and 10(c), respectively. As anticipated by Fig. 7(b), the waveforms consequently show a significant suppression of the $18\mathrm{th}$ and any surrounding harmonic current components ("notch filter") in the external supply current if the PSSW mitigation process is centered about the estimated parasitic dc bus resonance frequency.

B. Small Load Angle δ

Fig. 11 shows matching results for a reduced load angle, i.e., low load condition, confirming the generality of the AHS resonant damping concept using interactive adjustment of α and δ. Note that in this case, α is reduced from 2.95 (radians) to maintain ZVS operation of the secondary bridge with a dc bus voltage ratio of $d = 0.8$ [4].

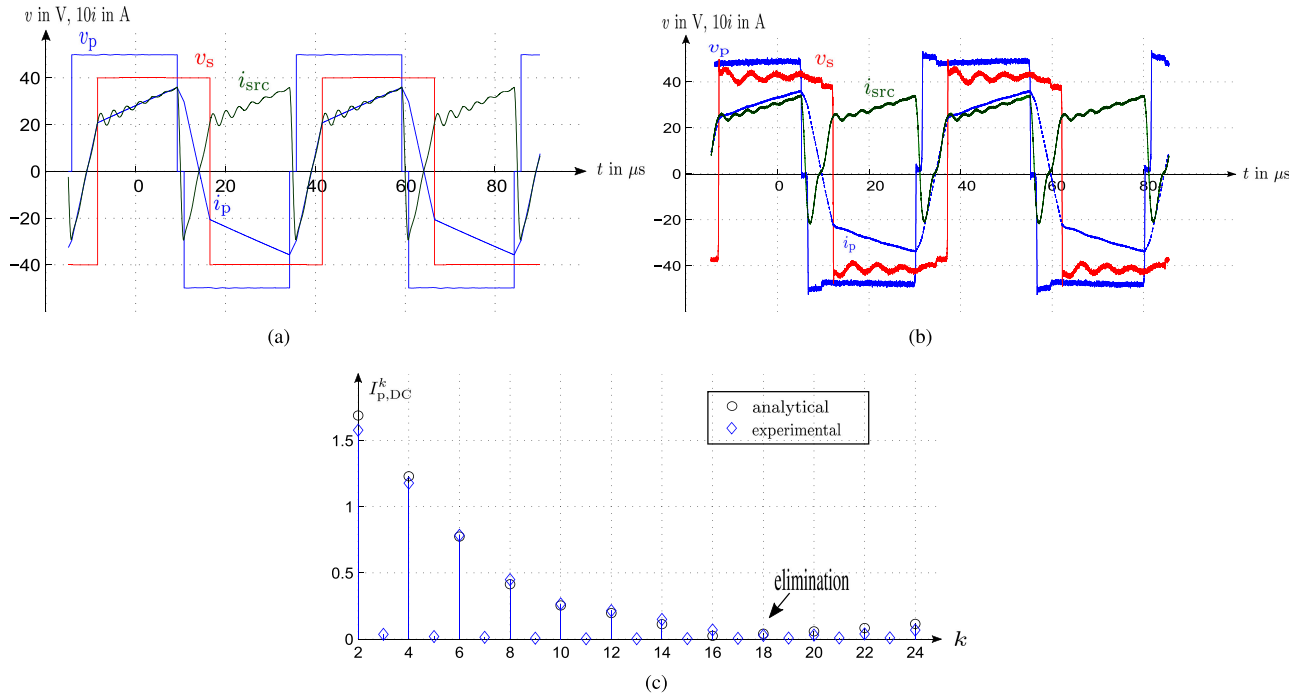

Fig. 9. Adaptive PSSW @ 1.9 A (OP2: $\alpha = 2.95$, $\delta = 0.82$). (a) Simulation. (b) Experiment. (c) Fourier spectrum of $i_{\mathrm{p,DC}}$.

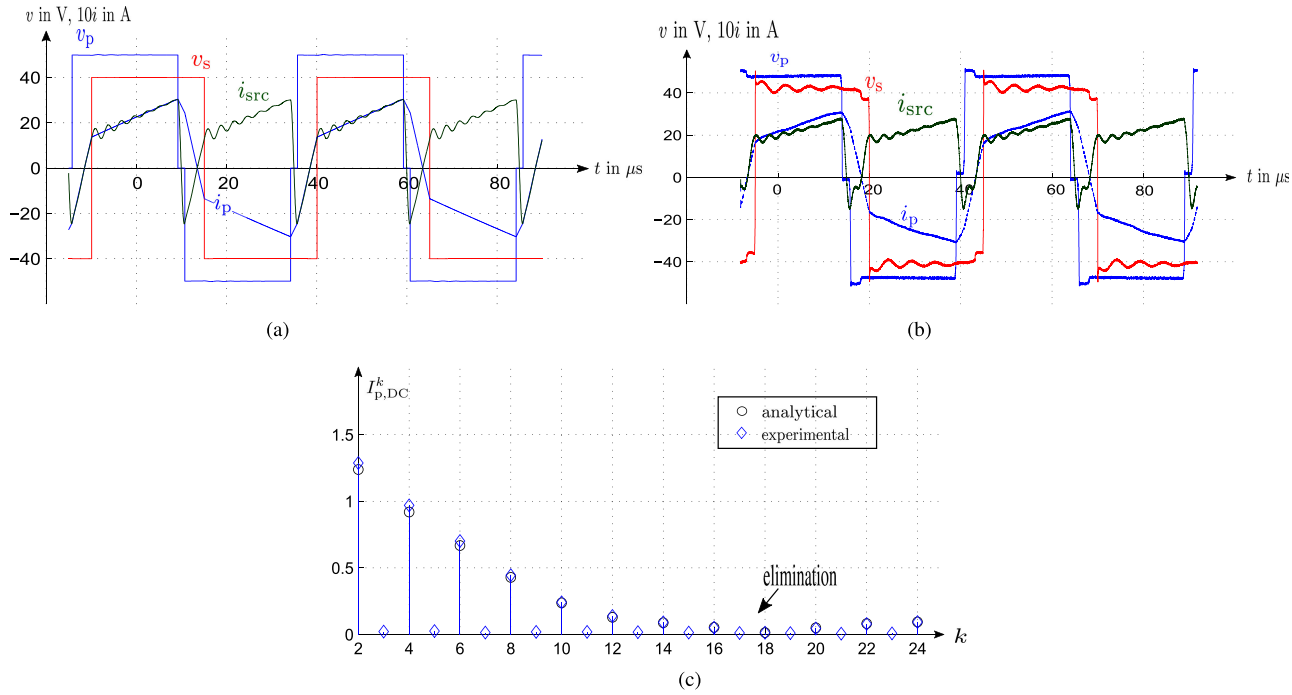

Fig. 10. Adaptive PSSW @ 1.6 A (OP4: $\alpha = 2.95$, $\delta = 0.64$). (a) Simulation. (b) Experiment. (c) Fourier spectrum of $i_{\mathrm{p,DC}}$.

V. Active Suppression of Primary and Secondary DC Bus Oscillation

Fig. 12 shows the selective AHS of the 18th harmonic in the primary dc bus for an average input current of 1.3 A. However, the ring in the experimental secondary bridge output voltage waveform v_{s} indicates that the physical arrangement of the secondary dc bus causes another dc bus resonance at the tenth harmonic (dominant: $f_{\mathrm{DC,res}} = 200$ kHz). The secondary (physically longer rail) dc bus inductance was therefore determined to be 650 nH for the same bridge capacitor ($C_{\mathrm{DC}} = 1\mu$F, $R^k_{\mathrm{ESR}} = 30\,\mathrm{m}\Omega$) and $R^k_{\mathrm{DC}} = 100\,\mathrm{m}\Omega$. The Bode plot of the corresponding LC transfer function in Fig. 13 in combination with the spectrum of injected dc bus current harmonics in Fig. 12(c) confirm this observation.

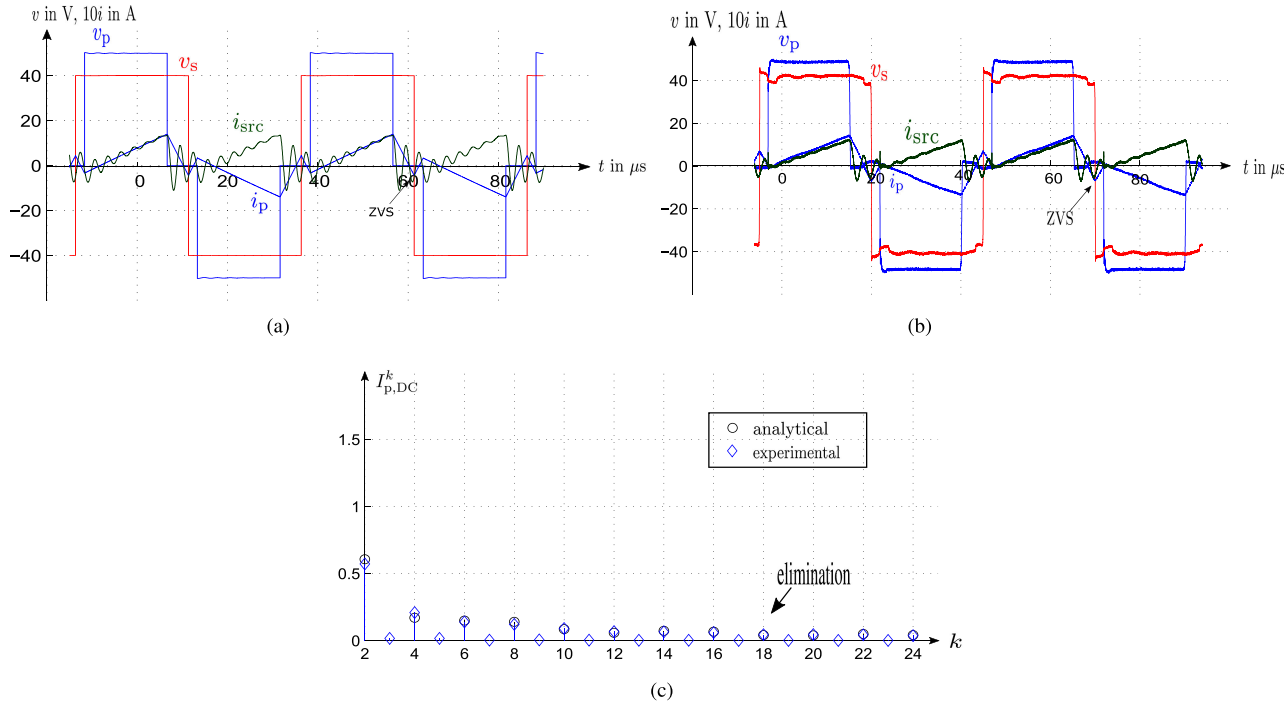

Fig. 11. Adaptive PSSW @ 0.4 A ($\alpha = 2.30$, $\delta = 0.17$). (a) Simulation. (b) Experiment. (c) Fourier spectrum of $i_{\mathrm{p,DC}}$.

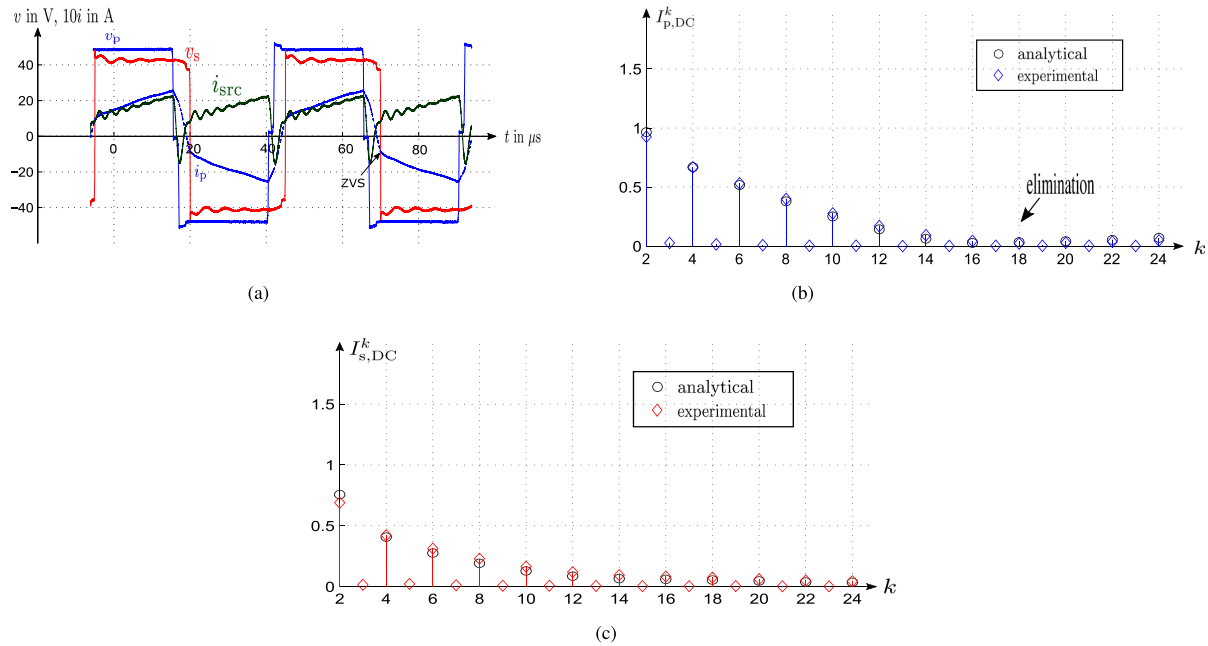

Fig. 12. Adaptive PSSW @1.3 A ($\alpha = 2.95$, $\beta = \pi$, $\delta = 0.48$). (a) Experiment. (b) Fourier spectrum of $i_{\mathrm{p,DC}}$. (c) Fourier spectrum of $i_{\mathrm{s,DC}}$.

Using AHS for the primary and the secondary DAB converter bridge, this secondary side dc bus resonance can be suppressed simultaneously by varying the secondary side bridge duty cycle β. Fig. 14 shows a smoothed secondary bridge voltage waveform, which confirms the capability to also mitigate the secondary side dc bus harmonic currents (here: $\beta = 2.60$).

Note however that the simultaneous suppression of particular harmonic currents in both dc buses can significantly constrain the power transfer capability and ZVS operation of the DAB, which becomes more severe as the order of the parasitic resonance frequencies reduces. Hard switching may hence be unavoidable for certain dc–dc bus voltage ratios and load conditions [as can be observed in Fig. 14(a) where the devices in phase leg HB4 experience hard turn-ON events]. For this particular application example, it may thus be more attractive to passively suppress the secondary dc bus oscillation by, e.g., using a larger bus capacitor (50–100 μF). In this context it is also mentioned that for DAB converters with a significant voltage boost ratio and winding turns ratio (in case of an actual high-frequency ac-link transformer), the AHS is preferably applied

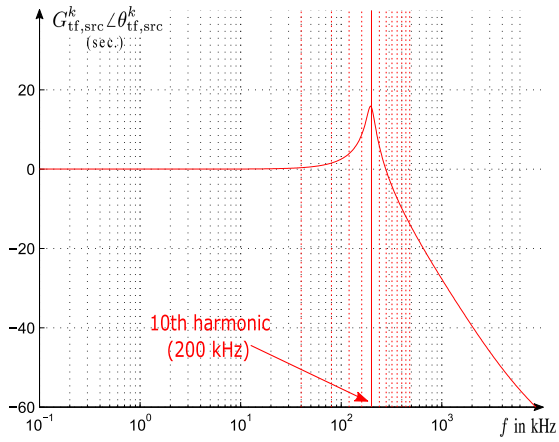

Fig. 13. Bode plot of secondary dc bus transfer function.

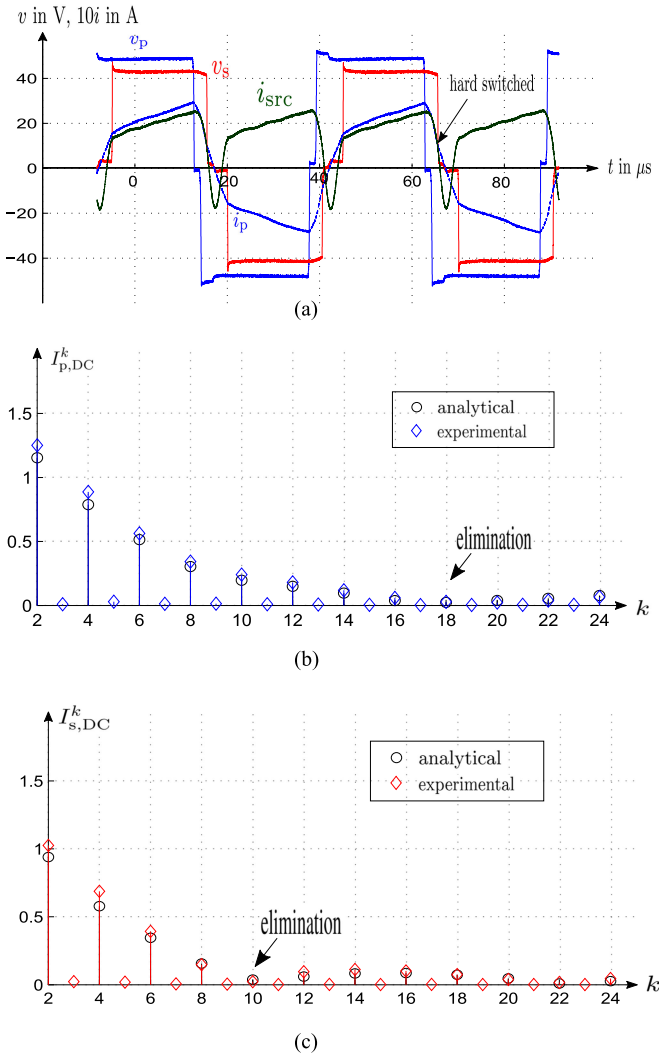

Fig. 14. Adaptive PSSW @1.3 A ($\alpha = 2.95$, $\beta = 2.60$, $\delta = 0.52$). (a) Experiment. (b) Fourier spectrum of $i_{\mathrm{p,DC}}$. (c) Fourier spectrum of $i_{\mathrm{s,DC}}$.

at the lower voltage dc bus/converter bridge if the voltage drop across the dc bus $R_{\mathrm{DC}}/L_{\mathrm{DC}}$ impedance—particularly at twice the fundamental frequency—is moderately low.

It should be recognized that the AHS approach reduces the control degrees of freedom provided by the three-level DAB modulation concept, which could otherwise be used to maximize the conversion efficiency at every operating point. For example, in [8] and [20] the primary objective is to set the modulation parameters to reduce the ac-link rms circulating currents, i.e., achieve an overall reduction of the (reactive power) harmonic distortion in the dc bus current, and maintain ZVS as the operating conditions vary. In contrast, the control strategy presented in this paper aims to suppress a particular resonant frequency in the dc bus currents for all operating conditions.

Another important loss aspect about AHS however is its potential to avoid additional heat dissipation in the dc bus components (e.g., capacitors) that would otherwise result from an undamped dc bus current oscillation. Ref. [17] shows typical impedance and ESR measurements for a wide range of metallized film PP capacitors across frequencies from kHz to MHz. For example, for the prototype converter considered in this paper, and the operating conditions shown in Figs. 5 and 6, the excited dc bus resonance more than doubles (i.e., up to 0.2%) the total filter network losses, compared to using AHS with the resulting reduced dc bus current oscillation, as shown in Figs. 9 and 10.

VI. Conclusion

This paper has shown how AHS can be used with adaptive PSSW modulation of a DAB dc–dc converter to suppress the dc bus oscillations that can occur for practical converters with unavoidable parasitic bus connection impedances. In contrast to the more conventional approach of relying on larger dc bus capacitors and passive damping, the method allows to significantly reduce the dc bus (capacitor) filter size of the DAB converter, although with the consequence that more of the lower order dc bus current harmonics created by the PSSW modulation process will be absorbed by the external source (e.g., a battery). The approach is particularly attractive to reduce the converter size and cost for low-voltage high-current applications. The AHS control strategy and the supporting frequency domain analysis of the dc bus harmonics have been confirmed by simulation and matching experimental results.

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