A Frequency Adaptive Phase Shift Modulation Control Based LLC Series Resonant Converter for Wide Input Voltage Applications

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***Abstract*—This paper presents an isolated LLC series resonant DC/DC converter with novel frequency adaptive phase shift modulation control, which suitable for wide input voltage (200–400 V) applications. The proposed topology integrates two half-bridge in series on the primary side to reduce the switching stress to half of the input voltage. Unlike the conventional converter, this control strategy increases the voltage gain range with zero-voltage-switching (ZVS) to all switches under all operating voltage and load variations. Adaptive frequency control is used to secure ZVS in the primary bridge with regards to load change. To do so, the voltage gain becomes independent of the loaded quality factor. In addition, the phase shift control is used to regulate the output voltage as constant under all possible inputs. The control of these two variables also significantly minimizes the circulating current, especially from the low-voltage side, which increases the efficiency as compared to a conventional converter. Experimental results of a 1-Kw prototype converter with 200–400-V input and 48-V output are presented to verify all theoretical analysis and characteristics.**

***Index Terms*—Frequency adaptive phase shift modulation control (FAPSM), LLC, resonant converter, wide gain range, zero-voltage-switching (ZVS).**

I. Introduction

THE renewable-energy sources, such as photovoltaic, wind power, and fuel cell system are highly promising sources to mitigate the power-generation crisis throughout the world. Power converters have become the essential part of generation systems to utilize the fluctuating renewable energy. The power converter which is capable of generating constant output with variable input is the most effective ones for the renewable power generation systems. It is also common to use a bidirectional converter to interface with energy storage systems (ESSs).

Dual active bridge (DAB) has drawn lots of interest in the ESSs due to having the bidirectional capability with high-efficiency, high-power density, and reliability [1]–[7]. The voltage gain of DAB is limited to unity to maintain zero-voltage-switching (ZVS) for all load variations [8], [9]. It also suffers from high circulating current in the secondary side and high turn-off losses. In order to extend the gain range with ZVS or minimize the circulating energy further, some control strategies were proposed in [1], [3], and [10]–[13]. However, these control strategies cannot overcome all the disadvantages at a time.

The resonant version of DAB is called DAB resonance converter has the same performance with improved efficiency [14]–[21]. In [16], a dual-full bridge series resonance converter with fixed frequency phase shift control has been proposed and analyzed using modified fundamental harmonic approximation (FHA) approach. The voltage gain of this converter has to be limited to unity to maintain the ZVS over the wide load range, and the circulating current in the low-voltage side is high as well. As a result, the efficiency is degraded, especially when the voltage gain deviates from the unity. Therefore, the converter becomes unsuitable for wide input voltage applications.

A bidirectional DAB LLC converter for ESSs has been proposed in [17]. This converter operated at a constant frequency, but the duty ratio is different based on desired voltage gain. An extra inductor is added to make the topology symmetrical in any operating modes, which increases the power loss and cost for the system. The gain is still limited to maintain high conversion efficiency. It is also operated in the capacitive slope region, which is suitable for ZCS realization.

The topology in [22] is an integration of a half bridge (HB) and full bridge (FB) LLC circuit. A simple pulse width modulation control technique with more switches has been used for wide input voltage applications. It can be used only for unidirectional power flow. For the certain input voltage, the time interval of the resonant current being equal to the magnetizing current is longer, which increased the conduction loss as well as hinders the improvement of efficiency.

Several attempts have taken to increase the input voltage range in the literature. Three-level DC/DC converters have been introduced to minimize the voltage stress across switches. They have been used to increase high-power density, operating over wide input voltage range and best suitable for high-voltage applications [23]–[25]. But all the converters related to unidirectional dc–dc applications. The three-level bidirectional LLC resonant converter has been proposed in [18], where the voltage stress across switches depends on voltage gain, and ZVS appeared only in the primary switches.

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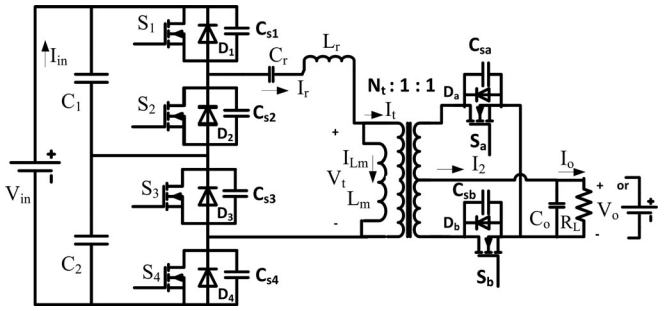

Fig. 1. Proposed LLC resonant converter.

In this topology, they used an extra flying capacitor and auxiliary switches, which make the converter operation complex and increased the cost of the system.

The major contribution of this paper is to propose a modified complete soft switched LLC resonant converter with a simple FAPSM control for a wide voltage gain range applications. This topology is composed of two HB connected in series but sharing the same resonance tank and high-frequency transformer. The series combination of four switches reduces the voltage stress across each switch equal to half of the input voltage. It also used active rectifier in the secondary side of the transformer and becomes the key component of an ESS [16] to enable the bidirectional power flow. The control proposed for this circuit based upon two control variables such as: switching frequency and phase shift angle of the secondary switches. The switching frequency changes with load in such a way that, it is secured ZVS in the primary side for all phase shift angles. Automatically, it maintains the converter gain characteristics identical regardless of load conditions over all phase shift angles. As a result, the proposed converter can be capable of operating at wide gain range with ZVS under all load conditions. On the other hand, the phase shift changes according to input variations only. It can be regulated the output voltage tightly and remains constant under all input voltages. This control overcomes the unity gain problem of conventional DAB LLC resonant converters. It makes that the converter voltage gain is independent of the quality factor Q. Unlike the conventional DAB LLC resonant converter [16], the proposed control increases the gain range and makes the converter best suitable for renewable-energy generation system. In addition, the simultaneous use of two variables also reduces the circulating current (or reactive power) from the secondary bridge, especially at light load conditions. Furthermore, proper design of the inductor ratio (which has no effects on voltage gain) reduces the conduction losses as well as increases the efficiency of the converter.

II. Converter Topology and Operating Principle

The proposed LLC resonant DC/DC converter with the active rectifier for the high and wide input voltage applications is shown in Fig. 1. The switches in both sides are connected in series with an LLC resonant tank and a high-frequency transformer. An extra inductor is used with transformer leakage inductor to get desired circuit operation. The series resonance capacitor C_r absorbs the dc component from the inverted signal,

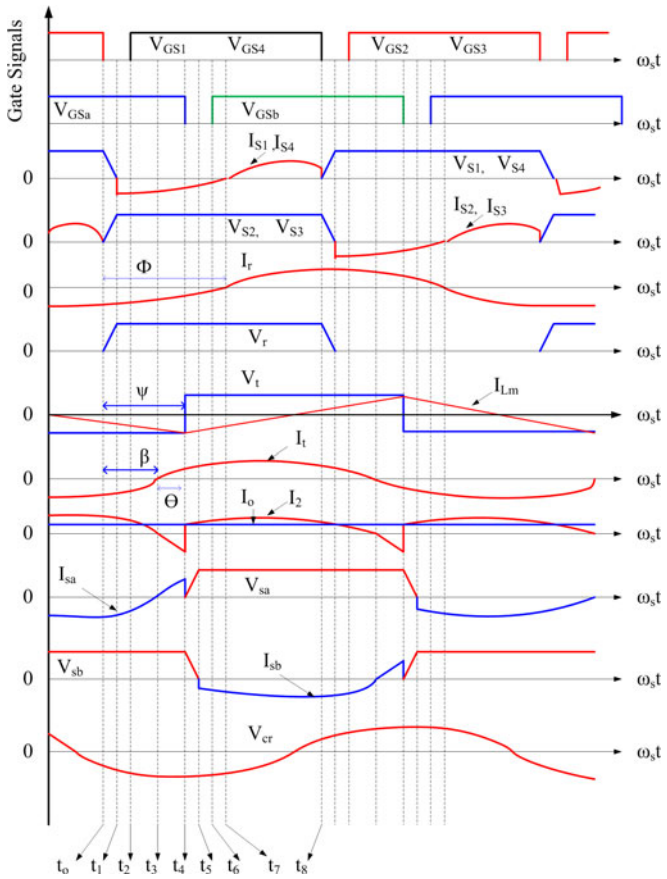

Fig. 2. Key operating waveforms of LLC resonant converter.

which hinders the transformer saturation. The input series capacitors C_1 and C_2 have the same capacitance value, and they used to clamp the primary switch voltage stress to half of the input voltage. The value of output capacitor C_o should be chosen high enough to keep the output voltage free from ripple. The transformer has to be designed in such a way, which keeps the L_m as high as possible to reduce the conduction losses from the system.

Fig. 2 shows the steady-state waveforms of a proposed converter, where all the switches in both primary and secondary side have the constant duty cycle of 0.5.The outer pair of a primary switches S_1 and S_4 share the same gate signals, while the inner pair of switches S_2 and S_3 turns on and off simultaneously. The secondary active rectifier switches S_a and S_b also turns on and off with a constant duty cycle of 0.5.The switching frequency always remains higher than the resonant frequency, thus, the converter operated in the negative slope region.

The phase-shift angle ψ between primary and secondary switches is used to control the power flow and output voltage regulation. If the phase-shift angle is greater than zero, i.e., $\psi > 0$, power flows from the primary side to the secondary side, otherwise (i.e., $\psi < 0$) power flows in the reverse direction. The operation of a proposed converter topology is symmetrical for both forward and backward power flow. So only the forward power flow has been analyzed in this paper. The operation modes of proposed DC/DC LLC resonant converter for each switching cycle are divided into the 16 stages. Only $t_0 - t_8$ is

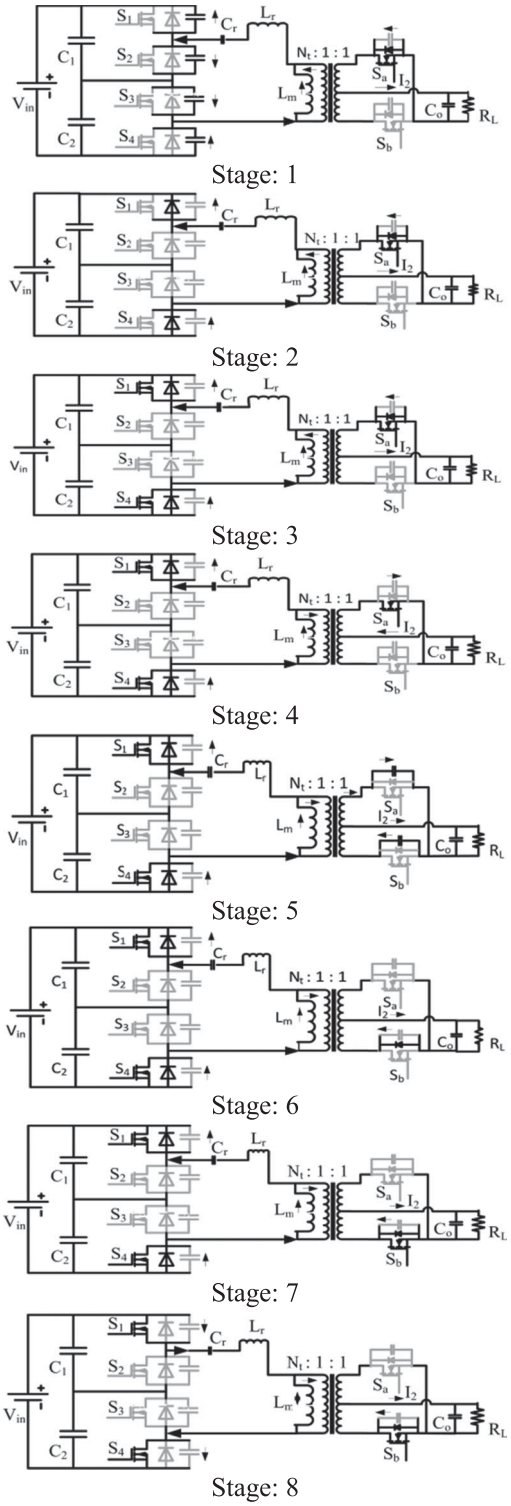

Fig. 3. Equivalent circuits for different time intervals in half of the switching cycle for the forward power flow.

introduced and explained due to the symmetrical nature of every half switching cycle. The corresponding equivalent circuits for half switching cycle are depicted in Fig. 3.

Stage 1 $[t_o - t_1]$: In the beginning of this interval ($t = t_0$), the gate signals across S_2 and S_3 are being removed. Then, the lossless snubbing capacitors C_{s2} and C_{s3} start charging by the resonance current I_r. Accordingly, the voltages V_{s2} and V_{s3} across S_2 and S_3 rise gradually from zero to half of the input voltage. On the other hand, the voltages V_{s1} and V_{s4} across S_1 and S_4 decrease rapidly from $V_{in}/2$ to zero by discharging of C_{s1} and C_{s4}. In this interval, S_2 and S_3 turn off with ZVS transition and the voltage across the resonant tank rises gradually to the V_{in}. This interval lasts until the snubbing capacitors in the primary side switches charged and discharged fully.

Stage 2 $[t_1 - t_2]$: This interval starts when V_{s1} and V_{s4} are forced to be zero at $t = t_1$; then, their antiparallel diodes D_1 and D_4 become in forward biased. Thus, tank power is pumped back into the primary side with a negative resonant current flowing through D_1 and D_4 while the secondary current still flows into the load through D_a. Stage-2 completes as the gating signals of the switch S_1 and S_4 are given.

Stage 3 $[t_2 - t_3]$: The signals for S_1 and S_4 are triggered, while D_1 and D_4 are still conducting. The current I_t and I_2 become zero at the end of this interval. Furthermore, the resonant current flows toward zero; consequently, zero voltage and zero current switching (ZVZCS) turn on can be achieved in S_1 and S_4.

Stage 4 $[t_3 - t_4]$: At t_3, I_t reaches zero and starts increasing toward positive value, while the secondary current flows in reverse direction through S_a. Reactive power (or, reverse power) persists throughout this interval, which increases the conduction losses. This stage ends when the S_a is turned off.

Stage 5 $[t_4 - t_5]$: In the beginning of this stage, the secondary current again flows in positive direction toward the load. The capacitors across S_a and S_b are charging and discharging gradually during this interval. Thus, ZVS turn off can be achieved in the secondary switch S_a. The reflected voltage across the transformer primary side is switched to a positive value, which increases the magnetizing current (I_{Lm}) linearly toward a positive direction.

Stage 6 $[t_5 - t_6]$: This interval begins when V_{sb} is forced to be zero at t_5, then the antiparallel diode D_b becomes in forward biased. This interval ends when the gate signal is applied across the switch S_b.

Stage 7 and *Stage 8* $[t_6 - t_8]$: In this interval switch, S_b turns on with ZVZCS. The resonant current I_r goes toward zero and shifts from diodes to corresponding switches. After the moment, the power is transferred from the primary side to the secondary side through the resonant tank. This interval completes when S_1 and S_4 are turned off.

III. Steady-State Analysis

The power is transferred from input to the load with the aid of resonant tank components, C_r, L_r, and L_m. Hence, the current in the resonant tank nearly sinusoidal as shown in Fig. 2.This allows the use of FHA to analyze the dc characteristic of the converter, which considers that only the fundamental component of the square wave is responsible for transferring the power to the load. Based on the FHA, the ac-equivalent two-port model is derived as shown in Fig. 4. All the inductors, capacitors, diodes, switches, and the high-frequency transformer are assumed to

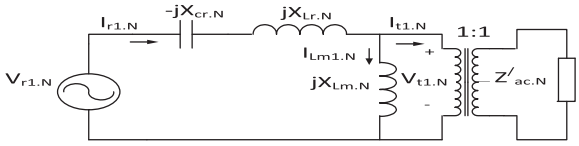

Fig. 4. AC-equivalent circuit of LLC resonant converter.

be ideal in the model. The parameters which are transferred to the primary side are denoted by superscript (/). The following parameters are normalized for the resonance converter:

$$V_{base} = \frac{V_{in}}{2}, Z_{base} = \sqrt{\frac{L_r}{C_r}} = \omega_r L_r = \frac{1}{\omega_r C_r}$$
$$\omega_{base} = \omega_r = \frac{1}{\sqrt{L_r C_r}}; \quad I_{base} = \frac{V_{base}}{Z_{base}} \tag{1}$$

where ω_r is the angular series resonance frequency.

The normalized switching frequency can be defined as

$$F = \frac{\omega_s}{\omega_r} \tag{2}$$

where $\omega_s = 2\pi f_s$ and f_s is the switching frequency.

The normalized reactances of the resonance tank can be expressed as

$$X_{L_r.N} = F; \quad X_{C_r.N} = \frac{1}{F}; X_{L_m.N} = \frac{F}{K} \tag{3}$$

where $K = \frac{L_r}{L_m}$ is defined as inductance ratio.

The current in the secondary side is always in continuous conduction mode in the proposed topology. There is phase difference Θ between the transformer secondary voltage and current as shown in Fig. 2. Thus, the circuit including HF transformer, active rectifier, output filter, and load can be represented by equivalent impedance "$Z'_{ac.N}$"

$$Z'_{ac.N} = \frac{\cos\Theta}{Q} < (-\Theta) \tag{4}$$

where $\Theta = (\psi - \beta)$ is the phase angle of the $Z'_{ac.N}$, and Q is the quality factor which can be expressed as follows:

$$Q = \frac{\pi^2 Z_{base} P_o}{8n^2 V_o^2}. \tag{5}$$

The relationship between the phase angle Θ, controllable phase shift ψ, and switching frequency can be calculated from the ac impedance network given in Fig. 4

$$\Theta = \tan^{-1}\left(\frac{FK + F - K/F}{Q(F^2 - 1)} - \cot\psi\right). \tag{6}$$

The input impedance of the two-port network shown in Fig. 4 can be calculated as follows:

$$Z_{in.N} = |Z_{in.N}| < \Phi$$

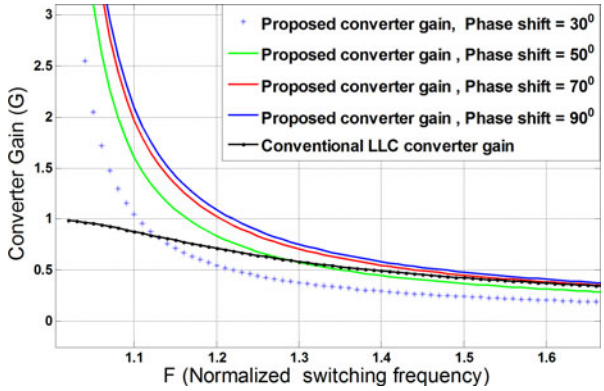

Fig. 5. Plots of voltage gain with regards to normalized switching frequency at K = 0.2, Q = 2.5.

$$\text{where, } \Phi = \tan^{-1}\left[\left(F - \frac{1}{F}\right)\left(\frac{K^2}{QF^2} - \frac{2K\tan\Theta}{F} + \frac{Q}{\cos^2\Theta}\right) + \frac{K}{FQ} - \tan\Theta\right]. \tag{7}$$

It can also be calculated the phase angle β in between $V_{r1.N}$ and $I_{t1.N}$ as follows:

$$\beta = \tan^{-1}\left(\frac{Q(F^2 - 1)\csc^2\psi}{K(F + F/K - 1/F)} - \cot\psi\right). \tag{8}$$

A. Converter Gain

From the equivalent circuit in Fig. 4, the voltage gain can be written as follows:

$$\text{Voltage gain, } G = \left|\frac{V_{t1.N}}{V_{r1.N}}\right|. \tag{9}$$

The voltage gain is simplified as (10) shown at the bottom of this page.

It is seen that, when $\Theta = 0$, the operation of the proposed LLC resonant converter is the same as a conventional LLC resonant converter with diode rectifier and equivalent load can be seen as a resistor [26], [27]. These two voltage gains are drawn in Fig. 5.

It is observed that the voltage gain of conventional LLC converter always remains under unity in the negative slope region at high Q values like 2.5. On the other hand, the gain of the proposed converter can be varied widely in the negative slope region even at high-quality factor. Thus, the proposed converter can be operated at wide input voltages from no load to full load.

B. Reverse Power

The reverse energy exists for the phase difference between transformer voltage and current, which means conduction losses

$$G = \frac{1}{\sqrt{\left\{(1 + K - K/F^2) - \left[\frac{Q(F^2-1)}{F} \times \left(\frac{FK+F-K/F}{Q(F^2-1)} - \cot\psi\right)\right]\right\}^2 + \left\{\frac{Q(F^2-1)}{F}\right\}^2}} \tag{10}$$

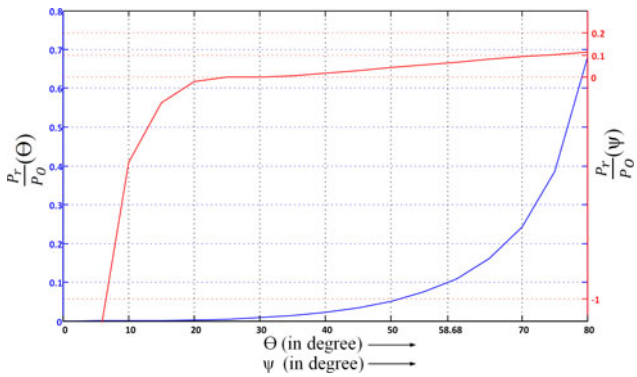

Fig. 6. Plots of power ratio with regards to Θ and ψ (K = 0.1, F = 1.11, Q = 2.5).

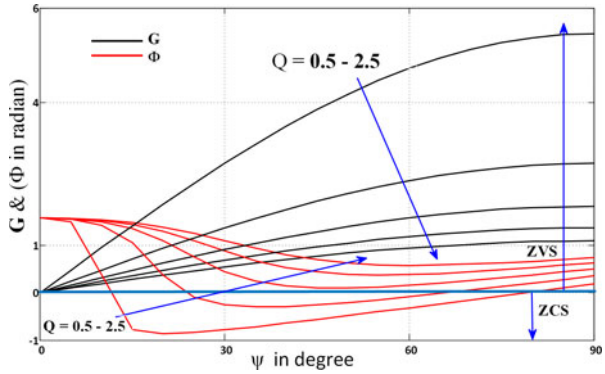

Fig. 7. Plots of Φ and **G** with regards to ψ for the fixed switching frequency (F = 1.2) and K (K = 0.6).

will be increased due to the part of the energy is transferred back and forth between output and input side. It will be high at minimum input voltage condition. The minimum input voltage has to be limited due to a large amount of reactive power in the system. To simplify the calculation, the reverse energy per unit time can be represented by the reactive power. The ratio of reverse power to the output power is given in (11), which is also shown in Fig. 6, [13], [17], [28]

$$\begin{cases} \frac{P_r}{P_O} = \frac{1}{2\pi}\tan\Theta - \frac{\Theta}{2\pi} \\ \frac{P_r}{P_O} = \frac{\left(\frac{FK+F-K/F}{Q\left(F^2-1\right)} - \cot\psi\right)}{2\pi} - \frac{\tan^{-1}\left(\frac{FK+F-K/F}{Q\left(F^2-1\right)} - \cot\psi\right)}{2\pi} \end{cases} . \quad (11)$$

From the Fig. 6, it is seen that reverse power becomes large at the high value of phase shift angle (i.e., minimum input voltage condition). With the proposed control technique, it does not depend on load and also limits the maximum voltage gain. In order to minimize conduction losses, reactive power should be low as possible.

IV. Parameter Design and ZVS Analysis

The designed is focused on ensuring constant output voltage with high and wide input voltage variation for all load conditions. The prime issues of the design objectives are to increase the gain range and maintain ZVS operation from no load to full load.

Design specifications:

1. Input voltage, $V_{in} = 200 - 400\,V$.
2. Output voltage, $V_o = 48\,V$.
3. Output power, $P_o = 1\,Kw$.

A. Selection of Q and ZVS in the Primary Side Switches

In order to secure the ZVS, the phase angle (Φ) of the input impedance should be positive (i.e., $\Phi > 0$). It can be expressed by (7) as

$$\tan^{-1}\left[\left(F - \frac{1}{F}\right)\left(\frac{K^2}{QF^2} - \frac{2K\tan\Theta}{F} + \frac{Q}{\cos^2\Theta}\right) + \frac{K}{FQ} - \tan\Theta\right] > 0. \quad (12)$$

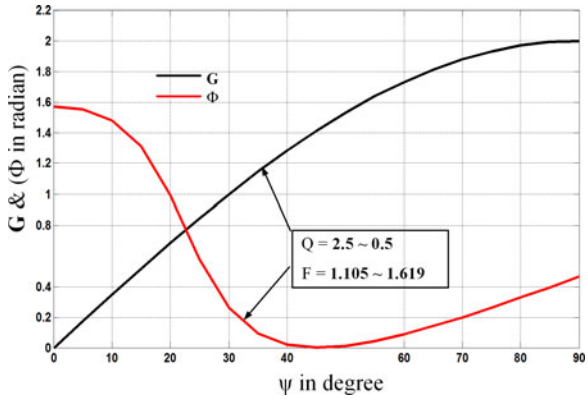

Fig. 8. Plots of Φ and **G** with regards to ψ at different Q and F values, respectively.

After some manipulation, (12) can be expressed as

$$\frac{\pi^2 Z_{base} P_o}{8\,n^2 V_o^2}\left(F - \frac{1}{F}\right) > \frac{\sin(2\psi)}{2}. \quad (13)$$

To satisfy the requirements of ZVS in the primary side, solving (13) at the extreme condition (i.e., $\psi = 45°$) yields to

$$\left(F - \frac{1}{F}\right) > \frac{4\,n^2 V_o^2}{(\pi^2 Z_{base} P_o)}. \quad (14)$$

In Fig. 7, describes the variations of Φ and G with respect to ψ for different Q values. It is seen that Φ goes to the negative value when the gain more than unity at light load conditions. So, it can be assumed that ZVS will be lost in the primary side switches if **G** is larger than one.

A new control technique has been introduced in proposed converter to overcome the aforementioned drawback. According to (14), the frequency will be selected sequentially with the load changes. Fig. 8 describes the variations of Φ and **G**, as compared to both phase shift angle and switching frequency for different Q values. In this technique, f_s increases with decreasing load, i.e., f_s changes until the Φ becomes positive for all ψ variations. It is also confirmed from the Fig. 8 that the frequency selection minimized the effect of Q values on converter voltage gain (G), i.e., the converter gain becomes independent on load conditions.

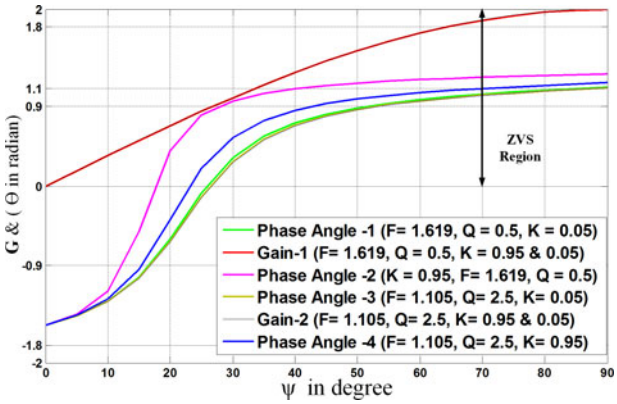

Fig. 9. Plots of Θ and **G** with respect to Phase-shift ψ at different Q, F, and K values, respectively.

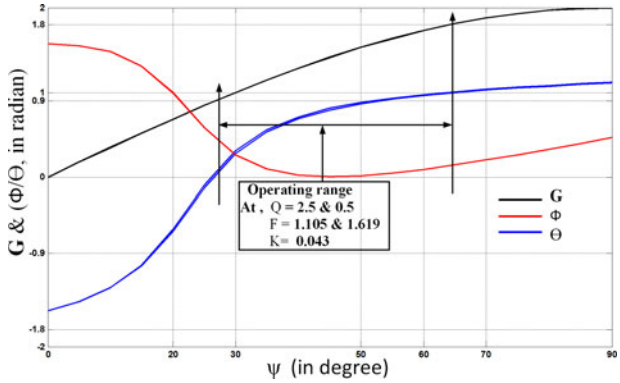

Fig. 10. Plots of Φ, Θ, and **G** with regards to ψ.

But Q (full load) should be low as possible to have small inductive reactive components. Moreover, the operating frequency range will be higher under all loads due to the selection of small Q (full load) value. So, based on the aforesaid discussion, Q = 2.5 at full load has been selected.

B. Gain Selection

Based on the full load Q value, it is seen from Fig. 8, that the maximum gain is limited to 2. The maximum gain also depends on the allowable reactive power in the converter circuit. Fig. 9 describes the relationship between Θ and **G** for different Q and F values. It is seen that Θ increases with **G** and in a particular **G** value, Θ becomes maximum at light load conditions (i.e., at low Q values). To allow maximum 10% reverse energy for every load condition, the value of Θ (in degree) is limited to 58.68° as mentioned in (11). Thus, maximum voltage gain $(M_{\max})$ is chosen for this converter to minimize the reactive power from the system as

$$M_{\max} = 1.8. \tag{15}$$

So, the transformer turn's ratio is calculated as follows:

$$\mathrm{n} = \frac{\mathrm{N_p}}{\mathrm{N_s}} = \frac{\mathrm{M_{max}.V_{in-min}}/2}{\mathrm{V_o}} = 15:4. \tag{16}$$

The minimum voltage gain is obtained as

$$\mathrm{M_{min}} = \frac{\mathrm{n.V_o}}{\mathrm{V_{in-max}}/2} = 0.9. \tag{17}$$

C. Selection of K and ZVS in the Secondary Side Switches

In the proposed converter, the inductor ratio K has no effects on the gain. Although K increases the range of ZVS on the secondary switches. To maintain the ZVS in the secondary side, Θ should be positive. From (10), it can be written as

$$\begin{cases} \Theta = \tan^{-1}\left(\frac{\mathrm{B}}{\mathrm{A}} - \sqrt{\frac{1}{\mathrm{A^2G^2}} - 1}\right) \\ \text{where } \mathrm{A} = \frac{\mathrm{Q}\left(\mathrm{F^2}-1\right)}{\mathrm{F}}; \mathrm{B} = 1 + \mathrm{K} - \mathrm{K}/\mathrm{F^2} \end{cases}. \tag{18}$$

If Θ is positive, (18) can be further simplified as follows:

$$\mathrm{K} > \left| \frac{\left[\mathrm{A}.\left(\sqrt{\frac{1}{\mathrm{A^2G^2}} - 1}\right) - 1\right]}{1 - \frac{1}{\mathrm{F^2}}} \right|. \tag{19}$$

According to the proposed control system, the switching frequency increases with decreasing load, and it will be high at no load. Thus, based on this fact, the inductor ratio K has to be calculated. The inductor ratio K at extreme condition like Q = 2.5 (i.e., full load) with $M_{\min} = 0.9$ and F = 1.105 (from (14)), calculated as

$$\mathrm{K} > 0.0429. \tag{20}$$

It can be confirmed from Fig. 9, the gain of the converter is unaffected by the inductor ratio K. It is observed that a small $\mathrm{L_m}$ (i.e., large K) is useful to extend the ZVS range on the secondary side. But with large K value, the reverse energy will be more due to the high value of Θ especially at light load condition. This reverse energy will increase the conduction losses, which are responsible for reducing the system efficiency. Thus, the choice of high K value is not reasonable, otherwise efficiency will be degraded. So K = 0.043 has to be selected in this system to reduce excessive reverse energy as well as to get suitable gain with ZVS.

With K = 0.043, the relationship among Φ, Θ, and G with regards to ψ for different Q and F values have been plotted in Fig. 10. It can be confirmed that Φ and Θ are always positive for the whole operating voltage gain range, i.e., ZVS transition on the both primary and secondary side switches is maintained when **G** is between 0.9 and 1.8. It is also confirmed that the value of Θ at the maximum gain point is equal to 57.29° (1 in radian), which indicates that the ratio between the reactive power to output power remains within 10% for all phase shift angles according to the desired gain range.

Finally, with the help of (1)–(3), (5) resonant tank elements are calculated as follows:

$$\mathrm{L_r} = \frac{8\mathrm{QR_L n^2}}{\pi^2 \omega_\mathrm{r}} \tag{21}$$

$$\mathrm{C_r} = \frac{\pi^2}{8\mathrm{QR_L}\omega_\mathrm{r}\mathrm{n^2}} \tag{22}$$

TABLE I
SPECIFICATIONS OF THE DESIGNED CONVERTER

Parameter - Symbol	Value – unit
Input voltage, V_{in}	200–400 V
Output voltage, V_o	48 V
Resonant Inductor, L_r	241.58 μH
Resonant Capacitor, C_r	55.93 nF
Parallel Inductor, L_m	5.61 mH
Rated load Resistance (full load)	2.304 Ω
Rated output power, P_o	1 kw

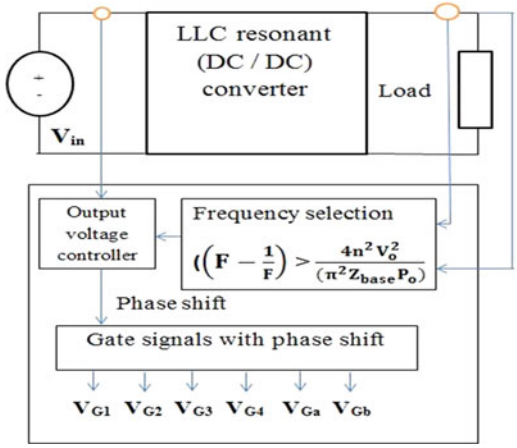

Fig. 11. Simplified block diagram of the proposed FAPSM control.

$$L_m = \frac{L_r}{K}. \tag{23}$$

The design specifications of the proposed converter are summarized in Table I.

V. CONTROL SCHEME

Switching frequency has to be selected in every load condition to ensure the ZVS in the primary side switches. This frequency selection minimized the effect of loaded Q values and kept the converter voltage gain characteristics identical for every phase shifted angle. Later, the phase shift angle (ψ) can be regulated the output voltage to the desired one with regards to input voltages. The method used to obtain such a signal is shown in Fig. 11.

The control law has been implemented on DSP TMS320F28335 from TI. The DSP samples the inputs by its A/D input and controls the switching frequency (f_s) and phase shift by simply changing the register values. Thus, the output can be regulated to the desired value based on the flowchart shown in Fig. 12.

VI. COMPARISON OF CONVERTER TOPOLOGIES

A comparison of five topologies is illustrated in Table II.

VII. SIMULATION AND EXPERIMENT RESULTS

To verify the analytical result, the proposed converter has been simulated in MATLAB. The simulation is carried out under

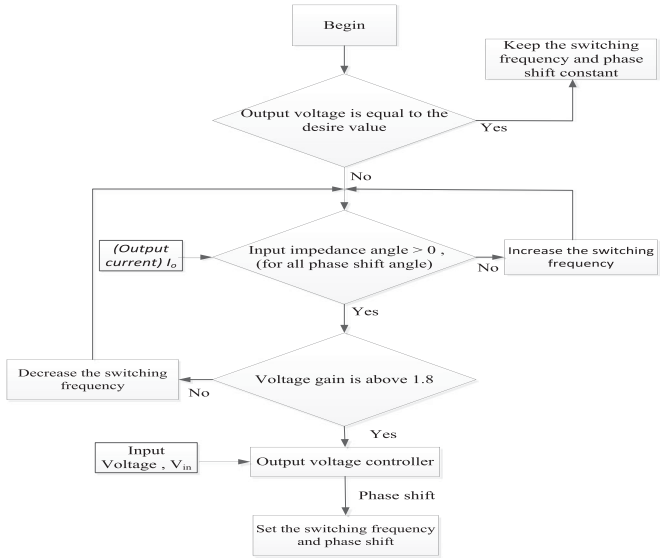

Fig. 12. Output voltage regulation using the proposed control scheme.

maximum and minimum input voltage with the full load and 20% load conditions. Fig. 13(a)–(d) shows the V_r, I_r, V_t, I_t, V_{cr}, and I_2 over different inputs and load conditions. Operating frequency changes as the load only and remains constant for the fixed load regardless of input voltages. To remain the output voltage constant, ψ changes with input variations irrespective of load conditions. It is seen that Θ becomes higher at low input voltage, which increases the reverse power as well as decreases the efficiency. Therefore, for the same output power, I_2 shows the more negative percentage at 200 V than 400 V input. It is also observed that all the stresses across the resonant tank become higher at low-input voltage condition. ZVS can be verified by evaluating the phase angles of I_r and I_t with respect to V_r and V_t, respectively.

A prototype converter has been built and tested in the lab to verify the proposed method. The resonant frequency can be chosen high to reduce the parasitic effects in the circuit. N95 material based ferrite core (PQ $50/50$) has been used to build the HF transformer. With the proper design, the resulted magnetizing inductance has been set to 5.61 mH. This high value of magnetizing inductance reduces the conduction loss of the transformer. HEXFET MOSFET IRFR-4620PbF and MOSFET IPP200N15N3G are adopted as the primary and secondary switches, respectively. The experimental waveforms of a proposed converter are shown in Fig. 14(a)–(f). Most of the results have similarities with simulation and theoretical calculations. As shown in Fig. 14(e), soft switching can be achieved in primary and secondary side switches. Since ZVZCS is observed on both sides during turn-on, thus the high-frequency turn-on switching losses become negligible. There are no considerable voltage spikes across the switch voltage (V_{ds}), which signifies the ZVS turn-off transition. The switch current commutates to the lossless snubbing capacitor instead of the switch itself and the MOSFET becomes switched off fully before the drain to source voltage rises significantly above zero. Due to ZVS, turn-off transition switching losses are reduced to the very small value. It is

TABLE II
COMPARISON OF RESONANT CONVERTER TOPOLOGIES

Topologies	DBSR LLC converter [16]	DAB LLC converter with new control scheme [17]	Three level LLC resonant converter with PWAM control [18]	DBSR LLC converter with phase shift Control [29]	Proposed LLC resonant converter with FAPSM
Number of switches	8	8	12	4	6
Voltage stress across the switches is equal to half of the input voltage (for all load and voltage gain)	No (Equal to the input voltage)	No (Equal to the input voltage)	No (Depends on the voltage gain)	No (Equal to the input voltage)	Half of the input voltage
Number of transformer's secondary windings	1	1	1	2	2
ZVS	Primary bridge: ZVS Secondary bridge: ZCS	Primary bridge: ZVS Secondary bridge: ZCS	Primary side: ZVS Secondary bridge: ZCS	Primary side: ZVS Secondary bridge: ZVS	Primary side: ZVS Secondary bridge: ZVS
Reactive power control	No	Yes	No	No	Yes
Flying capacitor	No	No	Yes	No	No
Modulation	PSM	FFPWM	PWAM	PSM	FAPSM
Gain range	Unity gain	Narrow	Wide	Unity gain only	Wide
Input range	110 V	75–130 V	240–480 V	200 V	200–400 V
Full-load measured efficiency	95%	96%	96%	94%	96.4%
Output Power	100 V/2 A	400 V/2.5 A	60 V/20 A	48 V/6.25 A	48 V/20.83 A

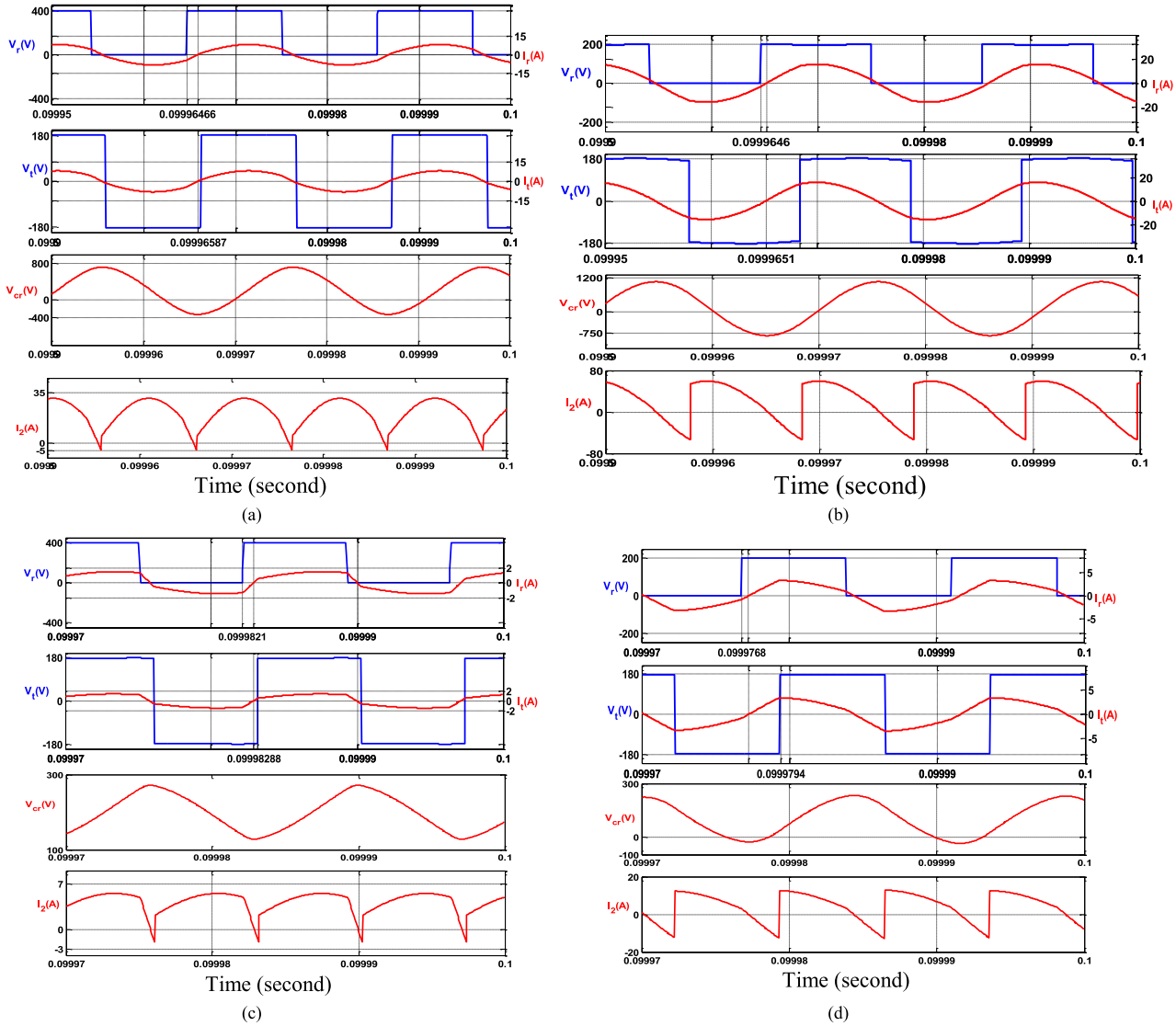

Fig. 13. (a) Simulation waveforms of proposed converter under 400-V input, 48-V output, and full load condition. (b) Simulation waveforms of proposed converter under 200-V input, 48-V output, and full load condition. (c) Simulation waveforms of proposed converter under 400-V input, 48-V output, and 20% load condition. (d) Simulation waveforms of proposed converter under 200-V input, 48-V output, and 20% load condition.

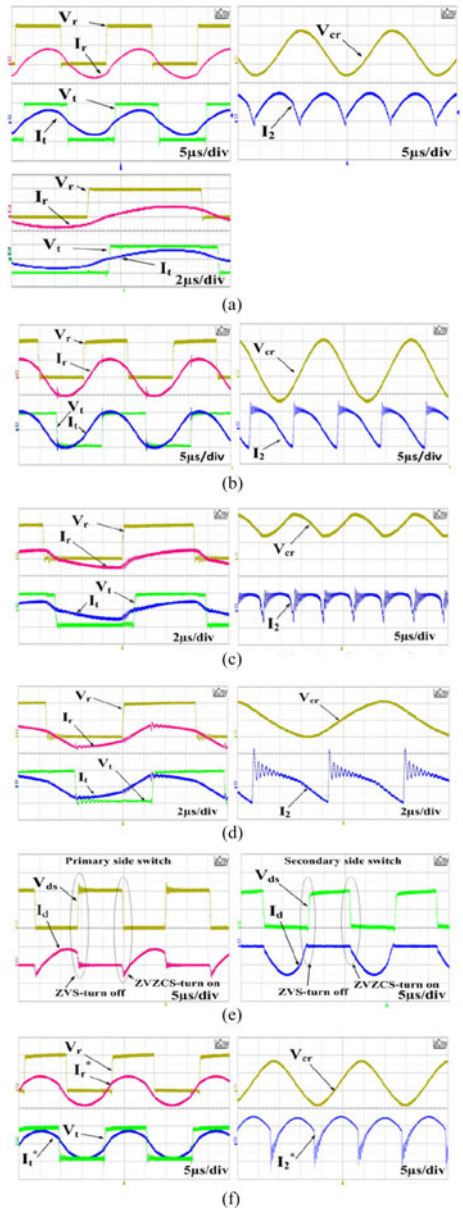

Fig. 14. (a) Experimental waveforms under 400-V input, 48-V output, and full load condition [V_r (200 V/div), I_r (10 A/div), V_t (200 V/div), I_t (10 A/div), V_{cr} (400 V/div), I_2 (20 A/div)]. (b) Experimental waveforms under 200-V input, 48-V output, and full load condition [V_r (100 V/div), I_r (15 A/div), V_t (200 V/div), I_t (15 A/div), V_{cr} (500 V/div), I_2 (50 A/div)]. (c) Experimental waveforms under 400-V input, 48-V output, and 20% load condition (V_r (200 V/div), I_r (3 A/div), V_t (200 V/div), I_t (3 A/div), V_{cr} (100 V/div), I_2 (5 A/div)). (d) Experimental waveforms under 200-V input, 48-V output, and 20% load condition [V_r (100 V/div), I_r (4 A/div), V_t (200 V/div), I_t (4 A/div), V_{cr} (100 V/div), I_2 (12 A/div)]. (e) Switching waveforms of Primary side switch (V_{ds} (100 V/div), I_d (10 A/div)) and Secondary side switch (V_{ds} (50 V/div), I_d (20 A/div)) at 400-V, full load condition. (f) Experimental waveforms of reverse power flow at 48-V input, 400-V output, full load condition [$I_r^* = -I_r, I_t^* = -I_t, I_2^* = -I_2$) ($V_r$ (200 V/div), I_r^* (10 A/ div), V_t (200 V/div), I_t^* (10 A/div), V_{cr} (400 V/div), I_2^* (20 A/div)].

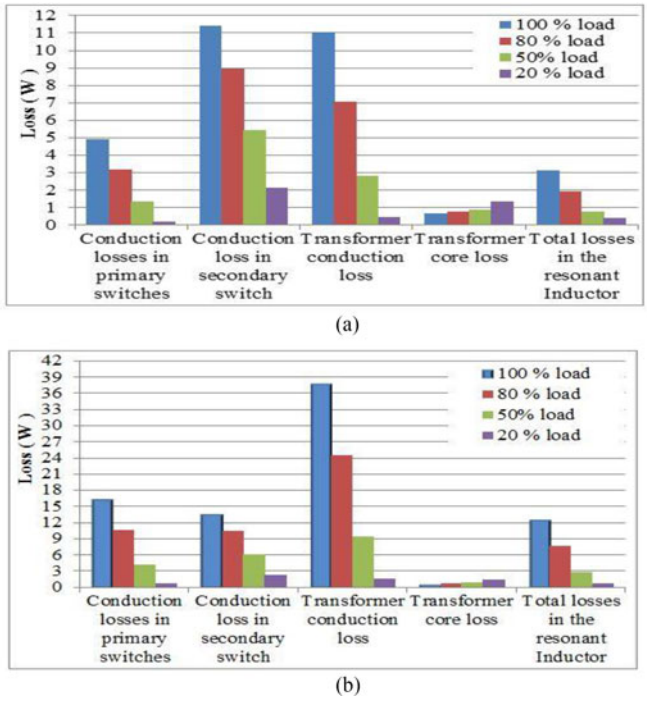

Fig. 15. Loss breakdown for (a) 400-V input and (b) 200-V input

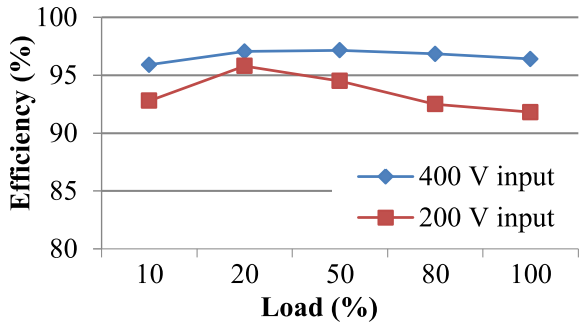

Fig. 16. Measured efficiency of the proposed LLC resonant converter.

also seen that the voltage stress of the primary switches is about 200 V, which is half of the input voltage. As a result, the low voltage rated MOSFET with low R_{dson} is employed to reduce the conduction losses.

For the reverse power flow, the control variable ψ should be negative. Fig. 14(f) shows the waveforms of V_r, I_r^* ($I_r = -I_r^*$), V_t, I_t^* ($I_t = -I_t^*$), V_{cr}, and $I_2{}^*$ ($I_2 = -I_2^*$) for the $\psi = -29.5^0$. ZVS operation can be confirmed by checking the phase angle of I_r^* and I_t^* with respect to V_r and V_t.

Fig. 15 represents the estimated power loss breakdown for different inputs and load conditions. It can be seen that conduction losses are the largest proportion of the total power loss. It is also seen that conduction losses are increased at the low-input voltage condition. The efficiency of the converter under 400 and 200 V on different load conditions is shown in Fig. 16. As it can be seen, the efficiency becomes higher all over the load range at 400 V due to the low value of circulating current in the secondary side. But efficiency degraded at 200 V as compared to 400 V because of higher circulating current (or reactive power) still exists on the secondary side. Calculated efficiency is slightly more than the measured value. However, the variation of efficiency from no load to full load for maximum input voltage is narrow.

To validate the steady-state analysis, a comparison of all important angles obtained from theoretical calculations,

TABLE III
COMPARISON OF DIFFERENT ANGLES

		ψ °	Φ °	Θ °
400 V, full load condition	Theoretical	27.5	22.99	5.39
	Simulation	27.5	21.12	5.71
	Experimental	29.5	24.2	6.1
400 V, 20% load condition	Theoretical	27.5	23.13	7.38
	Simulation	27.5	20.79	7.1
	Experimental	29.5	23.68	7.5
200 V, full load condition	Theoretical	65	8.12	57.16
	Simulation	65	8.61	55.12
	Experimental	68	12.2	58.3
200 V, 20% load condition	Theoretical	65	8.03	57.74
	Simulation	65	11.31	54.53
	Experimental	68	12.1	58.4

simulations, and experiments are given in Table III. All the results are almost close to each other and also all angles follow the increasing and decreasing trend according to phase shift angle.

VIII. CONCLUSION

In this paper, a variable frequency phase shift modulation control for a DAB LLC resonant converter has been incorporated. This control strategy makes the converter operating at a wide gain range with ZVS over all load conditions. The combination of two HB connected in series on the inverter side reduces the voltage stress across each switch, which also makes the converter capable of operating at high-voltage applications. The voltage stresses remain half of the input voltage over all load variations. With the proposed control, the voltage gain becomes independent of Q and K values. Thus, the process of parameter design can be simplified. The magnetizing inductance has been calculated as high to reduce the conduction loss. It also reduced the circulating current (or reactive power) from the secondary side even at light load condition, which increased the efficiency as compared to conventional DAB LLC resonant converter. The performance of the proposed LLC resonant converter is experimentally verified with 200–400-V input and 48-V output converter prototype. Therefore, the proposed converter becomes a good candidate for variable input and constant output voltage applications.

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