Triple Phase Shift Control of an LLL Tank Based Bidirectional Dual Active Bridge Converter

Shiva S. Muthuraj, *Student Member, IEEE*, V. K. Kanakesh, Pritam Das, *Senior Member, IEEE*, and Sanjib Kumar Panda, *Senior Member, IEEE*

***Abstract*—Isolated bidirectional dc–dc converters (IBDCs) with high efficiency and high power density demand for complete zero voltage switching (ZVS) of all active devices for its entire operating range. This paper presents a comprehensive analysis and optimization problem formulation of a triple phase shift (TPS)-controlled inductive link based voltage fed-dual active bridge (VF-DAB) converter. Limitation on natural ZVS range for the TPS-controlled inductive link based VF-DAB is presented. To extend the ZVS range in a TPS-controlled VF-DAB converter, passive auxiliary inductors are connected in parallel (LLL tank) to the primary and secondary sides of the high-frequency transformer. Analysis and subsequent numerical solutions for the TPS-controlled VF-DAB with auxiliary inductors show complete ZVS of all the MOSFETs for the entire operating range. Experimental results confirm complete ZVS of all MOSFETs under various voltage gains and load conditions. A comparative loss breakdown for the TPS-controlled LLL tank VF-DAB and the conventional inductive link VF-DAB at various operating conditions show the necessity of the additional auxiliary inductors in the conventional design for increasing optimal switching frequency of the IBDC.**

***Index Terms*—High-frequency (HF) transformer, isolated bidirectional dc–dc converter (IBDC), triple phase shift (TPS), voltage fed-dual active bridge (VF-DAB), zero voltage switching (ZVS).**

I. Introduction

THE research in the area of dual active bridge (DAB) based isolated bidirectional dc/dc converter (IBDC) has gained momentum in recent years due to the advancements in the fields of electrified transportation, integration of energy storage (ES) elements due to the intermittent nature of the distributed renewable energy generation, and other applications. The main focus of the research has been to achieve high power density, higher efficiency, superior dynamic performance, and improved reliability of the DAB converters [1]–[4]. Various forms of DABs are presented in the literature and are mainly classified based on the filter network, active switching network, and high-frequency (HF) reactive network [1], [2].

Manuscript received July 27, 2016; revised October 17, 2016; accepted November 28, 2016. Date of publication December 8, 2016; date of current version May 9, 2017. Recommended for publication by Associate Editor J. Biela.

The authors are with the Department of Electrical and Computer Engineering, National University of Singapore, 117583, Singapore (e-mail: a0103321@u.nus.edu; kanakesh.vk@bears-berkeley.sg; eleprdas@nus.edu.sg; eleskp@nus.edu.sg).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2637506

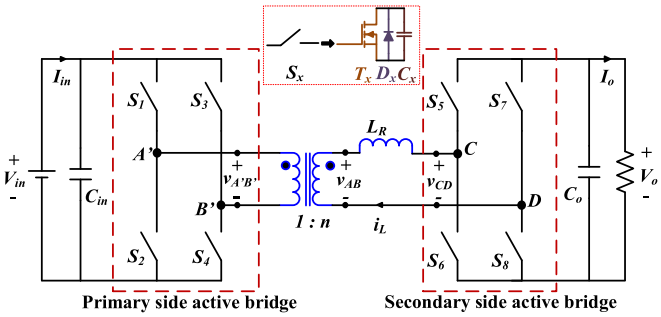

Fig. 1. Voltage fed-dual active bridge (VF-DAB) converter topology.

The dual active full bridge (DAFB) converter with an inductive-type reactive tank as shown in Fig. 1 has now become the most popular DAB-based IBDC for medium-voltage and low-voltage applications due to its additional control freedom and symmetric control on bidirectional power flow. The control strategy for the DAFB-based IBDC with the inductive-type reactive tank to improve the soft switching range and reduce the circulating current in the converter is one of the important research directions for this topology. The full bridge configuration can achieve three levels of pole voltages depending upon the switching states. The dual full bridge configuration with 50% duty on each switch and constant switching frequency offers three degrees of freedom to control power transferred by the converter as follows:

1) φ, the phase shift between the pole voltages of the two active bridges where $-\pi < \varphi < \pi$ in radians;
2) D_1, the duty ratio of the primary bridge pole voltage $v_{A'B'}$ where $0 < D_1 < 1$;
3) D_2, the duty ratio of the secondary bridge pole voltage v_{CD} where $0 < D_2 < 1$.

D_1 and D_2 represent intrabridge phase shift and can be varied by controlling the phase shift between the two legs of its corresponding active bridges. φ represents interbridge phase shift.

Single phase-shift (SPS) control based modulation which uses only one degree of control freedom is the most conventional modulation scheme for DAB [5]–[9]. The bidirectional power transfer in the SPS control is achieved by adjusting the phase-shift φ between pole voltages of the active bridges while keeping D_1 and D_2 as 1. However, SPS-controlled DAB suffers from drawbacks due to loss of soft switching and high circulating currents for wide variations in the terminal voltages and load. The drawbacks of the SPS control are severe, especially when

the voltage conversion ratio is not close to the turns ratio of the transformer [9].

An improved form of SPS is the extended phase-shift (EPS) control which is discussed in [10]–[14]. EPS control adds an extra degree of freedom to the SPS control by creating phase shift between the legs of the same bridge in any one of the two active bridges resulting in greater flexibility (two degrees of freedom which is either D_1 or D_2 and φ). Similar to the EPS control, the dual phase shift (DPS) control [15]–[19] also has two degrees of control freedom. In DPS control, the intraphase shift within the active bridges D_1 and D_2 is controlled and is kept the same ($D_1 = D_2$). Compared to the SPS control, EPS- and DPS-controlled DAFBs reduce the current stress, increase the zero voltage switching (ZVS) range, and minimize the filter capacitance.

Triple-phase-shift (TPS) control [3], [20]–[27] operates with three degrees of freedom in control (D_1, D_2, and φ). In [20], TPS control based triangular and trapezoidal modulation schemes have been discussed for obtaining the least transformer rms current at various operating conditions of the converter. But the modulation scheme suffers from losses incurred in the active devices due to zero current switching (ZCS). In [24], a composite scheme combining EPS and TPS control is proposed, which provides ZVS even for light load conditions with reduced rms current.

Even with TPS control, complete ZVS conditions for the entire operating conditions cannot be achieved by the fixed frequency modulation scheme in the DAB converter [3], [30]. The ZVS limitations of a DAB are most generally defined for any modulation strategy and ac link impedance network in [30]. Typically, partial or complete loss of ZVS occurs in a TPS DAB under the following operating conditions:

1) at light loads when the ratio of input dc voltage $V_{\rm in}$ to the output voltage V_o is almost the same as the transformer primary to secondary turns ratio $(1:\ n)$;
2) at mid loads when the input to output voltage ratio deviates away from the transformer turns ratio;
3) at high load conditions as the difference between the input to output voltage ratio and the turns ratio becomes very high; and
4) during look-up-table based closed loop implementation with off-line optimized control parameters which is another key aspect of the TPS-controlled DAB converter. The DAB is typically controlled using a look-up-table followed by feed-back control for adjusting the errors in the actual output power transfer and the desired output power. Based on $V_{\rm in}$, V_o, and power transfer (P_o), the corresponding optimal duty ratios are stored in the look-up-table memory for discrete operating conditions and new data points are constructed by interpolation for operating conditions which are not available in the look-up-table. Sensors are deployed for sensing the actual values of some of the parameters from the actual converter and quiescent values of the duty ratios are generated using the sensed values and stored data in the look-up table. There can be significant errors in the actual duty ratios fed to the converter due to errors in the sensed parameters and this can also lead to loss of ZVS in the converter.

The above-mentioned phenomena are explained in details in the subsequent sections. These drawbacks prevent the optimal switching frequency of the TPS DAB converter to be very high, typically restricting the switching frequency for such converters to 200 kHz or less [1]–[3], [25]–[29].

In [31], a single commutation inductor derived from the magnetizing inductance of the HF transformer is used to achieve complete ZVS of all the active devices. However, this requires the converter to operate at modes where one of the two bridges achieves ZVS by the main series inductor. This results in a requirement of high peak currents through the magnetizing inductor to achieve complete ZVS in the other active bridge. Also either optimal control parameters or the tank currents during the switching instances undergo an abrupt transition during mode transfer resulting in unwanted dynamics in the converter. A TPS-controlled single stage ac–dc DAB proposed in [32] and [33] achieves complete ZVS of all the MOSFETs with the addition of two parallel commutation inductors. However, the ratio of output voltage to input voltage is less than the transformer turns ratio (n) for the converter specifications chosen in [32] and [33], i.e., $m(=\ nV_{\rm in}/V_o) < 1$. It is a well-known fact that for most DAB applications, operating around $m = 1$ is preferred since it results in reduced peak currents [35].

It is a well-known fact that for most DAB applications, operating around $m = 1$ is preferred since it results in reduced peak currents [35].

This paper addresses the major drawbacks of TPS-controlled voltage fed (VF)-DAB with conventional inductive link based HF tank by the addition of auxiliary inductors in the HF tank design. A detailed design and analysis of the TPS-controlled LLL tank based DAB along with loss breakdown at various operating conditions of the converter is also presented. The analysis has been simulated and validated by experimental results.

This paper is organized as follows. The steady-state analysis of the TPS DAB along with the various modes of operation with respect to interbridge and intrabridge phase shifts is presented in Section II. An extensive optimization of a specific TPS-controlled VF-DAB is presented in Section III followed by some important generalized conclusions regarding the natural ZVS range and limitations of TPS DAB. Based on these analysis and conclusions, the design procedures for LLL tank based TPS DAB are discussed to improve the performance of conventional TPS DAB in Section IV. The experimental results of the TPS-DAB with LLL tank are presented in Section V to validate the claims. Comparative loss analysis of the TPS-controlled conventional inductive tank and LLL tank at various modes of operation is analyzed in Section VI. A brief performance comparison of the LLL tank based TPS-DAB with SPS, DPS, and TPS modulations for the conventional inductive link based DAB is presented in Section VII followed by the conclusion presented in Section VIII.

II. Steady-State Operation and Analysis of Triple-Phase Shift Controlled VF-DAB

The modes of operation of the converter for different interbridge and intrabridge phase shifts are discussed in this section. Mathematical equations for important instantaneous

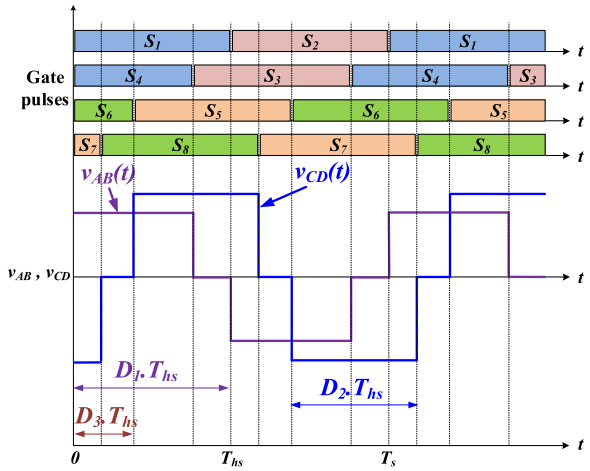

Fig. 2. Gating pulses and high-frequency ac bridge voltages of TPS-controlled DAB.

and rms values of currents and power transfer during each of these modes of operation are presented in this section. For the ease of analysis, the ripples in both the voltage ports are neglected in the entire paper and the converter is assumed to be lossless. The current in the lumped inductor L_R is positive when it flows from nodes *A* and *C*. These mathematical equations are also used for the optimization problem formulation presented in the paper so as to reduce the circulating currents and maximize the soft switching range.

In TPS modulation scheme, the phase shift is not just created between the two active bridges, but also within the legs of both the active bridges. This results in three possible levels for the HF ac output voltages from the primary side bridge reflected on the secondary side which is $v_{AB}(t)(= n \times v_{A'B'}(t))$ and secondary side bridge which is $v_{CD}(t)$ as shown in Fig. 1.

The three different voltage levels are possible for $v_{AB}(t)$ and $v_{CD}(t)$ are as follows:

$$v_{AB}(t) = \begin{cases} n \cdot V_{\text{in}} & \text{when } S_1, S_4 \text{ on; } S_2, S_3 \text{ off;} \\ & \text{when } S_1, S_3 \text{ on; } S_2, S_4 \text{ off;} \\ 0 & \text{when } S_2, S_4 \text{ on; } S_1, S_3 \text{ off;} \\ -n \cdot V_{\text{in}} & \text{when } S_2, S_3 \text{ on; } S_1, S_4 \text{ off;} \end{cases} \quad (1)$$

$$v_{CD}(t) = \begin{cases} V_0 & \text{when } S_5, S_8 \text{ on; } S_6, S_7 \text{ off;} \\ & \text{when } S_5, S_7 \text{ on; } S_6, S_8 \text{ off;} \\ 0 & \text{when } S_6, S_8 \text{ on; } S_5, S_7 \text{ off;} \\ -V_0 & \text{when } S_6, S_7 \text{ on; } S_5, S_8 \text{ off.} \end{cases} \quad (2)$$

The resulting voltage across the series inductor $v_L(t)$ is given by (1)

$$v_L(t) = v_{AB}(t) - v_{CD}(t). \quad (3)$$

D_1 corresponds to the duty ratio of primary side bridge voltage $v_{A'B'}(t)$ and D_2 corresponds to the duty of secondary side bridge voltage $v_{CD}(t)$ shown in Fig. 2.

D_1 and D_2 can vary between 0 and 1 based on the inner phase shifts between the two legs of the primary and secondary bridges, respectively, and $D_3 T_S$ indicates the duration between the rising edges of the voltages $v_{AB}(t)$ and $v_{CD}(t)$, respectively, as shown in Fig. 2 where $T_s(= 2 \times T_{\text{hs}})$ represents the time period of the switching frequency.

Based on the rising and falling edges of $v_{AB}(t)$ and $v_{CD}(t)$, the outer phase shift, which is the actual phase shift between the two bridge voltages D_φ, is defined by the following relation of the duty ratios:

$$D_\varphi = \frac{\varphi}{\pi} = D_3 + \frac{(D_2 - D_1)}{2}. \quad (4)$$

Note that D_1 and D_2 are the intrabridge duty ratios and D_φ is the interbridge duty ratio.

In order to find the most optimal duties (D_1, D_2, and D_φ) of operation for achieving least transformer rms current with ZVS constraints on all the active devices based on input voltage V_{in}, V_o, and P, generalized sets of equations are required based on the rising and falling edges of $v_{AB}(t)$ and $v_{CD}(t)$. The relative occurrence of the rising and falling edges of $v_{AB}(t)$ and $v_{CD}(t)$ defines different modes of operation of the TPS DAB.

A. Modes of Operation

Based on different sequences of the rising and falling edges of both the active bridge voltages, 12 different modes of operations are possible for the power transfer from the low-voltage to high-voltage side (positive power transfer) and high-voltage to low-voltage side (negative power transfer) each. However, the modes with outer phase shift (φ) greater than 90° are ignored in the analysis as they would result in higher circulating currents in the converter. Hence, D_φ is restricted between –0.5 and 0.5, resulting in five possible modes of operation for positive and five possible modes for negative power transfer operation. The power transferred is positive when D_φ is positive and the power transferred is negative when D_φ is negative [2], [26]. D_1 and D_2 can vary from 0 to 1. The ideal waveforms of voltages $v_{AB}(t)$, $v_{CD}(t)$, and the current in L_R are shown in Fig. 3 for different modes operation during power transfer from primary side to secondary side. The constraints on the duty ratios are as follows:

$$0 \le D_1 \le 1\, 0 \le D_2 \le 1 \text{ and } -0.5 \le D_\varphi \le 0.5.$$

In the upcoming analysis and mathematical formulations, only the positive power transfer (power transferred from the input voltage port V_{in} to the output voltage port V_o) is analyzed as the results of the analysis would be similar in the reverse power flow (power transferred from output voltage port V_o to input voltage port V_{in}) due to the symmetrical nature of the HF tank. Fig. 3 shows the five possible modes of operation for positive power transfer based on the above duty constraints. Also note that positive half of the voltage $v_{AB}(t)$ is initiated by the rising edge of gating pulse S_1 and ends with that of the gating pulse of S_2 while the positive half of the voltage $v_{CD}(t)$ is initiated by the rising edge of gating pulse S_5 and ends with that of the gating pulse of S_6.

B. Mathematical Analysis of the Modes of Operation

The current i_L in the inductor L_R at four switching instances t_0, t_1, t_2, or t_3 determines whether the MOSFET achieves complete ZVS or partial ZVS or hard switching during steady-state operation. The equations for the currents during the switching instances and transmission power of each mode are shown

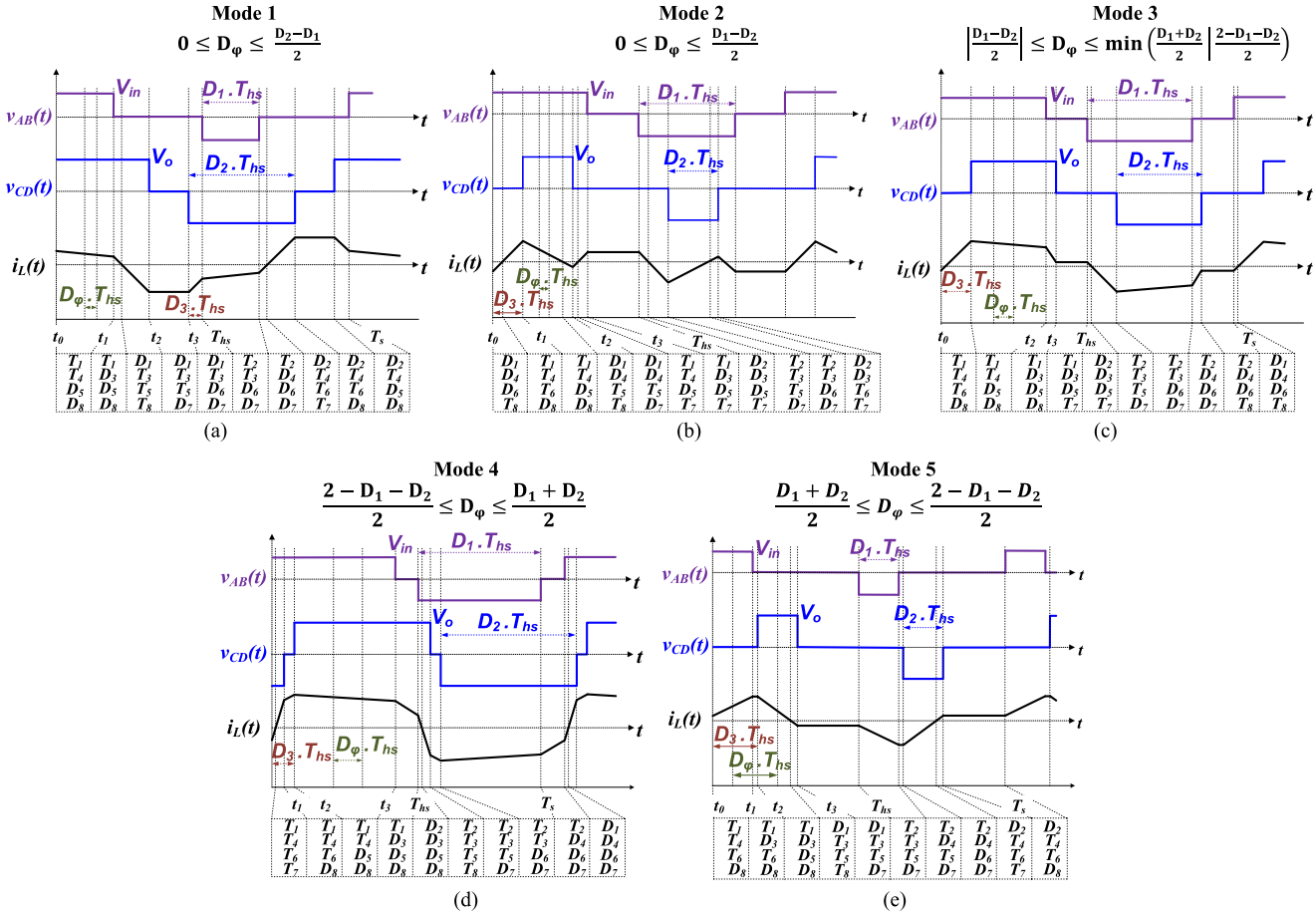

Fig. 3. Basic modes of operation on TPS-controlled DAB converter.

TABLE I
EQUATIONS OF SWITCHING INSTANT CURRENTS AND TRANSMISSION POWER OF EACH MODE

	Switching instant currents during rising and falling edges of v_{AB} and v_{CD}.	Power Transferred (P_O)
Mode 1	$i_L(t_0) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1) + V_o(D_2 + 2D_3)]$	$P_{Mode\ 1} = \frac{nV_{in}V_oT_s}{2L_R}[D_1.D_\varphi]$
	$i_L(t_1) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(-2D_1 + D_2 + 2D_3)]$	
	$i_L(t_2) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(-D_2)]$	
	$i_L(t_3) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(-D_2)]$	
Mode 2	$i_L(t_0) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1) + V_o(D_2)]$	$P_{Mode\ 2} = \frac{nV_{in}V_oT_s}{2L_R}[D_2 \cdot D_\varphi]$
	$i_L(t_1) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1 + 2D_3) + V_o(D_2)]$	
	$i_L(t_2) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1 + 2D_2 + 2D_3) + V_o(-D_2)]$	
	$i_L(t_3) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(-D_2)]$	
Mode 3	$i_L(t_0) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1) + V_o(D_2)]$	$P_{Mode\ 3} = \frac{nV_{in}V_oT_s}{2L_R}\left[\frac{D_1D_2}{4} + \frac{D_1D_\varphi}{2} + \frac{D_2D_\varphi}{2} - \frac{{D_1}^2}{8} - \frac{{D_2}^2}{8} - \frac{{D_\varphi}^2}{2}\right]$
	$i_L(t_1) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1 + 2D_3) + V_o(D_2)]$	
	$i_L(t_2) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(D_2 - 2D_1 + 2D_3)]$	
	$i_L(t_3) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(-D_2)]$	
Mode 4	$i_L(t_0) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1) + V_o(2 - D_2 - 2D_3)]$	$P_{Mode\ 4} = \frac{nV_{in}V_oT_s}{2L_R}\left[\frac{D_1}{2} + \frac{D_2}{2} + D_\varphi - \frac{{D_1}^2}{4} - \frac{{D_2}^2}{4} - {D_\varphi}^2 - \frac{1}{2}\right]$
	$i_L(t_1) = \frac{T_s}{4L_R}[n \cdot V_{in}(2D_2 - D_1 + 2D_3 - 2) + V_o(D_2)]$	
	$i_L(t_2) = \frac{T_s}{4L_R}[n \cdot V_{in}(2D_3 - D_1) + V_o(D_2)]$	
	$i_L(t_3) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(-2D_1 + D_2 + 2D_3)]$	
Mode 5	$i_L(t_0) = \frac{T_s}{4L_R}[n \cdot V_{in}(-D_1) + V_o(D_2)]$	$P_{Mode\ 5} = \frac{nV_{in}V_oT_s}{2L_R}\left[\frac{D_1D_2}{2}\right]$
	$i_L(t_1) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(D_2)]$	
	$i_L(t_2) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(D_2)]$	
	$i_L(t_3) = \frac{T_s}{4L_R}[n \cdot V_{in}(D_1) + V_o(-D_2)]$	

TABLE II
EQUATIONS OF TRANSFORMER RMS CURRENT REFERRED TO THE SECONDARY SIDE OF EACH MODE

Mode 1	$\sqrt{\frac{2}{Ts}\int_{0}^{D_1(Ts/2)}\left[i_L(t_0)+\frac{(nV_{\rm in}-V_o)t}{L_R}\right]^2dt+\frac{2}{Ts}\int_{D_1(Ts/2)}^{(D_2+D_3)(Ts/2)}\left[i_L(t_1)+\frac{(-V_o)(t-D_1(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_2+D_3)(Ts/2)}^{(1+D_3)(Ts/2)}[i_L(t_2)]^2dt+\frac{2}{Ts}\int_{(1+D_3)(Ts/2)}^{(Ts/2)}\left[i_L(t_3)+\frac{(-V_o)(t-(1+D_3)(Ts/2))}{L_R}\right]^2dt}$
Mode 2	$\sqrt{\frac{2}{Ts}\int_{0}^{D_3(Ts/2)}\left[i_L(t_0)+\frac{(nV_{\rm in})t}{L_R}\right]^2dt+\frac{2}{Ts}\frac{2}{Ts}\int_{D_3(Ts/2)}^{(D_2+D_3)(Ts/2)}\left[i_L(t_1)+\frac{(nV_{\rm in}-V_o)(t-D_3(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_2+D_3)(Ts/2)}^{(D_1)(Ts/2)}\left[i_L(t_2)+\frac{(nV_{\rm in})(t-(D_3+D_2)(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_1)(Ts/2)}^{(Ts/2)}[i_L(t_3)]^2dt}$
Mode 3	$\sqrt{\frac{2}{Ts}\int_{0}^{D_3(Ts/2)}\left[i_L(t_0)+\frac{(nV_{\rm in})t}{L_R}\right]^2dt+\frac{2}{Ts}\int_{D_3(Ts/2)}^{(D_1)(Ts/2)}\left[i_L(t_1)+\frac{(nV_{\rm in}-V_o)(t-D_3(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_1)(Ts/2)}^{(D_2+D_3)(Ts/2)}\left[i_L(t_2)+\frac{(-V_o)(t-(D_1)(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_2+D_3)(Ts/2)}^{(Ts/2)}[i_L(t_3)]^2dt}$
Mode 4	$\sqrt{\frac{2}{Ts}\int_{0}^{(D_2+D_3-1)(Ts/2)}\left[i_L(t_0)+\frac{(nV_{\rm in}+V_o)t}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_2+D_3-1)(Ts/2)}^{(D_3)(Ts/2)}\left[i_L(t_1)+\frac{(nV_{\rm in})(t-(D_2+D_3-1)(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_3)(Ts/2)}^{(D_1)(Ts/2)}\left[i_L(t_2)+\frac{(nV_{\rm in}-V_o)(t-(D_3)(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(D_1)(Ts/2)}^{(Ts/2)}\left[i_L(t_3)+\frac{(-V_o)(t-(D_1)(Ts/2))}{L_R}\right]^2dt}$
Mode 5	$\sqrt{\frac{2}{Ts}\int_{0}^{D_1(Ts/2)}\left[i_L(t_0)+\frac{(nV_{\rm in})t}{L_R}\right]^2dt+\frac{2}{Ts}\int_{D_1(Ts/2)}^{(D_3)(Ts/2)}[i_L(t_1)]^2dt+\frac{2}{Ts}\int_{(D_2+D_3)(Ts/2)}^{(1+D_3)(Ts/2)}\left[i_L(t_2)+\frac{(-V_o)(t-(D_3)(Ts/2))}{L_R}\right]^2dt+\frac{2}{Ts}\int_{(1+D_3)(Ts/2)}^{(Ts/2)}[i_L(t_3)]^2dt}$

in Table I. The equations of the switching instant currents at steady-state conditions are solved by taking $I(T_{hs}) = -I(t_0)$.

The power transfer by the converter is derived for each mode of operation as $P_{\rm Mode} = v_{AB}(t) \times i_L(t) = v_{CD}(t) \times i_L(t)$. If the current i_L at a certain switching instance is negative during the rising edge of $v_{AB}(t)$ and positive during the falling edge of $v_{AB}(t)$ during its positive half cycle, the primary side MOSFETs achieve complete or partial ZVS based on the energy stored in the reactive HF tank elements. Similarly, if the current i_L at a certain switching instance current is positive during the rising edge of $v_{CD}(t)$ and negative during the falling edge of $v_{CD}(t)$ during the positive half cycle, the high-voltage side secondary side MOSFETs achieve complete or partial ZVS based on the energy stored in the reactive HF tank elements.

C. Constraint for Complete ZVS Operation

It is well known that the parasitic output capacitance $C_{\rm OSS}$ of MOSFET is known to exhibit a nonlinear dependence on the drain–source voltage $V_{\rm DS}$. This results in the charge stored in parasitic capacitances also being a nonlinear function of the applied voltage. A charge equivalent output capacitance $C_{Q,\,\rm eq}(V_{\rm DS})$ introduced in [34] which exhibits the same amount of stored charge as the nonlinear capacitance at a certain value of drain–source voltage $V_{\rm DS}$ is used to determine the energy-related condition for achieving complete ZVS in the MOSFETs.

The energy condition for achieving complete ZVS is that the energy E_L in the series inductor L_R should be greater than the energy E_C stored in the charge equivalent output capacitance $C_{Q,\,\rm eq}(V_{\rm DS})$ of the MOSFET during its off state [34]. Neglecting the HF transformer parasitic capacitances, the capacitor energy is just confined to the MOSFETs charge based capacitance. Hence, the constraint taken in the optimization problem to ensure complete ZVS is

$$0.5 \times L_R \times i_L(t_x)^2 > 0.5 \times C_Q \times {V_{\rm in}}^2 \quad \text{for primary side bridge MOSFETs} \tag{5}$$

$$0.5 \times L_R \times i_L(t_x)^2 > 0.5 \times C_Q \times {V_o}^2 \quad \text{for secondary side bridge MOSFETs} \tag{6}$$

where t_x is the switching time instant which can be t_0, t_1, t_2, or t_3, and $i_L(t_x)$ is the inductor current during the switching instant and is defined for different modes in Table I. Similarly C_Q is $(2 \times C_{Q,\,\rm eq}(V_{\rm DS}))$ if the duty of the corresponding bridge is less than 1 and $(4 \times C_{Q,\,\rm eq}(V_{\rm DS}))$ if the duty of the corresponding bridge is equal to 1 where $C_{Q,\,\rm eq}(V_{\rm DS})$ indicates the charge equivalent output capacitance of the primary or secondary side MOSFET based on the device being switched at that instant.

Equations of rms currents for each mode can be derived from the switching instant currents as shown in Table II. RMS current is an indicator of the circulating current associated with the corresponding operating condition for a certain set of duties. The lower the rms current for a particular power transfer, the lower the circulating current.

Based on the equations and constraints of each mode shown in this section, the optimal operating conditions of a TPS DAB converter are derived in the next section. Also some important conclusions regarding the natural ZVS range have been discussed in Section III.

III. OPTIMIZATION OF TPS-CONTROLLED DAB

The optimization problem has a three-dimensional solution space with various combinations of D_1, D_2, and D_φ for a certain

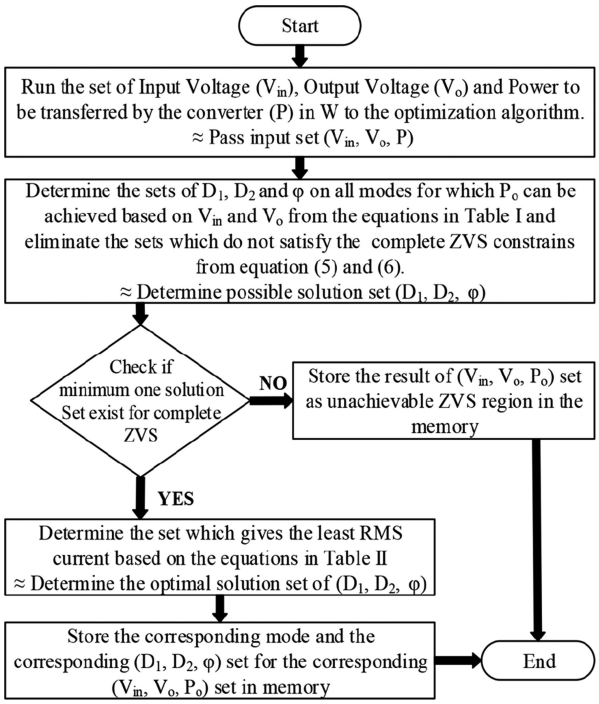

Fig. 4. Procedures to determine the optimal control parameters and ZVS range.

value of $V_{\rm in}$, V_o, and for a particular power transfer (P in watts) by the converter. Constraints of each mode are defined based on

1) the mutual constraints of the inter- and intrabridge duty ratios as shown in Fig. 3 and
2) the magnitude and direction of the link inductor currents during the switching instances necessary to achieve complete ZVS of all the MOSFETs.

The optimization function is defined to achieve the least HF reactive tank rms current. It should be noted that in most of the literature, the natural ZVS behavior of TPS DAB is determined simply in terms of the current direction of the link inductor and not the actual energy available in the HF tank for discharging the device output capacitance. This is why most optimization results may not be able to precisely predict the natural ZVS range of the TPS DAB converter and herein lay the importance of the optimization of the TPS DAB converter presented in the following sections. The equations of the transformer rms current referred to the secondary side at steady-state conditions for each mode are also shown in Table II. Different solutions of duty ratios result for a particular power transfer at a fixed input and output voltages. However, the circulating current and hence the reactive HF tank current vary for each solution [7]. Increase in circulating current leads to increased conduction loss in the MOSFETs and also copper loss in the HF transformer and Printed Circuit Board (PCB). Fig. 4 summarizes the optimization procedure to determine the optimal control parameters and ZVS range for the entire operating region of the conventional converter.

A. Specifications of the Hardware Prototype

The above optimization function is evaluated for the specifications of a 1 kW DAB hardware prototype. The specifications are given in Table III. The MOSFETs used in the secondary side bridge are C3M0065090D and the primary side bridge are IPB019N08N3 and charge equivalent output capacitance $C_{Q,\,\rm eq}(V_{\rm DS})$ of these MOSFETs are taken as constrains to ensure complete ZVS condition. The basic design and choice of these parameters for the example of the TPS DAB converter can be found in [26]. According to the design procedures given in [9] and [35], the maximum phase shift in steady state for the DAB is generally limited close to 45° at the nominal input voltage in order to avoid high circulating current at high loads. Hence, the value of the effective series inductance (L_R) associated with the transformer is designed as 74 μH for the analysis of the 1 kW converter. The series inductor L_R at the HF tank shown in Fig. 1 includes both the leakage inductance of the transformer referred to the secondary side (11.5 μH) and the external inductor (62.5 μH). The primary side voltage varies due to the terminal voltage variations of the ES element with respect to its state of charge.

The nominal voltage of the ES is 33.75 V where the converter operates most of the time. Hence, the turns ratio of the transformer is designed to have better converter performance around the nominal operating voltage of the ES element.

TABLE III
DC–DC CONVERTER SPECIFICATIONS

	Parameter		Value
1	Primary side nominal voltage	$V_{\rm in}$	30–38 V
2	Secondary side voltage	V_o	270 V
3	Switching frequency	f_s	100 kHz
4	Primary side capacitance	$C_{\rm in}$	30 × 10 μF/ 63 V/X7R(MLCC) in parallel
5	Secondary side capacitance	C_o	12 × 2.2 μF/ 450 V/X6S (MLCC) in parallel
6	Maximum power transferred	$P_{\rm max}$	1 kW
7	Series inductance	L_R	74 μH
8	Turns ratio	n	8
9	Primary side MOSFET	S_1, S_2, S_3, S_4	IPB019N08N3
10	Secondary side MOSFET	S_5, S_6, S_7, S_8	C3M0065090D

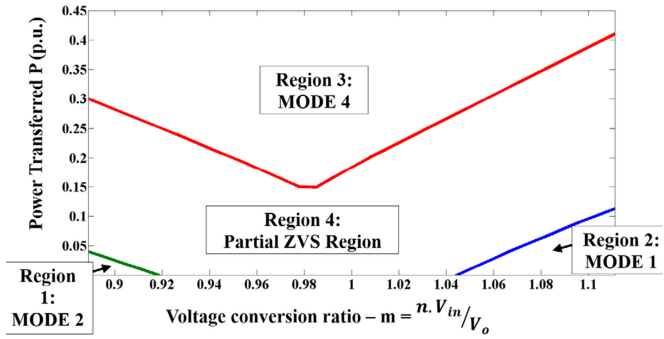

Fig. 5. Optimal operating modes for the converter operating conditions.

B. Inference on Controlled DAB Optimized Results of TPS

The optimization function to achieve reduced transformer rms current along with the constraints to achieve complete ZVS condition on all MOSFETs is evaluated on the converter specifications. The optimal operating modes for the operating conditions at mid light loads of the converter are shown in Fig. 5. The operating conditions above 0.7 p.u. of power transferred for the above converter specifications are not considered for analysis

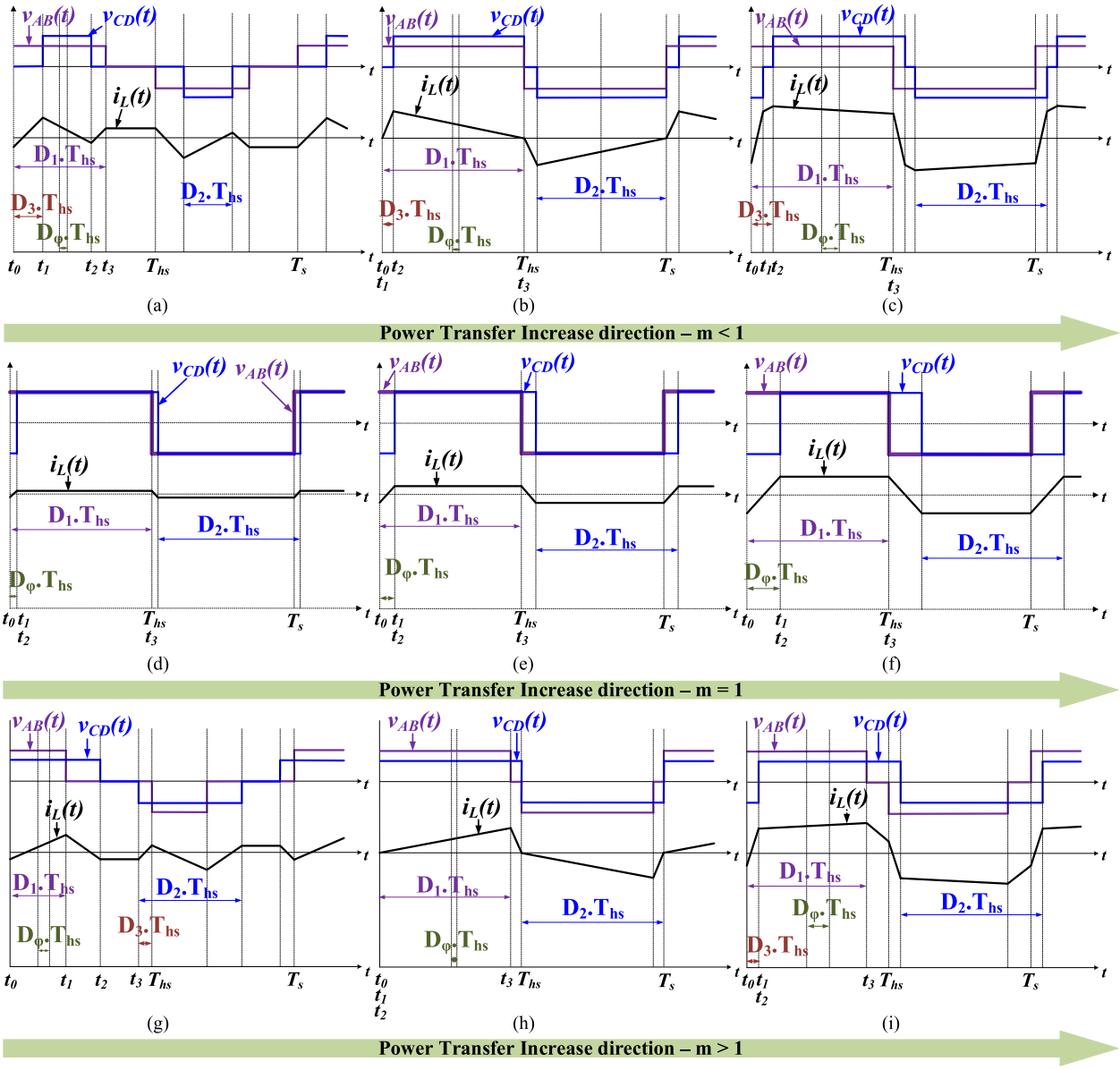

Fig. 6. Optimal operating conditions of TPS-controlled DAB.

in the subsequent sections as the DAB converters inherently achieve full range ZVS with higher values of D_φ operating at mode 4 [9], [26].

Based on the optimization results shown in Fig. 5, the various modes of operation and shapes of $I_L(t)$ for $nV_{\text{in}} < V_o$ as the power transfer increases are shown in Fig. 6(a)–(c). Note that the waveforms in Fig. 6 are the optimal versions of those shown in Fig. 3. Fig. 6(a) indicates mode 2 operation where both the intrabridge duty ratios (D_1 and D_2) are less than unity and they increase as power transferred by the converter increases. Fig. 6(b) indicates triangular modulation marking the boundary between modes 2 and 4, where D_2 becomes unity and D_1 is still less than unity. Fig. 6(c) indicates mode 4 operation where D_1 increases as the power transferred by the converter increases. The optimization results suggest that the boundary between modes 2 and 4 is marked with the HF tank current operating in the boundary conduction mode wherein the current waveform is triangular and three legs of the DAB operate in ZCS. The loss associated with the energy stored in the MOSFET capacitance being operated at ZCS is

$$E_{C\_\text{loss}} = 0.5 \times C_{Q,\,\text{eq}}\,(V_{\text{sw}}) \times {V_{\text{sw}}}^2 \times f_s \tag{7}$$

where V_{sw} can be either V_{in} or V_o based on the MOSFET being switched to its corresponding bridge voltage.

Also in the region close to modes 2–4 boundary, the MOSFETs achieve partial ZVS as the energy in the inductor is not sufficient enough as per (5) and (6) to discharge the capacitances of the MOSFETs (low values of I_L during switching instances). When $nV_{\text{in}} < V_o$, the converter operates in mode 2 [see Fig. 6(a)] during the light load conditions and as the power transferred by the converter increases, the converter operates in mode 4 [see Fig. 6(c)] after transition through the boundary between the two modes marked by the triangular shaped HF tank current [see Fig. 6(b)]. Similarly when $nV_{\text{in}} > V_o$, the converter

operates in mode 1 [see Fig. 6(g)] at the light load conditions and as the power transferred by the converter increases, the converter operates in mode 4 [see Fig. 6(i)] after transition through the boundary between the two modes marked by the triangular shaped HF tank current [see Fig. 6(h)].

The variations of the bridge duty cycles are similar to $nV_{\text{in}} < V_o$ except that D_1 reaches unity even before D_2 as the power transferred by the converter increases. But when $nV_{\text{in}} = V_o$, the optimal duties of the bridges D_1 and D_2 are always equal to unity as shown in Fig. 6(d)–(f). In all three cases, the optimal interphase shift D_φ increases as the power transferred by the converter increases.

The modes 4, 2, and 1 regions in Fig. 5 indicate the regions where the modulation scheme achieves complete ZVS of all the four MOSFET legs. The partial ZVS region shown in Fig. 5 includes the operating conditions where even one of the four MOSFET legs does not achieve complete ZVS. This partial ZVS region is of a concern as the optimal switching frequency of the converter is limited to lower values even if one of the four MOSFET legs does not achieve complete ZVS.

The partial ZVS and ZCS operation of MOSFETs results in hard turn-ON of the converter. Moreover, the error in voltage sensing elements and variations in practical circuit parameters from the parameters used in optimization to find the optimal duties can result in switching operation of the MOSFETs where there will be current in the body diode of the device after the bulk device is turned OFF. While the body diode is conducting and the complimentary device in the same leg is turned-ON there can be catastrophic consequences especially at high switching frequency operation due to cross conduction arising from turn-OFF of slow body diode of MOSFETs. The above-mentioned drawbacks limit very high switching frequency operation (typically more than 250 kHz [2]) of the VF-DAB converter. In order to ensure complete ZVS of all the MOSFETs in TPS-DAB with an accepted level of error in the sensing elements and practical variations in the circuit parameters that are not considered in the model used for optimization, a variation in the HF tank with passive auxiliary inductors connected in parallel (LLL tank) to the primary and secondary sides of the HF transformer is discussed in the next section.

IV. LLL Tank Based DAB Converter

From the optimization results of TPS-based DAB obtained for conventional inductive link, the partial ZVS region in the converter operating conditions always occur at higher values of intrabridge duty ratios D_1 and D_2. However, at operating conditions where the values of D_1 and D_2 are low, complete ZVS of all the MOSFETs are achieved by the modulation itself rather than the assistance of the external auxiliary inductor.

Hence, an LLL tank based DAB is analyzed in this section which is shown in Fig. 7 where a primary side auxiliary inductor (L_P) is connected in parallel to the bridge voltage source of the primary side and the secondary side auxiliary inductor (L_S) is connected in parallel to the bridge voltage source of the secondary side drawing additional circulating current proportional

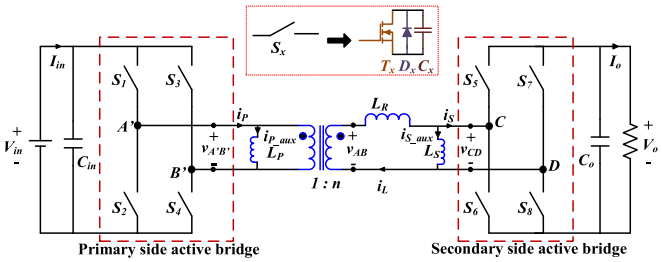

Fig. 7. Dual active bridge (DAB) converter topology with the LLL tank.

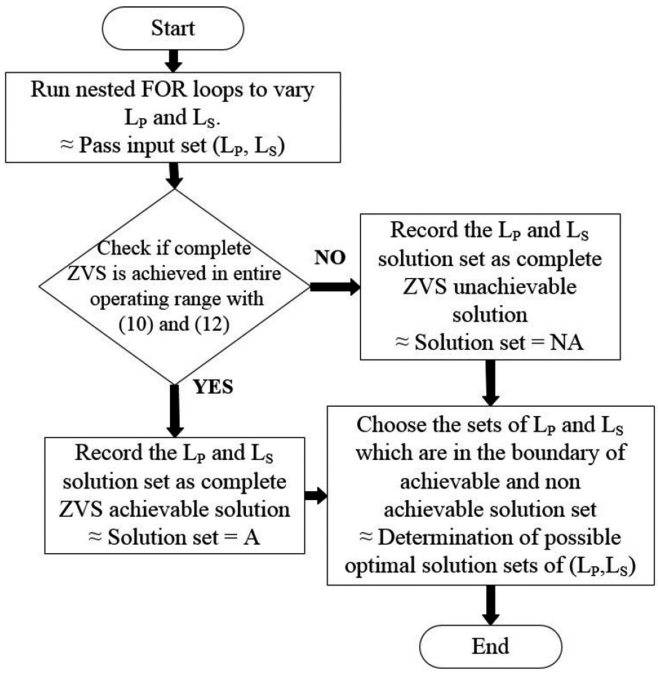

Fig. 8. Procedure to determine the values of the auxiliary inductor.

to the value of intrabridge duty ratios to achieve complete ZVS in the partial ZVS range of the conventional inductive link.

Both L_P and L_S draw inductive currents $i_{P\_\text{aux}}(t)$ and $i_{S\_\text{aux}}(t)$, respectively, with the peak value of the currents which can be derived as

$$I_{P\_\text{aux\_peak}} = \frac{V_{\text{in}}}{n \cdot L_P} \times \frac{D_1 \cdot T_s}{4} \tag{8}$$

$$I_{S\_\text{aux\_peak}} = \frac{V_o}{L_S} \times \frac{D_2 \cdot T_s}{4}. \tag{9}$$

Note that (8) and (9) give the peak current referred to the secondary side in the auxiliary inductors. The primary side bridge current (i_P) is the sum of the series inductor current (i_L) referred to the primary side and the primary auxiliary inductor current (i_{P_aux}). Similarly the secondary side bridge current (I_S) is the difference between the series inductor current (i_L) and the secondary side auxiliary inductor current (i_{S_aux}). However, the auxiliary inductor currents do not contribute to the power transferred by the converter.

Again neglecting the HF transformer parasitic capacitances, the capacitor energy is just confined to the MOSFETs charge based capacitance. Hence, the constraint taken in the optimization

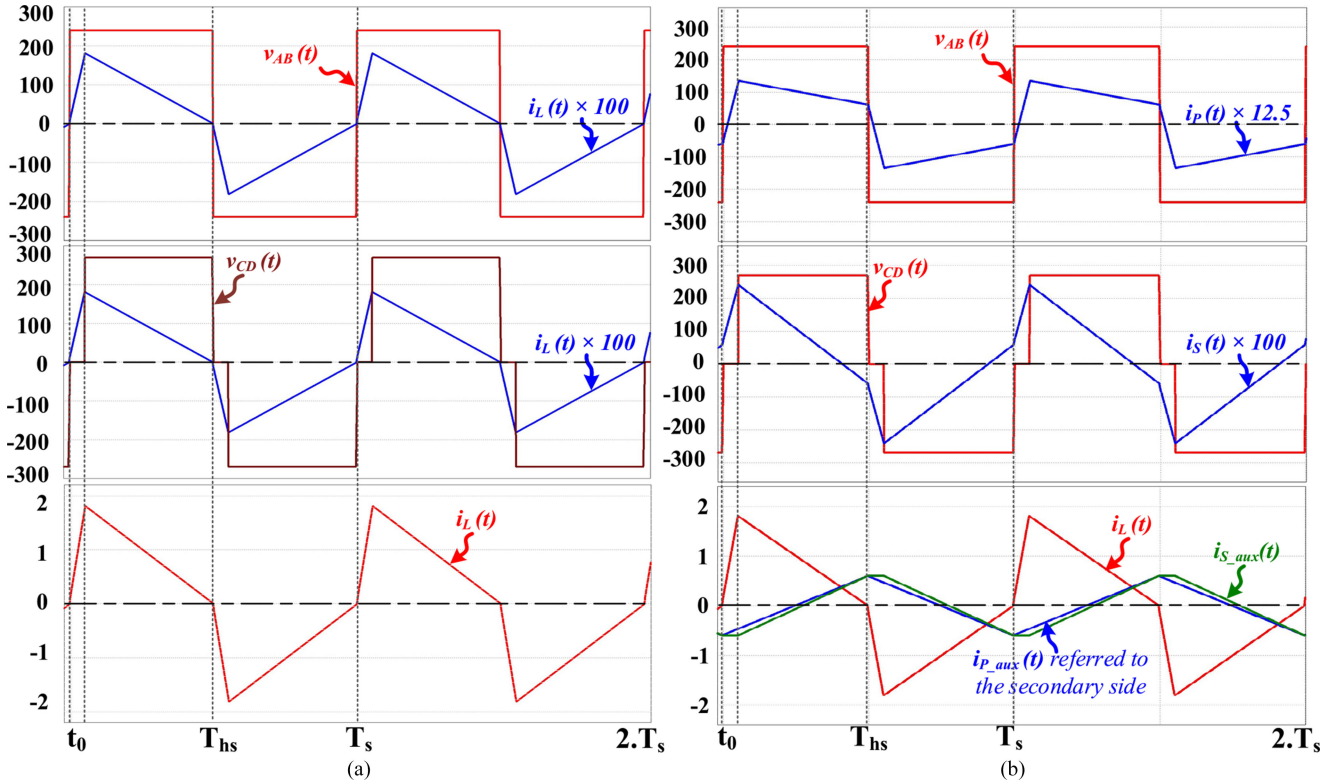

Fig. 9. Simulated waveforms (a) of traditional TPS-based DAB converter in the boundary of modes 2 and 4, (b) illustrating ZVS operation of MOSFETs in modes 2–4 boundary with triangular shaped series inductor (L_R) current for TPS-based LLL tank DAB.

problem to ensure complete ZVS is

$$\left[0.5 \times L_{y\_\mathrm{Aux}} \times {I_{y\_\mathrm{Aux\_Peak}}}^2 + 0.5 \times L_R \times i_L(t_x)^2\right] \gg 0.5 \times C_Q \times {V_{\mathrm{sw}}}^2 \tag{10}$$

where L_{y_Aux}, $I_{y\_\mathrm{Aux\_Peak}}$ indicate primary or secondary auxiliary inductor and its peak current based on the device being switched. V_{sw} can be either V_{in} or V_o based on the MOSFET being switched to its corresponding bridge voltage. Similarly C_Q is twice of $C_{Q,\,\mathrm{eq}}(V_{\mathrm{DS}})$ if the duty of the corresponding bridge is less than 1 and four times $C_{Q,\,\mathrm{eq}}(V_{\mathrm{DS}})$ if the duty of the corresponding bridge is equal to 1 where $C_{Q,\,\mathrm{eq}}(V_{\mathrm{DS}})$ indicates the charge equivalent output capacitance of the primary or secondary side MOSFET based on the device being switched at that instant.

In order to achieve complete ZVS, the dead time provided between the two MOSFETs in a leg should be sufficiently high for the MOSFETs output capacitances to charge and discharge depending on the magnitude currents $i_P(t)$ or $i_S(t)$. The change in tank currents is negligible during the switching transition because of the higher tank inductances and hence can be assumed as a current source.

The transition time is

$$T_{\mathrm{tran}} \approx \frac{V_{\mathrm{sw}} \times C_Q}{I\,(t_x)} \tag{11}$$

where $I(t_x)$ indicates the magnitude of switching instant currents and V_{sw} indicates V_{in} or V_o based on the device being switched. Hence the minimum value of the current during a switching instance should be greater than the minimum value of current to ensure ZVS of the MOSFETs for a predefined dead time $(I(t_x)_{\mathrm{min}})$ based on (11).

In order to ensure complete ZVS with an accepted level of error in the sensing elements and practical variations in the circuit parameters that are not considered in the model used for optimization, the minimum value of the required switching instant current magnitude is further increased by a value of I_{error} as

$$|i_L\,(t_x) + I_{y\_\mathrm{Aux\_Peak}}| > (I(t_x)_{\mathrm{min}} + I_{\mathrm{error}})\,. \tag{12}$$

The sign of these switching instant currents should be positive during the rising edge of $v_{CD}(t)$ and falling edge of $v_{AB}(t)$, and negative during the rising edge of $v_{AB}(t)$ and falling edge of $v_{CD}(t)$ to aid for achieving ZVS in the MOSFETs.

The values of the auxiliary inductors are designed to satisfy both (10) and (12) in the entire operating range of the converter. Higher values of the auxiliary inductor are preferred since they result in lower peak currents. However, the constraints in (10) and (12) set a limitation to a maximum values for the auxiliary inductances. The optimal solution sets of L_P and L_s obtained by the algorithm shown in Fig .8 are necessary to ensure complete ZVS of entire operating condition. The solution set where L_P referred to the secondary side and L_s are of equal value is chosen to have balanced ac-link currents on both sides of the tank and to avoid abrupt transition in the switching instant currents. The optimization for the specifications of the DAB shown in

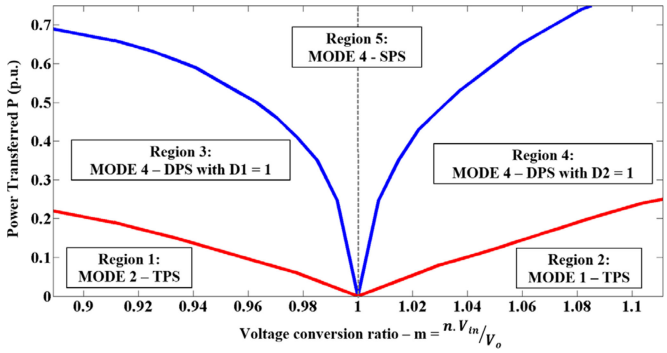

Fig. 10. Optimal operating modes for TPS-controlled LLL tank VF-DAB.

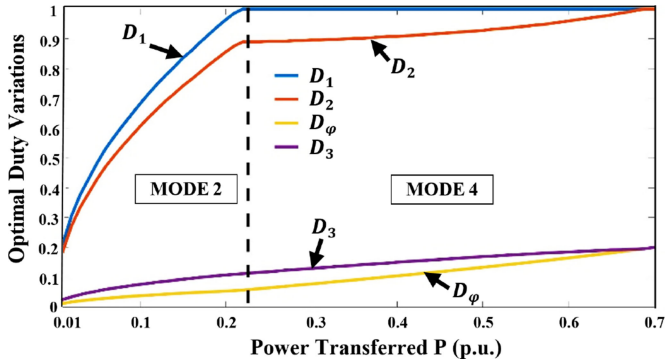

Fig. 11. Duty cycle variations for TPS-controlled LLL tank based VF-DAB $m = 0.88$ and $n = 8$.

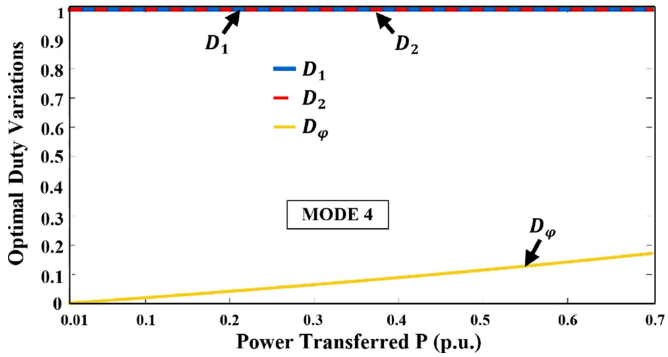

Fig. 12. Duty cycle variations for TPS-controlled LLL tank based VF-DAB $m = 1$ and $n = 8$.

Table III results in optimal primary auxiliary inductance L_P as 15.5 μH and secondary auxiliary inductance L_S as 950 μH.

Fig. 9(a) shows an operating condition wherein ZVS is lost in conventional inductive link TPS DAB when the series inductor current (i_L) is triangular in shape at voltage conversion ratio $m = 0.889$ and the normalized power transfer 0.21 p.u. During such operation, the triangular shape series inductor current $i_L(t)$ indicates the boundary between modes 2 and 4 where six of the eight MOSFETs operate at ZCS. Fig. 9(b) illustrates the same ideal operating condition as in Fig. 9(a) but the inclusion of auxiliary current. Fig. 9(b) indicates ZVS operation of MOSFETs with the help of the two auxiliary inductors. Note that the switching instant currents of i_P and i_S indicate complete ZVS of all the MOSFETs.

The optimal operating modes for the entire operating range obtained with the primary auxiliary inductance $L_P = 15.5$ μH and secondary auxiliary inductance L_S as 950 μH are shown in Fig. 10. These high values of L_P and L_S result in very low circulating currents drawn by these inductors, resulting in low conduction and copper losses of the converter. Fig. 10 shows that the TPS-controlled LLL tank based VF-DAB ensures complete ZVS in all MOSFETs. The auxiliary inductor energy helps charge and discharge the MOSFET capacitance in the partial ZVS region shown in Fig. 5. Based on the optimization results in Fig. 10, the following discussion on the soft-switching range by the TPS-controlled LLL tank is presented.

A. ZVS in LLL TPS DAB for $nV_{\text{in}} < V_o$

Fig. 11 shows optimal duty cycle variations to achieve the least transformer rms current and complete ZVS of all MOSFETs with respect to power transferred by the TPS-controlled LLL tank based VF-DAB for $m = 0.889$ ($nV_{\text{in}} < V_o$). The partial ZVS region occurs around the boundary of modes 2 and 4 where D_1 reaches unity and D_2 is almost close to 0.9. This region is generally pronounced with higher values of intrabridge duty cycles. It is in this vicinity of the boundary of modes 2 and 4 that the energy in the auxiliary inductors is imperative for ZVS of the MOSFET devices. Hence, the energy in the auxiliary inductor which is directly proportional to the duty cycle of the bridges should be sufficient to achieve complete ZVS. However, at low power transfer conditions where the duty cycle is low and so is the energy in the auxiliary inductors, complete ZVS of MOSFETs is achieved by the energy stored in the series inductor. At high-power conditions, both the series inductor and the auxiliary inductors contribute to achieve ZVS. It should be noted that the value of auxiliary inductors is much higher compared to the series inductor and hence do not contribute to large circulating currents even at full load conditions where the intrabridge duty cycles are very high.

B. ZVS in LLL TPS DAB for $nV_{\text{in}} = V_o$

Fig. 12 shows optimal duty cycle variations to achieve the least transformer rms current and complete ZVS of all MOSFETs with respect to power transferred by the TPS-controlled LLL tank based VF-DAB for $m = 1$ ($nV_{\text{in}} = V_o$). The converter always operates in mode 4 with D_1 and D_2 equal to 1 from no load operation to full load. Partial ZVS region in a TPS-controlled normal L-DAB occurs at no load and light load conditions where the phase shift between the two bridge voltages is very low and the energy in the series inductor tank during switching instant is not sufficient enough. However, the auxiliary inductor in the LLL tank assists complete ZVS at light load conditions as D_1 and D_2 are high.

C. ZVS in LLL TPS DAB for $nV_{\text{in}} > V_o$

Fig. 13 shows optimal duty cycle variations to achieve the least transformer rms current and complete ZVS of all MOSFETs with respect to power transferred by the TPS-controlled LLL tank based VF-DAB for $m = 1.11$ ($nV_{\text{in}} > V_o$). Around the

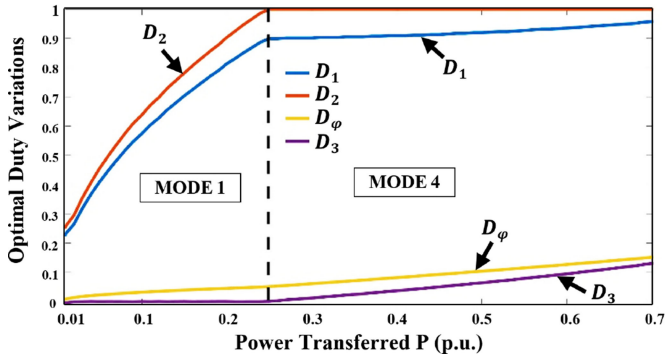

Fig. 13. Duty cycle variations for TPS-controlled LLL tank based VF-DAB with $m = 1.111$ and $n = 8$.

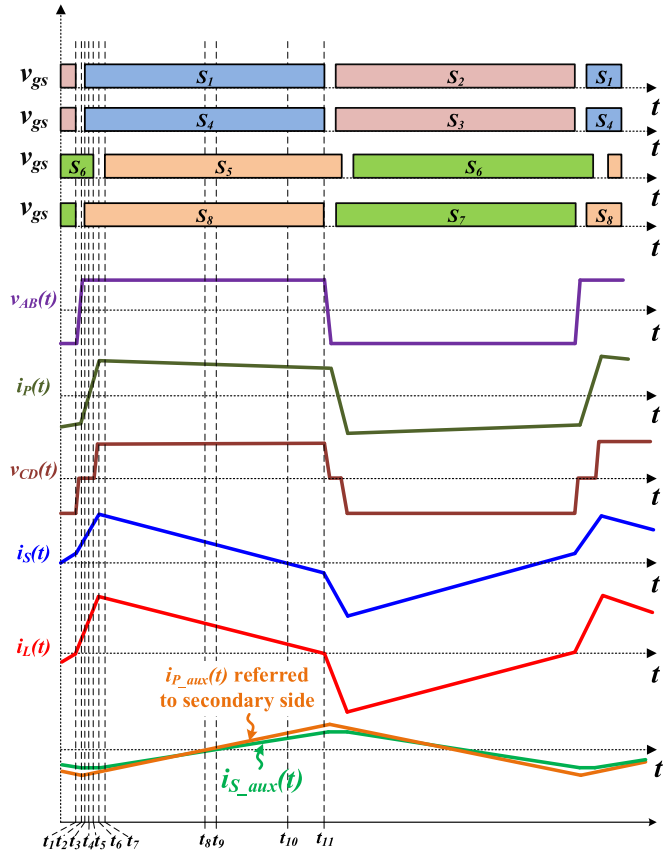

Fig. 14. Operating waveforms of TPS-controlled LLL tank based DAB at modes 2–4 boundary for $m < 1$.

boundary of modes 1 and 4 when D_2 reaches 1, D_1 is almost close to 0.9. Similar to the condition where $nV_{\text{in}} < V_o$, complete ZVS of the MOSFETs can be achieved with the inductive current of auxiliary inductors, and at the boundary between the two modes, same can be done only with the energy stored in the series inductor.

Fig. 14 shows the operating waveforms of TPS-controlled LLL tank based VF-DAB at the boundary condition of modes 2 and 4, for $m < 1$. The dead time provided between the MOSFETs of the same leg is represented by intervals $t_1 - t_3$ (both the primary legs and one of the secondary legs) and $t_5 - t_7$ (one of the secondary legs) for the first half-cycle in Fig. 14.

The equivalent circuits corresponding to each timing interval is shown in Fig. 15. Fig. 15(a) shows that at time instant t_1, $i_L(t_1) \approx 0$ and the energy in the auxiliary inductors is responsible for charging and discharging the outgoing and incoming MOSFETs output capacitances, respectively, thereby achieving complete ZVS. Fig. 15(b) shows that during interval $t_2 - t_3$, the body diodes of the incoming MOSFETs conduct after their output capacitances are completely discharged thereby assisting for ZVS. The gating pulses of the incoming MOSFETs are turned ON at instant t_3 while the currents are flowing through their body diodes resulting in lossless turn ON.

The HF tank currents transfer to the MOSFET channels from the body diodes during interval $t_3 - t_4$ as shown in Fig. 15(c) thereby avoiding increased conduction losses due to prolonged body diode conduction. Since the voltage across both auxiliary inductor and leakage inductor tends to increase their respective currents in positive direction, i_p becomes zero at instant t_4 and then continues to increase in positive direction through MOSFET channels of S_1 and S_4 till the time instant t_5 as shown in Fig. 15(d). Secondary side MOSFET S_6 is turned OFF at t_5, the current polarities in leakage inductor and secondary auxiliary inductor aid in charging the device capacitance of S_6 and discharging the device capacitance of S_5, this continues till time instant t_6 as shown Fig. 15(e). Fig. 15(f) shows interval $t_6 - t_7$. At time t_6, device capacitance of S_5 is fully discharged and its body diode gets forward biased due to the current polarity of auxiliary inductor current and the main leakage inductor current. Body diode of S_5 and MOSFET channel of S_8 carries the secondary bridge current during interval $t_6 - t_7$. The device S_5 is turned ON at instant t_7 while its body diode is conducting, resulting in its complete ZVS turn ON. The current through body diode of S_5 is now transferred to its MOSFET channel. The interval $t_7 - t_8$ is shown in Fig. 15(g). The primary and secondary auxiliary inductor currents reach zero at instant t_8 and t_9, respectively, and continues to rise in a positive direction owing to the polarity of voltage applied across them. The equivalent circuit during the intervals $t_8 - t_9$ and $t_9 - t_{10}$ is shown in Fig. 15(h) and (i), respectively. The polarity of the secondary side bridge current reverses at instant t_{10} and hence the MOSFET channels of S_5 and S_8 conduct current in positive direction until the device S_8 is turned OFF at instant t_{11}. The corresponding equivalent circuit during this interval $t_{10} - t_{11}$ is shown in Fig. 15(j).

The optimized results for the LLL tank based VF-DAB discussed in this section provide complete ZVS for the entire operating range of the converter. The modified tank design is evaluated experimentally in the next section.

V. Experimental Results

The specifications of the 1 kW VF-DAB laboratory prototype are shown in Table III. The designed HF transformer uses interleaved winding arrangement resulting in low leakage inductance and ac resistance. The measured primary leakage inductance $L_{\text{Lk\_Pri}}$ is 70 nH, secondary leakage inductance

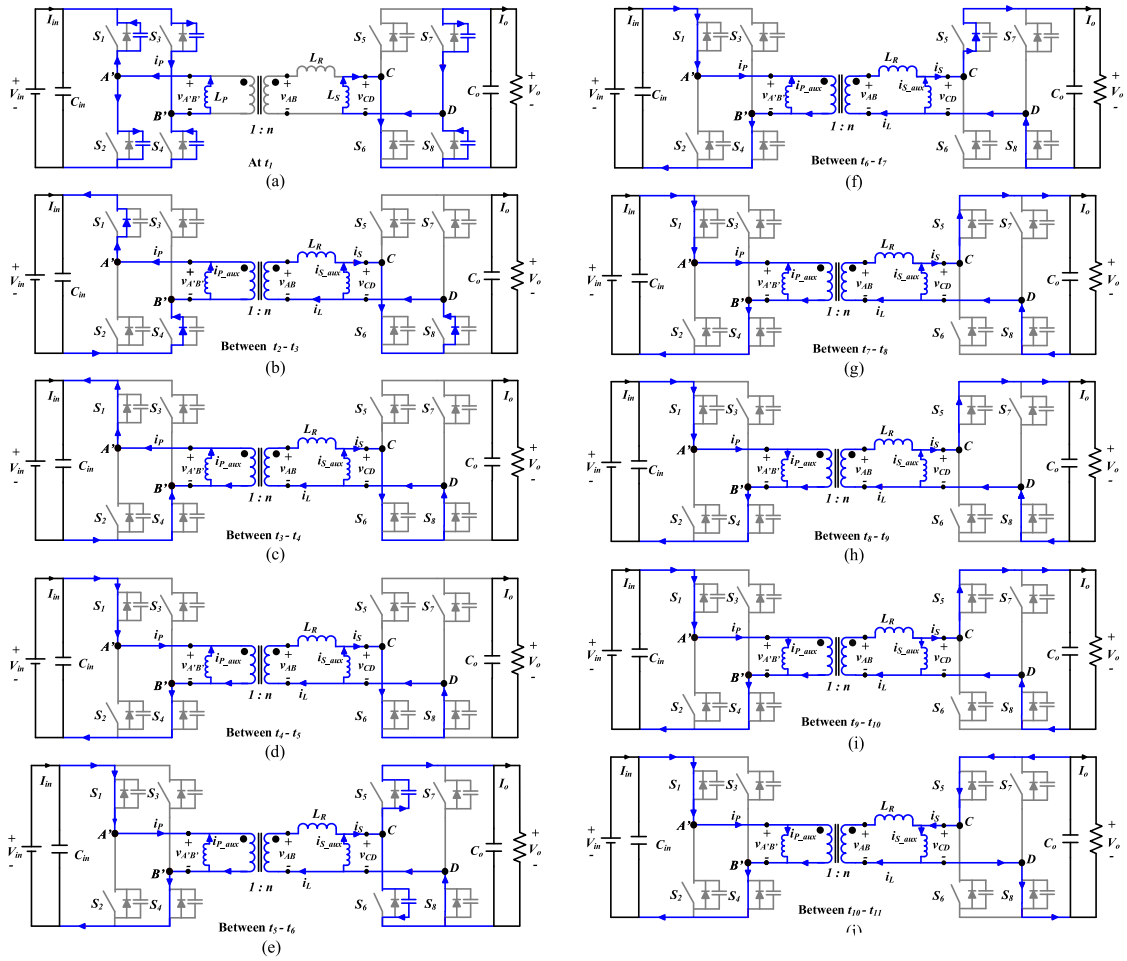

Fig. 15. Current paths and conducting devices in LLL tank based VF-DAB for a half-cycle operating at modes 2–4 boundary shown in Fig. 10 with during the transitions: (a) at instant t_1, (b) between $t_2 - t_3$, (c) between $t_3 - t_4$, (d) between $t_4 - t_5$, (e) between $t_5 - t_6$, (f) between $t_6 - t_7$, (g) between $t_7 - t_8$, (h) between $t_8 - t_9$, (i) between $t_9 - t_{10}$, and (j) between $t_{10} - t_{11}$.

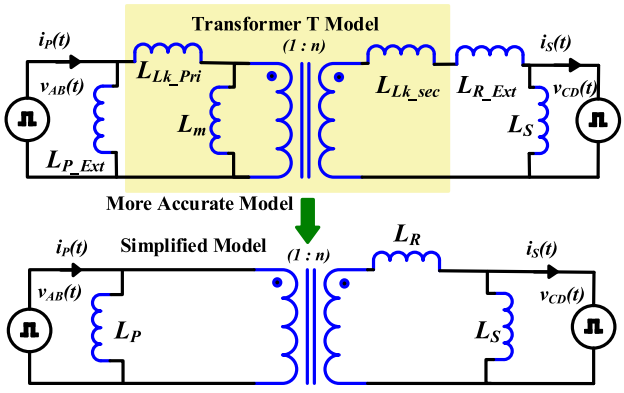

Fig. 16. Equivalent circuit model of the reactive HF tank.

$L_{\mathrm{Lk\_Sec}}$ is 7.1 μH, and the magnetizing inductance L_m is 45 μH. Fig. 16 shows a more accurate model of the hardware reactive tank being simplified into an LLL-based tank. Since $L_{\mathrm{Lk\_Pri}} \ll L_m$, the primary leakage inductance is shifted to the right side of L_m. The required primary auxiliary inductance (L_P) can be achieved either by L_m alone or by a parallel combination of an external primary auxiliary inductance (L_{P_Ext}) and L_m:

$$L_P = L_{P\_\mathrm{Ext}} \parallel L_m \tag{13}$$

$$L_R = n^2 \times L_{\mathrm{Lk_{Pri}}} + L_{\mathrm{Lk_{Sec}}} + L_{R_{\mathrm{Ext}}} \tag{14}$$

where L_{R_Ext} is the external series inductor which is 62.5 μH. L_S is the externally connected secondary side auxiliary inductor which is designed to be 1 mH. In order to achieve L_P close to 16 μH, L_{P_Ext} is designed to be 23 μH. The simplified model of the designed prototype thus has L_P (referred to the secondary side) $\approx$ 960 μH, L_S = 950 μH, and L_R = 74 μH.

The technical data on the magnetics of the hardware prototype are

1) Transformer: Turns ratio $n = 8$, two ETD 49/25/16 half-cores (3C95 core material), primary winding—4200 strands of AWG 42 litz wire in parallel, and secondary winding—660 strands of AWG 42 litz wire in parallel.
2) External series inductor (L_{R_Ext}): Two PQ 32/30 half-cores (3C95 core material), 660 strands of AWG 42 litz wire in parallel.
3) Externally connected primary side auxiliary inductor (L_{P_Ext}): Two PQ 20/16 half-cores (3C95

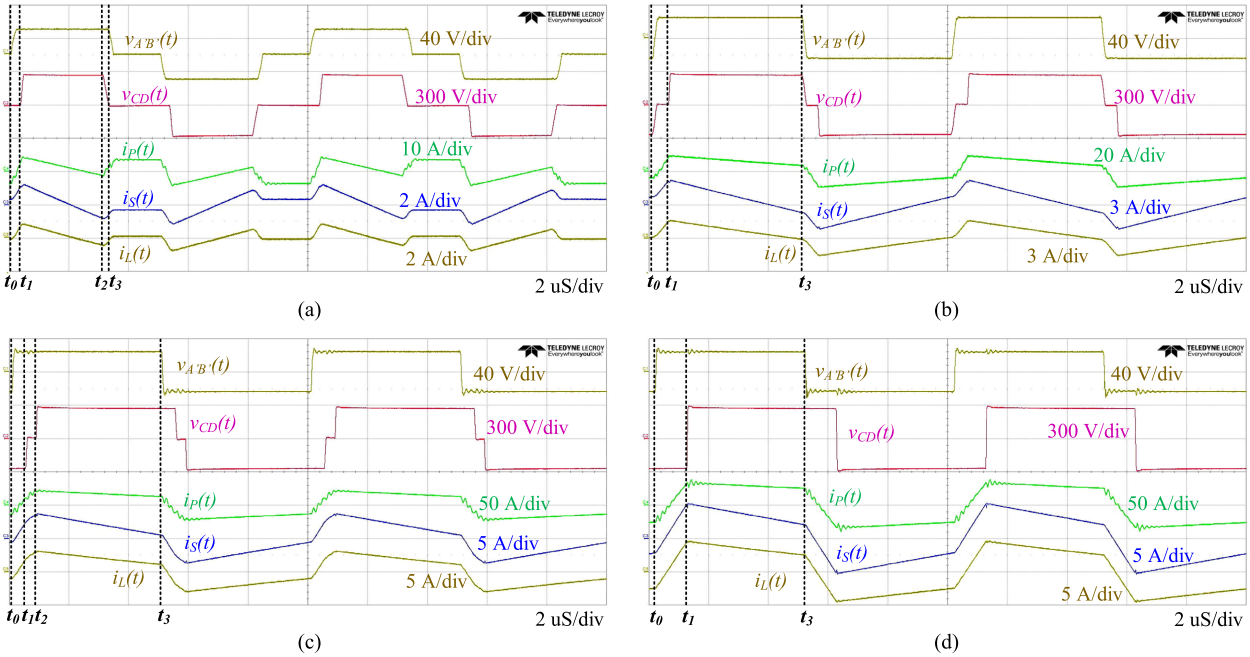

Fig. 17. Experimental waveforms for $V_{\text{in}} = 30$ V, $V_o = 270$ V, and $n = 8$. (a) Mode 2, $P = 26$ W. (b) Boundary between modes 2 and 4, $P = 178$ W. (c) Mode 4, $P = 456.4$ W. (d) Mode 4, $P = 700$ W.

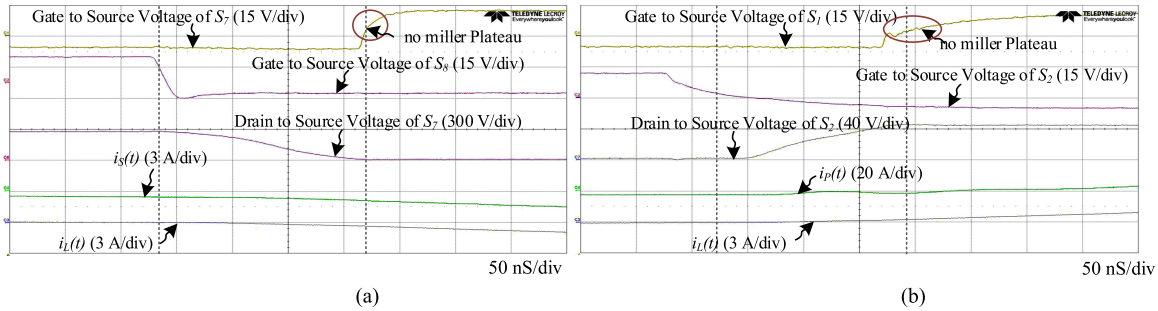

Fig. 18. Switching transition waveforms at the boundary condition between modes 2 and 4 for $V_{\text{in}} = 30$ V, $V_o = 270$ V, and $n = 8$. (a) ZVS switching transition for secondary side MOSFET. (b) ZVS switching transition for primary side MOSFET.

core material), 270 strands of AWG 42 litz wire in parallel.

4) Secondary side auxiliary inductor (L_S): Two PQ 20/16 half-cores (3C95 core material), 40 strands of AWG 42 litz wire in parallel.

The TPS control is implemented by using a TMS320F28335 DSP from Texas Instruments. Fig. 17 shows the experimental waveforms for $V_{\text{in}} = 30$ V from light loads to heavy load conditions. The experimental waveforms indicate the values of switching instant currents aiding to achieve ZVS for all the MOSFETs at various load conditions. ZVS is achieved even at less than 5% load conditions. Fig. 17(a) shows the operating waveform at light load condition where the converter operates at mode 2. As the power transfer increases, the converter is driven toward the boundary between modes 2 and 4 as shown in Fig. 17(b) and then enters mode 4 operation as the power transferred by the converter increases further as shown in Fig. 17(c) and (d). Fig. 17(d) shows the SPS operation of DAB at high power transfer region where D_1 and D_2 are equal to unity.

Fig. 18(a) indicates the ZVS transition of secondary side MOSFET leg for $V_{\text{in}} = 30$ V at the boundary condition between modes 2 and 4 with the series inductor switching instant current being zero for six MOSFET transitions. However, the secondary side bridge current has a negative value sufficient enough to achieve complete ZVS due to the addition of secondary side auxiliary inductor current. Hence, the drain to source voltage of device S_7 falls to zero before the gate to source voltage of S_7 is turned ON. The gate to source voltage of S_7 has no miller plateau indicating complete ZVS of S_7. Similarly, Fig. 18(b) indicates ZVS transition for primary side MOSFET leg for $V_{\text{in}} = 30$ V. The drain to source voltage of S_2 becomes 30 V and that of S_1 becomes almost zero before the gate to source voltage of S_1 is applied indicating complete ZVS of S_1.

Fig. 19 shows the experimental results of the LLL tank based VF-DAB operated with $V_{\text{in}} = 33.75$ V and $V_o = 270$ V at variable load conditions. It can be seen that the mode of operation remains the same for all possible load conditions since $m = 1$. From Fig. 19(a), it can be observed that at light load conditions

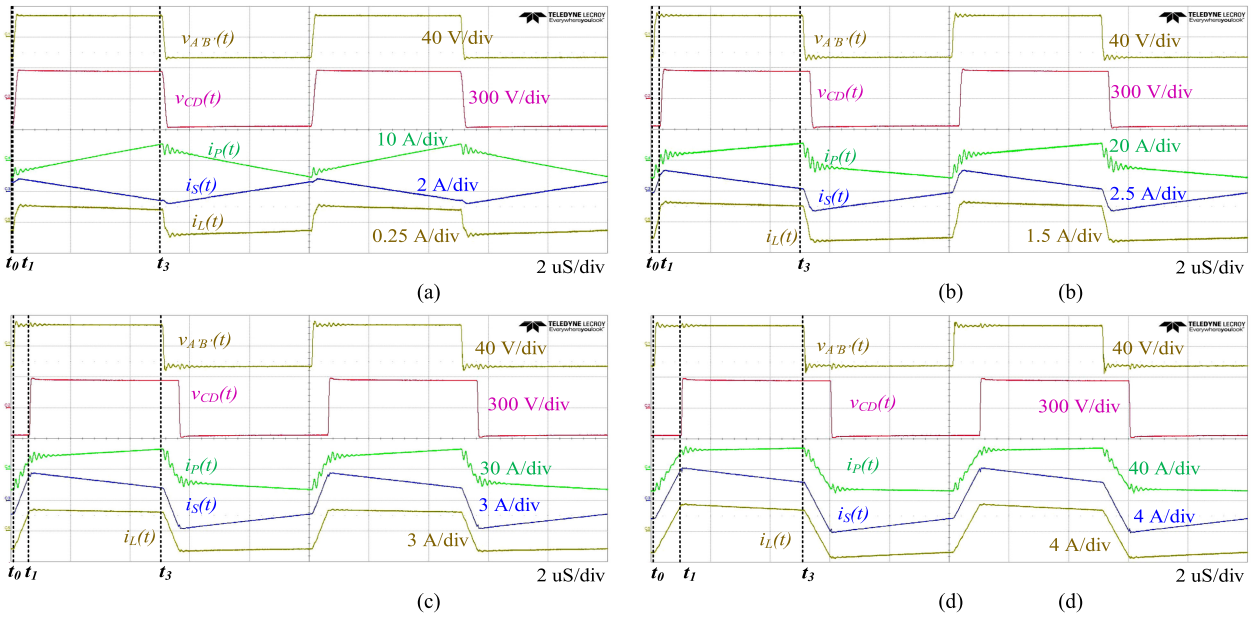

Fig. 19. Experimental waveforms for $V_{\text{in}} = 33.75$ V, $V_o = 270$ V, and $n = 8$. (a) Mode 4, $P = 29$ W. (b) Mode 4, $P = 230$ W. (c) Mode 4, $P = 476$ W. (d) Mode 4, $P = 704$ W.

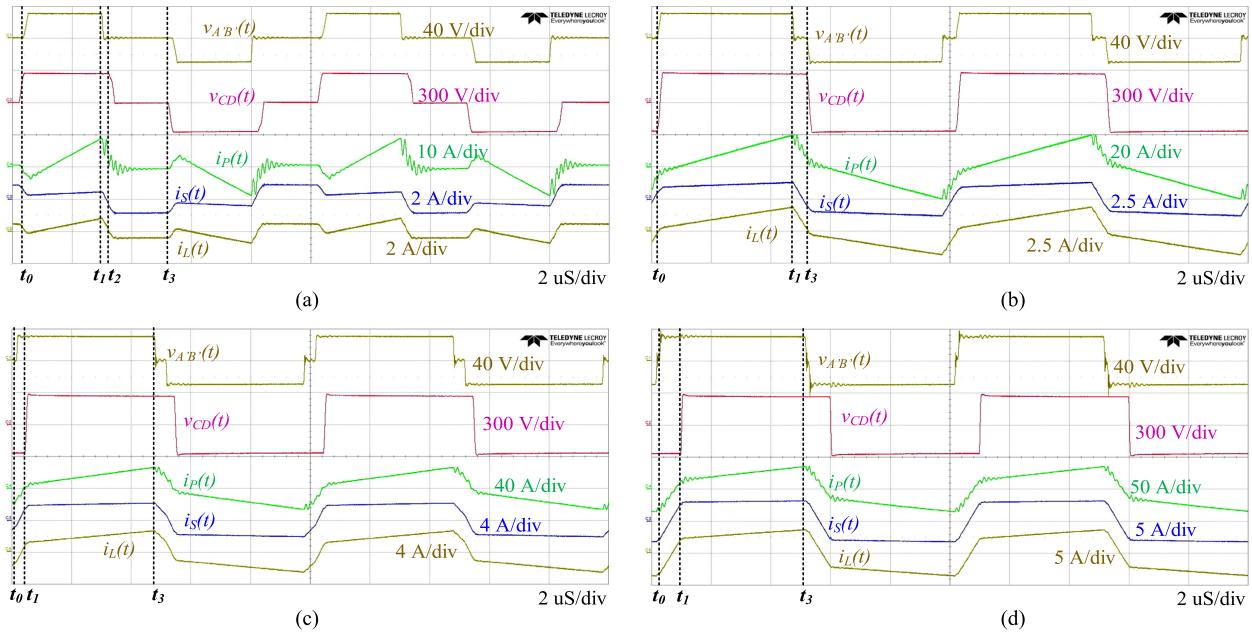

Fig. 20. Experimental waveforms for $V_{\text{in}} = 37.5$ V, $V_o = 270$ V, and $n = 8$. (a) Mode 1, $P = 49$ W. (b) Boundary between modes 1 and 4, $P = 253$ W. (c) Mode 4, $P = 481$ W. (d) Mode 4, $P = 731$ W.

the switching instant current in series inductor is not sufficient enough to provide complete ZVS for all active devices. However, the auxiliary inductor current ensures complete ZVS as the intrabridge duties D_1 and D_2 are equal to 1. Fig. 19(b)–(d) shows that the switching instant current of the series inductor is sufficient to achieve complete ZVS of all the MOSFETs. Hence circulating current generated by auxiliary inductors is undesirable at these operating conditions.

Fig. 20 shows the experimental results of LLL tank based VF-DAB operated with $V_{\text{in}} = 37.5$ V and $V_o = 270$ V at variable load conditions. It can be observed from Fig. 20(a) that at low power region, both auxiliary inductor current and series inductor current contribute to the ZVS of the MOSFETs.

Fig. 20(b) shows that when the output power for the given input voltage condition is 253 W, the converter operates at boundary condition of modes 1–4. It can be seen that series inductor current during switching instant t_3 is zero. Under this condition, complete ZVS for the all MOSFETs is achieved entirely by the current through the auxiliary inductors. The operating mode changes from 1 to 4 as the load is progressively increased. Fig. 20(c) and (d) shows the mode 4 operation of the converter at output power of 481 and 731 W, respectively. It is observed

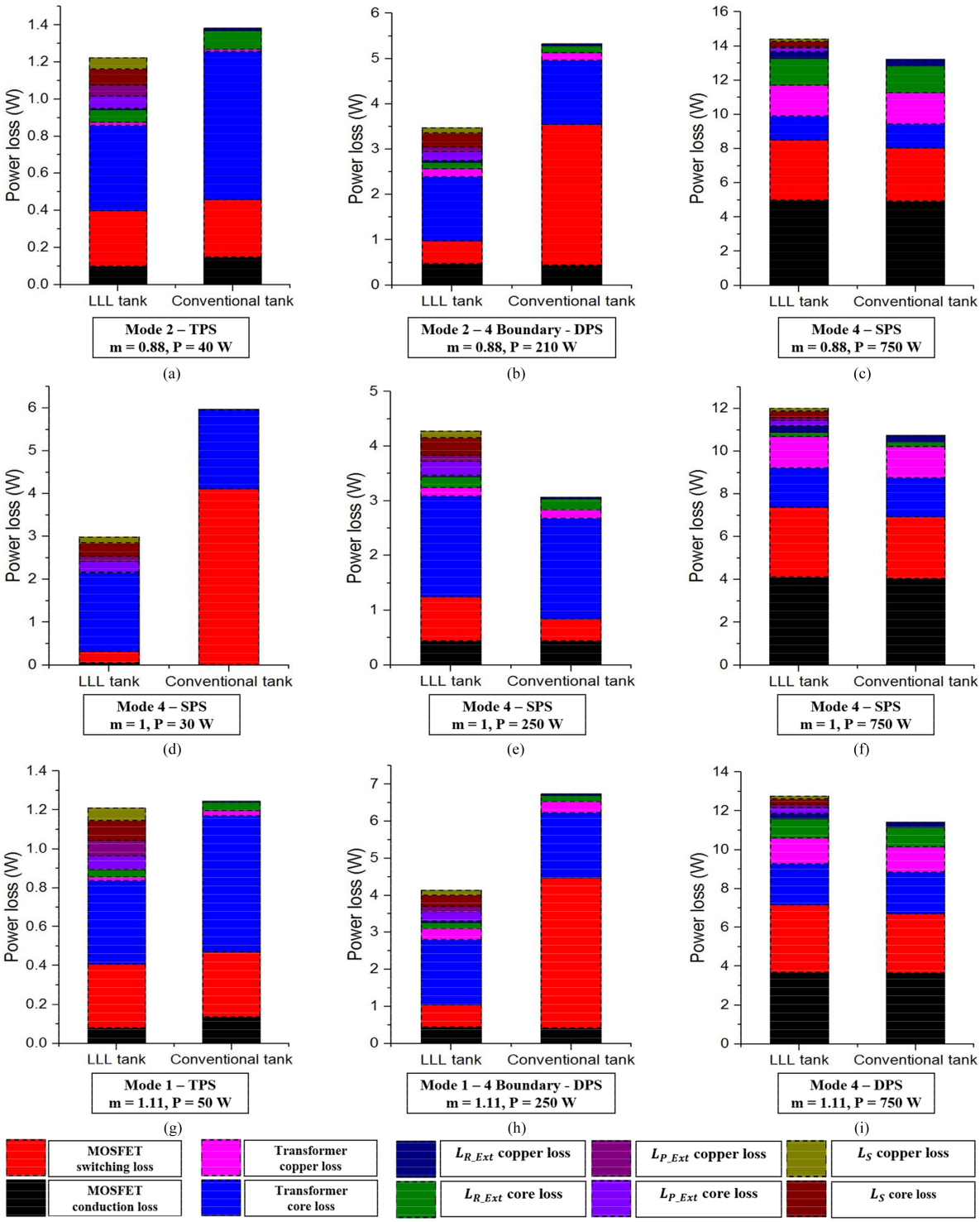

Fig. 21. Power loss analysis for various load and voltage gain.

from these results that the switching instant current in the series inductor alone can satisfactorily achieve complete ZVS of all the MOSFETs.

The experimental results suggest that the combined effect of auxiliary inductor and series inductor energies is helpful in achieving complete ZVS for the entire operating range of the converter. The experimental results of the LLL tank based VF-DAB are in accordance with the analysis presented in Section IV. A performance comparison of the LLL tank with the conventional inductive tank based DAB is presented in the next section.

VI. Steady-State Analysis: Loss Breakdown

Based on the previous analysis of ZVS and rms currents of the TPS-controlled DAB for both the conventional tank and the LLL

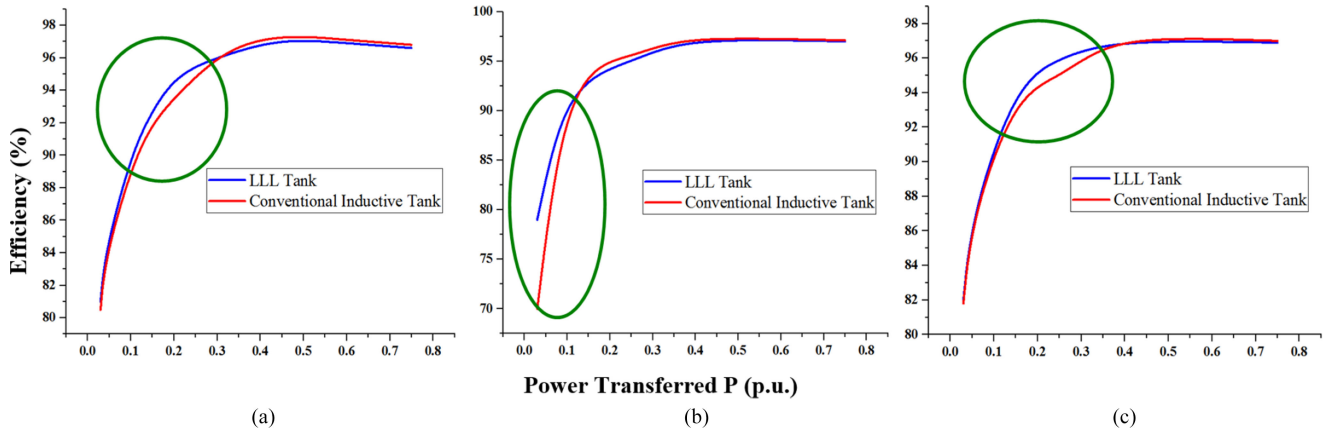

Fig. 22. Efficiency comparison of TPS-controlled LLL tank based DAB and conventional Inductive link based DAB.

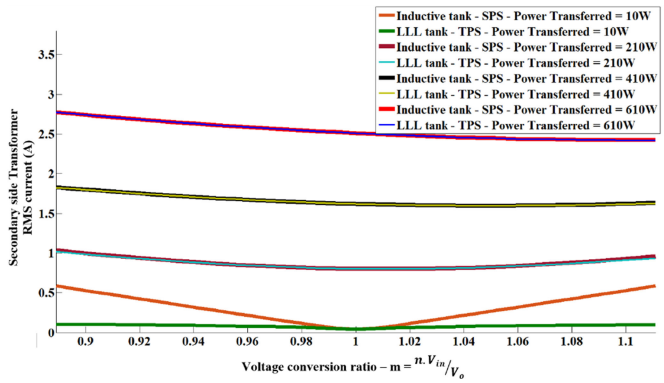

Fig. 23. Transformer rms current of TPS-controlled LLL tank based DAB- and SPS-controlled conventional inductive link based DAB.

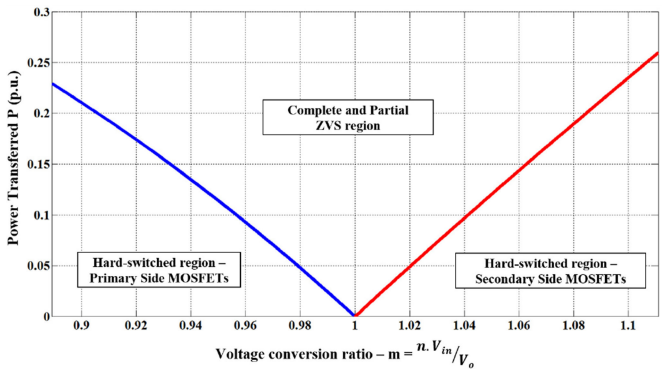

Fig. 24. ZVS range SPS-controlled conventional inductive link based DAB.

tank, loss analysis at various operating conditions is performed and analyzed. Fig. 19 provides the detailed loss breakdown for both the tank designs based on [2].

Significant remarks deduced from the loss analysis results are as follows.

1) *Operation at regions of modes 2 and 1 - TPS shown in* Fig. 5: Both the TPS-controlled conventional inductive tank and the LLL tank based VF-DAB achieve complete ZVS of all the active devices in this region. However, it is to be noted that the energy required to discharge the output capacitances of the MOSFETs comes from both the auxiliary inductors and the external series inductor in the LLL tank based DAB, while only the external series inductor aids for ZVS in the conventional inductive tank based DAB. Hence, lower values of intrabridge duties can generate the required circulating current to assist ZVS for the LLL tank compared to the conventional inductive tank based DAB for the same operating condition (P and m) due to the additional auxiliary inductor currents which are functions of the corresponding intrabridge duties. This results in reduced transformer core loss in the LLL tank based design. Also, the minimum current required during switching instance for the conventional inductive tank to achieve ZVS is higher compared to the LLL tank based tank design due to the value of the auxiliary inductance being higher compared to the series inductors. However, the LLL tank based design incurs additional auxiliary inductor core losses compared to the conventional inductive tank design. The losses related to summation of the conduction and the copper losses in the magnetics remain almost the same due to the same amount of circulating currents. Fig. 21(a) and (g) shows the loss breakdown for both the LLL tank and the conventional tank based design for mode 2 – TPS ($m < 1$) and mode 1 – TPS ($m > 1$), respectively. Hence, the overall efficiencies at these regions remain almost the same for both the tank designs.
2) *Operation at Partial ZVS region shown in* Fig. 5: The LLL tank based DAB achieves complete ZVS due to the current in the additional auxiliary inductor, while the energy in the series inductor of the conventional tank design is not sufficient enough to discharge the capacitance of the MOSFETs. Hence the switching losses of the conventional inductive tank tend to get higher as the operating region moves towards modes 2–4 boundary for $m < 1$, modes 1–4 boundary for $m > 1$ and at no load condition for $m = 1$. These mode boundaries are clearly shown in Fig. 10. Fig. 21(b), (h), and (d) shows the loss breakdown for both the LLL tank and the conventional inductive tank based design for modes 2– 4 boundary, modes 1–4 boundary,

TABLE IV
COMPARISON OF DIFFERENT MODULATION STRATEGIES

HF Reactive link	Modulation Technique	Soft-switching range Soft-switching range	Circulating current characteristics	Power density
Traditional Inductive tank	SPS modulation [5]–[9]	Limited ZVS range. Devices are hard-switched at certain operating conditions	Higher circulating current for wide range voltage variations	Low due to limitations in switching frequency and poor efficiency at certain operating regions
Traditional Inductive tank	EPS and DPS modulation [10]–[19]	Increased ZVS range than SPS control of inductive tank. Devices are still hard-switched at certain operating conditions	Reduced circulating current compared to SPS control of Inductive tank	Slightly higher power density compared to SPS control of inductive tank due to increased efficiency
Traditional Inductive tank	TPS modulation [3], [20]–[27]	Complete or partial ZVS for wide voltage variations and load conditions	Reduced circulating current compared to DPS control of inductive tank	Slightly higher power density compared to EPS and DPS control of inductive tank
LLL tank	Proposed TPS modulation	Complete ZVS for wide voltage variations and load conditions	Very slightly increased circulating current compared to TPS control of traditional Inductive tank at certain operating conditions especially at higher loads	Higher compared to TPS control of Inductive tank due to complete ZVS achievement

and at very light load condition for $m = 1$, respectively. During the modes 2– 4 boundary, all the primary side MOSFETs undergo ZCS and two of the four MOSFETs in the secondary side bridge undergo ZCS. Also during modes 1–4 boundary, all the secondary side MOSFETs undergo ZCS and two of the four MOSFETs in the primary side bridge undergo ZCS. When $m = 1$ at no load, all the MOSFETs on both the bridges undergo ZCS. These regions limit the optimal switching frequency of the conventional inductive tank based design to a lower value due to complete loss of ZVS.

3) *Operation at regions of mode 4 - shown in* Fig. 5: Both the TPS-controlled conventional inductive tank and the LLL tank based VF-DABs achieve complete ZVS of all the active devices in this region. During this region, the current through the series inductor during switching instances is sufficient to achieve complete ZVS of all the MOSFETs and the circulating current through the auxiliary inductors creates additional conduction loss along with its core loss in the LLL tank based design. Also the turn-OFF loss in the devices of the LLL tank based design is slightly higher compared to the conventional tank based design due to the additional current during switching instances resulting from the circulating energy in the tank. Fig. 21(c), (e), and (f) shows the loss breakdown for both the LLL tank and the conventional tank based TPS-controlled VF-DABs for mode 4 – SPS and Fig. 21(i) shows the comparative loss breakdown analysis for mode 4 – DPS. During this region, the conventional inductive tank based design is slightly more efficient compared to the LLL tank based design.

Fig. 22 shows the efficiency comparison of the TPS-controlled LLL tank based DAB and TPS-controlled conventional inductive link based DAB. Fig. 22(a) shows the efficiency curve for voltage conversion ratio $m = 0.889$ ($nV_{\rm in} < V_o$), Fig. 22(b) for $m = 1$ ($nV_{\rm in} = V_o$), and Fig. 22(c) for $m = 1.111$ ($nV_{\rm in} > V_o$). The regions marked by the green ellipse show where the LLL tank based DAB has significantly better efficiencies over the conventional inductive tank based DAB where it is in the partial ZVS regions shown in Fig. 5. The conventional inductive tank based DAB has slightly better efficiencies than the LLL tank based DAB in the region where the converter is operated at mode 4 due to the additional losses because of the auxiliary inductor. But it should be noted that the addition of parallel auxiliary inductors in the tank ensure complete ZVS in the entire operating range of the converter which will help to push the converters optimal switching frequency to higher values. Moreover, the difference between the two efficiency curves at the region enclosed by the green ellipse becomes significantly large as the switching frequency of the converter is pushed higher. However, the region outside the ellipse remains almost the same as the additional losses in the auxiliary inductor can be controlled by proper design considerations.

It should be noted that although there are some additional losses at some operating conditions in the LLL tank based DAB converter compared to the conventional DAB, the LLL tank enables complete ZVS operation of the conventional DAB for all operating conditions irrespective of the load and the voltage gain. This is critical for increasing switching frequencies in a DAB converter typically above 250 kHz.

The performance comparison of some widely used modulation strategies of VF-DAB converters is presented in the next section.

VII. PERFORMANCE COMPARISON

This section provides the performance comparison of TPS-controlled LLL tank based VF-DAB to the other modulation techniques for the conventional inductive tank based VF-DAB. Fig. 23 shows the comparative analysis of the circulating current of SPS-controlled conventional tank based VF-DAB and TPS-controlled LLL tank based VF-DAB.

TPS control significantly reduces the circulating current when operated under modes 1 and 2 thereby reducing the rms current through the magnetics and active devices. However, as the converter operation moves toward mode 4 operation in TPS control, the rms currents for both SPS and TPS control remain almost the same.

Fig. 24 shows the soft-switching range of SPS-controlled VF-DAB for an ideal switch. The active devices are hard-switched especially at light loads where the transformer turns ratio does not match the output to input voltage ratio ($n \neq V_{\rm in}/V_o$). However, the LLL tank based DAB with TPS control provides complete ZVS in the entire operating region of the converter.

The comparative analysis of the LLL tank based TPS-DAB with SPS, DPS, and TPS modulations for the conventional inductive link based DAB is presented in Table IV.

The TPS modulation scheme in the conventional inductive link provides reduced circulating currents compared to SPS, DPS, and EPS modulation schemes. However, all the fixed frequency modulation techniques for the conventional inductive link tank fail to achieve complete ZVS of the active devices for the entire operating conditions, while the TPS-controlled LLL tank based design provides full range ZVS for the entire operating conditions with reduced circulating currents.

VIII. Conclusion

This paper discusses the limitations of the conventional TPS-controlled inductive HF tank based VF-DAB converter in terms of soft switching performance, and analyses the region where complete ZVS is lost for various converter gains. A detailed design procedure for a modified HF tank that incorporates additional passive auxiliary inductors connected in parallel (LLL tank) to the primary and the secondary active bridges to achieve complete ZVS in the entire operating region of the converter is presented. *The modification in the tank design ensures complete ZVS in the entire operating range of the converter which is instrumental in operating VF-DAB converters at higher optimal switching frequencies*. The performance of the TPS-controlled LLL tank is experimentally evaluated with a 1 kW VF-DAB prototype. The experimental results show complete ZVS for various load conditions and voltage gains of the converter. A comparative loss breakdown analysis is provided for the TPS-controlled LLL tank VF-DAB and the conventional inductive link VF-DAB followed by efficiency results. A significant improvement in efficiencies of the TPS-controlled LLL tank based design is observed over the conventional inductive tank based VF-DAB due to the elimination of partial ZVS region. The LLL tank based design has slightly better efficiencies compared to the conventional inductive tank based VF-DAB when operated at mode 2 ($m < 1$) and mode 1 ($m > 1$) region. However, the conventional inductive HF tank has slightly better efficiency over the LLL tank based DAB when operated at mode 4 due to the additional losses incurred by the auxiliary inductors. Efficiency results and comparison with some widely used modulation strategies of DAB converters are also presented to emphasize the effectiveness of the TPS-controlled LLL tank based VF-DAB.

References

[1] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[2] F. Krismer, *Modeling and Optimization of Bidirectional Dual Active Bridge DC–DC Converter Topologies*. Zurich, Switzerland: Eidgenössische Technische Hochschule, No. 19177, 2010.

[3] W. Choi, K. M. Rho, and B. H. Cho, "Fundamental duty modulation of dual-active-bridge converter for wide-range operation," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4048–4064, Jun. 2016.

[4] K. Wu, C. W. de Silva, and W. G. Dunford, "Stability analysis of isolated bidirectional dual active full-bridge dc–dc converter with triple phase-shift control," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2007–2017, Apr. 2012.

[5] R. W. DeDoncker, M. H. Kheraluwala, and D. M. Divan, "Power conversion apparatus for dc/dc conversion using dual active bridges," U.S. Patent 5 027 264, June 25, 1991.

[6] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Dec. 1992.

[7] R. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[8] M. H. Kheraluwala and R. W. De Doncker, "Single phase unity power factor control for dual active bridge converter," in *Proc. Conf. Rec. 1993 IEEE Ind. Appl. Conf. 28th IAS Annu. Meeting*, 1993, pp. 909–916.

[9] A. Rodriguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control, "*IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, Feb. 2015.

[10] A. R. Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a dual active bridge for bidirectional dc/dc conversion," in *Proc. 2010 IEEE Energy Convers. Congr. Expo.*, 2010, pp. 1129–1135.

[11] S. Inoue and H. Akagi, "A bidirectional dc–dc converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, Nov. 2007.

[12] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional dc–dc converter for power distribution in microgrid," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4667–4680, Nov. 2012.

[13] G. Oggier *et al.*, "Extending the ZVS operating range of dual active bridge high-power dc–dc converters," in *Proc. 2006 37th IEEE Power Electron. Spec. Conf.*, 2006, pp. 1–7.

[14] G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1826–1838, Jul. 2009.

[15] G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge dc-dc converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr. 2011.

[16] G. D. Demetriades and H.-P. Nee, "Characterization of the dual-active bridge topology for high-power applications employing a duty-cycle modulation," in *Proc. 39th IEEE Power Electron. Spec. Conf.*, Rhodes, Greece, Jun. 2008, pp. 2791–2798.

[17] B. Zhao, Q. Song, and W. Liu, "Power characterization of isolated bidirectional dual-active-bridge dc–dc converter with dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4172–4176, Sep. 2012.

[18] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc–dc converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.

[19] H. Bai, Z. Nie, and C. C. Mi, "Experimental comparison of traditional phase-shift, dual-phase-shift, and model-based control of isolated bidirectional dc–dc converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1444–1449, Jun. 2010.

[20] M. A. Moonem and H. Krishnaswami, "Analysis and control of multi-level dual active bridge dc-dc converter," in *Proc. 2012 IEEE Energy Convers. Congr. Expo.*, 2012, pp. 1556–1561.

[21] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional dc–dc converter with dual-phase-shift control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4458–4467, Oct. 2013.

[22] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional dc–dc converter based on dual-phase-shift control for dc distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

[23] H. Zhou and A. M. Khambadkone, "Hybrid modulation for dual-active-bridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1434–1442, Jul. 2009.

[24] K. Wu, C. W. de Silva, and W. G. Dunford, "Stability analysis of isolated bidirectional dual active full-bridge dc–dc converter with triple phase-shift control," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2007–2017, Apr. 2012.

[25] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[26] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: comprehensive analysis and experimental verification," in *Proc. 2008 34th Annu. Conf. IEEE Ind. Electron.*, Orlando, FL, USA, 2008, pp. 909–915.
[27] B. Zhao, Q. Song, W. Liu, G. Liu, and Y. Zhao, "Universal high-frequency-link characterization and practical fundamental-optimal strategy for dual-active-bridge dc–dc Converter under PWM plus phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6488–6494, Dec. 2015.
[28] W. Feng and F. C. Lee, "Optimal trajectory control of LLC resonant converters for soft start-up," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1461–1468, Mar. 2014.
[29] W. Chen and Z. Lu, "Investigation on topology for Type-4 LLC resonant dc–dc converter," in *Proc. 2008 IEEE Power Electron. Spec. Conf.*, 2008, pp. 1421–1425.
[30] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "ZVS soft switching boundaries for dual active bridge DC-DC converters using frequency domain analysis," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–1.
[31] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J. W. Kolar, "Switching control strategy for full ZVS soft-switching operation of a dual active bridge ac/dc converter," in *Proc. 2012 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Orlando, FL, USA, 2012, pp. 1048–1055.
[32] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Charge-based ZVS soft switching analysis of a single-stage dual active bridge ac–dc converter," in *Proc. 2013 IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, 2013, pp. 4820–4829.
[33] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS modulation of single-phase single-stage bidirectional DAB ac–dc converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014.
[34] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.
[35] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, Feb. 2015, doi: 10.1109/TPEL.2014.230985.

Shiva S. Muthuraj (S'14) received the B.E. degree in electronic and electronics engineering from the Thiagarajar College of Engineering, Madurai, India, and the M.Sc. degree in automation and control from the Electrical and Computer Engineering (ECE) Department, National University of Singapore (NUS), Singapore. He is currently working toward the Ph.D. degree in the Electrical Machines and Drives Laboratory, ECE Department, NUS.

His research focuses on analysis, design, and optimization of high power density power electronic systems.

V. K. Kanakesh received the M.Tech. degree in electrical engineering from the Indian Institute of Technology Bombay, Mumbai, India, in 2014.

In 2014, he joined the National University of Singapore, Singapore, where he is currently working as a Research Engineer and is involved in the development of bidirectional cascaded dc–ac converter for UPS application. His main research interests include power electronic interfaces for utility system and high-frequency-link power conversion.

Pritam Das (S'09–M'12–SM'13) received the Master of Applied Science and Ph.D. degrees, both in electrical engineering from the University of Western Ontario, London, ON, Canada, in 2005 and 2010, respectively.

From 2010 to 2011, he was a Postdoctoral Fellow in the Queen's Centre for Energy and Power Electronics Research, Queen's University, Kingston, ON, Canada, and with PE Consultants, Kingston, ON, Canada. From 2011 to 2013, he was with Murata Power Solutions, Toronto, ON, Canada, as an Electrical Design Engineer. He has published more than 65 technical papers in referred journals and conferences and two applied US patents. He also founded PowerEff, a power solutions company. His present research is focused on developing reliable and high-efficiency high-power LED drivers for smart commercial lighting, ac–dc and dc–dc power converters for e-actuation in more-electric aircrafts, wide-band gap devices based power converters for electrified-transportation, data centers, energy storage in smart grid, etc.

Sanjib Kumar Panda (S'86–M'91–SM'01) received the B.Eng. degree from the South Gujarat University, Surat, India, in 1983, the M.Tech. degree from the Indian Institute of Technology, Banaras Hindu University, Varanasi, India, in 1987, and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1991, all in electrical engineering.

Since 1992, he has been holding a Faculty Position in the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, and currently serving as an Associate Professor and the Director of the Power & Energy Research Area. He has published more than 200 peer reviewed research papers, coauthored one book and contributed to several book chapters, and six patents. His research interests include high-performance control of motor drives and power electronic converters, condition monitoring and condition based maintenance, building energy efficiency, etc.

Dr. Panda received the Cambridge-Nehru Scholarship and M. T. Mayer Graduate Scholarship during his Ph.D. study (1987–1991). He is serving as an Associate Editor of several IEEE Transactions and the Editor of the *Journal of Power Electronics*, South Korea. He has served in various capacities for the two key conferences IEEE Power Electronics and Drive Systems Conference and IEEE International Conference on Sustainable Energy Technologies Conference series organized and managed by the IEEE Joint Industry Applications Society/ Power Electronics Society (PELS) Society Chapter, Singapore Section. He has served the IEEE Section Congress 2014 as a member of the Program Committee. He is serving as the IEEE R-10 Asia Pacific Liaison Officer for the IEEE PELS. He has received the IEEE Third Millennium Medal, the IEEE Singapore Section Outstanding Volunteer Award in 2010, and the IEEE Region-10 Outstanding Volunteer Award in 2014.