Single-Phase Inverter With Energy Buffer and DC–DC Conversion Circuits

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***Abstract*—This paper proposes a new single-phase inverter topology and describes the control method for the proposed inverter. The inverter consists of an energy buffer circuit, a dc–dc conversion circuit and an H-bridge circuit. The energy buffer circuit and H-bridge circuit enable the proposed inverter to output a multilevel voltage according to the proposed pulse width modulation (PWM) technique. The dc–dc conversion circuit can charge the buffer capacitor continuously because the dc–dc conversion control cooperates with the PWM. Simulation results confirm that the proposed inverter can reduce the voltage harmonics in the output and the dc–dc conversion current in comparison to a conventional inverter consisting of a dc–dc conversion circuit and H-bridge circuit. Experiments demonstrate that the proposed inverter can output currents of low total harmonic distortion and have higher efficiency than the conventional inverter. In addition, it is confirmed that these features of the proposed inverter contribute to the suppression of the circuit volume in spite of the increase in the number of devices in the circuit.**

***Index Terms*—DC–DC conversion, energy buffer circuit, pulse width modulation (PWM), single-phase inverter.**

I. Introduction

SINGLE-PHASE inverters are commonly used in many power applications. In recent years, single-phase inverters have been used as components of microgrid systems. In these systems, single-phase inverters are used as interfaces for renewable energy sources, such as fuel cells and photovoltaic energy, or for energy storage devices, such as batteries and ultracapacitors with the grid [1]–[7].

Various types of single-phase transformerless inverters, which have the advantages of a small size and light weight [8], have been studied [9]–[12]. Among these, H-bridge inverters have a relatively simple structure. The H-bridge inverters, however, suffer from common-mode voltage unlike inverters such as H5 inverter, HERIC inverter, and H6 inverters. In applications using batteries and ultracapacitors with output ratings of less than several hundreds of watts, the H-bridge inverter may be able to perform without the influence of the common-mode voltage. On the other hand, in applications with photovoltaic cells, the common-mode voltage causes a leakage current through parasitic capacitors between the photovoltaic cells and the ground. The leakage current degrades the performance and reliability of the inverter. However, this disadvantage can be mitigated with passive filters [13]–[15] and therefore the H-bridge inverter can be used in wide applications.

An inverter consisting of an H-bridge circuit involving a dc–dc conversion circuit can expand the voltage amplitude of the output. Therefore, this type of inverter is commonly used in applications for renewable energy sources and energy storage devices with voltages that are lower than the voltage amplitudes of the grid. The typical topologies for the dc–dc conversion are boost, and buck boost converters in addition to many other types of converters derived from these chopper topologies, including chopper inductors [16]–[18].

Inverters with an energy buffer circuit have been previously reported in [19]–[22]. An energy buffer circuit consists of switches and buffer capacitors and behaves like a charge pump circuit. Because the energy buffer circuit does not include any inductors, it can be designed with a compact form. The operation of the circuit allows the inverter to step up its dc-link voltage with the help of the voltage across the buffer capacitors. Furthermore, it allows the inverter to yield a multilevel output voltage. It is well known that in multilevel inverters, the output voltage can reduce the ripple in the output current, resulting in a lower output filter inductance [23]–[32]. Although the multilevel inverters have more output voltage vectors than the inverter with an energy buffer circuit, they generally cannot expand the voltage amplitude of the output.

However, inverters with only an energy buffer circuit have difficulty regulating the voltage of the buffer capacitor because the capacitor can be charged only when the inverter outputs a low voltage [20], [21]. Therefore, inverters containing both an energy buffer circuit and a dc–dc conversion circuit have been proposed [33], [34]. The variation in the energy of the buffer capacitor can be compensated for by the dc–dc conversion circuit. The multilevel energy buffer (MEB) inverter, which consists of the same circuit combination, has been proposed as part of the MEB microinverter in [33] and has been reported to have high efficiency and to allow a small filter inductance.

This paper proposes a new single-phase inverter topology with an energy buffer circuit, a dc–dc conversion circuit, and an H-bridge circuit. It has different configuration from the MEB inverter in [33], in particular, in terms of connection of the dc–dc conversion circuit. The most important thing is that the difference brings the following strong advantages over the MEB

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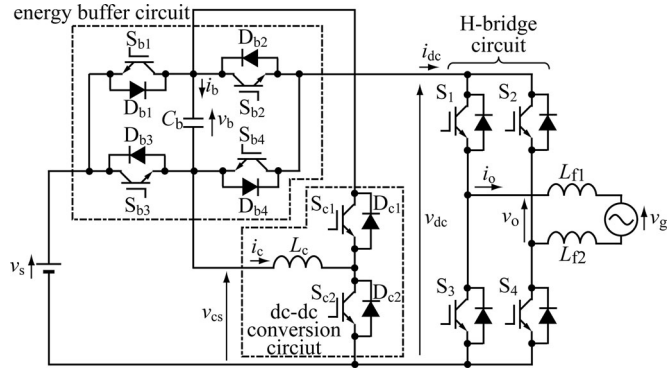

Fig. 1. Configuration of the proposed inverter.

inverter to the proposed inverter: Although the dc–dc conversion circuit in the MEB inverter cannot charge or discharge the buffer capacitor during the step-up operation because of the circuit configuration, the dc–dc conversion circuit in the proposed inverter can continuously charge or discharge it regardless of the operation mode. For this reason, the voltage variation of the buffer capacitor of the proposed inverter can be suppressed (refer to Appendix A) or the capacitance of the proposed inverter can be a smaller value. Furthermore, in general, the continuous charge operation is more effective than the intermittent charge operation; therefore, the proposed inverter can be operated with more effective performance than the MEB inverter.

For the proposed inverter, a pulse width modulation (PWM) technique for dc–ac and ac–dc conversions and a control technique for the dc–dc conversion circuit are described in this paper. The energy buffer circuit and H-bridge circuit are operated according to the PWM technique and yield multilevel outputs following the voltage command signal. Control of the dc–dc conversion circuit enables the circuit to charge the buffer capacitor continuously by cooperating with the PWM. Simulation results confirm that the proposed inverter can reduce the voltage harmonics in the output and the dc–dc conversion current in comparison to a conventional inverter consisting of a dc–dc conversion circuit and an H-bridge circuit. Experiments demonstrate that the proposed inverter outputs a current with low total harmonic distortion (THD) and have higher efficiency than the conventional inverter. Furthermore, it is confirmed that these features contribute to the suppression of the circuit volume in spite of an increase in the number of devices.

II. Circuit Configuration and Control Method

A. Circuit Configuration

Fig. 1 shows the configuration of the proposed inverter, which consists of an energy buffer circuit, a dc–dc conversion circuit, and an H-bridge circuit. The inverter is connected to the grid v_g through filter inductors L_{f1} and L_{f2}. The energy buffer circuit has four switches, four diodes, and a buffer capacitor C_b. The capacitor C_b has a positive voltage v_b. The energy buffer circuit positively or negatively superimposes v_b on the supply voltage v_s and sets the dc-link voltage $v_{\rm dc}$ to one of three levels depending on the state of the signals of switches $S_{b1} - S_{b4}$, as given in Table I. When the energy buffer circuit operates in

TABLE I
Modes of Operation of Energy Buffer Circuit

	$v_{\rm dc}$	switching signals
Mode 1	$v_s - v_b$	ON: s_{b1} and s_{b4} OFF: s_{b2} and s_{b3}
Mode 2	v_s	ON: s_{b3} and s_{b4} OFF: s_{b1} and s_{b2} or ON: s_{b1} and s_{b2} OFF: s_{b3} and s_{b4}
Mode 3	$v_s + v_b$	ON: s_{b2} and s_{b3} OFF: s_{b1} and s_{b4}

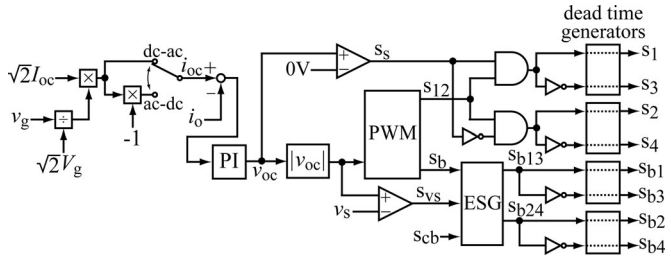

Fig. 2. Block diagrams of output voltage control for dc–ac and ac–dc conversions.

Mode 1, it steps down the dc-link voltage $v_{\rm dc}$ to $v_s - v_b$. In Mode 2, the dc-link voltage $v_{\rm dc}$ is equal to v_s. The stepped-up voltage $v_s + v_b$ is provided when the energy buffer circuit operates in Mode 3. Although, in Modes 1 and 3, the energy in the buffer capacitor is changed by the dc-link current $i_{\rm dc}$, the dc–dc conversion circuit consisting of two switches, two diodes, and the chopper inductor L_c is operated to maintain v_b at a constant level. The H-bridge circuit performs dc–ac or ac–dc conversion, cooperating with the energy buffer circuit.

B. Control for DC–AC and AC–DC Conversions

Fig. 2 shows control block diagrams capable of both dc–ac and ac–dc conversions. The output voltage command signal $v_{\rm oc}$ is generated by a proportional and integral (PI) controller so that the output current $i_{\rm o}$ follows the output current command signal $i_{\rm oc}$, which is synchronized with the grid voltage v_g. Based on the absolute value $|v_{\rm oc}|$ of the output voltage command signal, the signals s_{12} and s_b are generated in accordance with the PWM technique. The durations t_{12} and t_b of the ON-state of signals s_{12} and s_b, respectively, are calculated using the following equations defined for three ranges of $|v_{\rm oc}|$:

Range I: $0 \le |v_{\rm oc}| \le v_s - v_b$

$$t_{12} = \frac{|v_{\rm oc}|}{v_s - v_b} T, \tag{1a}$$

$$t_b = 0. \tag{1b}$$

Range II: $v_s - v_b \le |v_{\rm oc}| \le v_s$,

$$t_{12} = T, \tag{2a}$$

$$t_b = \frac{|v_{\rm oc}| - (v_s - v_b)}{v_b} T. \tag{2b}$$

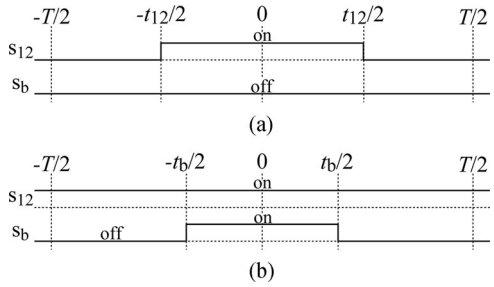

Fig. 3. Signal sequences during PWM period when $|v_{\rm oc}|$ is in (a) Range I and (b) Range II or III.

TABLE II
TRUTH TABLE FOR ESG

Input			Output		Mode of energy buffer circuit
s_b	s_{vs}	s_{cb}	s_{b13}	s_{b24}	
0	0	0	1	0	Mode 1
0	0	1	1	0	
0	1	0	0	1	Mode 3
0	1	1	0	1	
1	0	0	0	0	Mode 2
1	0	1	1	1	
1	1	0	0	0	
1	1	1	1	1	

Range III: $v_s \le |v_{\rm oc}| \le v_s + v_b$

$$t_{12} = T, \tag{3a}$$

$$t_b = \frac{(v_s + v_b) - |v_{\rm oc}|}{v_b} T \tag{3b}$$

where *T* is the PWM period. The signals are generated based on these durations, as shown in Fig. 3. The state of $s_{\rm vs}$ is given by comparing $|v_{\rm oc}|$ with v_s. Based on s_b and $s_{\rm vs}$, the energy buffer circuit signal generator (ESG), being a logic circuit, selects the appropriate mode for the energy buffer circuit, regardless of $s_{\rm cb}$, and assigns corresponding states to s_{b13} and s_{b24}, as given in Table II. When s_b is in the ON-state, the energy buffer circuit operates in Mode 2, regardless of $s_{\rm vs}$. In contrast, when s_b is in the OFF-state, if $s_{\rm vs}$ is in the ON-state, Mode 3 is selected by ESG; otherwise, Mode 1 is selected. As shown in Table I, operation in Mode 2 can be implemented under two sets of signal conditions, which are determined based on the state of $s_{\rm cb}$ as follows: When $s_{\rm cb}$ is in the ON-state, s_{b13} and s_{b24} are also in the ON-state; otherwise, s_{b13} and s_{b24} are in the OFF-state.

Using this control technique, the energy buffer circuit can generate the dc-link voltage waveform conceptually shown in Fig. 4(a). While $|v_{\rm oc}|$ is in Range II or III, the dc-link voltage $v_{\rm dc}$ has a PWM waveform with levels of $v_s - v_b$, v_s, and $v_s + v_b$. Conversely, while $|v_{\rm oc}|$ is in Range I, $v_{\rm dc}$ is maintained at $v_s - v_b$. The variation of the dc level is converted to a voltage variation of the ac level by the H-bridge circuit and is formed into an approximately sinusoidal wave following $v_{\rm oc}$, as shown in Fig. 4(b). The H-bridge circuit is operated based on s_s and s_{12}. The signal s_s, which expresses the sign of $v_{\rm oc}$, is referenced to assign a polarity to the voltage with the dc level. The signal s_{12} is employed to convert the voltage of $v_s - v_b$ to a portion of

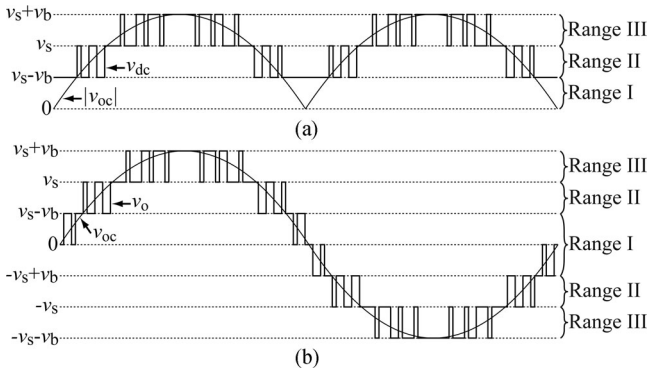

Fig. 4. Conceptual waveforms for (a) dc-link voltage $v_{\rm dc}$ and (b) output voltage $v_{\rm o}$.

an approximately sinusoidal wave with three levels, i.e., $v_s - v_b$, $-v_s + v_b$, and zero.

The MEB inverter in [33] employs a different PWM technique from this technique. The PWM technique of the MEB inverter uses the zero voltage as one of the voltage pulses, regardless of the range of $|v_{\rm oc}|$; therefore, the voltage harmonics in the output of the MEB inverter are larger than those of the proposed inverter (refer to Appendix B).

C. Control for DC–DC Conversion Circuit

The operation of the energy buffer circuit in Modes 1 and 3 changes the capacitor voltage v_b, which is controlled at a constant level by the dc–dc conversion circuit. Fig. 5 shows the modes of operation for the conversion circuit. The states of signals s_{c1} and s_{c2} for switches S_{c1} and S_{c2} in the circuit are complementary to each other. When s_{c1} is in the ON-state, current through L_c, the path of which is depicted in Fig. 5(a), charges or discharges C_b. When s_{c2} is in the ON-state, there are two possible current paths, depending on the states of s_{b1} and s_{b3} for the energy buffer circuit. When s_{b1} is in the ON-state, the current flows as shown in Fig. 5(b). As a result of switching S_{c1} and S_{c2}, the conversion circuit behaves either like a buck converter when C_b is charged or like a boost converter when C_b is discharged. Alternatively, when s_{b3} is in the ON-state, the current path is illustrated in Fig. 5(c) and the conversion circuit acts like a buck-boost converter. The former behavior of the conversion circuit can more effectively regulate v_b because the current continues flowing through C_b during a complete PWM period.

Fig. 6 shows the control block diagram for the dc–dc conversion circuit. The current command signal $i_{\rm cc}$ is calculated to maintain v_b at the command value $v_{\rm bc}$; then, the current i_c through the inductor L_c is controlled by each PI control block to follow $i_{\rm cc}$. The resulting voltage command signal $v_{\rm cc}$ is used to generate the signals s_{c1} and s_{c2} in the PWM block.

Fig. 7 shows the sequences for s_{c1} and s_{c2} during a PWM period. The duration t_c of the ON-state of s_{c2} is determined as follows. First, the duration $t_{\rm cb}$ is calculated as

$$t_{\rm cb} = \frac{v_{\rm cc} + v_b}{v_b + v_{\rm cs1}} T \tag{4}$$

where $v_{\rm cs1}$ is the value of $v_{\rm cs}$ during the time from $-t_b/2$ to $t_b/2$ in the cycle time of the PWM period. In Fig. 7, $v_{\rm cs1}$ is $v_s - v_b$

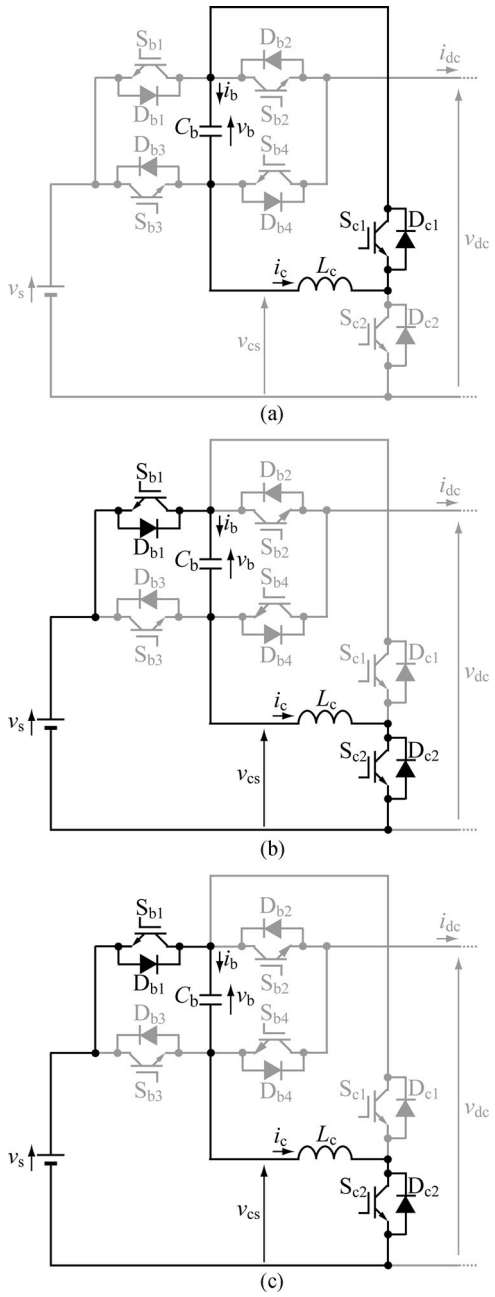

Fig. 5. Modes of operation of dc–dc conversion circuit: (a) ON-state of s_{c1}; (b) ON-states of s_{c2} and s_{b1}; and (c) ON-states of s_{c2} and s_{b3}.

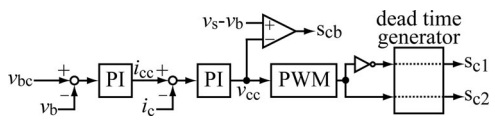

Fig. 6. Control block diagram for dc–dc conversion circuit.

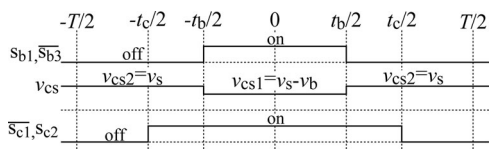

Fig. 7. Signal sequences for dc–dc conversion circuit during PWM period.

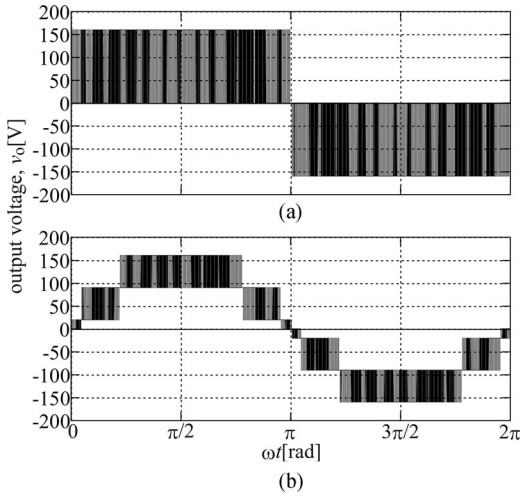

Fig. 8. Simulated waveforms of output voltages of (a) conventional inverter with $v_{\rm dc} = 160$ V and (b) proposed inverter with $v_s = 90$ V and $v_b = 70$ V. Effective value $V_{\rm oc}$ of the output voltage command signal is set at 100 V.

because s_{b1} is in the ON-state during this time. Then, comparing $t_{\rm cb}$ with t_b yields the duration t_c as follows.

If $t_{\rm cb}$ is less than t_b

$$t_c = t_{\rm cb} \tag{5}$$

otherwise

$$t_c = t_b + \frac{(v_{\rm cc} + v_b)\,T - (v_{\rm cs1} + v_b)\,t_b}{v_b + v_{\rm cs2}} \tag{6}$$

where $v_{\rm cs2}$ is the value of $v_{\rm cs}$ during the time from $-T/2$ to $-t_b/2$ and from $t_b/2$ to $T/2$ and depends on the states of s_{b1} and s_{b3} as well as $v_{\rm sc1}$. The states of the signals are determined based on the operational mode of the energy buffer circuit, i.e., whether the circuit is operated in Mode 1 or 3. Conversely, for operation in Mode 2, these signals can take any state. Therefore, in this mode, the signal state appropriate for the operation of the dc–dc conversion circuit can be selected. Generally, s_{b1} is required to be in the ON-state because this state leads to effective operation of the dc–dc conversion circuit. However, in this state, the conversion circuit cannot obtain the input voltage $v_{\rm cs}$ with a level higher than $v_s - v_b$. Therefore, if the voltage command signal $v_{\rm cc}$ is higher than $v_s - v_b$, s_{b1} is in the OFF-state. In the diagram shown in Fig. 6, $s_{\rm cb}$ is generated by comparing $v_{\rm cc}$ with $v_s - v_b$. This signal expresses the state of s_{b1} for the energy buffer circuit in Mode 2 and is used in the ESG shown in Fig. 2.

III. Simulations

A. Output Voltage and Its Harmonics

Fig. 8 compares the simulated waveforms of the output voltages on the conventional inverter shown in Fig. 9 with those for the proposed inverter. The results confirm that the proposed inverter produces a multilevel output voltage. Fig. 10 shows the harmonics in the output voltage. The maximum values of the harmonic voltage appear at 40 kHz, which corresponds with a PWM frequency. The conventional inverter has a maximum

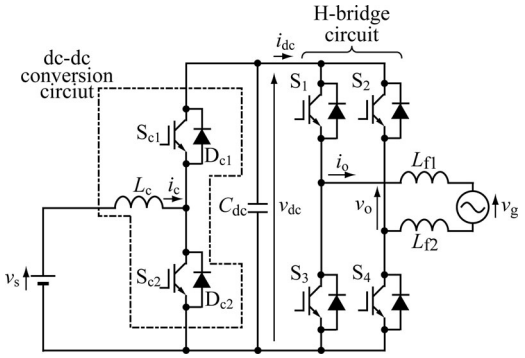

Fig. 9. Conventional inverter with dc–dc conversion circuit.

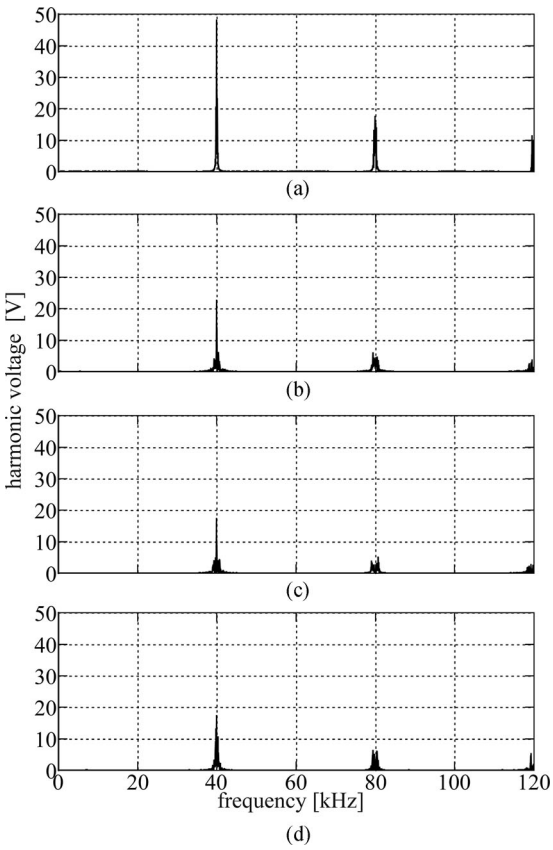

Fig. 10. Harmonics in output voltages of (a) conventional inverter with $v_{\rm dc} = 160\,{\rm V}$ and proposed inverter with (b) $v_s = 90\,{\rm V}$ and $v_b = 70\,{\rm V}$, (c) $v_s = 110\,{\rm V}$ and $v_b = 50\,{\rm V}$, and (d) $v_s = 130\,{\rm V}$ and $v_b = 30\,{\rm V}$, under $V_{\rm oc} = 100\,{\rm V}$.

voltage of 48 V, which is 2.2 times higher than the maximum of harmonic voltage produced by the proposed inverter under the conditions $v_s = 90\,{\rm V}$ and $v_b = 70\,{\rm V}$. Therefore, the proposed inverter can reduce the inductance of the filter inductors L_{f1} and L_{f2} at the same PWM frequency.

B. Charged Energy and Conversion Current

Fig. 11 shows the power P_b inputted into the buffer capacitor C_b during the operation of the energy buffer circuit and the resulting energy U_b stored in C_b during one cycle of the grid in the dc–ac conversion. The power P_b and energy U_b vary

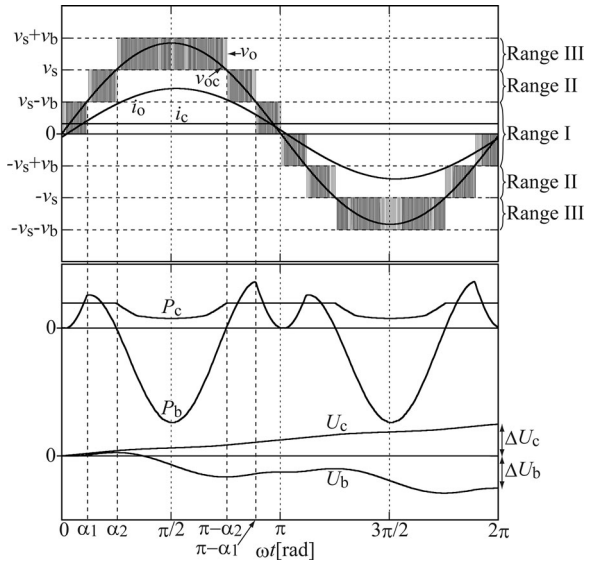

Fig. 11. Inputted powers and stored energies of C_b during one grid cycle.

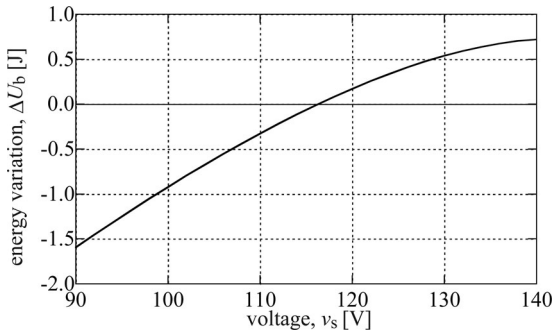

Fig. 12. Dependence of energy variation ΔU_b on voltage v_s with $V_g = 100\,{\rm V}$, $I_{\rm o} = 5\,{\rm A}$, $L_{f1} = L_{f2} = 1.5\,{\rm mH}$, and grid voltage frequency of 60 Hz.

depending on the command voltage $v_{\rm oc}$ as follows. P_b is a positive value and U_b increases when $|v_{\rm oc}|$ is in Ranges I and II; then, U_b peaks at α_2, where $|v_{\rm oc}|$ is equal to v_s. In contrast, P_b is a negative value and U_b decreases in Range III; U_b reaches a valley at $\pi - \alpha_2$. In the ac–dc conversion, the power P_b and the energy U_b vary in the opposite manner: for example, U_b increases in Range III and, otherwise, decreases.

The energy variation ΔU_b over one cycle of the grid in the dc–ac conversion is calculated as follows. It is assumed that the voltage command signal $v_{\rm oc}$ and the output current $i_{\rm o}$ vary sinusoidally and are expressed as

$$v_{\rm oc} = \sqrt{2} V_{\rm oc} \sin(\omega t), \tag{7}$$

$$i_o = \sqrt{2} I_o \sin(\omega t - \theta) \tag{8}$$

where

$$V_{\rm oc} = \sqrt{\{\omega(L_{\rm f1} + L_{\rm f2}) I_o\}^2 + V_g^2}, \tag{9}$$

$$\theta = \tan^{-1}\left(\frac{\omega(L_{\rm f1} + L_{\rm f2}) I_o}{V_g}\right). \tag{10}$$

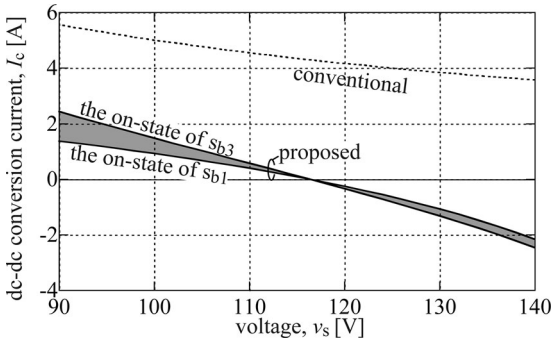

Fig. 13. Dependence of dc–dc conversion current I_c on voltage v_s with $V_g = 100\,\mathrm{V}, I_o = 5\,\mathrm{A}, L_{f1} = L_{f2} = 1.5\,\mathrm{mH}$, and grid voltage frequency of 60 Hz.

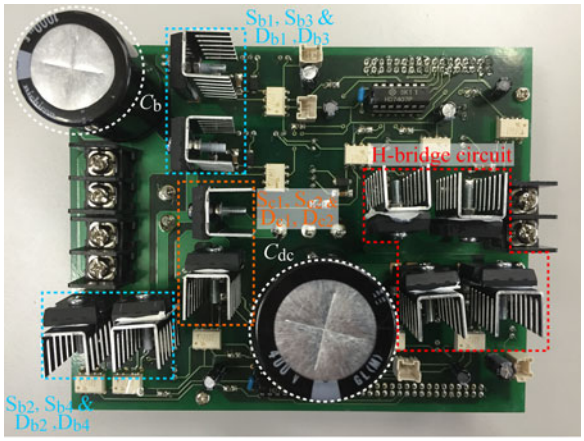

Fig. 14. Test circuit.

The variables V_g and I_o are the effective values of the grid voltage and output current, respectively, and ω is the angular frequency of the grid voltage. The energy variation is calculated in three ranges of the electrical angle ωt as follows:

For $0 \le \omega t \le \alpha_1$

$$\Delta U_{b[0,\alpha_1]} = \frac{2v_b V_{\mathrm{oc}} I_o}{\omega (v_s - v_b)} \int_0^{\alpha_1} \sin(\omega t) \sin(\omega t - \theta)\, d\omega t. \tag{11}$$

For $\alpha_1 \le \omega t \le \pi - \alpha_1$

$$\Delta U_{b[\alpha_1,\pi-\alpha_1]} = \frac{1}{\omega} \int_{\alpha_1}^{\pi-\alpha_1} \sqrt{2} I_o \sin(\omega t - \theta) \times \left\{ v_s - \sqrt{2} V_{\mathrm{oc}} \sin(\omega t) \right\} d\omega t. \tag{12}$$

For $\pi - \alpha_1 \le \omega t \le \pi$

$$\Delta U_{b[\pi-\alpha_1,\pi]} = \frac{2v_b V_{\mathrm{oc}} I_o}{\omega (v_s - v_b)} \int_{\pi-\alpha_1}^{\pi} \sin(\omega t) \sin(\omega t - \theta)\, d\omega t. \tag{13}$$

The angle α_1 represents the electrical angle at $|v_{\mathrm{oc}}| = v_s - v_b$ and is expressed as

$$\alpha_1 = \sin^{-1}\left(\frac{v_s - v_b}{\sqrt{2} V_{\mathrm{oc}}} \right). \tag{14}$$

TABLE III
EXPERIMENTAL CONDITIONS

Grid	Grid voltage, V_g	100 V
	Frequency	60 Hz
Circuit constants	Filter inductance, L_{f1} and L_{f2}	1.5 mH
	Inductance L_c in dc-dc conversion circuit	2.5 mH
	Capacitance, C_b and C_{dc}	1.0 mF

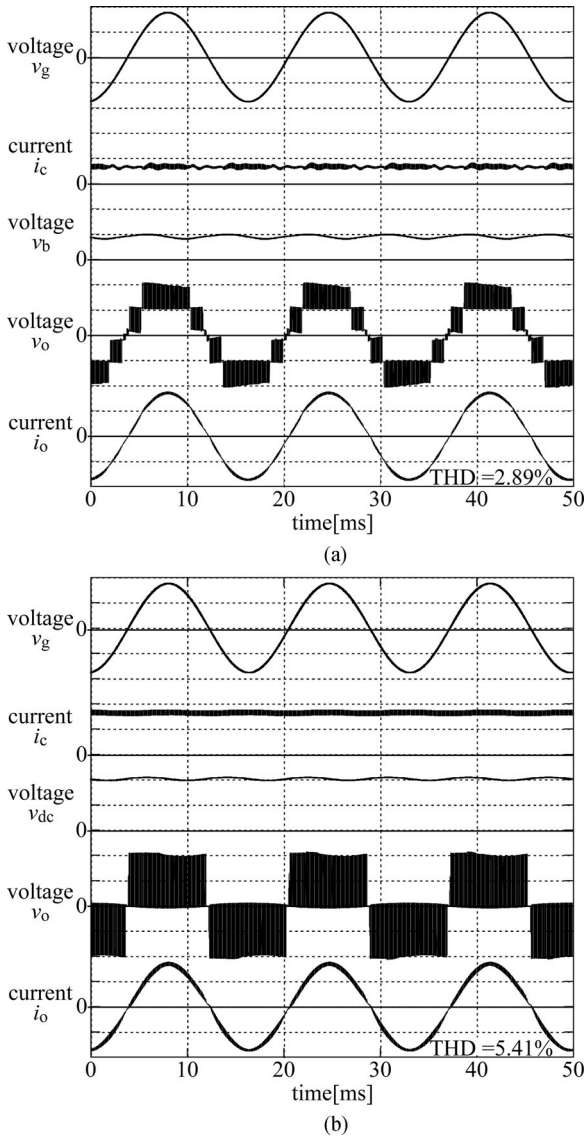

Fig. 15. Waveforms for (a) proposed inverter and (b) conventional inverter during dc–ac conversion under conditions of $P_{\mathrm{ac}} = 500\,\mathrm{W}, v_s = 90\,\mathrm{V}, v_b = 70\,\mathrm{V}$ and dc-link command voltage $v_{\mathrm{dcc}} = 160\,\mathrm{V}$ (the scales for v_g, v_b, v_{dc}, and v_o are $80\,\mathrm{V/div.}$, and those for i_c and i_o are $4.0\,\mathrm{A/div.}$).

Based on these equations, the energy variation ΔU_b over one cycle of the grid is given by

$$\Delta U_b = \frac{2I_o}{\omega} \left\{ \frac{2\alpha_1 v_s V_{\mathrm{oc}}}{v_s - v_b} - \pi V_{\mathrm{oc}} + \sqrt{2} v_s \cos\alpha_1 \right\} \cos\theta. \tag{15}$$

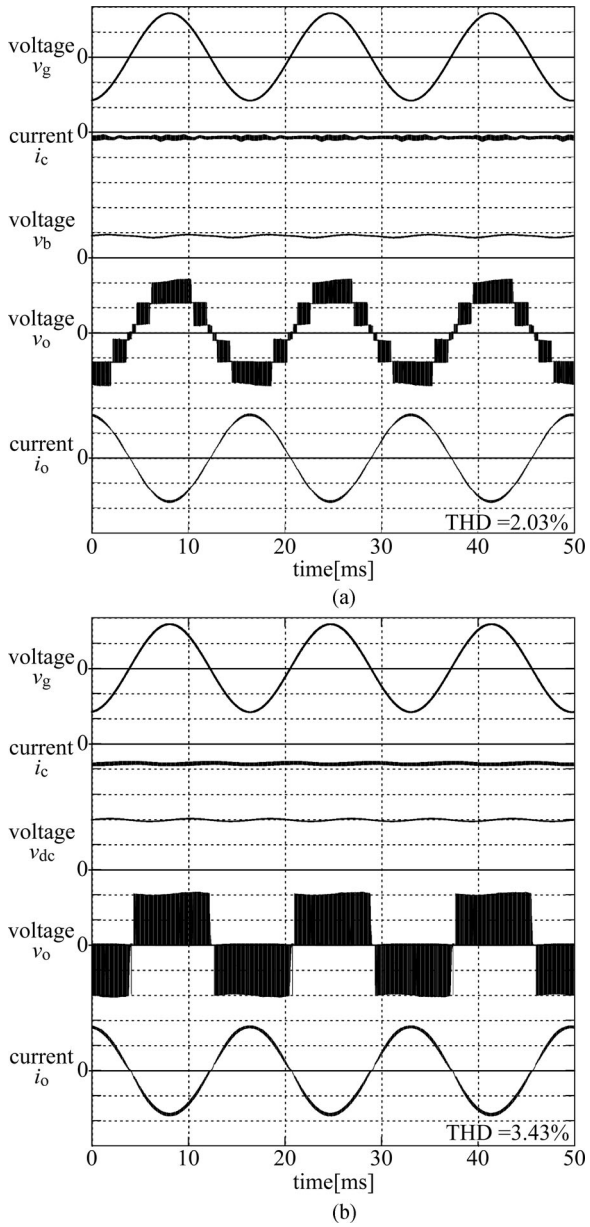

Fig. 16. Waveforms of (a) proposed inverter and (b) conventional inverter during ac–dc conversion under conditions of $P_{\rm dc} = 500\,{\rm W}$, $v_s = 90\,{\rm V}$, $v_{\rm bc} = 70\,{\rm V}$, and $v_{\rm dcc} = 160\,{\rm V}$ (the scales for v_g, v_b, $v_{\rm dc}$ and $v_{\rm o}$ are $80\,{\rm V/div.}$, and those for i_c and $i_{\rm o}$ are $4.0\,{\rm A/div.}$).

Fig. 12 shows the dependence of the energy variation ΔU_b on the dc supply voltage v_s during the dc–ac conversion. The capacitor voltage v_b is set to $160 - v_s$. It is found that the variation becomes zero only at $v_s = 117\,{\rm V}$. Therefore, when the voltage v_s is not 117 V, to compensate for energy variation and then maintain v_b at a constant value, the dc–dc conversion circuit must be operated.

The dc–dc conversion current i_c is controlled at a constant value during one cycle of the grid. The power P_c transferred into C_b from the dc–dc conversion circuit varies as shown in Fig. 11. The power varies depending on the state of the signals s_{b1} and s_{b3}. The power remains at a low level while $|v_{\rm oc}|$ is in

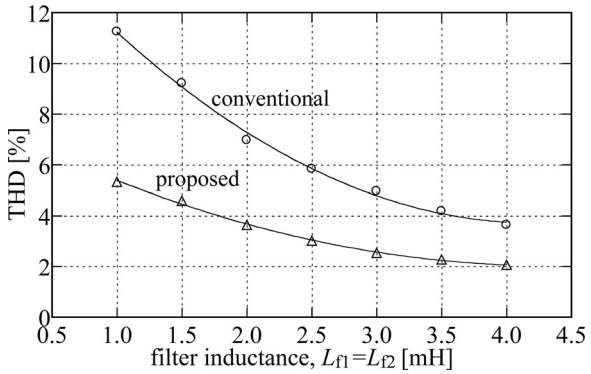

Fig. 17. Dependence of THD of output current on filter inductances in dc–ac conversion under conditions of $P_{\rm ac} = 300\,{\rm W}$, $v_s = 90\,{\rm V}$, $v_{\rm bc} = 70\,{\rm V}$ and $v_{\rm dcc} = 160\,{\rm V}$.

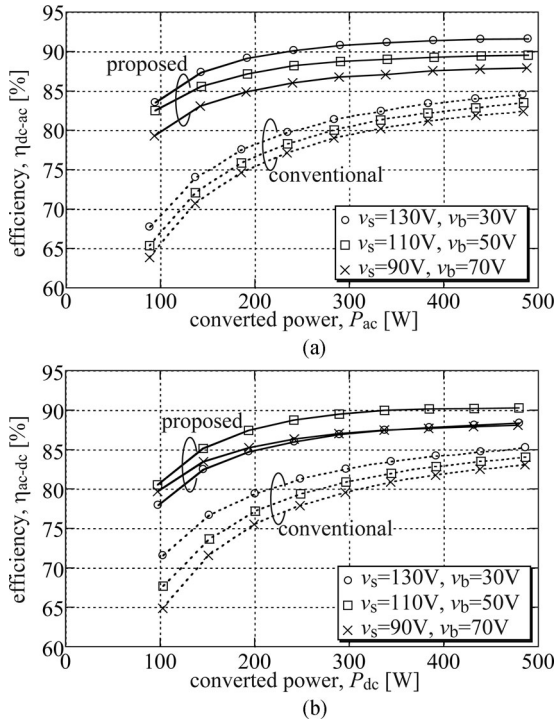

Fig. 18. Efficiencies for $\eta_{\rm dc-ac}$ and $\eta_{\rm ac-dc}$ on (a) dc–ac and (b) ac–dc conversions.

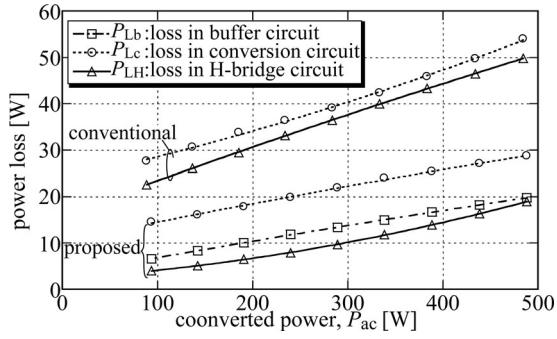

Fig. 19. Power losses in each circuit during dc–ac conversion under conditions of $v_s = 90\,{\rm V}$, $v_{\rm bc} = 70\,{\rm V}$ and $v_{\rm dcc} = 160\,{\rm V}$.

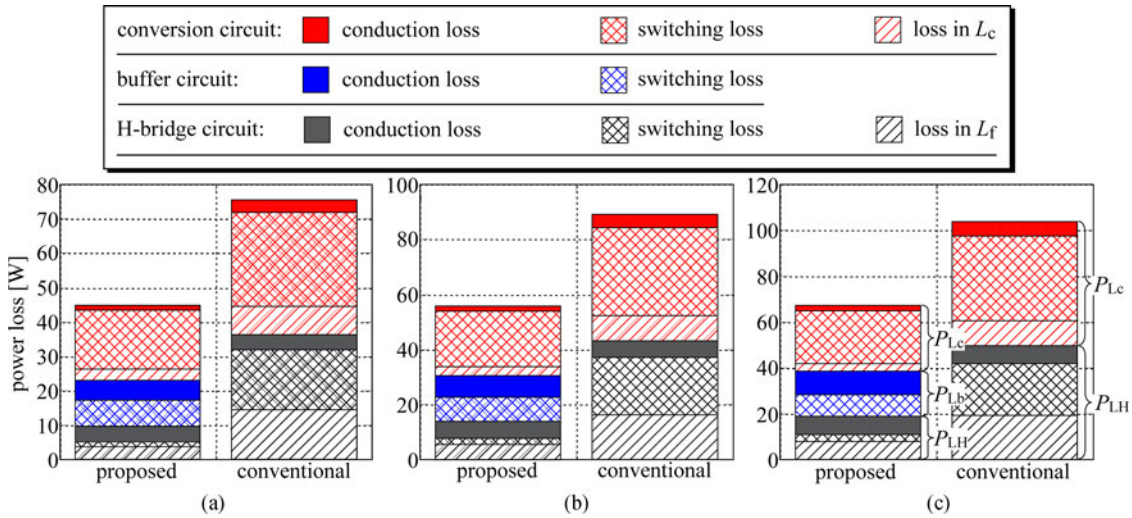

Fig. 20. Comparison between detailed losses of the proposed and conventional inverters during dc–ac conversion of (a) $P_{\rm ac} = 300\,{\rm W}$, (b) $P_{\rm ac} = 400\,{\rm W}$, and (c) $P_{\rm ac} = 500\,{\rm W}$ under conditions of $v_s = 90\,{\rm V}$, $v_{\rm bc} = 70\,{\rm V}$, and $v_{\rm dcc} = 160\,{\rm V}$.

TABLE IV
VOLTAGE APPLIED TO DEVICES IN THE PROPOSED INVERTER

	applied voltage
S_1–S_4	v_s+v_b
S_{b1}–S_{b4}	v_b
S_{c1} and S_{c2}	v_s+v_b
C_b	v_b

TABLE V
VOLTAGE APPLIED TO DEVICES IN THE CONVENTIONAL INVERTER

	applied voltage
S_1–S_4	v_{dc}
S_{c1} and S_{c2}	v_{dc}
C_{dc}	v_{dc}

Range III because s_{b3} is often in the ON-state in this range. On the other hand, the power reaches a high level in Ranges I and II because s_{b1} is always in the ON-state. It is noted that, in Fig. 11, the signal s_{b1} is assumed to be in the ON-state when the energy buffer circuit is operated in Mode 2. In contrast, if s_{b3} is in the ON-state in Mode 2, the power P_c would move toward a lower level in Ranges II and III. The energy U_c is an integration result of P_c and represents the energy transferred into C_b from the dc–dc conversion circuit. When the energy variation ΔU_c over one cycle of the grid corresponds with ΔU_b, the voltage v_b can be periodically kept at a constant value.

Fig. 13 shows the dc–dc conversion current I_c necessary to keep v_b at a constant value. The shaded area between the two curves is the possible range of I_c. One curve represents the results when s_{b1} is in the ON-state and the other shows when s_{b3} is in the ON-state. It is confirmed that the current I_c is zero at $v_s = 117\,{\rm V}$. At voltages below 117 V, the positive current charges C_b. In contrast, over 117 V, the current is negative, and the energy in C_b is transferred to the dc voltage source v_s by the circuit. The dotted curve in Fig. 13 represents the conversion current I_c of the conventional inverter. The figure demonstrates that the current for the proposed inverter is smaller than that of the conventional inverter. This result implies that the inductor L_c in the proposed inverter can be downsized in comparison to that in the conventional inverter.

IV. EXPERIMENTS

Fig. 14 shows a test circuit of the proposed inverter. This test circuit can be changed to the conventional inverter by changing the connections. Therefore, comparison between the proposed and conventional inverters can be carried out because they use identical devices except for the capacitors as $C_{\rm dc}$ for the conventional inverter and C_b for the proposed inverter. Table III shows the experimental conditions. Figs. 15 and 16 show the waveforms during dc–ac and ac–dc conversions, respectively, for converted powers $P_{\rm ac}$ and $P_{\rm dc}$ of 500 W. In terms of the proposed inverter, the conversion current i_c can be successfully controlled at a constant value and the voltage v_b can be maintained at a command value of 70 V. As a result, the proposed inveter can perform multilevel outputs in both dc–ac and ac–dc conversions. The output current $i_{\rm o}$ can be formed into a sinusoidal wave that is in phase with the grid voltage v_g. The current $i_{\rm o}$ of the proposed inverter achieves a smaller THD than that of the conventional inverter. Fig. 17 shows the dependence of the THD of $i_{\rm o}$ on the filter inductances L_{f1} and L_{f2}. The proposed inverter requires a filter inductance of 1.0 mH to obtain a THD of 5.0%. The conventional inverter, however, requires a filter inductance of 3.0 mH. Thus, the proposed inverter can reduce the filter inductance.

Fig. 18 shows the efficiency of each inverter under various voltage conditions. The proposed inverter has a higher efficiency than the conventional inverter. Fig. 19 shows the power losses

TABLE VI
ESTIMATED VOLUME

		conventional inverter			proposed inverter		
		volume per unit [mm^3]	number	volume in subtotal[mm^3]	volume per unit [mm^3]	number	volume in subtotal [mm^3]
switches	buffer circuit		0	0	1300	4	5200
	dc-dc converter	3100	2	6200	1900	2	3800
	H-bridge circuit	3100	4	12400	1300	4	5200
heat sinks	buffer circuit		0	0	800	4	3200
	dc-dc converter	1700	2	3400	1700	2	3400
	H-bridge circuit	1700	4	6800	1700	4	6800
capacitor		5500	1	5500	3800	1	3800
total volume				34300			31400

P_{Lb}, P_{Lc}, and P_{LH} in the energy buffer, dc–dc conversion, and H-bridge circuits. The losses P_{Lc} and P_{LH} of the proposed inverter are smaller than those of the conventional inveter. The loss P_{Lb} is comparatively small. Fig. 20 shows the comparison between the detailed losses of the proposed and conventional inverters. Although the proposed inverter has larger conduction losses in the switches and diodes in total, the swithcing losses and the losses in the inductors are much smaller than those of the conventional inverter. Based on these results, the superiority of the efficiency of the proposed inverter is considered to occur because of the following factors:

1) The reduction of the current i_c through the chopper inductor L_c, which generates an energy loss because of the inner resistance of L_c.
2) The lower voltage applied to the switches and therefore the decreased switching loss. Therefore, the losses in the dc–dc conversion and the H-bridge circuits are reduced, and in particular, the loss of the H-bridge circuit is reduced to 18% in comparison to the conventional inverter.
3) The smaller ripple in the output current, which leads to a reduction in the iron loss in the filter inductors L_{f1} and L_{f2}.

V. VOLUME CONSIDERATION

Tables IV and V give the voltages applied to the devices in the proposed and conventional inverters (refer to Appendix C). Considering that the voltages of $v_s + v_b$ and v_{dc} nearly correspond with the amplitude of the grid, the switches in the H-bridge and the dc–dc conversion circuits in the proposed inverter require the same voltage rating as the switches in the conventional inverter. On the other hand, the applied voltage to the switches $S_{b1} - S_{b4}$ in the energy buffer circuit is low. Therefore, switches $S_{b1} - S_{b4}$ can be exchanged with switches with smaller volume. In the test circuit, MOSFET FMW30N60S1HF of Fuji Electric Co., Ltd., which has a voltage rating of 600 V, is used as the switch. For example, using the switch MOSFET FQP22N30 of Fairchild Semiconductor International, Inc, which has a voltage rating of 300 V, provides a 50% smaller volume. Furthermore, the heat sink attached to the switches in the proposed inverter can also be downsized in comparison to that for the conventional inverter, according to the measured loss shown in Fig. 19. If the required volume of the heat sink is, for simplicity, in proportion to the loss dissipated in the respective switches under an inverter output of 500 W, the volume of the heat sinks used in the energy buffer, dc–dc conversion, and H-bridge circuits in the proposed inverter can be reduced to 40%, 60%, and 40%, respectively. In addition, the capacitor C_b satisfies a smaller voltage rating than C_{dc}. Therefore, the capacitor C_b can have a smaller volume than C_{dc} as shown in the test circuit. Although these in the test circuit have the same capacitance, the volume of C_b is 30% smaller than that of C_{dc}. Table VI gives the estimated volume of these devices. The proposed inverter has a slightly smaller volume than the conventional inverter. Although this superiority may be canceled by the volume of the drive circuit for the switches, this consideration confirms that the volume increase caused by an increase in the number of the devices can be suppressed significantly.

VI. CONCLUSION

This paper proposed a new single-phase inverter topology with an energy buffer circuit and a dc–dc conversion circuit, and described the control method for this proposed topology. The proposed inverter can output a multilevel voltage, which results in a decrease in the PWM harmonics in the output current. The proposed inverter can perform both dc–ac and ac–dc conversions with higher efficiency than a conventional inverter. The switches, the heat sinks attached to the switches and the capacitor used in the proposed inverter can all be downsized, because of the small applied voltage, and low loss dissipated in these devices. Furthermore, as a result of its multilevel output, the proposed inverter has a reduced filter inductance at the same THD. In addition, because of the reduction of the dc–dc conversion current, the chopper inductor can also be downsized. Consequently, the volume increase caused by the increase in the number of devices can be suppressed significantly. The proposed inverter is confirmed to be useful in practical applications.

APPENDIX A

Fig. A1 shows the simulated waveforms of the proposed inverter and the MEB inverter in [33]. The voltage v_b across the buffer capacitor of the MEB inverter pulsates with an amplitude level of 23 V, which is over double the amplitude level of the proposed inverter. In addition, the current i_c through the inductor in the dc–dc conversion circuit of the MEB inverter has triple the magnitude of that of the proposed inverter. This degrades the efficiency of the MEB inverter.

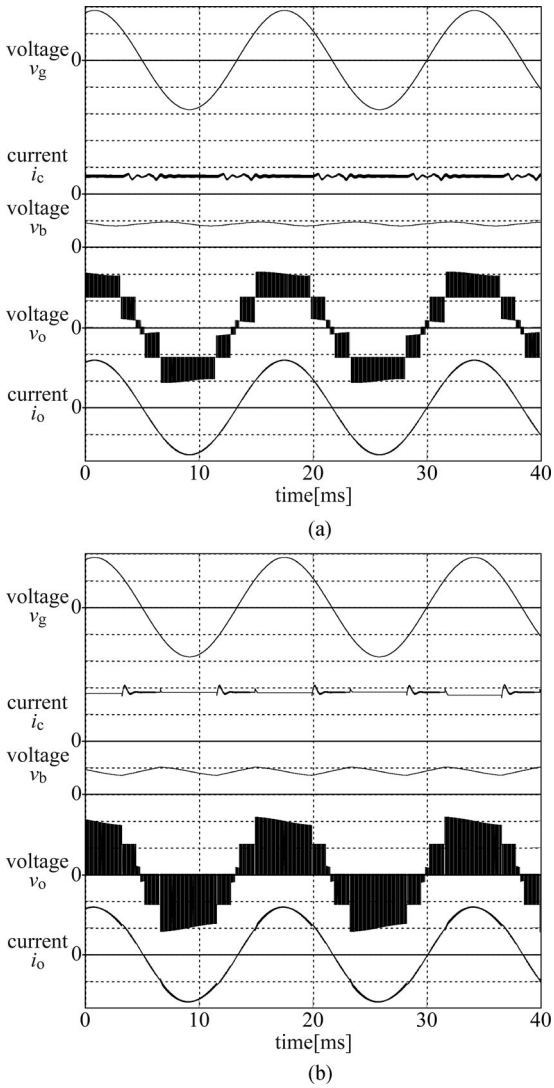

Fig. A1. Simulated waveforms of (a) the proposed inverter and (b) MEB inverter with a buffer capacitance of 1 mF during dc–ac conversion under conditions of $P_{\rm ac} = 500\,{\rm W}$, $v_s = 90\,{\rm V}$, and $v_{\rm bc} = 70\,{\rm V}$ (the scales for v_g, v_b, and $v_{\rm o}$ are $80\,{\rm V/div.}$, and those for i_c and $i_{\rm o}$ are $4.0\,{\rm A/div.}$).

Appendix B

Fig. A2 shows the output voltage waveform and harmonics in the output voltage of the MEB inverter in [33] under the condition of $v_s = 90\,{\rm V}$ and $v_b = 70\,{\rm V}$. The comparison with Fig. 10(b) confirms that the MEB inverter has higher harmonics than the proposed inverter.

Appendix C

Fig. A3 shows the simulated voltages and currents of the switches and antiparallel diodes in the proposed inverter under the same simulation as Fig. A1. The subscript of the variables, v and i denotes the switches; for example, v_{sb1} denotes voltage across switch S_{b1}. The current with a positive value flows through the switch and the current with a negative value flows through the antiparallel diode.

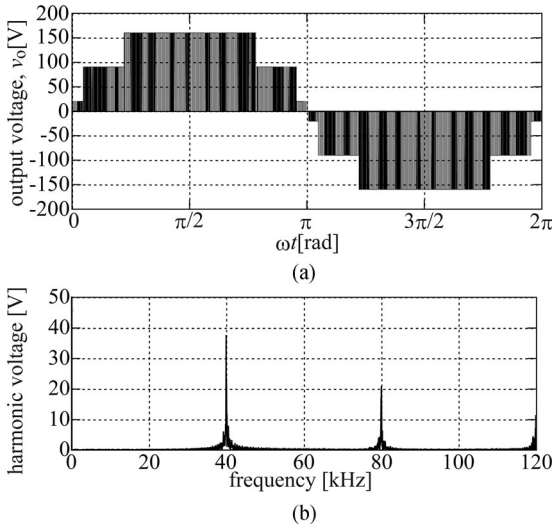

Fig. A2. Output voltage waveform and harmonics in the output voltage of the MEB inverter under the conditions of $v_s = 90\,{\rm V}$ and $v_b = 70\,{\rm V}$.

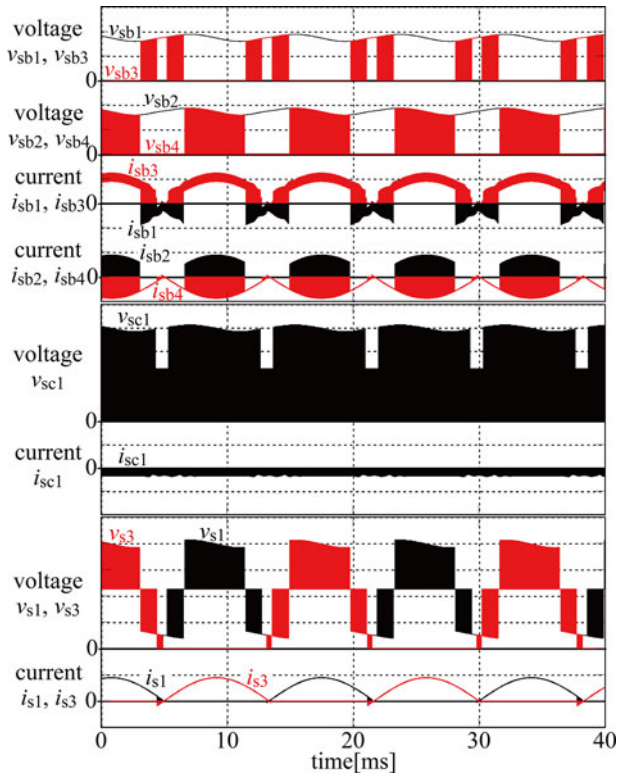

Fig. A3. Simulated voltages and currents of the switches and the antiparallel diodes in the proposed inverter under the simulation of Fig. A1(a) (the scales for the voltages are $40\,{\rm V/div.}$, and those for the currents are $8.0\,{\rm A/div.}$).

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