Improved Dual Boost Inverter With Half Cycle Modulation

Yu Tang, *Member, IEEE*, Yang Bai, Jiarong Kan, *Member, IEEE*, and Fei Xu

***Abstract*—The output voltage of a traditional full-bridge inverter is lower than the input dc voltage. In applications when the input voltage is low, the front-end step-up converter is usually required, presenting a two-stage power conversion. Dual boost inverter (DBI) can realize single-stage conversion, which has the advantages of a simple structure, less power devices, and buck–boost ability. The traditional modulation strategy of DBI makes all power switches operate in high frequency and sustain high voltage/current stress, which leads to heavy conduction and switching loss. This paper proposed a modulation strategy, namely, half cycle modulation (HCM), which makes power switches work in high frequency just in half cycle, and can greatly reduce the conduction and switching loss of the power devices. Furthermore, to reduce the current circulation loss in DBI, an improved DBI with two clamping switches is proposed based on HCM, which can bypass the inductor current with low stress switches; therefore, the loss caused by circulation current can be greatly reduced. A detailed analysis and comparison between the traditional and HCM strategies are given in this paper. Finally, a 500 VA DBI prototype is designed in the lab. The advantages of the proposed HCM strategy and improved DBI with two clamping switches are verified by experimental results.**

***Index Terms*—Dual boost inverter (DBI), half cycle modulation (HCM), voltage/current stress.**

I. Introduction

A FULL-BRIDGE inverter is the mostly used topology to realized dc–ac power conversion. It can be seen as a buck inverter, and the output ac voltage is always lower than the input dc voltage. In applications when the input voltage is low, an additional front-end dc–dc converter is required to realize voltage step-up conversion [1], [2]. The two-stage structure is complex in system structure and controller design, and the efficiency is influenced by two stages.

Although a line frequency transformer can be utilized to step up the input voltage, it will be voluminous. In order to minimize the power components, many single-stage inverters were proposed [3]–[9], which is beneficial to the improvement of power density and efficiency due to its simple structure and less power device. A Z-source inverter, which can be viewed as a quasi-single-stage inverter, takes the advantage of the passive network to boost voltage and allows shoot-through situation in bridge legs [10], [11]. But the drawbacks of high Z-source capacitor voltage stress and huge inrush surge may influence the efficiency, and vast passive components will also go against integration. Paper [12] has proposed a novel active buck–boost inverter, which can boost the voltage and perform buck and boost conversion in a quasi-single-stage inverter. But this single-stage inverter has too many power switches.

Paper [3] proposed the dual boost inverter (DBI) based on two symmetrical bidirectional boost dc–dc converters. The DBI consists of two boost converters whose outputs are out-of-phase sinusoidal voltages with the same dc bias. The output voltage of DBI can be higher than the dc input voltage [13]–[15] based on the step-up characteristic of a boost converter. To mitigate the low-frequency ripple current, a waveform control was presented in [16]. A dynamic linearizing modulator-based boost inverter was proposed to improve its power bandwidth in [17]. Traditional modulation method makes each group of the bidirectional boost dc/dc converters produce the sinusoidal ac voltage with same dc bias [18]–[21]. However, all power switches of the converter operate in high frequency under this modulation and the power switches sustain high voltage/current stress, which leads to a heavy conduction and switching loss. Meanwhile, a circulation current will flow through the inductors, The output current will flow through the inductor, and the loss of inductor will decrease the whole efficiency.

This paper proposes the half cycle modulation (HCM) strategy, which makes two boost groups operate by turns and each group outputs a "half-steamed bread-wave" voltage with a dc bias. The output side can get a pure sinusoidal ac voltage output by differing the two outputs. HCM can reduce the number of power switches working in high frequency and reduce the stress of the switches and inductors. The switching and conduction loss of switches can be greatly reduced, and the core loss and the copper loss of inductors can be reduced. Furthermore, to reduce the current circulation loss in DBI, an improved DBI with two clamping switches is proposed based on HCM. The improved topology can achieve higher efficiency with low-stress clamping switches operating in half cycle and line frequency.

This paper is organized as follows: circuit analysis of DBI under HCM is shown in Section II; the detailed comparison of the traditional and HCM schemes is given in Section III; in

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Y Tang, Y. Bai, and F. Xu are with Jiangsu Key Laboratory of New Energy Generation and Power Conversion, Nanjing University of Aeronautics and Astronautics, Nanjing 210916, China (e-mail: ty8025@hotmail.com; hello9272@163.com; xuf_xuf@163.com).

J. Kan was with Jiangsu Key Laboratory of New Energy Generation and Power Conversion, Nanjing University of Aeronautics and Astronautics, Nanjing 210916, China. He is now with the School of Electrical Engineering, Yancheng Institute of Technology, Yancheng 224051, China (e-mail: kanjr@163.com).

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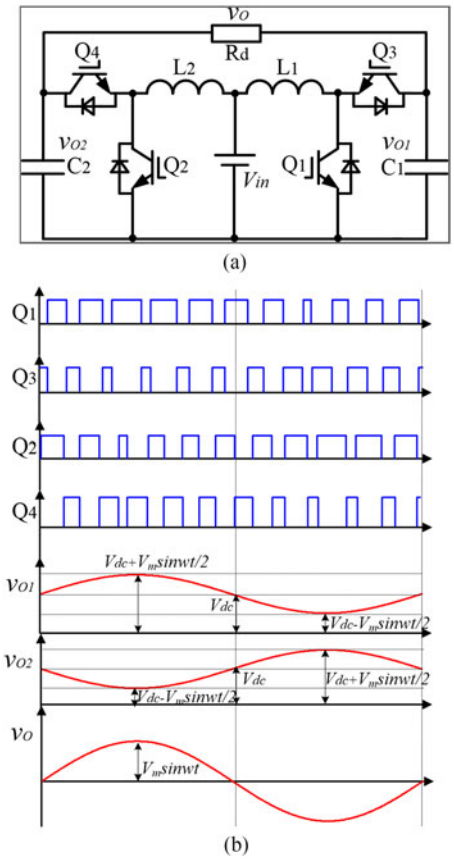


Fig. 1. Traditional modulation strategy and key waveforms. (a) Main circuit and (b) key waveforms.

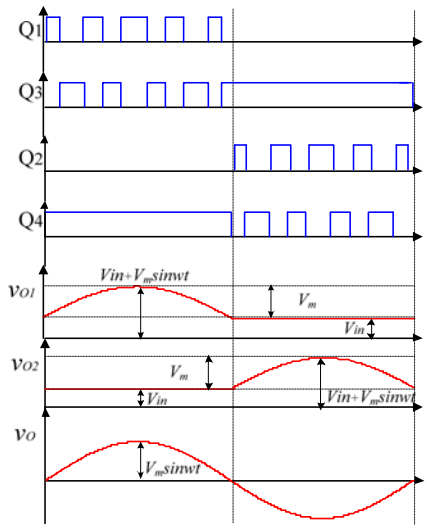


Fig. 2. HCM strategy and key waveforms.

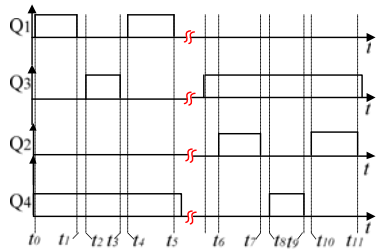


Fig. 3. Control strategy under HCM.

Section IV, the improved DBI with two clamping switches is taken into analysis; experimental results are presented to verify the improved methods in Section V; and finally, conclusions are given in Section VI.

II. Traditional and Proposed Modulation Strategies

Fig. 1(a) shows the main circuit of DBI, and Fig. 1(b) shows the key waveforms under traditional modulation strategy. The output of a boost converter is a sinusoidal ac voltage with the same dc bias.

The operational principle of the DBI converter under traditional modulation strategy is given as follows. Four power switches are all working in high frequency, as shown in Fig. 1(b). Let us define v_{o1} and v_{o2} as the voltages of C_1 and C_2, respectively; $V_{\rm dc}$ the offset voltage; $V_{\rm in}$ the input dc voltage; V_m the magnitude of the output ac voltage; and d_1 and d_2 as the duty cycles of Q_1 and Q_2, respectively. Through the appropriate control logic, v_{o1}, v_{o2} can be obtained as follows:

$$v_{o1}(t) = V_{\rm dc} + \frac{1}{2}\cdot V_m \cdot \sin(\omega {\rm t}) \tag{1}$$

$$v_{o2}(t) = V_{\rm dc} + \frac{1}{2}\cdot V_m \cdot \sin(\omega {\rm t} - \pi) \tag{2}$$

$$v_o(t) = v_{o1}(t) - v_{o2}(t) = \frac{V_{\rm in}}{1-d_1(t)} - \frac{V_{\rm in}}{1-d_2(t)} \tag{3}$$

where $V_{\rm dc} \geq V_{\rm in} + \frac{V_m}{2}$.

From (1) – (3)

$$d_1(t) = \frac{\frac{V_m}{2} + \frac{V_m}{2}\cdot\sin(\omega {\rm t})}{V_{\rm in} + \frac{V_m}{2} + \frac{V_m}{2}\cdot\sin(\omega {\rm t})} \tag{4}$$

$$d_2(t) = \frac{\frac{V_m}{2} - \frac{V_m}{2}\cdot\sin(\omega {\rm t})}{V_{\rm in} + \frac{V_m}{2} - \frac{V_m}{2}\cdot\sin(\omega {\rm t})}. \tag{5}$$

From (1) – (5)

$$v_o(t) = v_{o1}(t) - v_{o2}(t) = V_m \cdot \sin(\omega {\rm t}). \tag{6}$$

The waveforms of v_{o1}, v_{o2}, and v_o are shown in Fig. 1(b); the voltages v_{o1}, v_{o2} are sinusoidal with a dc bias. The output voltage v_o is sinusoidal by differing the v_{o1}, v_{o2}. The output voltage v_o is sinusoidal wave by differing.

The proposed HCM strategy is shown in Fig. 2. In the positive half cycle of the output voltage, switches Q_1, Q_3 worked in high frequency, complementary to each other; Q_2 is turned off; Q_4 is turned on; the output voltage of capacitance C_1 can be obtained as (7); and the voltage of C_2 is $V_{\rm in}$. In the negative period of the output voltage, switches Q_2, Q_4 worked in high frequency, complementary to each other; Q_1 is turned off; Q_3 is turned on; the output voltage of capacitance C_2 can be obtained as (8); and

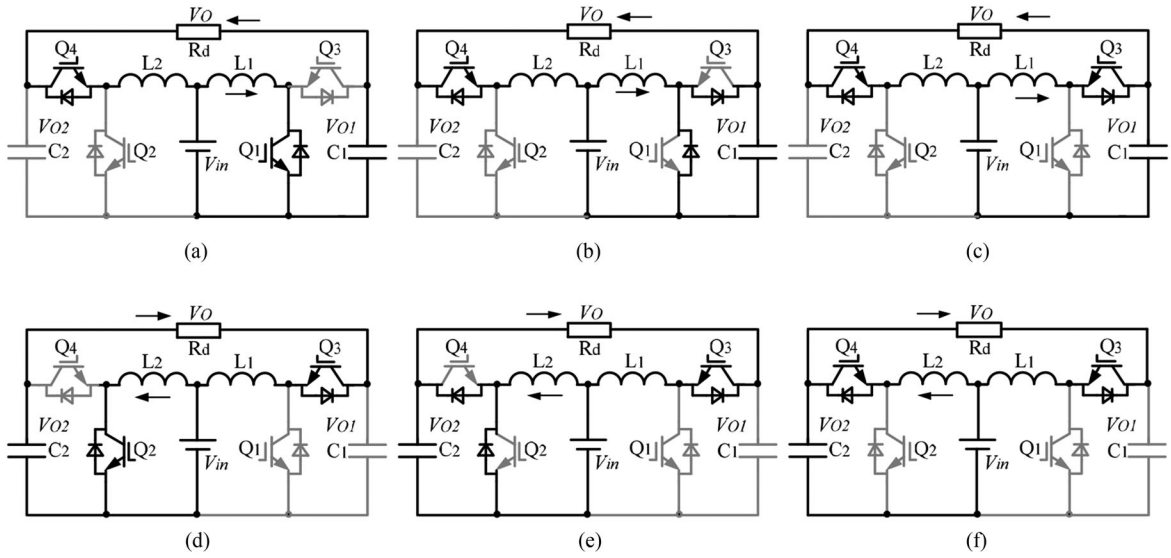


Fig. 4. Equivalent circuits of switching modes. (a) $[t_0,\ t_1]$, (b) $[t_1, t_2]$ or $[t_3, t_4]$, (c) $[t_2, t_3]$, (d) $[t_6, t_7]$, (e) $[t_7, t_8]$ or $[t_9, t_{10}]$, and (f) $[t_8, t_9]$.

the voltage of C_1 is $V_{\rm in}$

$$\begin{cases} v_{o1}(t) = V_m \cdot \sin(\omega {\rm t}) + V_{\rm in} \\ v_{o2}(t) = V_{\rm in} \end{cases} \tag{7}$$

$$\begin{cases} v_{o1}(t) = V_{\rm in} \\ v_{o2}(t) = V_m \cdot \sin(\omega {\rm t} - \pi) + V_{\rm in} \end{cases} \tag{8}$$

$$v_o(t) = v_{o1}(t) - v_{o2}(t) = \frac{V_{\rm in}}{1 - d(t)} - V_{\rm in}. \tag{9}$$

From (7) – (9)

$$d(t) = \frac{V_m \cdot \sin(\omega {\rm t})}{V_{\rm in} + V_m \cdot \sin(\omega {\rm t})} \tag{10}$$

where $d(t)$ is the duty cycle of $Q_1,\ Q_2$. The output voltage can be achieved by finding the difference between v_{o1} and v_{o2}

$$\begin{aligned} v_o(t) &= v_{o1}(t) - v_{o2}(t) = \frac{V_{\rm in}}{1 - d(t)} - V_{\rm in} \\ &= V_m \cdot \sin(\omega {\rm t}). \end{aligned} \tag{11}$$

In a switching cycle, the converter under HCM has four switching modes. Fig. 3 shows the control strategy of HCM, and Fig. 4 shows the equivalent circuits of the switching modes in the switching cycle. Before the following analysis, the following are some assumptions: 1) all the switches and diodes are ideal; 2) all the capacitors and inductors are ideal; and 3) $C_1 = C_2,\ L_1 = L_2$.

In the period that the output voltage is positive:

1) Mode 1 $[t_0,\ t_1]$: At $t_0,\ Q_1,\ Q_4$ are turned on, the input voltage is applied on L_1, and the input current charges L_1. Load current i_o flows through $Q_4\ (D_4)$ to $V_{\rm in}$, which is supplied by C_1, as shown in Fig. 4(a).
2) Mode 2 $[t_1, t_2]$: The period is dead time. At $t_1,\ Q_1,\ Q_2,$ and Q_3 are turned off, Q_4 is turned on, and the current i_{L1} flows through D_3 or D_1 (according to the current direction), as shown in Fig. 4(b). Load current i_o flows through $Q_4\ (D_4)$ to $V_{\rm in}$.
3) Mode 3 $[t_2, t_3]$: At $t_2,\ Q_3$ is turned on and i_{L1} flows through $Q_3(D_3)$. Load current i_o flows through $Q_4(D_4)$ to $V_{\rm in}$. The current-flow path is shown in Fig. 4(c).
4) Mode 4 $[t_3, t_4]$: The period is also dead time, and the operating mode is the same as that of mode 2.

In the period that the output voltage is negative:

5) Mode 5 $[t_6, t_7]$: At $t_6,\ Q_2,\ Q_3$ are turned on, the input voltage is applied on L_2, and the input current charges L_2. Load current i_o flows through $Q_3(D_3)$ to $V_{\rm in}$, which is supplied by C_2, as shown in Fig. 4(d).
6) Mode 6 $[t_7, t_8]$: The period is dead time. At $t_7,\ Q_1,\ Q_2,$ and Q_4 are turned off, Q_3 is turned on, and the current i_{L2} flows through D_4 or D_2(according to the current direction), as shown in Fig. 4(e). Load current i_o flows through $Q_3\ (D_3)$ to $V_{\rm in}$.
7) Mode 7 $[t_8, t_9]$: At $t_8,\ Q_4$ is turned on and i_{L2} flows through $Q_4(D_4)$. Load current i_o flows through $Q_3(D_3)$ to $V_{\rm in}$. The current-flow path is shown in Fig. 4(f).
8) Mode 8 $[t_9, t_{10}]$: The period is also dead time, and the operating mode is the same as that of mode 6.

III. Comparision of Two Modulations

According to the analysis above, we can know that under HCM, a sinusoidal output voltage can be generated by differing the voltages of C_1 and C_2, as done in case of traditional modulation. The detailed comparison between two modulation strategies is given in the following. The traditional method is called T-M here to simplify. Switches tubes are not entirely working in high frequency under HCM. In the period that the output voltage is positive, Q_4 has no switching loss and Q_2 has neither switching loss nor conduction loss compared with T-M. In the period that the output voltage is negative, Q_3 has no

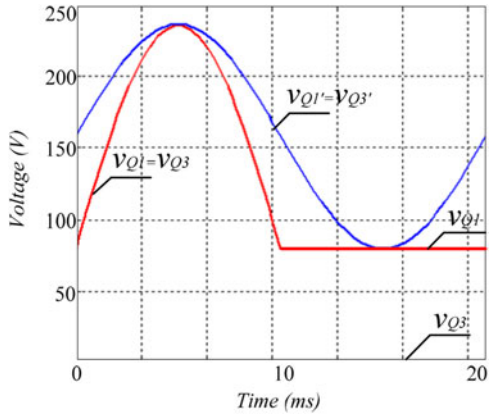


Fig. 5. Voltage stress of switches.

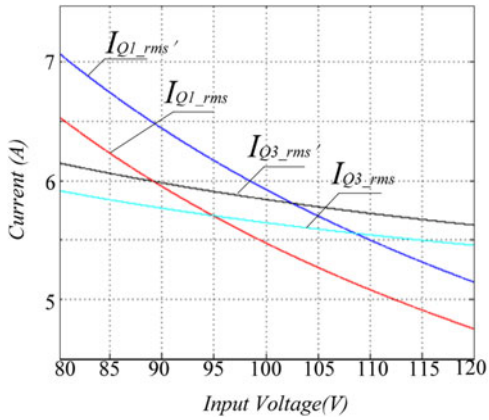


Fig. 6. Current stress of switches.

switching loss and Q_1 has neither switching loss nor conduction loss compared with T-M. In addition, the voltage/current stress of the component under HCM is also lower. Due to the symmetry of the circuit, we will make a comparison of the voltage/current stress and the inductor current ripple between two modulation strategies. The parameters of the inverter prototype are given as follows: 1) $V_{\text{in}} = 80$ V dc and $V_o = 110$ V ac, and 2) $L_1 = L_2 = 500$ μH and $C_1 = C_2 = 20$ μF.

We define v_{Q1}, v_{Q3} as the voltage stress sustained by Q_1, Q_3 under HCM and $v_{Q1}{}'$, $v_{Q3}{}'$ are the voltage stress sustained by Q_1, Q_3 under T-M. In the period that the output voltage is positive, the expressions of v_{Q1}, v_{Q3}, $v_{Q1}{}'$, $v_{Q3}{}'$ are shown as (12). In the period that the output voltage is negative, the expressions of v_{Q1}, v_{Q3}, $v_{Q1}{}'$, $v_{Q3}{}'$ are shown as (13). Fig. 5 shows the voltage stress of Q_1, Q_3 during the period

$$\begin{cases} v_{Q1} = V_{\text{in}} + V_m \cdot \sin(\omega t) \\ v_{Q3} = V_{\text{in}} + V_m \cdot \sin(\omega t) \\ v_{Q1}{}' = V_{\text{in}} + \dfrac{V_m}{2} + \dfrac{V_m}{2} \cdot \sin(\omega t) \\ v_{Q3}{}' = V_{\text{in}} + \dfrac{V_m}{2} + \dfrac{V_m}{2} \cdot \sin(\omega t) \end{cases} \tag{12}$$

$$\begin{cases} v_{Q1} = V_{\text{in}} \\ v_{Q3} = 0 \\ v_{Q1}{}' = V_{\text{in}} + \dfrac{V_m}{2} + \dfrac{V_m}{2} \cdot \sin(\omega t) \cdot \\ v_{Q3}{}' = V_{\text{in}} + \dfrac{V_m}{2} + \dfrac{V_m}{2} \cdot \sin(\omega t) \end{cases} \tag{13}$$

Fig. 5 indicates that in the period that the output voltage is positive, the voltage stress of Q_1 , Q_3 under HCM is obviously lower than T-M, except the time that the output voltage getting its maximum. In the period that the output voltage is negative, the voltage stress of Q_3 is zero and Q_1 is equal to V_{in}, which is also lower than T-M.

Fig. 6 shows the root-mean-square (rms) current of Q_1, Q_3. We define I_{Q1_rms}, I_{Q3_rms} as the current stress of Q_1, Q_3 under H-M, $I_{Q1\_\text{rms}}{}'$, $I_{Q3\_\text{rms}}{}'$ is the current stress of Q_1, Q_3 under T-M. The expression of I_{Q1_rms}, I_{Q3_rms}, $I_{Q1\_\text{rms}}{}'$, $I_{Q3\_\text{rms}}{}'$ is

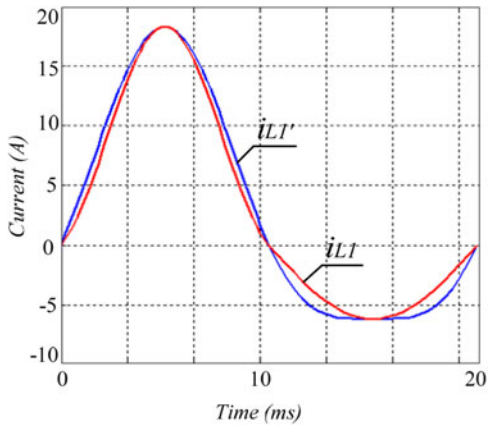


Fig. 7. Current stress of inductor.

given by

$$\begin{cases} I_{Q1\_\text{rms}}{}' = \sqrt{\dfrac{1}{2\pi}\left[\displaystyle\int_0^{\pi}\left(\frac{i_o}{1-d_1(t)}\right)^2 d_1(t)d\theta + \int_{\pi}^{2\pi}\left(\frac{i_o}{1-d_2(t)}\right)^2 d_2(t)d\theta\right]} \\ I_{Q3\_\text{rms}}{}' = \sqrt{\dfrac{1}{2\pi}\left[\displaystyle\int_0^{\pi}\left(\frac{i_o}{1-d_1(t)}\right)^2 (1-d_1(t))d\theta + \int_{\pi}^{2\pi}\left(\frac{i_o}{1-d_2(t)}\right)^2 (1-d_2(t))\right] d\theta} \\ I_{Q1\_\text{rms}} = \sqrt{\dfrac{1}{2\pi}\displaystyle\int_0^{\pi}\left(\frac{i_o}{1-d(t)}\right)^2 d(t)d\theta} \\ I_{Q3\_\text{rms}} = \sqrt{\dfrac{1}{2\pi}\displaystyle\int_{\pi}^{2\pi}\left[\frac{{i_o}^2}{1-d(t)} + {i_o}^2\right] d\theta} \end{cases} \tag{14}$$

As shown in Fig. 6, the rms current of I_{Q1_rms}, I_{Q3_rms} is lower than that of $I_{Q1\_\text{rms}}{}'$, $I_{Q3\_\text{rms}}{}'$ under different input voltages. Besides, I_{Q1_rms} is higher than I_{Q3_rms} when the input

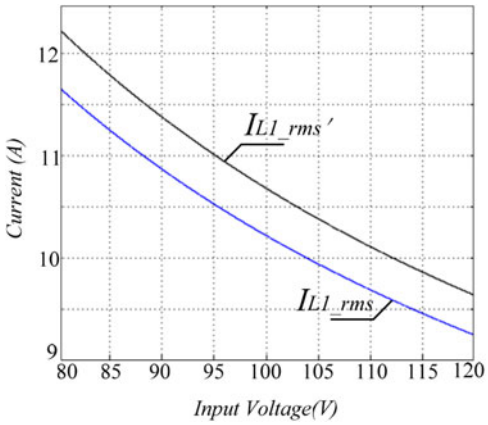


Fig. 8. Fundamental current of inductor.

voltage is low and I_{Q1_rms} is lower than I_{Q3_rms} with the increase in the input voltage. The relation of $I_{Q1\_\mathrm{rms}}{}'$ and $I_{Q3\_\mathrm{rms}}{}'$ is similar to I_{Q1_rms} and I_{Q3_rms}, with the change in input voltage.

In order to compare the inductor current stress, we neglect the current ripple in the analysis. Fundamental current of inductor is defined as $i_{L1}(t)$ under HCM; $i_{L1}(t)'$ belongs to T-M. Fig. 7 shows the expressions of $i_{L1}(t)$ and $i_{L1}(t)'$. In the period that the output voltage is positive, the expressions of $i_{L1}(t)$ and $i_{L1}(t)'$ are given in (15). In the period that the output voltage is negative, the expression of $i_{L1}(t)$, $i_{L1}(t)'$ is shown as (16). Fig. 8 shows the rms current of inductor. We define I_{L1_rms} as the current stress of inductor under HCM, and $I_{L1\_\mathrm{rms}}{}'$ is the current stress of inductor under T-M. The expressions of I_{L1_rms} and $I_{L1\_\mathrm{rms}}{}'$ are given in (17) and (18)

$$\begin{cases} i_{L1}(t) = \dfrac{i_o(t)}{1-d(t)} = i_o(t) \\ \quad + \dfrac{V_m \sin(\omega t)}{V_{\mathrm{in}}} i_o(t) \\ i_{L1}(t)' = \dfrac{i_o(t)}{1-d_1(t)} = i_o(t) \\ \quad + \dfrac{V_m + V_m \sin(\omega t)}{2V_{\mathrm{in}}} i_o(t) \end{cases} \tag{15}$$

$$\begin{cases} i_{L1}(t) = i_o(t) \\ i_{L1}(t)' = \dfrac{i_o(t)}{1-d_2(t)} = i_o(t) \\ \quad + \dfrac{V_m - V_m \sin(\omega t)}{2V_{\mathrm{in}}} i_o(t) \end{cases} \tag{16}$$

$$I_{L1\_\mathrm{rms}} = \sqrt{\frac{1}{2\pi}\left(\int_0^{\pi} i_{L1}^2(t)dt + \int_{\pi}^{2\pi} i_{L1}^2(t)dt\right)} \tag{17}$$

$$I_{L1\_\mathrm{rms}}{}' = \sqrt{\frac{1}{2\pi}\left(\int_0^{\pi} i_{L1}'^2(t)dt + \int_{\pi}^{2\pi} i_{L1}'^2(t)dt\right)}. \tag{18}$$

Fig. 7 illustrates that $i_{L1}(t)$ is lower than $i_{L1}(t)'$, which means the core loss and the copper loss of the inductor under H-M is lower than that under T-M, as shown in Fig. 8.

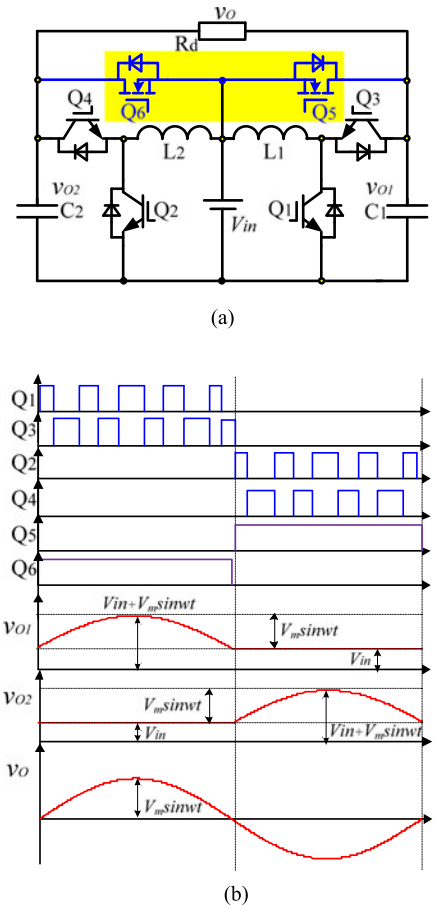


Fig. 9. HCM strategy with clamping switches. (a) Improved main circuit and (b) key waveforms.

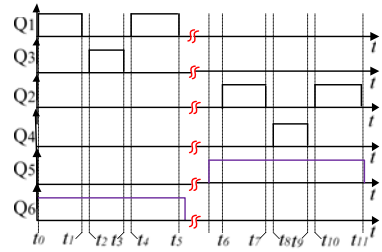


Fig. 10. Control logic under HCM with clamping switches.

According to the aforementioned analysis, some significant results can be concluded. As shown in Fig. 5, voltage stress of Q_1, Q_3 under HCM is obvious lower than that of T-M during the period. The condition is the same for Q_2, Q_4 considering the symmetrical operation of the two groups. Fig. 6 illustrates that the current stress of Q_1, Q_3 under HCM is also lower than that of T-M under different input voltage. Fig. 7 indicates that fundamental current and rms current of inductance under HCM is also lower than that of T-M. That means the switching loss and conduction loss of switches, and the copper loss of inductors under HCM is always lower than that of T-M, which can greatly improve the system overall efficiency.

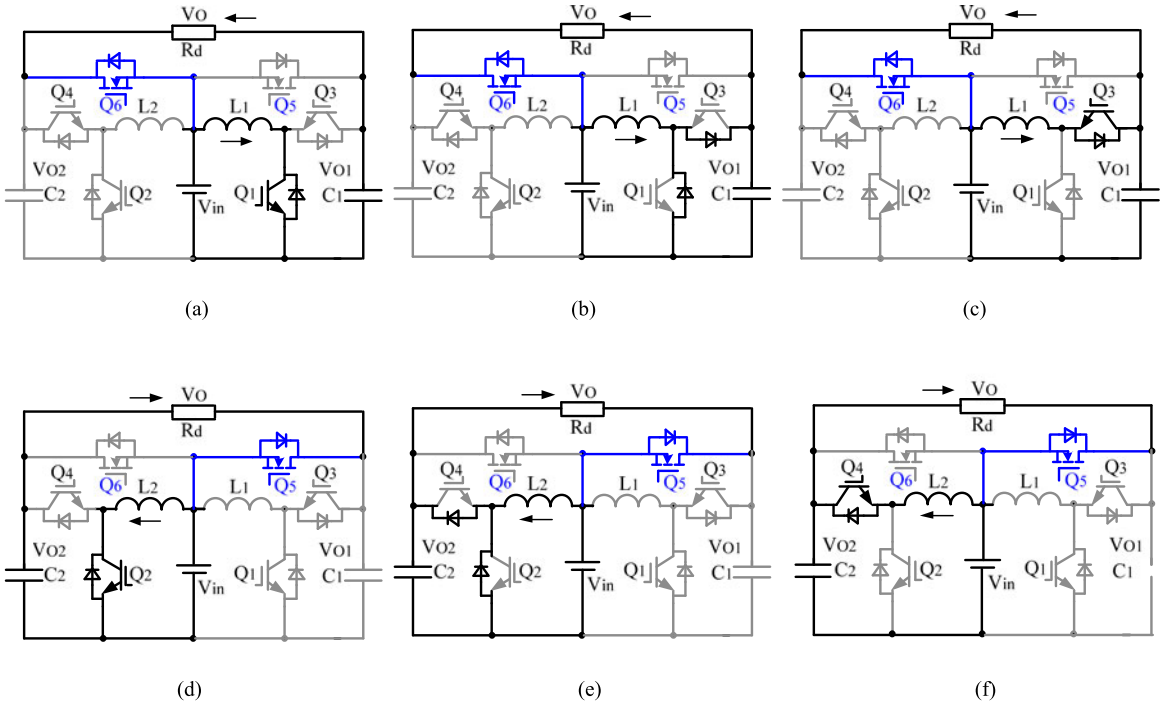


Fig. 11. Equivalent circuits with clamping switches of the switching modes. (a) $[t_0,\ t_1]$, (b) $[t_1, t_2]$ or $[t_3, t_4]$, (c) $[t_2, t_3]$, (d) $[t_6, t_7]$, (e) $[t_7, t_8]$ or $[t_9, t_{10}]$, and (f) $[t_8, t_9]$.

IV. Improved DBI With Two Clamping Switches

Whether traditional modulation method or HCM strategy is utilized, current circulation of the converter still exists, which means the core loss and the copper loss of inductors L_1, L_2 will exist all the time. In half line cycle, only one inductor is needed to play a booster role under HCM strategy; the other output side can be clamping to $V_{\rm in}$ by using a clamping switch. The clamping switches operate in line frequency, and the voltage stress is much lower. For low-voltage-stress applications, low-cost MOSFET can be utilized, which means the conduction loss is lower than IGBT in the same condition; therefore, low-cost MOSFETs can be applied. The topology is shown in Fig. 9(a). Fig. 9(b) shows the modulation strategy and the key waveforms.

The switching mode of the converter with clamping switches is similar to HCM. In the period that the output voltage is positive, Q_4 is turned off, voltage of C_2 is clamped to $V_{\rm in}$ by clamping switch Q_6, and the load current i_o flows through Q_6 to $V_{\rm in}$, which is supplied by C_1. In the period that the output voltage is negative, Q_3 is turned off, voltage of C_1 is clamped to $V_{\rm in}$ by clamping switch Q_5, and the load current i_o flows through Q_5 to $V_{\rm in}$, which is supplied by C_2. Fig. 10 shows the control logic under HCM with clamping switches. Fig. 11 shows the detail modes of the improved converter with clamping switches.

The converter with clamping switch mode is the same as the mode under HCM. The voltage/current stress is the same as HCM, except clamping switches. The current stress of clamping switch is i_o, and the voltage stress of clamping switch is $(V_o - V_{\rm in})$, which is lower than both of T-M and HCM. The clamping switches obviously have a further lower voltage stress, leading to a lower conduction loss. Moreover, clamping switches reduce the inductor core loss and copper loss generated by circulation current.

TABLE I
Comparsion of Loss

P	Loss	Low-Frequency IGBT/MOSFET	Inductor
300 W	DBI	4.64 W	0.95 W
	Improved DBI	0.11 W	0
500 W	DBI	7.65 W	2.13 W
	Improved DBI	0.3 W	0

TABLE II
Parameters of the Prototype

Parameter	Symbol	Value
Input voltage	$V_{\rm in}$	80 V
Output voltage	V_O	110 V
Rated capacity	P_O	500 VA
Fundamental Frequency	f_O	50 Hz
Switching frequency	$f_{\rm sw}$	20 kHz
Inductance	$L_1,\ L_2$	500 μH
Capacitance	$C_1,\ C_2$	20 μF

Because the operating states of high-frequency switches are the same, the conduction loss of the line frequency conduction path in the improved DBI and DBI with HCM is shown in Table I. The loss calculation only include: 1) in the positive cycle, the conduction loss of Q_4 and the copper loss of L_2 of DBI and the conduction loss of Q_6 of improved DBI; 2) in the negative cycle, the conduction loss of Q_3 and the copper

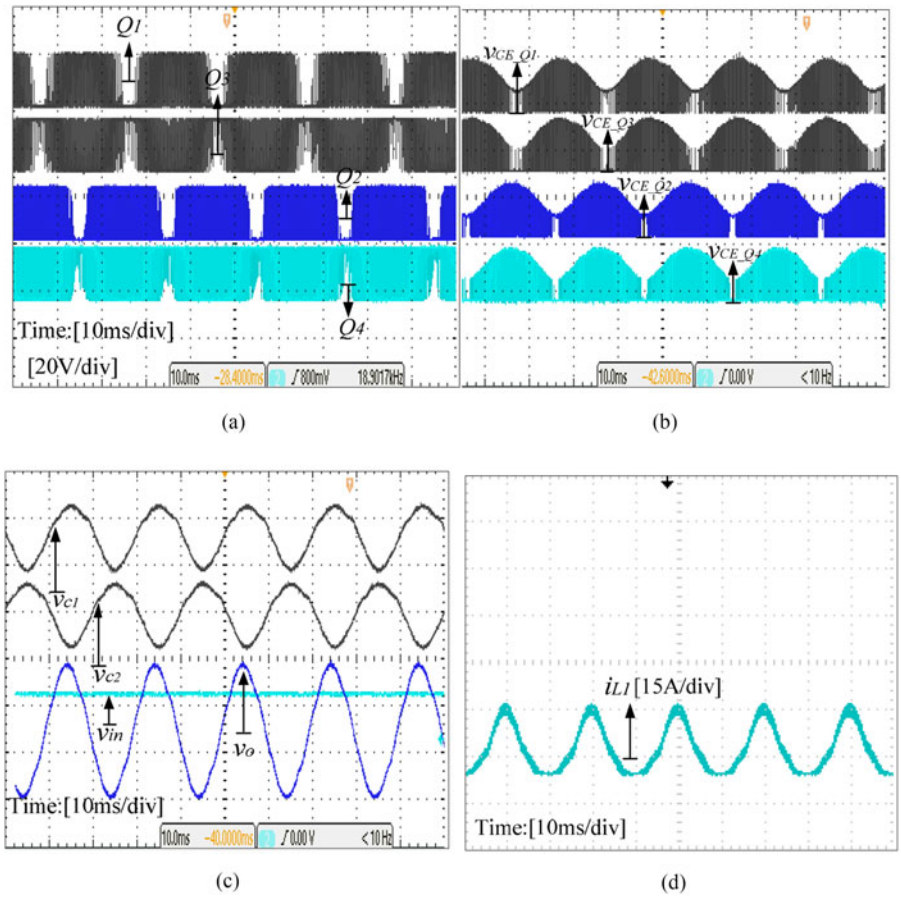


Fig. 12. Key waveforms of the traditional modulation. (a) Driver waveforms, (b) voltage stress of switches waveforms, (c) output and input voltage key waveforms, and (d) current waveforms of inductor.

loss of L_1 of DBI and the conduction loss of Q_5 of improved DBI. Table I shows that when the output power is 300 W, the efficiency increases by 1.83% and that when the output power reaches the full load, the efficiency increases by 1.9%.

V. Experimental Results

A 500 VA prototype was constructed to verify the HCM strategy and the effectiveness of the improved topology with clamping switches. The main switches were implemented using IGBT (IKW75T60) and clamping switches using MOSFET (IRFP4768PbF). The controller was implemented by DSP (TMS320F2812). The detail parameters are shown in Table II.

Fig. 12 shows the experimental results of the traditional modulation strategy. As shown in Fig. 12(a), all switches are working in high frequency, which will generate large switching loss. Fig. 12(b) illustrates that all the switches sustained voltage stress, as expressed in (12) and (13).

Fig. 13 shows the experimental results of the HCM strategy. Fig. 13(a) illustrates that only half of the switches are working in high frequency during the period under HCM strategy, which can greatly reduce the switching loss. Fig. 13(b) shows that the voltage stress of switches is lower compared with Fig. 12(b), the same as the expression (12), (13).

Fig. 14 shows the experimental results of the HCM strategy with clamping switches. Fig. 14(a) shows that Q_1 and Q_3 are working in high frequency, Q_2 and Q_4 are turned off, and Q_6 is turned on, which will reduce the core loss and the copper loss of inductance because of the current circulation in the period that the output voltage is positive. Q_2 and Q_4 are working in high frequency, Q_1, Q_3 are turned off, and Q_5 is turned on in the period that the output voltage is negative. Fig. 14(b) shows that the voltage stress of Q_1, Q_3 is the same; as shown in Fig. 13(b), the clamping switches sustain a further lower voltage stress, which can reduce the conduction loss further.

The difference between Figs. 12(c) and 13(c) indicate v_{C1}, v_{C2} is verified as expressed (1-2), (7-8). Figs. 12(d) and 13(d) illustrate that the fundamental current and the ripple current of the inductor under HCM are obviously lower than traditional modulation. Fig. 14(c) illustrates that i_O flows through Q_6 rather than inductor; as we can see, inductor L_2 has no current in the period that the output voltage is negative, which will further reduce the inductor current.

Fig. 15 shows the efficiency of DBI prototype with three methods at different output power. Fig. 15 shows that the HCM strategy applied in DBI can raise the efficiency because of lower voltage/current stress and that less switches worked in high frequency. In addition, the efficiency of HCM with clamp-

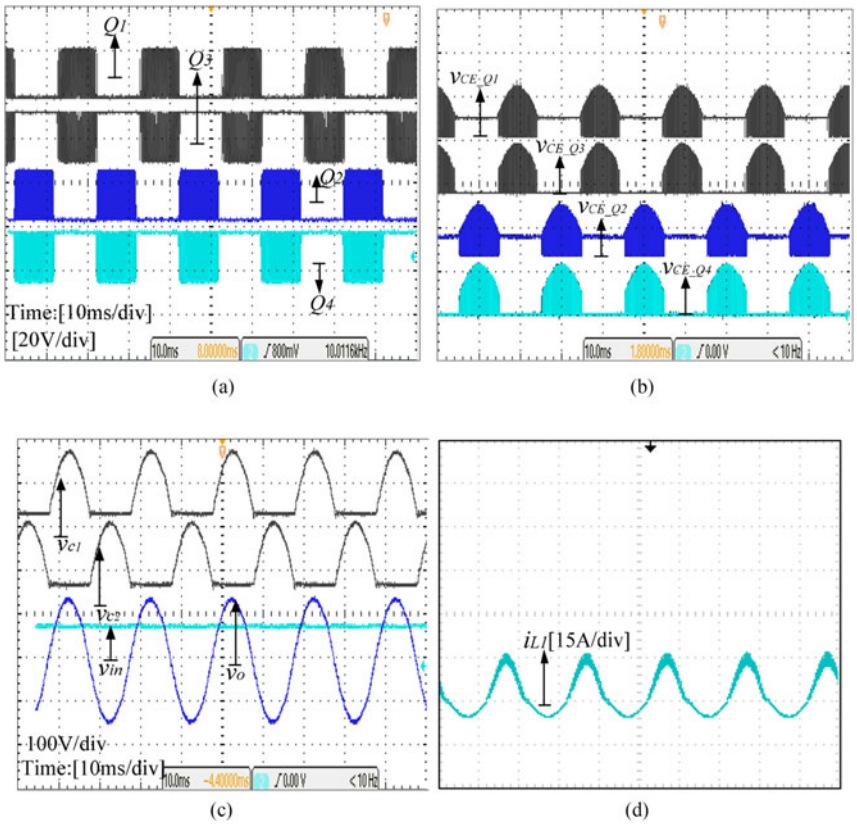


Fig. 13. Key waveforms of the HCM. (a) Driver waveforms, (b) voltage stress of switches waveforms, (c) output and input voltage key waveforms, and (d) current waveforms of inductor.

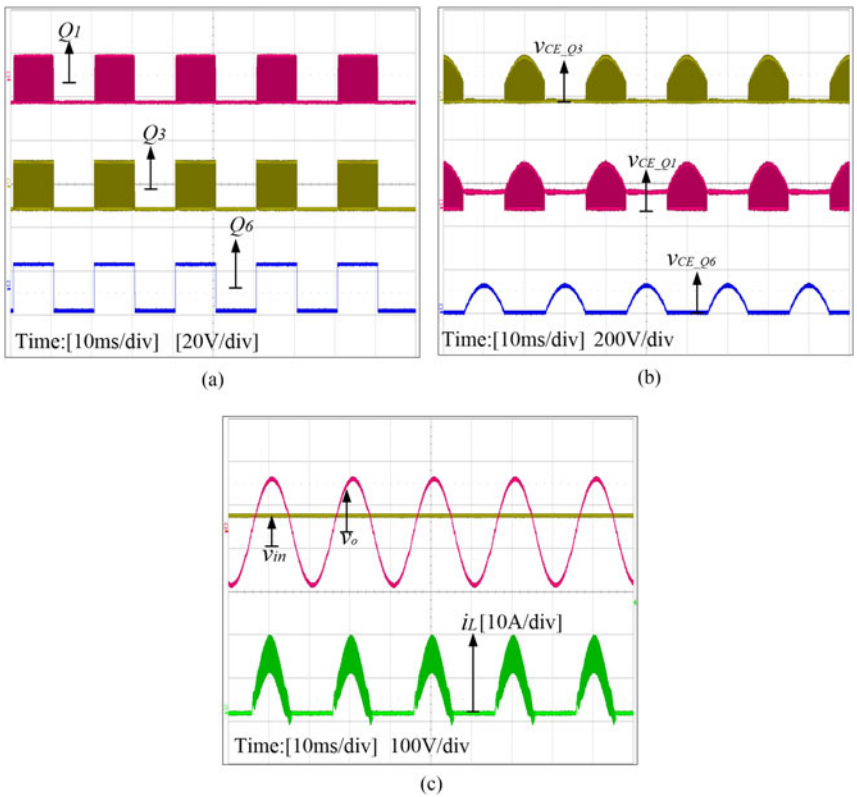


Fig. 14. Key waveforms of the HCM with clamping switches. (a) Driver waveforms, (b) voltage stress of switches waveforms, and (c) output and input voltage key waveforms.

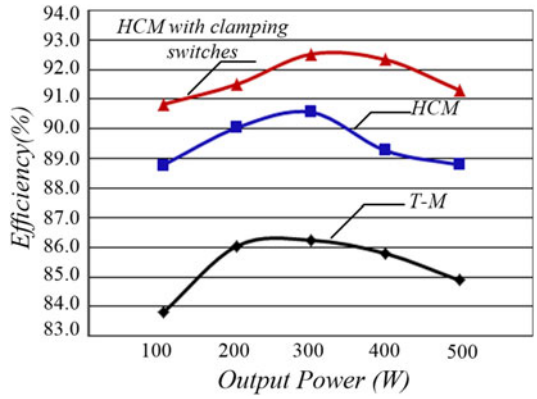


Fig. 15. Measured efficiency of DBI with three methods.

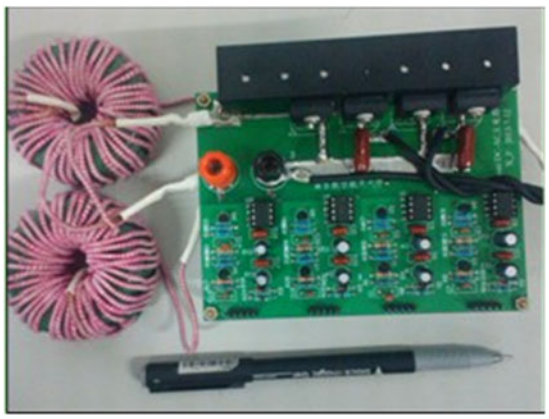


Fig. 16. Main circuit prototype of DBI.

ing switches was measured to be further higher, thanks to the clamping MOSFETs with low conduction loss. Fig. 16 shows the main circuit prototype of DBI.

VI. Conclusion

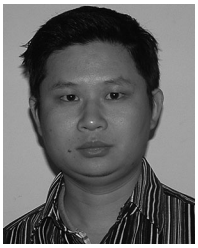
This paper proposed an improved DBI under HCM with clamping switches. According to the analysis and experimental results, the HCM strategy with clamping switches of DBI keeps the advantage of buck–boost ability. Furthermore, it brings the following advantages over the original one:

1) Only half of the switches are working in high frequency under HCM compared with T-M, which obviously reduces the switching loss of the DBI.
2) The voltage/current stress of the switches is lower with HCM than T-M, which will further reduce the switching loss and conduction loss of the power switches.
3) The inductor current is lower with HCM, which also reduces the magnetic loss.
4) Clamping switches is helpful to lower the current circulation loss of inductor and IGBT. With low-stress MOSFET, it can also reduce the conduction loss of circulation current. The efficiency of DBI can be improved with HCM because high-frequency switches is less than traditional modulation, also the inductor current stress is lower; in addition, the improved DBI can further improve the efficiency because of the low conduction loss by introducing low stress switches. The theoretical analysis and experiment results have been given to verify the analysis.

References

[1] B. Bose, "Global warming: Energy, environmental pollution, and the impact of power electronics," *IEEE Trans. Ind. Electron. Mag.*, vol. 4, no. 1, pp. 6–17, Mar. 2010.
[2] W. Zhao, C. Lu, and V. G. Agelidis, "Current control of grid-connected boost inverter with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2825–2832, Oct. 2011.
[3] R. O. Caceres and I. Barbi, "A boost DC–AC converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, Jan. 1999.
[4] Y. Chen and K. Smedley, "Three-phase boost-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2301–2309, Sep. 2008.
[5] B. Mirafzal, M. Saghaleini, and A. K. Kaviani, "An SVPWM based switching pattern for stand-alone and grid-connected three-phase single-stage boost inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1102–1111, Apr. 2011.
[6] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configurations," *IEEE Trans. Ind. Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.
[7] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.
[8] G. S. Ilango, P. S. Rao, A. Karthikeyan, and C. Nagamani, "Single-stage sine-wave inverter for an autonomous operation of solar photovoltaic energy conversion system," *Renew. Energy*, vol. 35, no. 1, pp. 275–282, 2010.
[9] L. S. Yang and T. J. Liang, "Analysis and implementation of a novel bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 422–434. Jan. 2012.
[10] Y. Zhou and W. Huang, "Single-stage boost inverter with coupled inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1885–1893, Apr. 2012.
[11] Y. Li, S. Jiang, J. G. Cintron-Rivera, and F. Zheng Peng, "Modeling and control of quasi-Z-source inverter for distributed generation applications," *IEEE Trans. Power Electron.*, vol. 60, no. 4, pp. 1532–1541, Apr. 2013.
[12] Y. Tang, X. Dong, and Y. He, "Active buck–boost inverter," *IEEE Trans. Power Electron.*, vol. 60, no. 8, pp. 4691–4697, 2014.
[13] T. F. Zhou, and W. X. Huang, "Single-stage boost inverter with coupled inductor," *IEEE Trans. Ind. Electron.*, vol. 27, no. 4, pp. 1885–1893, Apr. 2012.
[14] M. Jang and V. G. Agelidis, "A minimum power-processing-stage fuel-cell energy system based on a boost-inverter with a bidirectional backup battery storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1568–1576, May 2011.
[15] J. S. Lai, "Power conditioning circuit topologies," *IEEE Ind. Electron. Mag.*, vol. 3, no. 2, pp. 24–34, Jun. 2009.
[16] G. R. Zhou, S. C. Tan, K. W. Wang, and C. K. Tse, "Waveform control of fuel-cell inverter systems," in *Proc. Energy Convers. Congr. Expo.*, 2012, pp. 4457–4463.
[17] K. Jha and S. Mishra, "A dynamic linearizing modulator based boost inverter," in *Proc. Appl. Power Electron. Conf. Expo.*, 2013, pp. 2369–2373.
[18] P. Sanchis, A. Ursaea, and E. Gubia, "Boost DC–AC inverter: A new control strategy," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 343–353, Mar. 2005.
[19] M. Jang, M. Ciobotaru, and V. G. Agelidis, "A single-phase grid-connected fuel cell system based on a boost-inverter," *IEEE Trans. Ind. Electron.*, vol. 28, no. 1, pp. 279–288, Jan. 2013.
[20] C. Pan and C. Lai, "A high efficiency high step-up converter with low switch voltage stress for fuel cell system applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 1998–2006, May 2010.
[21] M. Jang, M. Ciobotaru, and V. G. Agelidis, "A single-stage fuel cell energy system based on a buck–boost inverter with a backup energy storage unit," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2825–2834, Jun. 2012.

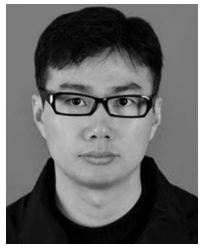
[22] D. Cortes, N. Vazquez, and J. A. Gallegos, "Dynamical sliding-mode control of the boost inverter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 9, pp. 3467–3476, Sep. 2009.



Yu Tang (M'09) received the B.S. and the Ph.D. degrees both in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2003 and 2008, respectively.

Since 2008, he has been with the Electrical Engineering Department, NUAA, where he is currently an Associate Professor. He has authored or coauthored more than 70 papers in journals and conference proceedings. His current research interest includes power electronics in renewable energy generation.

Yang Bai was born in China in 1992. He received the B. S. degree from the College of Electrical Engineering and Automation, Anhui University, Hefei, China, in 2014. He is currently working toward the M.S. degree at the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, China.



Jiarong Kan (M'13) was born in Jiangsu, China, in 1979. He received the M.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2007.

Since 2007, he has been with the School of Electrical Engineering, Yancheng Institute of Technology, Yancheng, China, where he is currently an Associate Professor. He holds three patents and has authored or coauthored more than 30 technical papers. His current research interest includes power electronics in renewable energy generation.

Fei Xu was born in China in 1989. He received the B.S. degree from the College of Electrical Engineering and Automation, Anhui University, Hefei, China, in 2013. He is currently working toward the M.S. degree at the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, China.