Effects of Auxiliary-Source Connections in Multichip Power Module

Helong Li, Stig Munk-Nielsen, *Member, IEEE*, Xiongfei Wang, *Member, IEEE*, Szymon Bęczkowski, Steve R. Jones, and Xiaoping Dai

***Abstract*—Auxiliary-source bond wires and connections are widely used in power modules with paralleled MOSFETs or insulated gate bipolar transistor (IGBTs). This paper investigates the operation mechanism of the auxiliary-source connections in multichip power modules. It reveals that the auxiliary-source connections cannot fully decouple the power loop and the gate loop such as the Kelvin-source connection, owing to their involvement in the loop of the power source current. Three effects of the auxiliary-source connections are then analyzed, which are 1) the common source stray inductance reduction, 2) the transient drain–source current imbalance mitigation, and 3) the influence on the steady-state current distribution. Finally, simulations and experimental results validate the theoretical analysis.**

***Index Terms*—Auxiliary connection, direct-bonded copper (DBC) layout, power module, SiC MOSFET.**

I. Introduction

MULTICHIP power modules with paralleled power semiconductor devices are widely used with today's power electronics applications, such as the renewable power systems [1]–[3], variable speed drives [4], and electrification of transport [5], [6]. With the new generation of power semiconductor devices switching faster, e.g., wide band gap (WBG) devices, the effects of the parasitic circuit parameters in the power module tend to be more apparent [7]–[10]. One challenge is that the common source stray inductance limits the switching speed and causes more switching losses [11]. Common source stray inductance is the stray inductance in both the gate–source current loop and the drain–source current loop. To avoid the common source stray inductance, auxiliary-source connections are usually used in fast switching multichip power modules [7], [12].

Auxiliary-source connection for a single die is called as Kelvin-source connection. The CoolMOS devices released by Infineon are equipped with Kelvin-source connections, and the Wolfspeed 900V SiC MOSFETs (C3M0065090J) in the D2PAK package also have Kelvin-source connection, which are shown in Fig. 1 [11], [13].

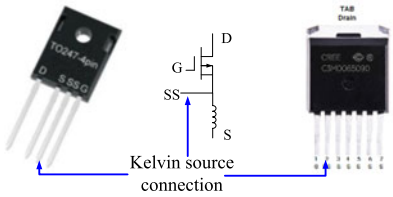


Fig. 1. Kelvin-source connection for a single device.

The Kelvin-source connection decouples the gate–source current loop and the drain–source current loop, which thus eliminates the effect of common source stray inductance on a single die, and consequently improves the switching speed with the reduced switching losses [11], [14]–[17]. It shows that using the Kelvin source connection can reduce up to 44% turn-on loss and up to 40% turn-off loss [14], [17]. This loss reduction substantially improves the thermal performance of device and the system efficiency. Furthermore, increasing the switching speed by using the Kelvin-source connection is preferred over the reduction of the gate resistor, since the latter will increase gate current and leads to extra gate oscillations [17].

In the multichip power modules with the auxiliary-source connections [12], [18], [19], it is usually deemed that the auxiliary-source connections can have similar effects to the Kelvin-source connections, i.e., avoiding the adverse effects of the common source stray inductance, and therefore improving the switching speed with reduced switching losses. However, in this paper, it is revealed that there are differences between the effects of the Kelvin-source connection on the single device and that of the auxiliary-source connections in the multichip power modules. The operation mechanism and effects of auxiliary-source connections are further analyzed in detail.

This paper is organized as follows: the auxiliary-source connections are described in Section II, where the differences between the Kelvin-source connection and the auxiliary-source connections are discussed with mathematic analysis and circuit modeling. It is found that the auxiliary-source connections are involved in the power current loop, which causes the circulating current among the auxiliary-source connections. Then, the effects of auxiliary-source connections on the switching performance of power modules are systematically analyzed in Section III, which include the reduction of the common source

Manuscript received September 9, 2016; revised October 27, 2016; accepted December 5, 2016. Date of publication December 13, 2016; date of current version May 9, 2017. Recommended for publication by Associate Editor Baoxing Chen.

H. Li and S. Jones are with the Dynex Semiconductor Ltd., Lincoln LN6 3LF, United Kingdom (e-mail: helong.li@dynexsemi.com; Steve_Jones@dynexsemi.com).

S. Munk-Nielsen, X. Wang, and S. Bęczkowski are with the Department of Energy Technology, Aalborg University, Aalborg 9100, Denmark (e-mail: smn@et.aau.dk; xwa@et.aau.dk; sbe@et.aau.dk).

X. Dai is with the State Key Laboratory of Advanced Power Semiconductor Devices, Zhuzhou 412000, China (e-mail: daixp@csrzic.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2639327

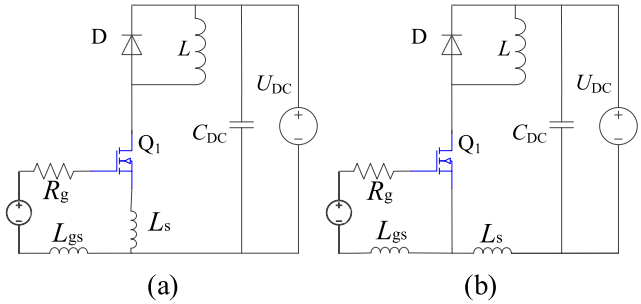


Fig. 2. Single MOSFET (a) without the Kelvin-source connection and (b) with the Kelvin-source connections.

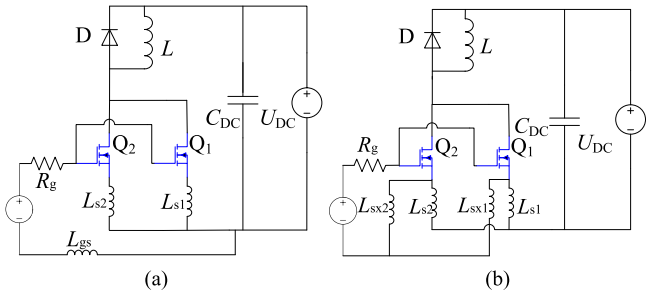


Fig. 3. Two-paralleled MOSFETs (a) without auxiliary-source connections and (b) with auxiliary-source connections.

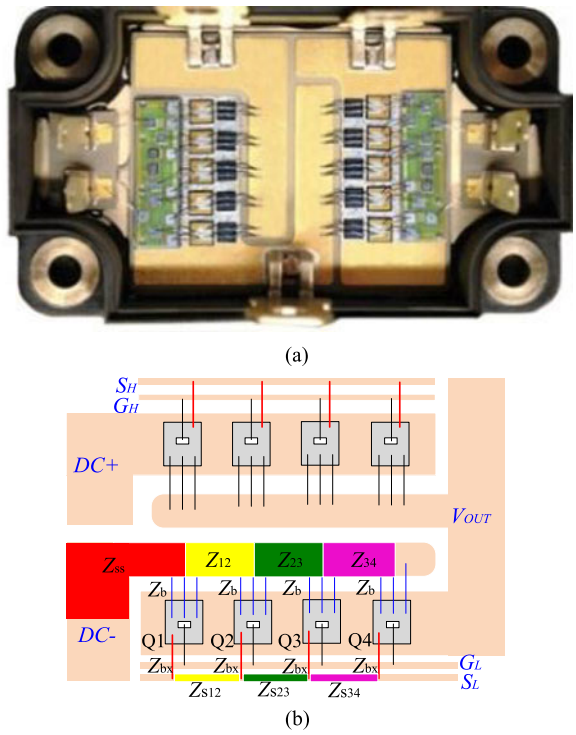


Fig. 4. (a) Multichip power module with auxiliary-source connections and (b) multichip DBC layout with auxiliary-source connections.

stray inductance, the mitigation of the transient drain–source current imbalance, and the influence on the steady-state current distribution in the bond wire. The experimental results are presented in Section IV, which validate the theoretical analysis and the effects of the auxiliary-source connections. Finally, conclusions are presented in Section V.

II. Kelvin-Source and Auxiliary-Source Connection

A. Kelvin-Source Connection and Auxiliary-Source Connection

A single MOSFET device with and without the Kelvin-source connection is illustrated in the double pulse test circuit shown in Fig. 2. In Fig. 2(a), Q_1 is the MOSFET. D is the diode. L is the load inductor. $C_{\rm dc}$ is dc link capacitor. $U_{\rm dc}$ is the dc link voltage. $L_{\rm gs}$ is the stray inductance only included in the gate–source loop, regardless of Kelvin-source connection. L_s is included in both in the gate–source loop and the drain–source loop without Kelvin-source connection. In contrast, Fig. 2(b) clearly shows that with the Kelvin-source connection, the gate–source current loop and the drain source current loop are fully decoupled. Hence, the Kelvin-source connection can avoid the effect of the common stray inductance, thus improving switching speed and reducing switching losses [9].

Fig. 3 illustrates the use (or not) of the auxiliary-source connections with two paralleled MOSFETs in the double-pulse test circuit. Fig. 3(a) shows that L_{s1} and L_{s2} are the common source stray inductances for Q_1 and Q_2, respectively. Fig. 3(b) depicts the use of the auxiliary-source connections, i.e., $L_{\rm sx1}$ and $L_{\rm sx2}$ to decouple the stray inductances L_{s1} and L_{s2}.

However, by taking a closer look at Fig. 3(b), it can be found that $L_{\rm sx1}$ and $L_{\rm sx2}$ still form a current loop with power source currents of MOSFETs Q_2 and Q_1. For example, the drain current of Q_2 can go through $L_{\rm sx2} - L_{\rm sx1} - L_{s1}$, and then back to the dc link. This means that the auxiliary-source connections for the paralleled devices cannot fully decouple the gate–source current loop and the drain–source current loop, as single device with Kelvin-source connection.

The magnitude of the current going through $L_{\rm sx2}$ and $L_{\rm sx1}$ depends on the impedance of the path $L_{\rm sx2} - L_{\rm sx1} - L_{s1}$ and the path of L_{s2}. Hence, considering the parasitic resistances, the impedance Z, instead of the inductance L, is used in the following analysis.

B. Auxiliary-Source Connections Within Multichip Power Modules

A SiC MOSFET multichip half-bridge power module with the auxiliary-source connections is shown in Fig. 4(a). The direct bonded copper (DBC) layout of this power module is shown in Fig. 4(b). To elaborate the effect of the auxiliary source connection on the multichip power module, a circuit model of the DBC layout with the auxiliary-source connections is shown in Fig. 5.

$Z_{\rm bn}$ is the impedance of power source bond wires. Z_{12}, Z_{23}, Z_{34}, and $Z_{\rm ss}$ are the impedances of the DBC traces, as stated in Fig. 4(b). Z_{s12}, Z_{s23}, Z_{s34} are the impedance of the auxiliary DBC traces. $Z_{\rm bx}$ is the impedance of the auxiliary-source bond wires.

Similar to the case of paralleling two MOSFETs, the auxiliary-source connections in the multichip power module are also

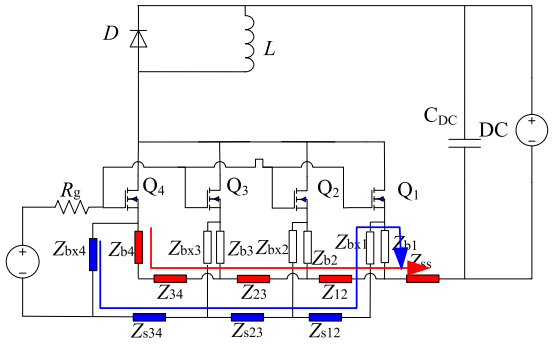


Fig. 5. Modeling of the DBC layout in a double pulse test circuit with auxiliary-source connections.

involved in the power source current loops. For instance, the MOSFET drain current I_{D4} can go back to the dc-terminal via $Z_{b4} - Z_{34} - Z_{23} - Z_{12} - Z_{\rm ss}$, which is the expected path, as depicted with the red curve. But it can also go through $Z_{\rm bx4} - Z_{s34} - Z_{s23} - Z_{s12} - Z_{\rm bx1} - Z_{b1} - Z_{\rm ss}$, as illustrated with the blue curve, even though this current loop has much higher impedance than the expected one. The current distribution in the DBC layout depends on the impedance relationship of the different paths, which will be analyzed in Section III.

III. Effects of Auxiliary-Source Connections

A. Reduction of Common Source Stray Inductance

Although the auxiliary-source connections are involved in the power source current loop, they can still mitigate the effect of the common source stray inductance in the power module. With the auxiliary-source connections illustrated in Fig. 4, the inductance of the DBC traces $Z_{\rm ss}$ is not involved in gate source current loop any more, which means that it is excluded from the common source stray inductance of the whole power module, i.e., the common source stray inductance of the whole power module is reduced. Therefore, one of the auxiliary-source connection effects is the reduction of the common source stray inductance for the whole power module. Consequently, it can improve the switching speed of the power module and reduce the power losses, as the effect of Kelvin-source connection.

B. Mitigation of Transient Current Imbalance

The paralleled dies in this DBC layout have the mismatched value of common source stray inductance and the current coupling effect, which may lead to the large transient current imbalance [6]. In the saturation region, the small signal model of the MOSFET drain current and the gate–source voltage is

$$i_D = g_{\rm fs}(V_{\rm GS} - V_{\rm th}). \tag{1}$$

And the gate–source voltage is

$$V_{\rm GS} = V_{\rm driver} - i_G R_G - L_s \frac{di_s}{dt} = V_{\rm driver} - i_G R_G - \triangle V_{\rm LS}. \tag{2}$$

The paralleled dies usually have a common gate driver. Compared to drain–source current, the gate–source current is

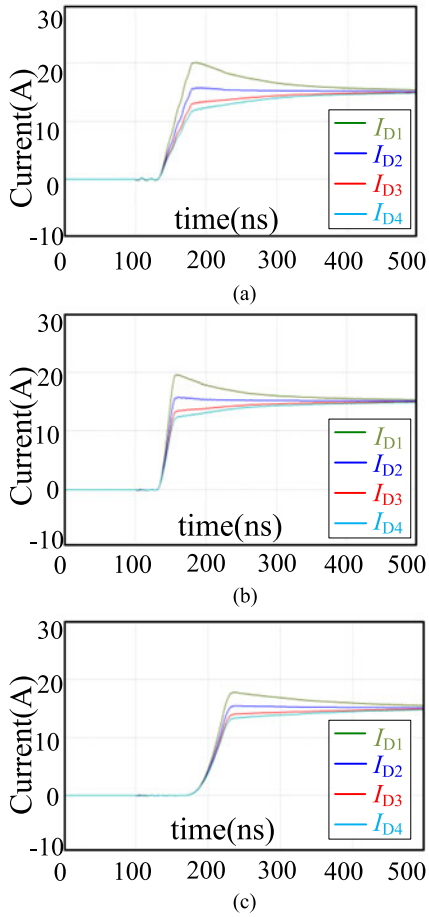


Fig. 6. Simulation results of transient drain current distribution (a) without auxiliary-source connections ($R_g = 10\,\Omega$), (b) with auxiliary-source connections ($R_g = 10\,\Omega$), and (c) with auxiliary-source connections ($R_g = 23\,\Omega$).

negligible, and thus the difference in the gate voltage potentials of the paralleled MOSFETs is very small. Therefore, the difference in gate–source voltages between paralleled MOSFETs is the voltage potential difference between the source pads of the paralleled MOSFETs, i.e., V_{s1s2}. The transient current imbalance between two paralleled dies can be described as

$$i_{D1} - i_{D2} = g_{\rm fs}(V_{\rm GS1} - V_{\rm GS2}) = g_{\rm fs} V_{s2s1}. \tag{3}$$

The auxiliary connections can be considered as a parallel path to the power source path, thus reducing the total impedance for the power source current paths. Assuming that the impedance relationships of the auxiliary-source connections and the power source traces are $Z_{\rm bx} = 3Z_b$ and $Z_{s12} = Z_{s23} = Z_{s34} = 3Z_{12} = 3Z_{23} = 3Z_{34}$, the transient current simulation results of the paralleled four dies with this DBC layout are shown in Fig. 6.

The di/dt for MOSFET1 in Fig. 6(a) is about 0.7 A/ns while in Fig. 6(b) the di/dt for MOSFET1 is about 1.6 A/ns. di/dt in Fig. 6(b) is larger than that in Fig. 6(a) and it verifies that the auxiliary-source connections reduce the total common source stray inductance, similarly to that of the Kevin-source connection. di/dt by increasing the gate resistance in Fig. 6(c) is also

similar to that in Fig. 6(a), but the current imbalance in Fig. 6(c) is reduced compared to that in Fig. 6(a).

C. Steady-State Current Distribution in the Power Source Bond Wires

Assuming again the impedance relationships of the power trace and the auxiliary-source connections as $Z_{\rm bx} = 3L_b$ and $Z_{s12} = Z_{s23} = Z_{s34} = 3Z_{12} = 3Z_{23} = 3Z_{34}$, the steady-state current distributions of the power-source bond wires $Z_{b1} - Z_{b4}$ and the auxiliary-source bond wires can be calculated as

$$\begin{cases} I_{\rm Zbx1} = -\dfrac{31}{84}I_D, & I_{\rm Zbx2} = \dfrac{1}{84}I_D, \\ & I_{\rm Zbx3} = \dfrac{13}{84}I_D, \quad I_{\rm Zbx4} = \dfrac{17}{84}I_D \\ I_{\rm Zb1} = \dfrac{115}{84}I_D, & I_{\rm Zb2} = \dfrac{83}{84}I_D, \\ & I_{\rm Zb3} = \dfrac{71}{84}I_D, \quad I_{\rm Zb4} = \dfrac{67}{84}I_D \end{cases}. \tag{4}$$

I_D is the steady-state drain current of the MOSFET. $I_{\rm Zbxn}$ is the current going through the auxiliary-source bond wires. $I_{\rm Zbn}$ is the current going through the power source bond wires.

It is noted that Z_{b1} has the highest current stress while Z_{b4} has the lowest current stress. This fact proves that the auxiliary-source bond wires are not only carrying on the gate current, but they are also stressed by the current flowing through the drains. The simulation results of the current distribution in the power source bond wires and the auxiliary-source bond wires are shown in Fig. 7.

The impedance of the DBC traces and bond wires in the power module may be different from the case of $Z_{\rm bx} = 3Z_b$. However, the auxiliary-source connection will take the steady-state power current. Based on the mathematic analysis and simulation, the auxiliary-source effects can be summarized as follows.

1) First, the auxiliary-source connections can reduce the common source stray inductance of the power module, the effect of which is similar with the Kelvin-source connection.
2) Second, the auxiliary-source connection can mitigate transient current imbalances among the paralleled dies, since the power currents also go through the auxiliary-source connections. Consequently, the current going through the power traces and bond wires are reduced. With the same switching period, di/dt is reduced. Therefore, the source voltage potential differences are also reduced, which will mitigate the transient current imbalances.
3) Third, the auxiliary-source connections are involved in the power current loop, which will increase the current stresses on the auxiliary-source connections and current imbalances in the power source bond wires. The steady-state current distribution in the power source bond wires is affected by auxiliary-source connections.

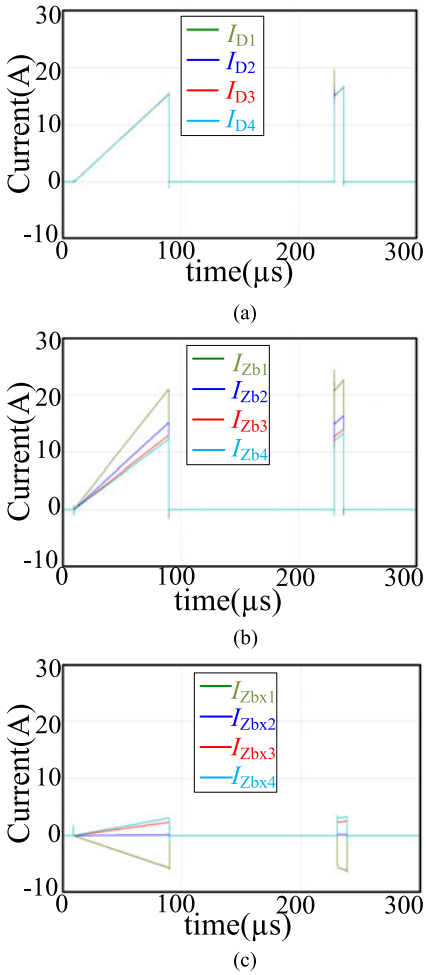


Fig. 7. Simulation results of the steady-state current distributions (a) four MOSFETs drain currents, (b) currents in the power source bond wires, and (c) currents in the auxiliary-source bond wires.

IV. Experimental Study

The experimental study of the current distributions in the multichip power module is performed with printed circuit board (PCB) circuits, which are designed to have the similar layout of the DBC, as shown in Fig. 8.

A. Reduction of Common Source Stray Inductance

The experimental results of the total current of four paralleled SiC MOSFETs are shown in Fig. 9. Fig. 9(a) shows the total current of the paralleled four SiC MOSFETs without the auxiliary-source connections while Fig. 9(b) shows the total current with auxiliary-source connections. These two experimental results are carried out with the same gate driver condition.

The turn-on maximum di/dt of the total current without the auxiliary source connections is about 3.1 A/ns while the turn-on maximum di/dt of the total current with the auxiliary source connections is increased up to 4.3 A/ns. During the turn-off process, the maximum di/dt without the auxiliary source connections is about 1.9 A/ns and the maximum di/dt with the

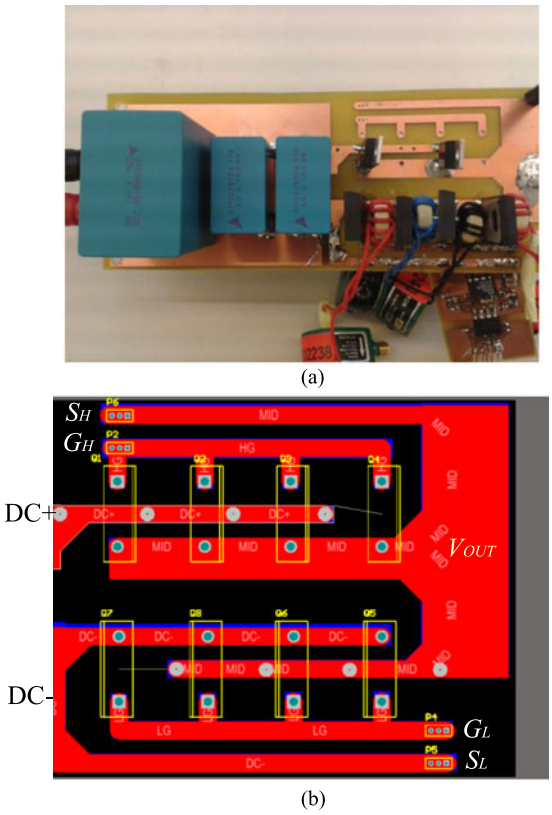


Fig. 8. Experimental study with PCB circuit (a) PCB hardware circuit and (b) PCB layout.

auxiliary source connections is up to 3.2 A/ns. The total current turn-on and turn-off switching speeds with auxiliary-source connections are around 38% and 68% faster than that without the auxiliary-source connections, respectively. It validates that the auxiliary-source connections reduce the total common source stray inductance and improve the power module switching speed.

The total current overshoot is caused by the parasitic capacitance from the freewheeling diode and the load inductor. Since the switching speed of the total current is increased with the auxiliary source connection, the overshoot of the total current is also larger than that without the auxiliary source connection.

B. Mitigation of Transient Current Imbalance

The transient current distribution among the paralleled MOSFETs is shown in Fig. 10(a) without auxiliary-source connections and in Fig. 10(b) with auxiliary-source connections.

In Fig. 10(a), MOSFET1 has a turn-on maximum di/dt about 1.6 A/ns which is about four times higher than that of MOSFET4 about 0.4 A/ns. In Fig. 10(b), MOSFET1 has a turn-on maximum di/dt about 1.5 A/ns and MOSFET4 has a turn-on maximum di/dt about 0.8 A/ns.

It can be seen that the transient current imbalance among the paralleled MOSFETs is mitigated with the auxiliary-source connections. With the auxiliary source connections, the turn-off delay time is reduced dramatically, from about 20 ns to only 5 ns. However, the transient current imbalance still exists.

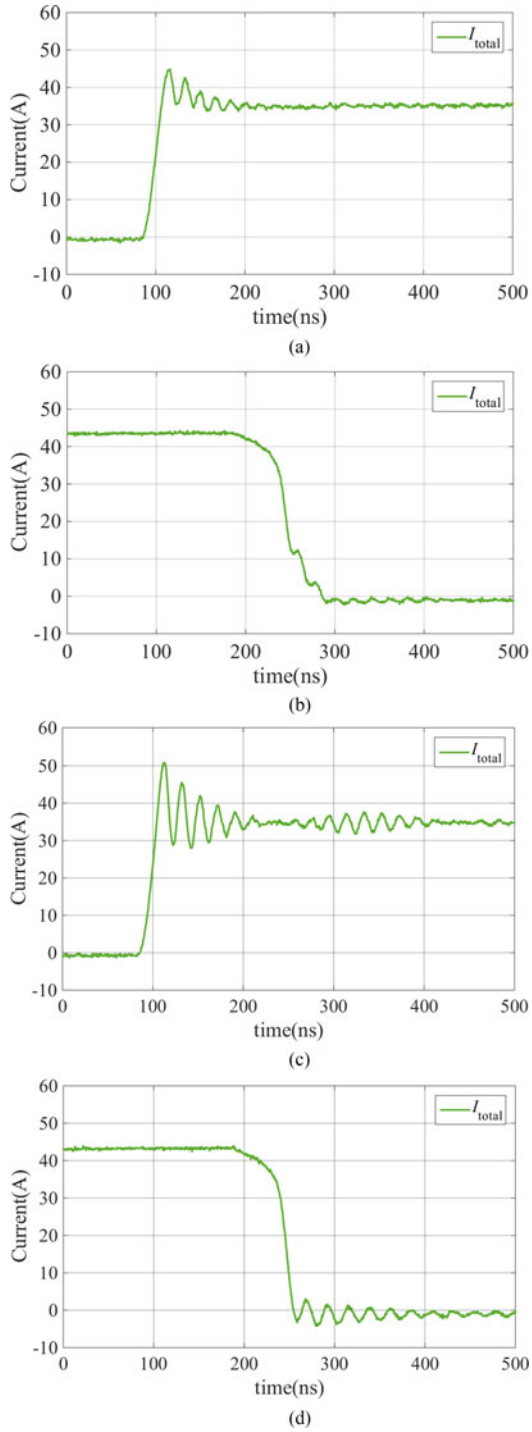


Fig. 9. Experimental results of the total SiC MOSFETs current (a) without auxiliary-source connections and (b) with auxiliary-source connections.

Auxiliary-source connections can mitigate the transient current imbalance but the mitigation effect is limited.

Simulation results with the parasitic parameters close to the PCB circuit are shown in Fig. 11. The simulation results of Fig. 11(a) and (b) are consistent with the experimental results in Fig. 9(a) and Fig. 10(a), respectively, which validates the effectiveness of the equivalent circuit model as well as the transient current distribution analysis with the PCB circuits.

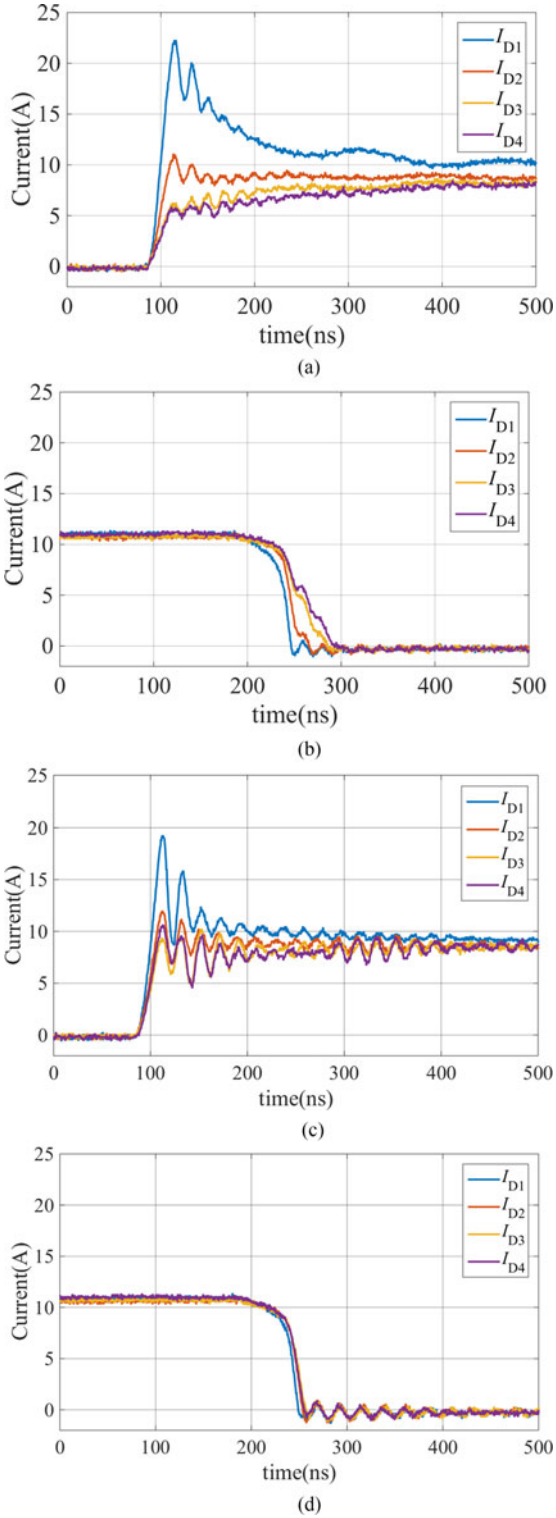


Fig. 10. Transient MOSFETs drain current distribution (a) without auxiliary-source connections and (b) with auxiliary-source connections.

C. Steady-State Current Distribution

The steady-state current distribution is done with a higher current level in order to see the currents in the auxiliary-source connections. The MOSFETs drain currents and the currents in the auxiliary-source connections are shown in Fig. 12. The

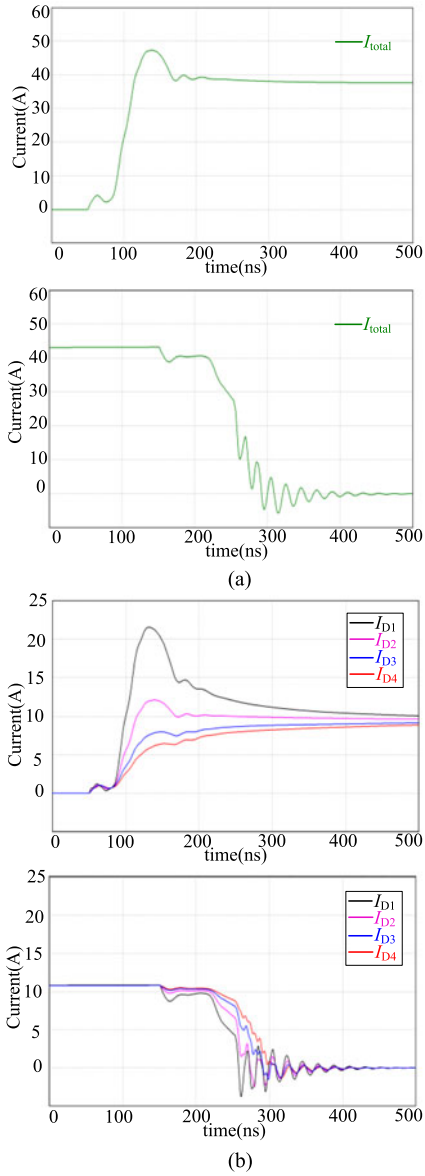


Fig. 11. Transient MOSFETs current simulation results with PCB circuit parasitic parameters and without auxiliary source connections (a) total current (b) individual MOSFETs currents.

auxiliary-source connections take much higher current than the gate current.

In this experimental study, the ratio of the drain currents flowing through the auxiliary-source connections is larger than expected in a power module. This is because the auxiliary-source connections in this experimental study were made with copper wires which have impedance comparable to that of the PCB traces of the drain connection. Therefore, the relationship between the impedance of the auxiliary-source connections and that of the drain connection is much smaller than that in a power module. Normally in a power module, the impedances of the auxiliary-source connections are a few orders of magnitude bigger than the ones of the drain connection. The current flowing through the auxiliary-source connection should be much smaller when compared to the one flowing through the drain connection.

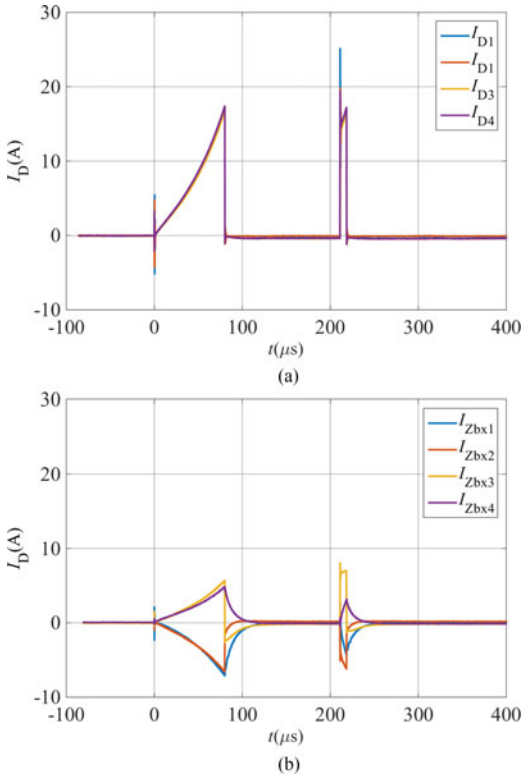


Fig. 12. Steady-state current distribution of (a) MOSFETs drain currents and (b) auxiliary-source connections currents.

V. Conclusion

This paper investigates the effects of auxiliary-source connections in multichip power modules with paralleled MOSFETs. Auxiliary-source connections can reduce common source stray inductances for multichip power modules. But they cannot totally decouple the gate–source loop and the drain–source loop because they are still in the loop of drain currents. Moreover, auxiliary-source connections are able to mitigate the transient MOSFETs current imbalances. Simultaneously, they also lead to steady-state current imbalances in the bond wires of the power source traces due to currents flowing through the auxiliary-source connections. Simulation and experimental results validate the analysis of current distributions during both transient period and steady-state period. In the design of the fast switching multichip power module, auxiliary source connections can help improve the switching speed of the power module and mitigate the transient current imbalances. But there may be steady-state circulating current among the auxiliary source connection. One possible solution to suppress the auxiliary-source steady-state currents is inserting source resistors in the auxiliary-source connections, by which the impedance of the auxiliary source connections can be significantly increased.

References

[1] R. J. Callanan *et al.*, "Recent progress in SiC DMOSFETs and JBS diodes at cree," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, 2008, pp. 2885–2890.

[2] A. Volke and M. Hornkamp, *IGBT Modules*. Munich, Germany: Infineon Technol. A.G., 2012.

[3] P. Ghimire, K. B. Pedersen, A. R. Vega, B. Rannestad, S. Munk-Nielsen, and P. B. Thogersen, "A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application," in *Proc. 8th Int. Conf. Integr. Power Electron. Syst.*, 2014, pp. 1–6.

[4] Z. Xu, D. Jiang, M. Li, P. Ning, F. Wang, and Z. Liang, "Development of Si IGBT phase-leg modules for operation at 200°C in hybrid electric vehicle applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5557–5567, Jan. 2013.

[5] J. Bauer, T. Duetemeyer, and L. Lorenz, "New IGBT development for traction drive and wind power," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 768–772.

[6] X. Perpiñà, L. Navarro, X. Jordà, M. Vellvehi, J. Serviere, and M. Mermet-Guyennet, "Reliability and lifetime prediction for IGBT modules in railway traction chains," 2012 [Online]. Available: http://www.intechopen.com/books/reliability-and-safety-inrailway/reliability-and-lifetime-prediction-for-igbt-modules-in-railwaytraction-chains

[7] Z. Chen et *al.*, "Development of a 1200 V, 120 A SiC MOSFET module for high-temperature and high-frequency applications," in *Proc. Wide Bandgap Power Devices Appl.*, 2013, pp. 52–59.

[8] H. Li, S. Beczkowski, S. Munk-Nielsen, R. Maheshwari, and T. Franke, "Circuit mismatch and current coupling effect influence on paralleling SiC MOSFETs in multichip power modules," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2015, pp. 1–8.

[9] H. Li *et al.*, "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[10] H. Li and S. Munk-Nielsen, "Challenges in switching SiC MOSFET without ringing," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2014, pp. 1–6.

[11] F. Stueckler and E. Vecino, "Cool MOS C7 650V switch in a kelvin source configuration," *Infineon Appl. Note*, [Online]. Available: http://www.infineon.com/dgdl/Infineon+-+Application+Note+-+TO-247-4pin+-+650V+CoolMOS+C7+Switch+in+a+Kelvin+Source+Configuration.pdf?fileId=db3a30433e5a5024013e6a9908a26410

[12] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[13] Wolfspeed, "C3M0065090J," Datasheet, 2013.

[14] Infineon, "TRENCHSTOP 5 IGBT in a Kelvin Emitter Configuration," *Infineon Appl. Note*, [Online]. Available: http://www.infineon.com/dgdl/Infineon-Application+Note+TRENCHSTOP%E2%84%A2+5+in+TO-247+4pin-AN-v01_00-EN.pdf?fileId=5546d4624933b875014974f4d97e09ea

[15] V. Scarpa and F. Brucchi, "Kelvin emitter configuration further improves switching performance of TRENCHSTOP 5 IGBT," *Infineon Appl. Note*, [Online]. Available: http://www.powerguru.org/kelvin-emitter-configuration-further-improves-switching-performance-of-trenchstop-5-igbts/

[16] C. G. Stella, M. Laudani, A. Gaito, and M. Nania, "Advantage of the use of an added driver source lead in discrete power MOSFETs," in *Proc. Appl. Power Electron. Conf. Expo.*, 2014, pp. 2574–2581.

[17] V. Crisafulli and M. Antretter, "Kelvin source connection for high current IGBTs. A way to get high energy efficiency," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2015, pp. 1–7.

[18] P. Ning *et al.*, "SiC wirebond multichip phase-leg module packaging design and testing for harsh environment," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 16–23, 2010.

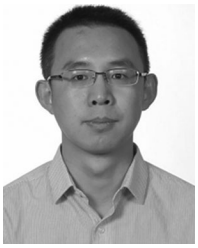
[19] F. Xu *et al.*, "High temperature packaging of 50 kW three-phase SiC power module," in *Proc. 3rd IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2427–2433.

Helong Li received the B.Sc. degree and the M.Sc. degree in power electronics from School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin, China, in 2010 and 2012, respectively. He received the PhD degree in power electronics from Department of Energy Technology, Aalborg University, Denmark, in 2015.

Since 2016, he has been with Dynex Semiconductor Ltd., Lincoln, U.K., where he is currently a Senior R&D Engineer in R&D Center. His research interests include power semiconductor (e.g., IGBT and SiC MOSFET) packaging and application.

Stig Munk-Nielsen (S'92–M'97) received the M.Sc. and Ph.D. degrees in power electronics from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.

He is currently a Professor in the Department of Energy Technology, Aalborg University. In the last ten years, he has been involved or has managed 12 research projects, including national and European Commission projects. He is the holder of patents on resonant converters. His research interests include LV and MV inverters, permanent magnet biased inductors, failure modes, accelerated lifetime test, dc/dc converters, and fleet monitoring.



Xiongfei Wang (S'10–M'13) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree from the Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2013.

Since 2009, he has been with the Aalborg University, where he is currently an Assistant Professor in the Department of Energy Technology. His research interests include modeling and control of power converters, grid converters for renewable energy systems and microgrids, harmonic analysis, and stability of power electronics based power systems.

Dr. Wang is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS and the Guest Associate Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS Special Issue on Harmonic Stability and Mitigation in Power Electronics Based Power Systems.

Szymon Bęczkowski received the M.Sc. degree in electrical engineering from the Warsaw University of Technology, Warsaw, Poland, in 2007, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2012.

He is currently working as an Assistant Professor in the Department of Energy Technology, Aalborg University. His research interests include high-voltage power electronic converters and SiC technology.

Steve R. Jones received the B.Eng. (Hons.) degree in electrical and electronic engineering and the Ph.D. degree in semiconductor physics from the Sheffield University, Sheffield, U.K.

Currently, he is working as an IGBT Technology Manager at Dynex Semiconductors Ltd., Lincoln, U.K. Previous work experience includes AEI Semiconductors, Marconi Electronic Devices Ltd., GEC Plessey Semiconductors Ltd., Eurotec (Danfoss Silicon Power), and Semelab PLC, spanning 40years.

Xiaoping Dai received the Graduate degree in semiconductor manufacturing technology from Xi'an Jiaotong University, Xi'an, China.

He has engaged in developing high-power semiconductor technology for more than 20 years, he is currently looking after R&D Center, SBU Zhuzhou CRRC Times Electric Ltd., Zhuzhou, China, and Dynex Semiconductor Ltd., Lincoln, U.K.