Dynamic Response Improvements of Parallel-Connected Bidirectional DC–DC Converters for Electrical Drive Powered by Low-Voltage Battery Employing Optimized Feedforward Control

Deshang Sha, *Member, IEEE*, Jiankun Zhang, Xiao Wang, *Student Member, IEEE*, and Wenqi Yuan

***Abstract*—Parallel-connected modular current-fed bidirectional dc–dc converters are used for the AC motor drive system powered by batteries with low voltage and wide voltage range. The input current ripple can be reduced significantly by employing interleaving technology not only for individual module but also for all the modules. A current sharing control strategy is applied for the constituent modules. Double pulse width modulation plus double phase shifted control with equal duty cycles for one module can minimize the circulation loss and avoid nonactive power issue. Factors affecting dynamic performance are investigated based on the small-signal modeling. The leakage inductance value is optimized in view of system reliability and better dynamic performance. Besides, to improve the dynamic performance further, feedforward control employing optimized feedforward coefficient based on the small-signal analysis is implemented. A 4-kw prototype composed of two bidirectional dc–dc converters is built to verify the effectiveness for the proposed control strategy in AC motor drive application with fast regenerative braking.**

***Index Terms*—Current sharing, dc–dc converter, dynamic performance, feedforward control, motor drive, parallel connected.**

I. INTRODUCTION

ELECTRICALdrive supplied by the battery is widely used for electrical vehicles and some servo systems [1], [2]. The power electronic converter is preferred to have bidirectional power flow capability, i.e., energy can be transferred between the battery and motor to operate in motoring mode or regeneration mode [3]. Thus, a bidirectional dc–dc converter is needed to work as the interface [4] between the high voltage dc link and the battery side. If the battery voltage is high at the dc-link voltage level, a nonisolated bidirectional dc–dc converter such as buck/boost can be used [5]–[9]. To use a nonisolated dc–dc converter between the high voltage dc link and the battery, a number of battery packs must be connected in series to meet the voltage level. However, too many battery packs [10] connected in series reduce the volumetric efficiency [11]. Besides, voltage equalizer for each cell is needed due to the series connection. In some applications, such as aeronautic application, the battery voltage is rather low and the equalizer circuit is not needed. Therefore, an isolated bidirectional converter is required to work as an interface between the low-voltage battery and a high-voltage dc bus [12].

For flexible voltage gain, power density, cost, and safety considerations, high-frequency isolated bidirectional dc–dc converters are widely used. Among them, voltage-fed dual-active bridge (VF-DAB) is a preferred topology [13]–[17]. Many control strategies for VF-DAB have been proposed. Single phase shift (SPS) control is implemented by modulating both the two H-bridges with 50% duty cycles [18]. The output power capacity and the direction are regulated by only the phase shift between the two high-frequency square waveforms. Zero voltage switching (ZVS) of power switches and unified control can be achieved. Unfortunately, when the magnitudes of the input/output voltages are not matched, ZVS may be lost in a wide load range and the conduction loss increases significantly. Energy storage systems using ultracapacitors or batteries usually feed a dc bus where the voltage has to be regulated. The voltage variation across the ultracapacitor or battery depends on many parameters like its depth of discharge, the input/output power, and temperature and can even reach one-half the rated voltage. This fact requires the existence of a power interface with a wide voltage conversion ratio capability. By using VF-DAB, if the voltage conversion ratio varies too much, the inductor current slew rate during the power transfer stage may not be kept to be zero, thus the inductor root-mean-square (rms) current cannot be optimized to be the minimum. For an energy storage system, the VF-DAB is not suited since its significant current ripple may reduce the lifetime of some energy storage devices [19].

Comparatively, for energy storage applications requiring wide voltage conversion ratio and low charging/discharging current ripple, a current-fed (CF) DAB may be a good option. A CF boost type dc–dc using only SPS control can reduce the current ripple significantly [20]. The CF-DAB can reduce the low

Manuscript received May 19, 2016; revised October 31, 2016; accepted December 1, 2016. Date of publication December 21, 2016; date of current version May 9, 2017. This work was supported in part by the National Natural Science Foundation of China under Grant 51577012, in part by the Program for New Century Excellent Talents in University of China under Grant NCET-13-0043, in part by Technology Foundation for Selected Overseas Chinese Scholar (2014) supported by the Ministry of Human Resources and Social Security of China, and in part by 2016 Fundamental Research Fund of Beijing Institute of Technology. Recommended for publication by Associate Editor B. Lehman. *(Corresponding author: Deshang Sha.)*

The authors are with the Advanced Power Conversion Center, School of Automation, Beijing Institute of Technology, Beijing 100081, China (e-mail: shadeshang@bit.edu.cn; backpacker47@bit.edu.cn; i_virtualsky@126.com; yuanwenkey@163.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2637370

voltage side (LVS) current ripple significantly by interleaving technology [21], [22]. But the circulation loss is relatively high as the voltage conversion ratio varies. To deal with this issue, a naturally clamped zero-current commutated CF converter was proposed [23]. But ZVS may be lost for CF side switches. An active clamp CF converter with pulse width modulation (PWM) plus phase shift control was proposed [24], [25], in which the LVS is PWM modulated while effective duty cycle for the high voltage side (HVS) switches are fixed as 50% neglecting the effect of the dead time. However, this causes nonactive power issue. It also brings high current spike when the LVS voltage is low and additional nonactive power when the LVS voltage is high. A CF-DAB with dual PWM control was proposed [26], [27]. But ZVS may be lost for CF side switches. In PV applications [28], the voltage is designed to be unmatched purposely to achieve ZVS. It is effective in unidirectional power flow situations. The effectiveness needs to be considered more in in reverse power flow applications.

In the low voltage and high power rating applications, it is not good for one module to handle such large current at LVS. Parallel-connected modular power converters can be a good solution [29]. A bidirectional interleaved CF converter was proposed for the energy storage system [30]. Current sharing can be achieved by common phase shift [31] or common duty cycle [32] control for parallel-connected bidirectional dc–dc converters [33] or unidirectional dc–dc converters. The unidirectional is not really modular configuration due to the connection of the rectifier stage. The dynamic performance may be limited due to the lack of current loops.

Besides, steady-state performances of the DAB, such as circulation loss and nonactive current reduction, soft switching for LVS side switches, have been discussed extensively in previous works [13]–[28], [34], [35]. The equivalent leakage inductance value has been designed in an optimal way to achieve ZVS, but its effect on the dynamic performance is seldom addressed. Actually, dynamic performance is also important for DAB converters especially for electrical motor drive application that requires fast dynamic response. During the motor acceleration stage, the voltage of the dc bus will drop and may cause under voltage protection for the inverter. On the other hand, the dc bus voltage may increase sharply during the braking stage. Thus, fast dynamic performance must be obtained in electrical drive application where the motor acceleration and braking occur frequently.

To obtain fast dynamic performance, the small-signal analysis is widely used [36]–[38]. The state-space averaging technique can be used to derive the small-signal model, and a closed two-loop controller is designed for CF-DAB to obtain good transient performance [39]. To improve the dynamic response and suppress the second harmonics further, feedforward control is used for unidirectional dc–dc converters employing PWM control [40]–[44]. In comparison, for bidirectional DAB dc–dc converters, the switches are not only PWM modulated but also phase shifted, its small-signal model is very complicated since there are more subintervals during one entire switching cycle. The output impedance expression of the DAB dc–dc is more complicated as well.

In this paper, parallel-connected high-frequency isolated CF bidirectional dc–dc converters supplied by a low-voltage battery are proposed for inverter-driven motor drive in order to handle the high charging/discharging battery current. A power sharing control strategy employing current loops is given. Based on the dual PWM plus double phase shifted (DPDPS) control with equal duty cycles, small-signal modeling for the converter is built. Factors contributing to the dynamic improvements are investigated. An optimized feedforward control with the optimal coefficient is presented. This paper is organized as follows. The proposed motor drive system overview and DPDPS control is given in Section II. Control strategy and small-signal modeling is described in Section III. The feedforward effect on the dynamic performance is given in Section IV. The leakage inductance effect on the steady-state and dynamic performance is given in Section V. In Section VI, experiments are made to verify the effectiveness of the control strategy. Section VII gives the conclusion.

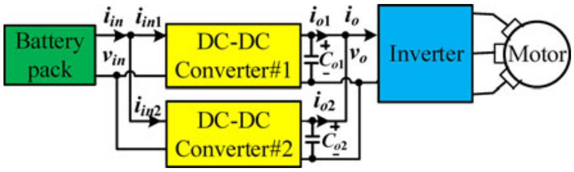

Fig. 1. Basic block diagram of the motor drive system.

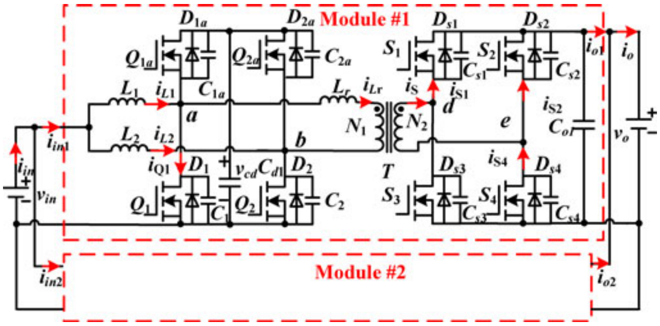

Fig. 2. Parallel connection of CF-DAB dc–dc converters.

II. Drive System Overview and DPDPS Control

The basic block diagram of the motor drive system is shown in Fig. 1. The system is composed of a battery pack, a dc–dc converter, a dc–ac inverter, and a motor. The dc–dc converter consists of two parallel-connected CF-DAB dc–dc modules. The LVS is connected to the battery pack whose voltage range is 18–28 V. The HVS is connected to the dc–ac inverter and its rated voltage is 300 V/dc.

The proposed topology is shown in Fig. 2. For the HVS, a full bridge is made of S_1–S_4. In the LVS, L_1 and L_2 are the dc inductors. Q_1 and Q_2 are bottom MOSFETs, whereas Q_{1a} and Q_{2a} are top switches. The equivalent leakage inductance L_r represents the sum of the external ac inductance and the primary-referred transformer leakage inductance.

To minimize the nonactive power and peak current, PWM control can be employed just like the LVS with the same duty cycle for the HVS. Thus, both v_{ab} and v_{de} have the same shape but they are phase shifted according to the transferred power. The steady-state waveforms in boost and buck modes of module #1 during one complete period can be seen in Fig. 3. With the

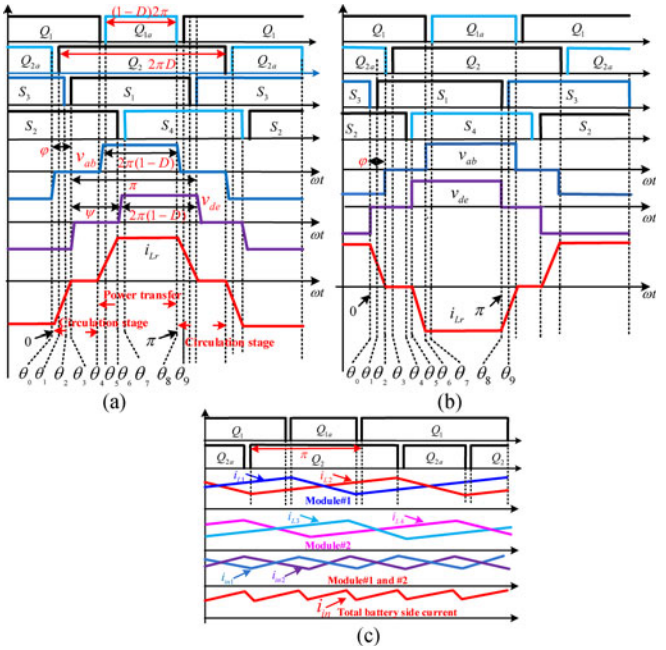

Fig. 3. Steady-state waveforms of DPDPS with identical duty cycles in boost and buck modes: (a) boost mode for module#1, (b) buck mode for module#1, and (c) battery side current reduction by interleaving technology.

interleaving PWM modulation not only for one module but also for two modules, the LVS current ripple can be minimized, which can be seen in Fig. 3(c). Fig. 3(a) illustrates the operating waveforms in the boost mode. The LVS top and bottom switches are gated with complementary PWM signals. The PWM duty cycles for LVS bottom switches Q_1 and Q_2 are equal, but their PWM gating signals are interleaved with each other. φ is defined as the phase shift angle between rising edges of Q_2 and S_1. The voltage v_{ab} is high frequency alternating voltage. The voltage v_{ab} leads v_{de}. During the circulation stage $[\theta_3,\ \theta_4]$, the leakage current drops to zero and stays at zero within the circulation stage range $[\theta_3,\ \theta_4]$ until the power transfer stage begins. Thus, during the circulation stage, the conduction loss can be reduced. ZVS can be ensured for the LVS switches in spite of the power flow direction [33]. For the HVS, the lagging leg S2 and S4 can achieve ZVS on, whereas the leading leg switches S1 and S3 can obtain ZCS on. In the buck mode, as shown in Fig. 3(b), for the HVS switches, the lagging leg switches S2 and S4 can achieve ZCS, whereas the leading leg switches S1 and S3 can obtain ZVS on. It is worth noting, during one complete cycle, there is no nonactive power by neglecting the effect of the magnetizing inductance. Fig. 3(c) plots the battery side current curves by using the interleaving technology not only for each module but also between the two modules. In this way, the battery side current ripple frequency is four times the switching frequency and the current ripple can be reduced significantly.

III. Current Sharing and Small-Signal Modeling

A. Implementation of the Current Sharing

The control block diagram for two modules in parallel connection is shown in Fig. 4. As can be seen in Fig. 4, the current sharing control scheme consists of one common output-voltage loop and two inner current loops. The sum of the voltage compensation loop output and the feedforward current provides the common reference for both the individual inner current loops. Therefore, current sharing between the two modules can be obtained. For individual modules, the control is composed of a phase shift control and a PWM control loop [24], [25], [33]. It should be noted that the high voltage current i_o is sensed for the feedforward control.

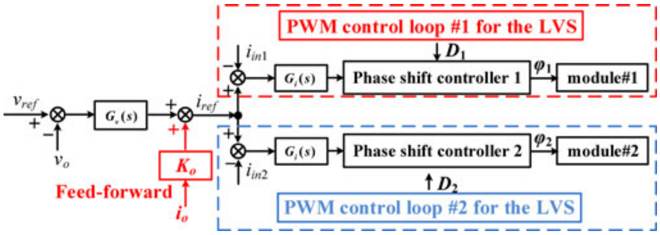

Fig. 4. Current sharing control for the two modules.

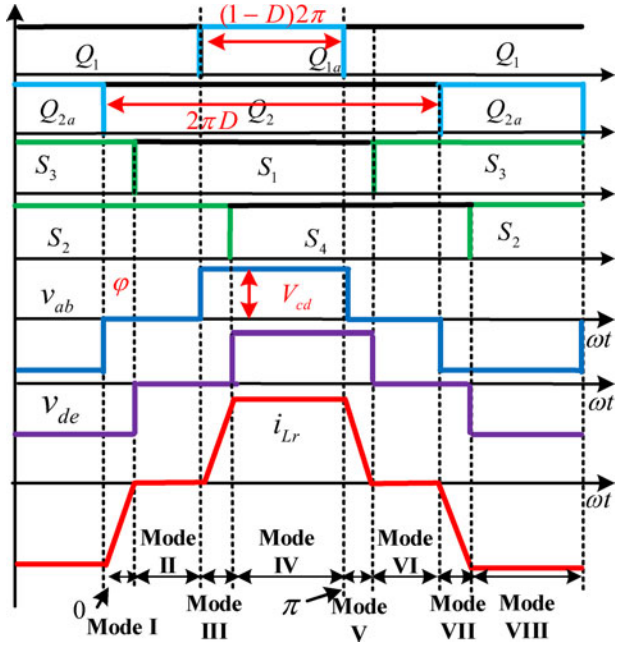

Fig. 5. Simplified waveforms in a switching cycle.

B. Small-Signal Modeling

To simplify the analysis, the dead time effect is ignored. There are eight operation modes in a switching cycle. Fig. 5 shows the simplified key waveforms of all the modes in a complete switching cycle for module #1.

As can be seen in Fig. 2, the values i_{L1}, i_{L2}, and v_{cd} are viewed as state variables; d is the duty cycle for bottom switches Q_1 and Q_2; φ is the phase shift angle; v_{in} is the LVS voltage; v_o is the HVS voltage; $\varphi = \Phi + \hat{\varphi}$; $d = D + \hat{d}$; the initial currents in L_r, L_1, and L_2 are I_s, I_{L1}, and I_{L2}, respectively. The turns ratio of the transformer is $N_1{:}N_2 = N$.

The small-signal model of each module can be derived as follows:

Mode I [0,φ]:	$\begin{cases} c_d \frac{dv_{cd}}{dt} = 0,\ L_1 \frac{di_{L1}}{dt} = v_{\text{in}},\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}} \\ i_{Lr} = \frac{\langle v_{cd} \rangle_{Ts}}{\omega L_r}(\theta - \varphi) \end{cases}$
Mode II [φ,(2d −1)π]:	$c_d \frac{dv_{cd}}{dt} = 0,\ L_1 \frac{di_{L1}}{dt} = v_{\text{in}},\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}},\ i_{Lr} = 0$
Mode III [(2d −1)π,(2d −1)π+φ]:	$\begin{cases} c_d \frac{dv_{cd}}{dt} = i_{L1} - i_{Lr}, & L_1 \frac{di_{L1}}{dt} = v_{\text{in}} - v_{cd} \\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}}, & i_{Lr} = \frac{\langle v_{cd} \rangle_{Ts}}{\omega L_r}[\theta - (2d-1)\pi] \end{cases},$
Mode IV [(2d−1)π+φ,π]:	$\begin{cases} c_d \frac{dv_{cd}}{dt} = i_{L1} - i_{Lr}, & L_1 \frac{di_{L1}}{dt} = v_{\text{in}} - v_{cd} \\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}}, & i_{Lr} = \frac{\langle v_{cd} \rangle_{Ts}}{\omega L_r}\varphi \end{cases}$
Mode V [π,π+φ]:	$\begin{cases} c_d \frac{dv_{cd}}{dt} = 0,\ L_1 \frac{di_{L1}}{dt} = v_{\text{in}},\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}}, \\ i_{Lr} = \frac{\langle v_{cd} \rangle_{Ts}}{\omega L_r}[\pi - \theta + \varphi] \end{cases}$
Mode VI [π+φ,2$d\pi$]:	$c_d \frac{dv_{cd}}{dt} = 0,\ L_1 \frac{di_{L1}}{dt} = v_{\text{in}},\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}},\ i_{Lr} = 0$
Mode VII [2$d\pi$,2$d\pi$+φ]:	$\begin{cases} c_d \frac{dv_{cd}}{dt} = i_{L2} + i_{Lr}, & L_1 \frac{di_{L1}}{dt} = v_{\text{in}}, \\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}} - v_{cd}, & i_{Lr} = -\frac{\langle v_{cd} \rangle_{Ts}}{\omega L_r}(\theta - 2d\pi) \end{cases}$
Mode VIII [2$d\pi$+φ,2π]:	$\begin{cases} c_d \frac{dv_{cd}}{dt} = i_{L2} + i_{Lr}, & L_1 \frac{di_{L1}}{dt} = v_{\text{in}}, \\ L_2 \frac{di_{L2}}{dt} = v_{\text{in}} - v_{cd}, & i_{Lr} = -\frac{\langle v_{cd} \rangle_{Ts}}{\omega L_r}\varphi \end{cases}$

where $< v_{cd} >_{Ts}$ denotes the average of v_{cd} over an interval of length T_{s}: $\langle v_{cd} \rangle_{Ts} = (\int_t^{t+T_s} v_{cd} d\tau)/T_s$.

Then, the average model can be derived as follows:

$$\begin{cases} c_d \frac{d\hat{v}_{cd}}{dt} = (1-D)\hat{i}_{L1} + (1-D)\hat{i}_{L2} - \frac{2V_{cd}}{\omega L_r}\left(1 - D - \frac{\Phi}{2\pi}\right)\hat{\varphi} \\ -\left(I_{L1} + I_{L2} - \frac{2V_{cd}\Phi}{\omega L_r}\right)\hat{d} - \frac{2\left[(1-D)\Phi - \frac{\Phi^2}{4\pi}\right]}{\omega L_r}\hat{v}_{cd} \\ L_1 \frac{d\hat{i}_{L1}}{dt} = \hat{v}_{\text{in}} - (1-D)\hat{v}_{cd} + V_{cd}\hat{d} \\ L_2 \frac{d\hat{i}_{L2}}{dt} = \hat{v}_{\text{in}} - (1-D)\hat{v}_{cd} + V_{cd}\hat{d} \end{cases} . \tag{1}$$

The transfer function of the phase angle perturbation $\hat{\varphi}$ to the two dc inductor current perturbations $\hat{i}_{L1}$ and $\hat{i}_{L2}$, respectively, can be expressed as follows:

$$G_{i_{L1}\varphi}(s) = \left.\frac{\hat{i}_{L1}(s)}{\hat{\varphi}(s)}\right|_{\substack{\hat{d}s=0 \\ v_{\text{in}}(s)=0 \\ \hat{v}_o(s)=0 \\ \hat{i}_{L2}(s)=0}} = \frac{2(1-D)\left(1 - D - \frac{\Phi}{2\pi}\right)V_{cd}}{\omega L_1 L_r C_d s^2 + 2\left[(1-D)\Phi - \frac{\Phi^2}{4\pi}\right]L_1 s + (1-D)^2 \omega L_r} \tag{2}$$

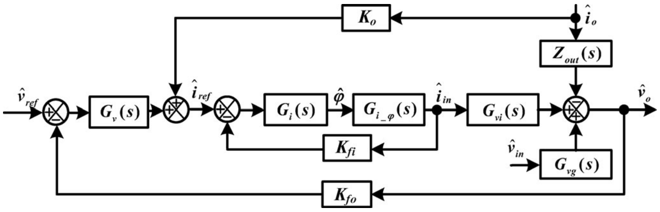

Fig. 6. Complete block diagrams on the small-signal model.

$$G_{i_{L2}\varphi}(s) = \left.\frac{\hat{i}_{L2}(s)}{\hat{\varphi}(s)}\right|_{\substack{\hat{d}s=0 \\ v_{\text{in}}(s)=0 \\ \hat{v}_o(s)=0 \\ \hat{i}_{L1}(s)=0}} = \frac{2(1-D)\left(1 - D - \frac{\Phi}{2\pi}\right)V_{cd}}{\omega L_2 L_r C_d s^2 + 2\left[(1-D)\Phi - \frac{\Phi^2}{4\pi}\right]L_2 s + (1-D)^2 \omega L_r}. \tag{3}$$

Supposing that $L_1 = L_2 = L, C_{d1} = C_d = C$, and $V_{cd} = NV_o$, the transfer function from $\hat{\varphi}$ to $\hat{i}_{\text{in}}$ (input current perturbation of module #1) can be written by

$$G_{i\_\varphi\#1}(s) = \frac{\hat{i}_{\text{in}1}(s)}{\hat{\varphi}_1(s)} = \frac{4(1-D)\left(1 - D - \frac{\Phi}{2\pi}\right)NV_o}{\omega L L_r C s^2 + 2\left[(1-D)\Phi - \frac{\Phi^2}{4\pi}\right]Ls + (1-D)^2 \omega L_r}. \tag{4}$$

According to the power conservation $v_o i_o = v_{\text{in}} i_{\text{in}}$, the perturbation of the output voltage is written by

$$\hat{v}_o = \frac{V_{\text{in}}\hat{i}_{\text{in}} + \hat{v}_{\text{in}} I_{\text{in}} - V_o \hat{i}_o}{I_o}. \tag{5}$$

The complete block diagram of the regulator system on the small-signal model of module #1 is shown in Fig. 6. K_o is the feedforward control coefficient. Therefore, the output voltage variations $\hat{v}_o$ can be expressed as a linear combination of three independent inputs: the input voltage variations $\hat{v}_{\text{in}}$, the input current variations $\hat{i}_{\text{in}}$, and the load current variations $\hat{i}_o$, where

$$G_v(s) = K_{p\_v} + \frac{K_{i\_v}}{s},\ G_i(s) = K_{p\_i} + \frac{K_{i\_i}}{s},$$
$$G_{vi}(s) = \frac{V_{\text{in}} Z_{\text{out}}}{V_o},\ G_{vg}(s) = \frac{I_{\text{in}} Z_{\text{out}}}{V_o}. \tag{6}$$

As can be seen in the control system block diagram shown in Fig. 6, when K_o is 0, the converter output impedance of the closed loop is written by

$$Z_{o1}(s) = \left.\frac{\hat{v}_o(s)}{-\hat{i}_o(s)}\right|_{\substack{\hat{v}_{\text{in}}=0 \\ \hat{v}_{ref}=0}} = \frac{Z_{\text{out}}(s)}{1 + T(s)},$$
$$T(s) = \frac{K_{fo} G_v(s) G_{vi}(s) G_i(s) G_{i\_\varphi}(s)}{1 + K_{fi} G_i(s) G_{i\_\varphi}(s)} ='' \text{loop gain}'' \tag{7}$$

where the loop gain *T*(*s*) is defined in general as the product of the gains around the forward and feedback paths of the loop. If K_o is not zero, the feedforward control works and the output impedance of the closed loop can be expressed as (8) as shown at the bottom of the next page.

C. Analysis of the Current Sharing

According to (4), for module #2, this transfer function can be expressed as

$$G_{i\_\varphi\#2}(s) = \frac{\hat{i}_{\mathrm{in}2}(s)}{\hat{\varphi}_2(s)} = \frac{4(1-D_s)\left(1-D_s-\frac{\Phi_s}{2\pi}\right)N_sV_o}{\omega L_s L_{r\,s} C_s s^2 + 2\left[(1-D_s)\Phi_s - \frac{{\Phi_s}^2}{4\pi}\right]L_s s + (1-D_s)^2\omega L_{r\,s}}. \tag{9}$$

And define the following

$$A_1 = \frac{a_1}{b_1s^2+c_1s+d_1} = G_{i\_\varphi\#1}(s),$$
$$A_2 = \frac{a_2}{b_2s^2+c_2s+d_2} = G_{i\_\varphi\#2}(s). \tag{10}$$

From the control loop shown in Fig. 6, the phase shift angle perturbations can be written as

$$\hat{\varphi}_1(s) = E_1\hat{v}_o + F_1\hat{i}_o + H_1\hat{i}_{\mathrm{in}1},\ \hat{\varphi}_2(s) = E_2\hat{v}_o + F_2\hat{i}_o + H_2\hat{i}_{\mathrm{in}2}$$
$$E_1 = E_2 = -K_{fo}G_vG_i,\ F_1 = F_2 = K_oG_i,$$
$$H_1 = H_2 = -K_{fi}\left(K_{p\_i} + \frac{K_{i\_i}}{s}\right) = \frac{ls+m}{s} \tag{11}$$

where

$$l = -K_{fi}K_{p\_i},\ m = -K_{fi}K_{i\_i}. \tag{12}$$

From (5) and (9)–(12), the transfer function from the total LVS current to the difference between the two LVS currents is written by

$$\frac{\hat{i}_{\mathrm{in}1}-\hat{i}_{\mathrm{in}2}}{\hat{i}_{\mathrm{in}}} = \frac{(A_1E_1-A_2E_2)V_{\mathrm{in}}/I_o + (A_1F_1-A_2F_2)V_{\mathrm{in}}/V_o}{(1-A_1H_1)(1-A_2H_2)}. \tag{13}$$

In combination with expressions of A_1, E_1, F_1, H_1, A_2, E_2, F_2, and H_2, the characteristic equation can be derived as

$$\begin{aligned}G(s) = {} & b_1b_2s^6 + (b_1c_2+b_2c_1)s^5 \\ & + (c_1c_2 + b_1d_2 - b_1a_2l + b_2d_1 - b_2a_1l)s^4 \\ & + (-a_1b_2m - a_2b_1m + c_2d_1 - a_1c_2l + c_1d_2 - a_2c_1l)s^3 \\ & + (-a_1c_2m - a_2c_1m + d_1d_2 - a_1d_2l - a_2d_1l + a_1a_2l^2)s^2 \\ & + (-a_1d_2m - a_2d_1m + 2a_1a_2lm)s + a_1a_2m^2.\end{aligned} \tag{14}$$

As can be seen in (14), the feedforward coefficient K_o does not exist in the characteristic equation. This implies that the system reliability is not affected by different feedforward coefficient K_o. As can be seen in (14), $b_1b_2 > 0$. For the system to be stable, the first of the Routh array must have the same sign. So, the proper selection of different compensator parameters can be done by (14).

D. System Stability Analysis

The system is stable when the load variation or source voltage variation is large. The root locus of a single CF dc–dc converter is given to show the stability. From the small-signal model block diagram illustrated in Fig. 6, the transfer function for one module can be derived as

$$\frac{\hat{v}_o(s)}{\hat{v}_{\mathrm{ref}}(s)} = \frac{G_{vi}(s)G_v(s)G_i(s)G_{i\_\varphi}(s)}{K_{fo}G_{vi}(s)G_v(s)G_i(s)G_{i\_\varphi}(s) + K_{fi}G_i(s)G_{i\_\varphi}(s) + 1}. \tag{15}$$

Then, the system characteristic equation can be obtained as

$$q_4s^4 + q_3s^3 + q_2s^2 + q_1s + q_0 = 0 \tag{16}$$

where

$$q_4 = \omega LL_rC_d$$
$$q_3 = 2L\left[(1-D)\Phi - \frac{\Phi^2}{4\pi}\right]$$
$$\begin{aligned}q_2 = {} & 4K_{fo}\frac{V_{\mathrm{in}}Z_{\mathrm{out}}}{V_o}K_{p\_v}K_{p\_i}(1-D)\left(1-D-\frac{\Phi}{2\pi}\right)NV_o \\ & + 4K_{fi}K_{p\_i}(1-D)\left(1-D-\frac{\Phi}{2\pi}\right)NV_o + (1-D)^2\omega L_r\end{aligned}$$
$$\begin{aligned}q_1 = {} & 4K_{fo}\frac{V_{\mathrm{in}}Z_{\mathrm{out}}}{V_o}(1-D)\left(1-D-\frac{\Phi}{2\pi}\right)NV_o \\ & \times (K_{p\_v}K_{i\_i} + K_{i\_v}K_{p\_i}) \\ & + 4K_{fi}K_{i\_i}(1-D)\left(1-D-\frac{\Phi}{2\pi}\right)NV_o\end{aligned}$$
$$q_0 = 4K_{fo}\frac{V_{\mathrm{in}}Z_{\mathrm{out}}}{V_o}(1-D)\left(1-D-\frac{\Phi}{2\pi}\right)NV_oK_{i\_v}K_{i\_i}.$$

Fig. 7 illustrates the root locus curves when the output power P_o changes at $v_{\mathrm{in}} = 18$ V based on (16) and the system specifications given in Table I. The 4 roots of the system characteristic equation are illustrated in Fig. 7(a). The 2 roots that closed to the imaginary axis are overlapped, and they are shown in detail in Fig. 7(b)–(d). As can be seen, when the output power changes from 100 W to 2 kW, all the system poles are in the left half-plane. That means the system is stable at different loads.

Fig. 8 illustrates the root locus curves when the output power P_o changes at $v_{\mathrm{in}} = 28$ V. As can be seen, all the system poles

---

$$\left.\begin{aligned}Z_{o2}(s) &= \left.\frac{\hat{v}_o(s)}{-\hat{i}_o(s)}\right|_{\substack{\hat{v}_{\mathrm{in}}=0\\ \hat{v}_{\mathrm{ref}}=0}} = \frac{Z_{\mathrm{out}}(s) - \frac{K_oT(s)}{K_{fo}G_v(s)}}{1+T(s)} = \frac{Z_{\mathrm{out}}(s)\,(1-M(s))}{1+T(s)} \\ M(s) &= \frac{K_oT(s)}{K_{fo}G_v(s)Z_{\mathrm{out}}(s)} = \frac{K_oG_i(s)G_{i\_\varphi}(s)}{(V_o/V_{\mathrm{in}})[1+K_{fi}G_i(s)G_{i\_\varphi}(s)]}\end{aligned}\right\}. \tag{8}$$

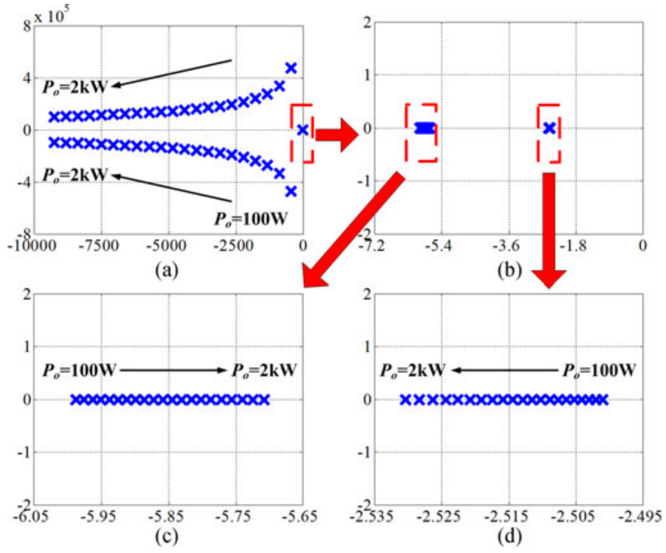

Fig. 7. Root locus when P_o changes at 18 V input.

TABLE I
CALCULATION SPECIFICATIONS

Rated Power P_o	4 kW	$L_1 = L_2 = L$	11 μH
HVS (v_o)	300 V	C_d, C_{o1}	30 μF/22 μF
LVS (v_{in})	18–28 V	$N_1 : N_2$	2:10
Switching *f*	50 kHz	L_r	1.0 μH

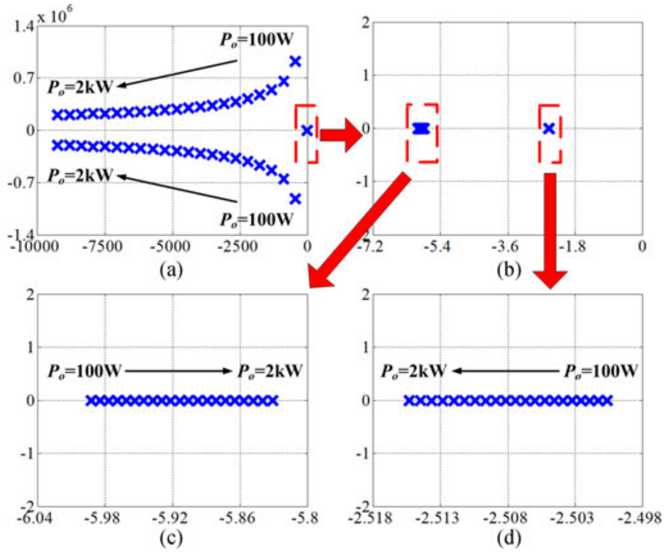

Fig. 8. Root locus when P_o changes at 28 V input.

are in the left half-plane, the system is stable at different loads at $v_{\text{in}} = 28$ V.

In conclusion, if the controller parameters are designed properly, the system is stable when v_{in} is in the range of 18–28 V and P_o is lower than the rated 4 kW output.

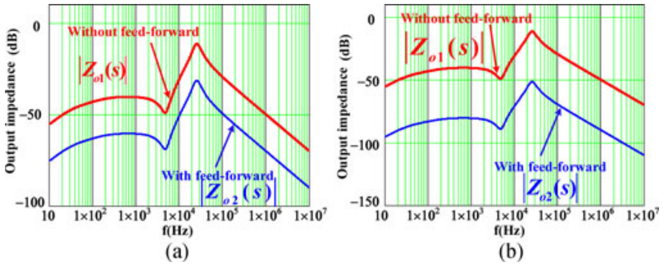

Fig. 9. Magnitude curves: (a) $1 - M(s) = 0.1$, and (b) $1 - M(s) = 0.01$.

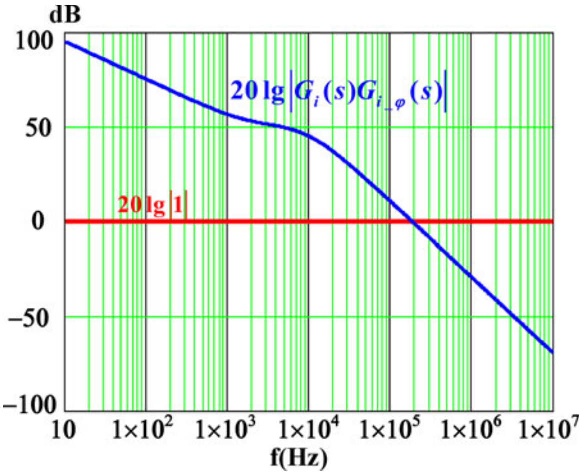

Fig. 10. Magnitude–frequency curve of 1 and $G_i(s)G_{i_\varphi(s)}$.

IV. FEEDFORWARD EFFECT ON THE DYNAMIC PERFORMANCE

A. *Design of the Feedforward Coefficient* K_o

According to (7) and (8), if $1-M(s)=0$, the output impedance is zero, so the feedforward coefficient K_o should be

$$K_o = \frac{K_{fo} G_v(s) Z_{\text{out}}(s)}{T(s)} = \frac{(V_o/V_{\text{in}})[1 + K_{fi} G_i(s) G_{i\_\varphi}(s)]}{G_i(s) G_{i\_\varphi}(s)}. \tag{17}$$

As can be seen in (17), the expression of feedforward coefficient K_o is rather complicated and hard to be implemented if the output impedance is controlled to be zero ideally.

Actually, to simplify the design, the value of $1-M(s)$ can be chosen to be a very tiny value. Fig. 9 illustrates the magnitude curves for the closed-loop output impedance without and with the feedforward using different coefficients. As can be seen in Fig. 9(a) and (b), when the feedforward is effective, the output impedance can be reduced dramatically. As illustrated, the output impedance drops as the value of $1-M(s)$ decreases.

According to (8), the magnitude curve of 1 and $G_i(s)G_{i_\varphi}$ (s) is shown in Fig. 10. As seen, when the frequency is in the low-frequency range, the value $G_i(s)G_{i\_\varphi}(s)| \gg |1|$. Because the load is the motor, the perturbation of the load current variations $\hat{i}_o$ mainly comes from the low-frequency range. So, the feedforward coefficient K_o can be optimized and selected approximately as

$$K_o \approx (V_o/V_{\text{in}}) K_{fi} = K_{\text{op}}. \tag{18}$$

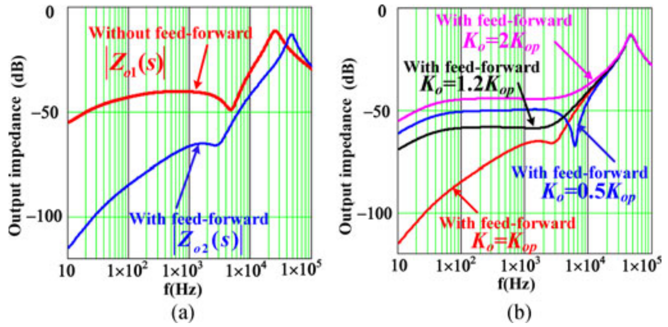

Fig. 11. Magnitude curves of output impedance Z_{o2}: (a) $M(s) = M_{\mathrm{op}(s)}$, and (b) with different K_o.

Substituting (18) into (8) yields

$$M(s) = \frac{K_o T(s)}{K_{fo} G_v(s) Z_{\mathrm{out}}(s)} \approx \frac{K_{fi} G_i(s) G_{i\_\varphi}(s)}{1 + K_{fi} G_i(s) G_{i\_\varphi}(s)} = M_{\mathrm{op}}(s). \tag{19}$$

B. Feedforward Effect on the Dynamic Performance

As can be seen in Fig. 11(a), if K_o has been selected as the optimized value K_{op}, it is easy to be implemented in practical application. When the feedforward control is effective, the output impedance can be reduced dramatically. As can be seen in Fig. 11(b), if the feedforward coefficient K_o is greater than or less than the optimal K_{op}, the output impedance is not the minimum in the low-frequency region. This shows that K_{op} is the optimal feedforward coefficient. It is well known that the output voltage is less sensitive to the load current variation as output impedance becomes smaller. So the feedforward loop can improve the dynamic performance.

C. Simulation Verification

Fig. 12 shows the simulation results of one module in facing load transients and braking using the power electronics simulation software (PSIM) with and without the feedforward control. As illustrated in Fig. 12(a), better dynamic response in facing step load change from 200 W to 3 kW can be obtained with the feedforward control. As can be seen in Fig. 12(b), with the feedforward control, the dc bus voltage spike can be suppressed compared to that without the feedforward control. Thus, the feedforward control can improve the system dynamic performance.

V. LEAKAGE INDUCTANCE EFFECT ON THE STEADY-STATE AND DYNAMIC PERFORMANCE

A. Leakage Inductance Value Optimal Design and Its Effect on the Steady-State Performance

If the leakage inductance value is designed to be very small, leakage inductance current may be very high especially during the startup procedure. Fig. 13 shows the leakage inductance current curve during the startup procedure since the output voltage is rather small initially. It should be noted that the worst case is that the duty cycle of the primary transformer voltage v_{ab} is 50%, whereas the output voltage is zero.

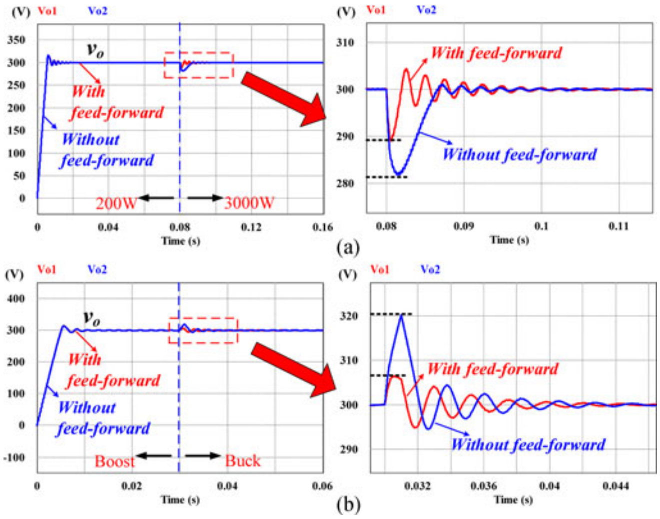

Fig. 12. Simulation results with feedforward and without feedforward: (a) load change from 200 W to 3 kW, and (b) braking.

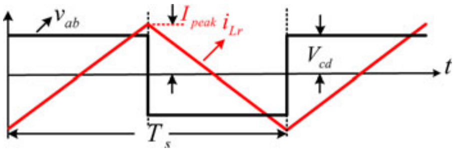

Fig. 13. Leakage inductance current during the startup.

As can be seen in Fig. 13, the voltage across the leakage inductance is that $L_r \cdot di/dt = V_{cd} = N_1 V_o / N_2 = 60$ V. The peak current can be expressed by

$$I_{\mathrm{peak}} = \frac{V_{cd}}{L_r} \times \frac{T_s}{2} \times \frac{1}{2} = \frac{V_{cd} T_s}{4 L_r}. \tag{20}$$

Since the LVS switch Q_1 is two IXFN360N15T2 in parallel connection, the rated current of the MOSFET is 310 A. Thus, the maximum peak current is designed to be the half of the rating current

$$I_{\mathrm{peak}} = \frac{V_{cd} T_s}{4 L_r} < 310A \Rightarrow L_r > 0.96\ \mu H. \tag{21}$$

Therefore, to suppress the rush current especially at the startup process, the leakage inductance value L_r is designed not less than 1.0 μH. But different leakage inductance values may cause different current stress. As can be seen in Fig. 3, the leakage inductance current i_{Lr} rms and peak values of one module can be written by

$$\begin{cases} I_{Lr\_\mathrm{rms}} = \sqrt{\dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} i_{Lr}(\theta)^2 d\theta} = \dfrac{V_{cd}\varphi}{\omega L_r}\sqrt{\dfrac{6\pi - 6D\pi - \varphi}{3\pi}} \\ I_{Lr\_\mathrm{peak}} = \dfrac{V_{cd}\varphi}{\omega L_r} \end{cases}. \tag{22}$$

Based on (22), the rms and peak values of current i_{Lr} versus the LVS voltage v_{in} in the boost mode are illustrated in Fig. 14.

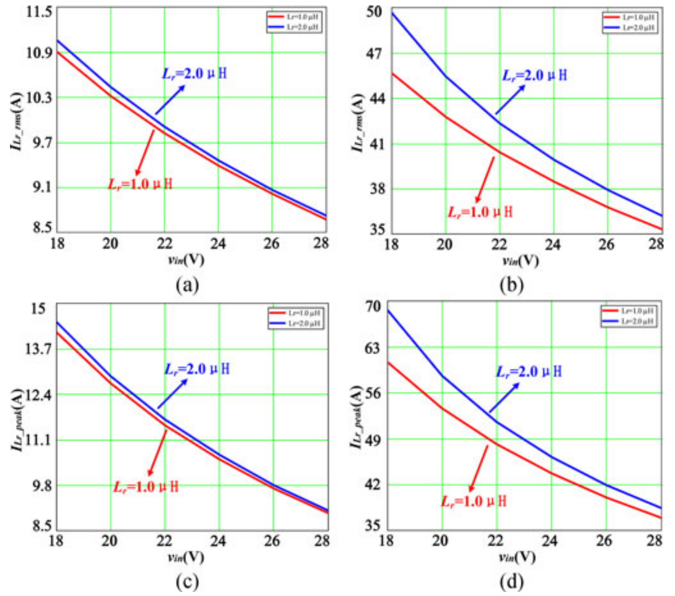

Fig. 14. Comparison of current i_{Lr} in boost mode: (a) rms value at 500 W output, (b) rms value at 2 kW output, (c) peak value at 500 W output, and (d) peak value at 2 kW output.

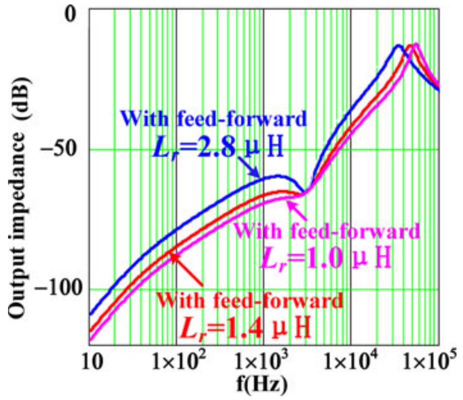

Fig. 15. Magnitude curves of output impedance Z_{o2} with different L_r.

As seen, when $L_r = 1.0$ μH, the rms and peak values of the leakage inductance current can be reduced significantly at the same load, LVS voltage, and HVS voltage.

B. Feedforward Effect on the Dynamic Performance

According to (8) and (19), Fig. 15 shows the comparison of magnitude curves of the closed-loop output impedance at different leakage inductances. As can be seen in Fig. 15, as the equivalent leakage inductance value decreases, the output impedance value drops as well. It is well known that the output voltage is less sensitive to the load current variation as output impedance becomes smaller. Thus, the smaller the leakage inductance is, the better the dynamic performance is.

Fig. 16 shows the simulation results of one module during the startup process, load transients, and braking stage using the PSIM with different leakage inductance values. In Fig. 16(a), better dynamic response in facing step load change from 200 W to 3 kW can be obtained when the leakage inductance value is smaller. As can be seen in Fig. 16(b), the dc bus voltage spike is lower during the braking stage with smaller leakage inductance value. Thus, the converter is preferred to operate with smaller leakage inductance to achieve better dynamic performance.

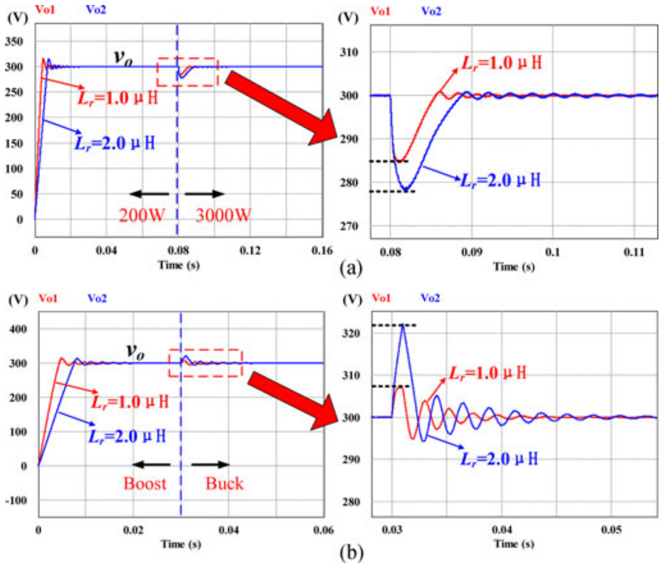

Fig. 16. Simulation results with $L_r = 1.0$ μH and $L_r = 2.0$ μH: (a) load change from 200 W to 3kW, and (b) braking.

Fig. 17 illustrates the circuit ac sweep results by PSIM simulation. As seen, the crossover frequency varies from 400 to 790 Hz as the leakage inductance value decreases from 2.0 to 1.0 μH. Thus, smaller leakage inductance leads to better dynamic performance.

VI. EXPERIMENTAL VERIFICATIONS

A. Prototype

A 4-kW experimental prototype has been built in order to verify the effectiveness of the converter with the proposed control. Fig. 18 shows the lab prototype picture.

B. Steady-State Operation

Fig. 19 shows the experimental results of module #1 at rated load (2 kW) in the boost mode with the minimum and maximum input voltages. As can be seen, with the proposed DPDPS control, the leakage inductance peak current is reduced, and the circulation loss can be minimized because the leakage inductance current remains as zero during the circulation stage.

Fig. 20 shows the experimental results of module #1 at rated load (2 kW) in buck mode with the minimum and maximum output voltages. As can be seen, with the proposed DPDPS control, the leakage inductance peak current is reduced, and the circulation loss can be minimized.

C. Soft Switching Waveforms

With the proposed control strategy, all the switches on the LVS can achieve ZVS turn-on. For the HVS, half of the switches can

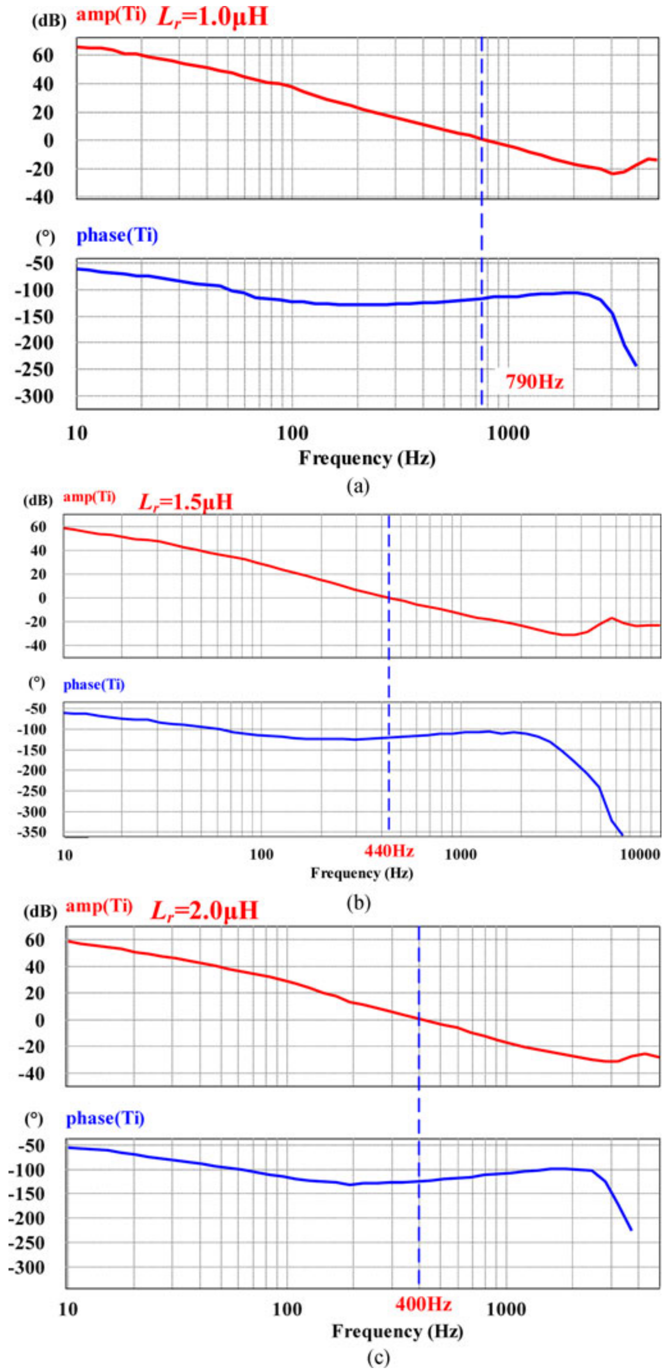

Fig. 17. Compensated voltage regulator loop gains using circuit ac sweep: (a) $L_r = 1.0\ \mu$H, (b) $L_r = 1.5\ \mu$H, and (c) $L_r = 2.0\ \mu$H.

be turned ON at ZVS, whereas the other switches can be turned on at ZCS. The experimental results shown in Fig. 21 have verified the theoretical analysis.

Fig. 21 shows the soft switching states for the switches at full load (2 kW) with 24 V input in the boost mode. As shown in Fig. 21(a) and (b), both Q_1 and Q_{1a} can be turned on with ZVS. As can be seen in Fig. 21(c) and (d), for the HVS switches, the leading leg switch S_1 can achieve ZCS turn-on, whereas the lagging switch S_2 can achieve ZVS turn-on. The soft-switching waveforms are similar in the buck mode.

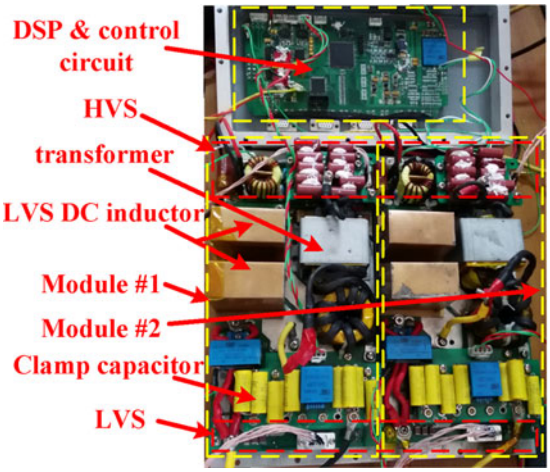

Fig. 18. Prototype picture.

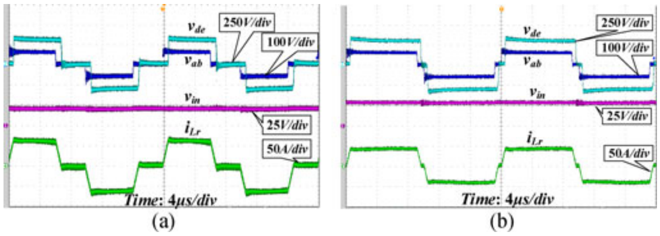

Fig. 19. Experimental results of module #1 with DPDPS control in boost mode at 2 kW output: (a) with $v_{\rm in} = 18$ V, and (b) with $v_{\rm in} = 28$ V.

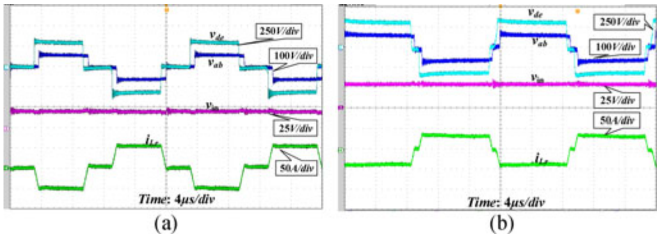

Fig. 20. Experimental results of module #1 with DPDPS control in buck mode at 2 kW output: (a) with $v_{\rm in} = 18$ V, and (b) with $v_{\rm in} = 28$ V.

D. Dynamic Performance With Inverter-Driven AC Motor

Fig. 22 shows the experimental results of motor drive, without and with feedforward, respectively. v_o is the HVS voltage of the dc–dc converter, i_o is the HVS total current. $i_{\rm in}$ is the LVS total current. As seen, during the braking period, the braking kinetic energy is converted into the electrical energy, making the HVS voltage increase. This makes the power flow from the HVS to LVS and charges the battery. As can be seen in Fig. 22(a) and (d), due to the feedforward control, the voltage drop is obviously reduced from 125 to 25 V and the dynamic performance is better and greatly improved. As can be seen in Fig. 22(b) and (c), when the feedforward coefficient K_o $(0.5K_{\rm op}$ or $1.2K_{\rm op})$ is greater than or less than the optimal value $K_{\rm op}$, the voltage drop is obviously reduced from 125 to 107 V and 100 V, respectively. The dynamic performance is not the best.

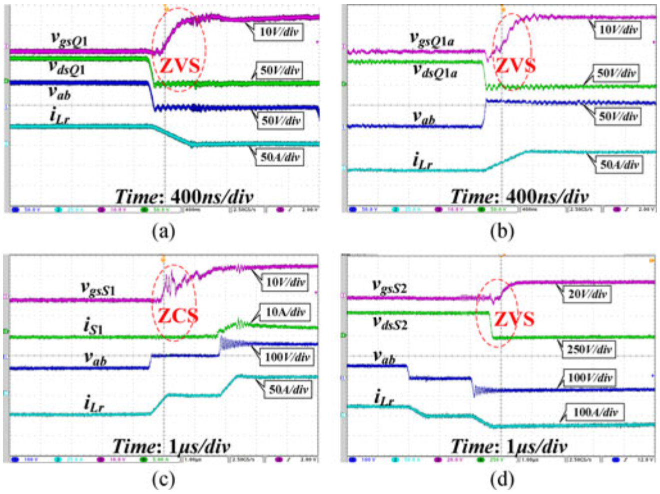

Fig. 21. Soft-switching waveforms of module #1 with DPDPS control in the boost mode at 24 V input and 2 kW output condition: (a) ZVS of Q_1, (b) ZVS $Q_{1\,\mathrm{a}}$, (c) ZVS of S_1, and (d) ZCS of S_2.

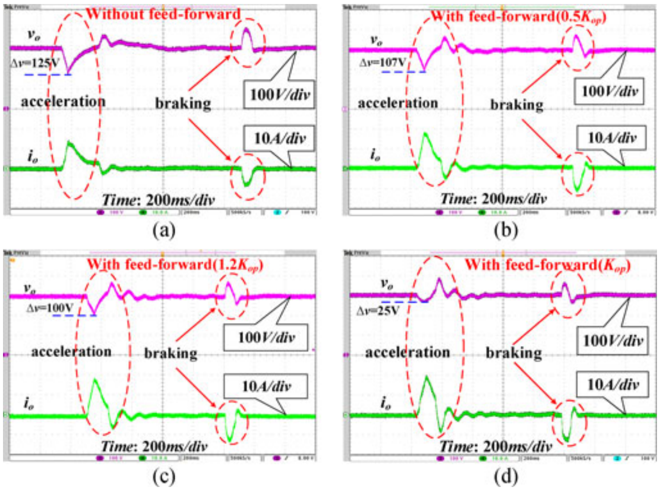

Fig. 22. Experimental results with motor drive: (a) without feedforward, (b) with feedforward coefficient 0.5 K_{op}, (c) with feedforward coefficient 1.2 K_{op}, and (d) with feedforward coefficient K_{op}.

E. Experimental Results of Current Sharing

As can be seen in Fig. 23(a), the output currents of the two modules are equal to each other during the acceleration and braking periods. It implies excellent power sharing can be achieved even in transients. As can be seen in Fig. 23(b), with the interleaving PWM modulation, the LVS current ripple can be minimized, increasing the battery lifetime.

F. Efficiency

The efficiency of the system at different loads and different source voltages is shown in Fig. 24. At rated load at 28 V input, the efficiency is over 95%. Since the conduction loss is larger at low battery voltage (18 V) than high battery voltage (28 V), the efficiency is higher at high source voltage (28 V) at heavy load.

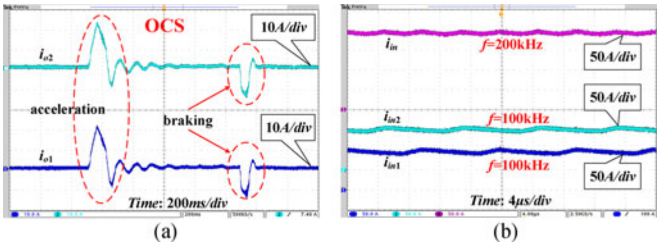

Fig. 23. Experimental results of current sharing: (a) OCS between two modules, and (b) ripple of input current.

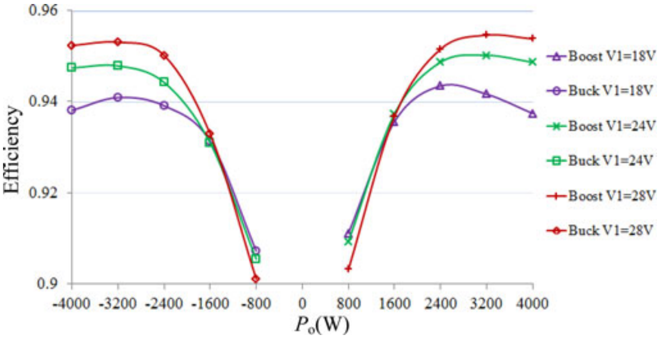

Fig. 24. Conversion efficiency.

VII. CONCLUSION

This paper proposes parallel-connected CF modular bidirectional dc–dc converters for electrical drive powered by low-voltage battery. Based on the small-signal modeling employing the DPDPS control, the feedforward control with the optimal coefficient can improve the system dynamic performance significantly. If the leakage inductance value can ensure the safe operation of the system, the smaller value can improve the system dynamic performance, reduce the rms and peak current. With the proposed current sharing strategy, excellent power sharing can be obtained not only under steady state, but also in transients including the motor acceleration and braking regeneration. The ripple for the charge/discharge current of the battery can be minimized significantly with the interleaving technology not only within each module, but also among all the constituent modules. The validity of the control strategy and converter has been verified by experimental results of a 4-kW prototype.

REFERENCES

[1] F. Crescimbini, A. Lidozzi, G. Lo Calzo, and L. Solero, "High-speed electric drive for exhaust gas energy recovery applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2998–3011, Jun. 2014.

[2] F. Lin, J. Hwang, P. Chou, and Y. Hung, "FPGA-based intelligent-complementary sliding-mode control for PMLSM servo-drive system," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2573–2587, Oct. 2010.

[3] H. Wu, K. Sun, L. Zhu, and Y. Xing, "An interleaved half-bridge three-port converter with enhanced power transfer capability using three-leg rectifier for renewable energy applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 04, no. 2, pp. 606–616, June. 2016.

[4] H. Wu, J. Zhang, X. Qin, T. Mu, and Y. Xing, "Secondary-side-regulated soft-switching full-bridge three-port converter based on bridgeless boost rectifier and bidirectional converter for multiple energy interface," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4847–4860, Jul. 2016.

[5] Y. Han *et al.*, "Non-isolated three-port DC/DC converter for +-380V DC microgrids," in *Proc. PCIM Eur. 2016/Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manag.*, Nuremberg, Germany, 2016, pp. 1–8.

[6] Y. Hu, X. Song, W. Cao, and B. Ji, "New SR drive with integrated charging capacity for plug-in hybrid electric vehicles (PHEVS)," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5722–5731, Oct. 2014.

[7] M. B. Camara, H. Gualous, F. Gustin, A. Berthon, and B. Dakyo, "DC/DC converter design for supercapacitor and battery power management in hybrid vehicle applications—Polynomial control strategy," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 587–597, Feb. 2010.

[8] M. Stojadinovic and J. Biela, "Comparison of high power non-isolated multilevel DC–DC converters for medium-voltage battery storage applications," in *Proc. 2015 17th Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1–10.

[9] O. C. Onar, J. Kobayashi, A. Khaligh, "A fully directional universal power electronic interface for EV, HEV, and PHEV applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 1228–1236, Dec. 2013.

[10] X. Sun, Y. Shen, W. Li, and H. Wu, "A PWM and PFM hybrid modulated three-port converter for a standalone PV/battery power system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 984–1000, Dec. 2015.

[11] S. S. Williamson, A. K. Rathore, and F. Musavi, "Industrial electronics for electric transportation: Current state-of-the-art and future challenges," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3021–3032, May 2015.

[12] T. Bhattacharya, V. S. Giri, K. Mathew, and L. Umanand, "Multiphase bidirectional flyback converter topology for hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 78–84, Jan. 2009.

[13] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC–DC converter based on dual-phase-shift control for DC distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

[14] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.

[15] D. Segaran, D. G. Holmes, and B. P. McGrath, "Enhanced load step response for a bidirectional DC–DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 371–379, Jan. 2013.

[16] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-time effect of the high-frequency isolated bidirectional full-bridge DC–DC converter: Comprehensive theoretical analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1667–1680, Apr. 2014.

[17] J. Kan, S. Xie, Y. Tang, and Y. Wu, "Voltage-fed dual active bridge bidirectional DC/DC converter with an immittance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3582–3590, Jul. 2014.

[18] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[19] H. Wu, K. Sun, L. Chen, L. Zhu, and Y. Xing, "High step-up/step-down soft-switching bidirectional DC–DC converter with coupled-inductor and voltage matching control for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2892–2903, May 2016.

[20] F. Peng, H. Li, G. Su, and J. Lawler, "A new ZVS bi-directional DC–DC converter for fuel cell and battery applications," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[21] Z. Wang and H. Li, "A soft switching three-phase current-fed bidirectional DC–DC converter with high efficiency over a wide input voltage range," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 669–684, Feb. 2012.

[22] J. Zhang, H. Wu, X. Qin, and Y. Xing, "PWM plus secondary-side phase-shift controlled soft-switching full-bridge three-port converter for renewable power systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7061–7072, Nov. 2015.

[23] X. Pan and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*,vol. 61, no. 5, pp. 2307–2315, May 2014.

[24] H. Xiao and S. Xie, "A ZVS bidirectional DC–DC converter with phase shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.

[25] D. Sha, Q. Lin, F. You, X. Wang, and G. Xu, "A ZVS bidirectional three-level DC–DC converter with direct current slew rate control of leakage inductance current," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2368–2377, May/Jun. 2016.

[26] X. Pan and A. K. Rathore, "Naturally clamped soft switching current-fed three-phase bidirectional DC/DC converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3316–3324, May 2015.

[27] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, design, and experimental results of wide range ZVS active-clamped L-L type current-fed DC/DC converter for fuel cells to utility interface," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 473–485, Jan. 2012.

[28] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized operation of current-fed dual active bridge DC–DC converter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, May 2015.

[29] W. Chen and X. Ruan, "Modularization structure for series-parallel connected converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 1531–1535.

[30] X. Pan and A. K. Rathore, "Novel interleaved bidirectional snubberless soft-switching current-fed full-bridge voltage doubler for fuel-cell vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5535–5546, Dec. 2013.

[31] J. Shi, L. Zhou, and X. He, "Common-duty-ratio control of input-parallel output-parallel (IPOP) connected DC–DC converter modules with automatic sharing of currents," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 1–10, Jul. 2012.

[32] J. Shi, T. Liu, J. Cheng, and X. He, "Automatic current sharing of an input-parallel output-parallel (IPOP)-connected DC–DC converter system with chain-connected rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2997–3016, Jun. 2015.

[33] J. Cheng, J. Shi, and X. He, "A novel input-parallel output-parallel connected dc-dc converter modules with automatic sharing of currents," in *Proc. IEEE Power Electron. Motion Control Conf.*, Jun. 2012, vol. 3, pp. 1871–1876.

[34] D. Sha, F. You, and X. Wang, "A high efficiency current fed semi dual active bridge DC–DC converter for low input voltage applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2155–2164, Apr. 2016.

[35] H. Wen, W. Xiao, and B. Su, "Nonactive power loss minimization in a bidirectional isolated DC–DC converter for distributed power systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6822–6831, Dec. 2014.

[36] H. Li and F. Peng, "Modeling of a new ZVS bi-directional DC–DC converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 17, no. 3, pp. 272–283, Jan. 2004.

[37] X. Zhang *et al.*, "Small-signal modeling and controller design of an isolated quasi-switched-capacitor DC/DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1032–1038.

[38] Y. Cho and J. Lai, "High-efficiency multiphase DC–DC converter for fuel-cell-powered truck auxiliary power unit," *IEEE Trans. Veh. Technol.*, vol. 62, no. 6, pp. 2421–2429, Jul. 2013.

[39] X. Pan and A. K. Rathore, "Small-signal analysis of naturally commutated current-fed dual active bridge converter and control implementation using cypress PSoC," *IEEE Trans. Veh. Technol.*, vol. 64, no. 11, pp. 4996–5005, Nov. 2015.

[40] G. Zhu, X. Ruan, L. Zhang, and X. Wang, "On the reduction of second harmonic current and improvement of dynamic response for two-stage single-phase inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1028–1041, Feb. 2015.

[41] L. Zhang, X. Ruan, and X. Ren, "Second-harmonic current reduction and dynamic performance improvement in the two-stage inverters: An output impedance perspective," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 394–404, Jan. 2015.

[42] C. Yao, X. Ruan, and X. Wang, "Automatic mode-shifting control strategy with input voltage feed-forward for full-bridge-boost dc–dc converter suitable for wide input voltage range," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1668–1682, Mar. 2015.

[43] Y. Yang, X. Ruan, L. Zhang, J. He, and Z. Ye, "Feed-forward scheme for an electrolytic capacitor-less AC/DC led driver to reduce output current ripple," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 394–404, Oct. 2014.

[44] C. Yao, X. Ruan, W. Cao, and P. Chen, "A two-mode control scheme with input voltage feed-forward for the two-switch buck-boost DC–DC converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2037–2048, Apr. 2014.

Deshang Sha (M'09) was born in 1977. He received the B.S. degree from the Luoyang Institute of Technology, Luoyang, China, in 1998, the M.S. degree from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2001, and the Ph.D. degree from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2005, all in electrical engineering.

From 2005 to 2007, he was the Chief Engineer of the Full-Digitalized Welding Power Research Department, Time Group Inc., Beijing, China. Since 2008, he has been with the School of Automation, Beijing Institute of Technology, Beijing, China, where he is currently an Associate Professor. From 2012 to 2013, he was a Visiting Scholar with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His current research interests include the modeling and control of power converters, high-efficiency power conversion, and power electronics applications in renewable energy power generation.

Jiankun Zhang was born in 1992. He received the B.S. degree in electrical engineering in 2014 from Beijing Institute of Technology (BIT), Beijing, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interest includes dc/dc converters and dc/ac inverters.

Xiao Wang (S'16) was born in Beijing, China, in 1993. He received the B.S. degree in electrical engineering in July 2015 from Beijing Institute of Technology, Beijing, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interest includes dc/dc power conversion and solid-state transformer.

Wenqi Yuan was born in Hubei, China, in 1992. He received the B.S. and M.S. degrees in electrical engineering from Beijing Institute of Technology, Beijing, China, in 2014 and 2016, respectively.

He is currently an Engineer in the United Automotive Electronic Systems Co., Ltd., Shanghai, China. His research interests include dc/dc converters and magnetic design.