Digital Implementation of Soft Start-Up and Short-Circuit Protection for High-Frequency *LLC* Converters With Optimal Trajectory Control (OTC)

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***Abstract*—Achieving soft start-up and short-circuit protection have always been challenging for resonant converters due to severe stresses in the resonant tank. Optimal trajectory control (OTC) has been proven to be the most effective control method to optimize energy delivery with given stresses. This paper proposes a method to implement soft start-up and short-circuit protection for *LLC* converters by using low-cost microcontrollers (MCUs) with minimum stresses and optimal energy delivery. Our current understanding of the relationship between the switching frequency and the output voltage is based on the state-plane analysis, and the requirement for the controllers is significantly reduced when using the lookup table. Further improvement enables the application of the proposed control method to high-frequency *LLC* converters without increasing the cost for the controllers. This paper proposes a method to protect the *LLC* converter from abrupt short-circuit with low-cost MCUs, which improves transient response to short-circuit significantly, and investigates limitations when operating the high-frequency *LLC* converter under short-circuit conditions. The proposed methods minimize the CPU resource requirement and can be further integrated with other state-trajectory control functions within one MCU. Experimental results are demonstrated on a 500-kHz 1-kW 400-V/12-V *LLC* converter with 60-MHz MCU TMS320F28027.**

***Index Terms*—Digital control, *LLC* resonant converter, optimal trajectory control (OTC), short-circuit protection, soft start-up.**

I. Introduction

THE *LLC* resonant converter has been widely used as a dc–dc converter due to its high efficiency and hold-up capability [1], [2]. With the property of zero-voltage-switching (ZVS) for the primary switches and zero-current-switching for the secondary synchronous rectifiers (SRs), using *LLC* converters can also reduce electromagnetic interference [3]. However, the control characteristics of the resonant converter are complex due to the dynamics of the resonant tank, especially under start-up and short-circuit conditions. The start-up performance of commercial analog controllers are investigated in [4], and large stresses are found with commercial analog controllers due to the conflict between the linear property of the analog controllers and the nonlinear performance of the resonant converters. To describe and analyze the nonlinear behavior of the resonant tank, first state-trajectory analysis and control are employed for the series resonant converter [5], [6], [7]. Further efforts have been made to apply the state-trajectory analysis and control to solving the challenges in the control of the *LLC* converters, and theories on how to achieve optimal performance have been derived, including soft start-up [4], unpredictable dynamics [8], and burst mode for light-load efficiency [9].

Digital controllers are gradually taking the place of the analog controllers in power management [10], since digital controllers have advantages that make them superior to analog controllers; such as configurability, nonlinear control capability, and the ability to communicate with the ambient. Among the digital controllers, low-cost microcontrollers (MCUs) are preferred in industrial applications and have become mainstays in the front-end converters used for server and datacenter applications [10], [11], [12]. High-frequency *LLC* converters have become more popular in recent years due to their high power density and integrated magnetics, which reduce the total cost [13], [14]. With the fast development of wideband gap devices and novel magnetic materials, the trend of raising the switching frequency f_S will continue. *LLC* converters capable of MHz-level operation with GaN devices have been designed for different applications [15], [16], [17], and these demonstrate significantly improved power density. However, when applying low-cost MCUs to control the high-frequency *LLC* converter, the impact of digital delay will become significant. Severe stresses during transient may happen and the requirement for controller resources may increase a lot. It is of great importance to tackle the challenges in the control of the high-frequency *LLC* converters with low-cost MCUs.

Many efforts have been made to control the start-up and short-circuit protection of the *LLC* converters. Different overcurrent protection methods are discussed in [18]; frequency control is simple but it is very difficult to determine the frequency for different designs; pulse width modulation (PWM) control will lose the benefit of ZVS for the primary switches; adding clamping diodes requires additional components and may have limited effect, depending on the parameters of the power stage. An additional clamping circuit was used in [19], and its effect is similar to adding the clamping diodes. Using multielement resonant converters can effectively limit the f_S for given stresses

Manuscript received July 3, 2016; revised September 22, 2016; accepted November 14, 2016. Date of publication November 22, 2016; date of current version May 9, 2017. Recommended for publication by Associate Editor L. Corradini.

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Digital Object Identifier 10.1109/TPEL.2016.2631467

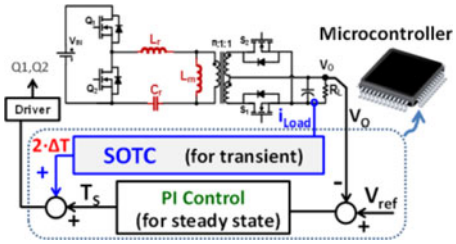

Fig. 1. Microcontroller (MCU)-based SOTC for *LLC* converters.

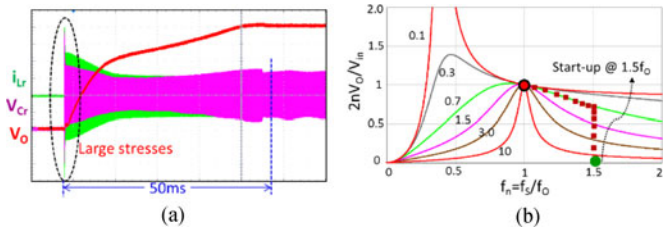

Fig. 2. Start-up of a commercial controller with an initial f_S of $1.5{\cdot}f_O$. (a) Experimental waveforms. (b) f_S trajectory on the gain curve.

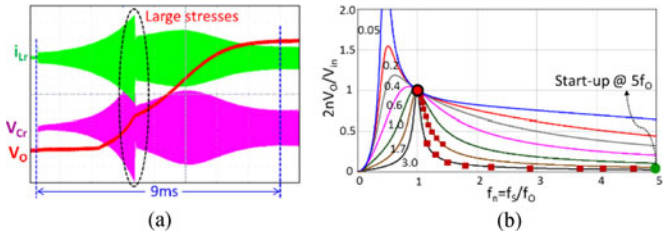

Fig. 3. Start-up of a commercial controller with an initial f_S of $5{\cdot}f_O$. (a) Experimental waveforms. (b) f_S trajectory on the gain curve.

during start-up and short-circuit [20], [21], but it requires additional resonant elements. Phase-shift modulation is used in [22]; however, it requires the primary side to be a full-bridge configuration and has a limited ZVS range when the output voltage V_O is low. The start-up process is analyzed and the parameters are optimized for analog controllers in [23] using state-plane analysis. Digital controllers are employed in the control of *LLC* converters in some applications, most of which focus on converters with f_S of around 100 kHz [4], [8], [24], [25]. Only a few papers [9], [26] have been able to demonstrate the control of high-frequency *LLC* converters, but they require very high-performance digital controllers. Fei *et al*. [27] first proposed to implement all the state-trajectory control functions in one low-cost MCU for a 130-kHz *LLC* converter based on the concept of simplified optimal trajectory control (SOTC), as shown in Fig. 1. Further efforts have been made to investigate the impact of digital delay on the implementation of state-trajectory control functions, and several methods have been proposed to minimize the controller resource utilization so that these control functions can be achieved for high-frequency *LLC* converters with low-cost MCUs, including soft start-up [28], fast transient response [29], burst mode for light-load efficiency [30], and adaptive SR driving [31].

It is worthwhile to investigate digital delay impact on the control performance for high-frequency *LLC* converters and figure out methods to minimize the delay impact. Specifically, in this paper, the frequency limitation for OTC to soft start-up and transient response to short-circuit under the impact of digital delay are investigated. Methods are proposed to minimize digital delay impact on soft start-up and improve the transient response to short-circuit significantly. Furthermore, the proposed methods can minimize the controller resource utilization for soft start-up and short-circuit protection, which potentially enables integration of all state-trajectory control functions within one MCU.

Section II of this paper investigates OTC for soft start-up and the impact of digital delay in MCU implementation. Section III proposes a method to reduce digital delay in the MCU implementation for soft start-up. Section IV investigates how to apply the proposed method to high-frequency *LLC* converters. Section V proposes a short-circuit protection method for *LLC* converters and investigates the limitations of the high-frequency *LLC* converters when operating under short-circuit conditions. Section VI presents the experimental results of using a 500-kHz *LLC* converter with a 60-MHz MCU TMS320F28027. A summary is given in Section VII.

II. Optimal Trajectory Control (OTC) for Soft Start-Up

Start-up is the most critical process in the control of the *LLC* converters. There can be very large resonant current i_{Lr} and resonant voltage V_{Cr} stresses during start-up if the process is not well controlled. To limit these stresses, f_S during start-up must be increased to be above the resonant frequency f_O during start-up. The control strategy of most controllers is as follows: the controllers set an initial f_S for start-up, then decreases f_S linearly or exponentially; if i_{Lr} exceeds the limit, the controllers increase f_S abruptly and, then, decrease f_S gradually again.

If the initial f_S for start-up is not high enough, there will be very large stresses. Fig. 2 shows the start-up of a commercial controller with an initial f_S of $1.5{\cdot}f_O$ [32]. The controller keeps the f_S of $1.5{\cdot}f_O$ for some time, and then, gradually decreases f_S to f_O. In this example, the maximum i_{Lr} stress is four times as large as the full-load steady-state stress, and the maximum resonant voltage V_{Cr} stress is twice as large as the full-load steady-state stress.

Even when the initial f_S is high enough, it is still very difficult to avoid large stresses during the start-up process. Fig. 3 shows the start-up of a commercial controller with an initial f_S of $5{\cdot}f_O$ [33]. Since the initial f_S is very high, i_{Lr} and V_{Cr} stresses are small. However, during the start-up process, the controller decreases f_S too fast, and large stresses still occur, which trigger the overcurrent protection. The controller then abruptly increases f_S to limit the stresses. It takes a long time to start-up and there are still large stresses during start-up.

OTC for soft start-up is first proposed in [4]. The whole start-up process is divided into three stages, as illustrated in Fig. 4. Stage 1 sets an asymmetrical current-limiting band, $+I_{\max N}$ and $-I_{LmN}$ (the suffix N means normalized), to settle V_{Cr} to half of input voltage V_{in} (for half-bridge primary configuration).

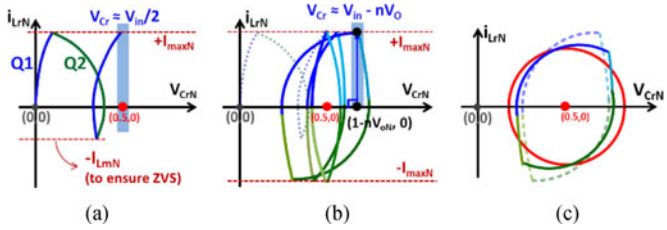

Fig. 4. OTC for soft start-up. (a) Stage 1. (b) Stage 2. (c) Stage 3.

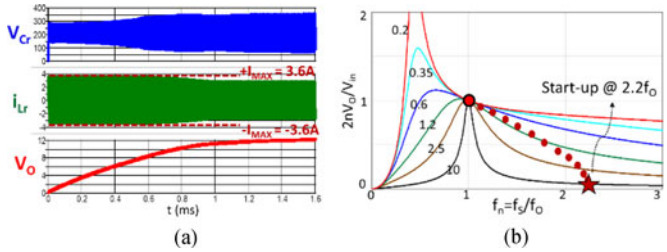

Fig. 5. Simulation of OTC for soft start-up. (a) Simulation waveforms. (b) f_S trajectory on the gain curve.

Stage 2 sets a symmetrical current-limiting band, $+I_{\max N}$ and $-I_{\max N}$, to optimize the energy delivery. Stage 3 decreases f_S gradually until V_O reaches steady state, which is 12 V in this case.

OTC for soft start-up is based on the graphical state-trajectory analysis of the resonant tank. Hence, it can minimize the resonant tank stresses and optimize the energy delivery, thus ensuring a safe start-up process in a very fast manner. Fig. 5 shows the simulation result of OTC for soft start-up. The parameters for the *LLC* converter are: resonant inductor $Lr = 55\,\mu$H, resonant capacitor $Cr = 24$ nF, and magnetizing inductor $Lm = 280\,\mu$H. The simulation result shows that i_{Lr} stress during the whole start-up process is only a little bit larger than that of the full-load steady state. The f_S trajectory of start-up on the gain curve is very smooth. It is obvious that OTC for soft start-up is advantageous over other control methods.

Since OTC for soft start-up has advantages over other control methods and low-cost MCUs are the preferred controllers in industrial applications, it is worthwhile to implement OTC for soft start-up using low-cost MCUs. However, there are still technical challenges if an MCU is employed directly to implement OTC for soft start-up due to the large stresses caused by the digital delay. To better illustrate the impact of the digital delay, a 60-MHz MCU TMS320F28027 is selected as an example for the following analysis, which is a popular low-cost MCU and widely used in telecom and server power supplies [11], [12].

All the required state variables are sensed through the analog-to-digital converter (ADC) and processed by the CPU, as shown in Fig. 6(a). If the MCU senses i_{Lr} and compares it with $I_{\max N}$, there would be a digital delay of at least 0.8 μs. The impact of this 0.8 μs digital delay will cause very large i_{Lr} stress in Stage 1, as shown in the shaded areas of Fig. 1 Microcontroller (MCU)-based SOTC for *LLC* converters.

Fig. 6(b), where the dashed line represents the desired trajectory and the solid line represents the actual trajectory with digital delay. Since the initial f_S for start-up should be very high, even

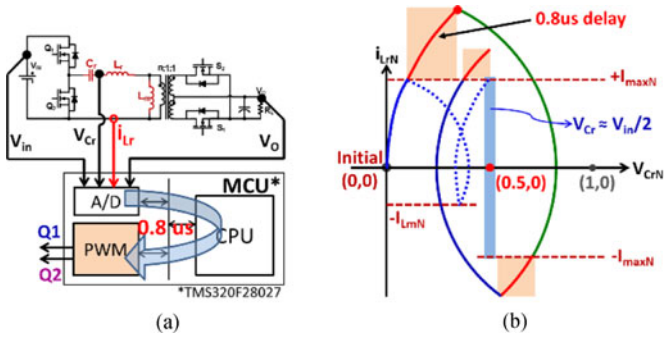

Fig. 6. Implementing OTC for soft start-up by MCU directly. (a) System scheme. (b) Trajectory of Stage 1 with digital delay.

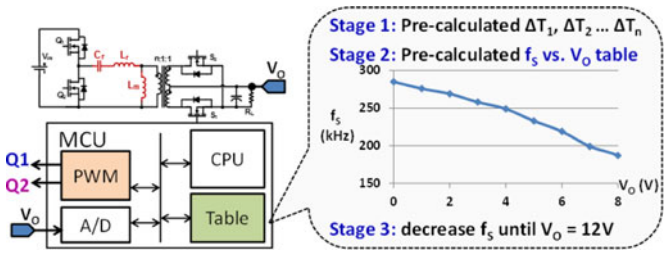

Fig. 7. Digital implementation with lookup tables for 130-kHz *LLC* converter.

a very small digital delay will cause a large i_{Lr} stress. Specifically, the 0.8 μs digital delay will cause twice as large as the full-load current stress for a 130-kHz *LLC* converter and more than three times the full-load current stress for a 500-kHz *LLC* converter.

It is clear that further effort need to be spent on reducing the impact of digital delay so that soft start-up, as well as short-circuit protection, can be implemented with the low-cost MCUs. The following sections present analysis and propose methods to solve these challenges.

III. Proposed Method to Implement OTC for Soft Start-up Based on Output Voltage

To solve the challenges caused by digital delay in ADC and calculation, MCU-based implementation with lookup tables is proposed, as shown in Fig. 7, which only requires sensing V_O. The table in Fig. 7 is based on the parameters of a 130-kHz 300-W *LLC* converter. The start-up process is as follows: when V_{in} reaches around 400 V, the MCU will begin the soft start-up process; in Stage 1, the MCU generates the precalculated ΔT_1, ΔT_2 ... ΔT_n consequently; in Stage 2, the MCU senses V_O and controls f_S based on the precalculated f_S versus V_O table; then in Stage 3, the MCU decreases f_S gradually until $V_O = 12$ V, which is the same as OTC for soft start-up. Detailed derivation for the tables appears below.

In Stage 1, V_O is considered to be approximately 0 V because the output capacitor is very large and there are only a few switching pulses in Stage 1. The initial condition is: $V_{Cr} = 0$ and $i_{Lr} = 0$ because there is no energy in the resonant tank before start-up. The trajectories to calculate ΔT_1 and ΔT_2 are shown in Fig. 8. And ΔT_1 and ΔT_2 are calculated using (1), (2), (3), (4),

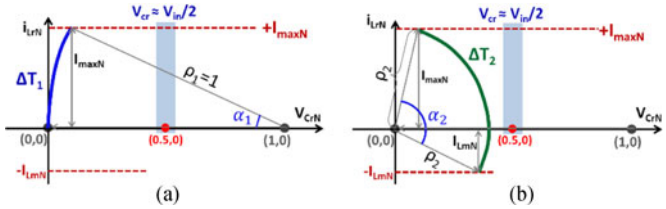

Fig. 8. Trajectories to calculate ΔT_1 and ΔT_2. (a) ΔT_1. (b) ΔT_2.

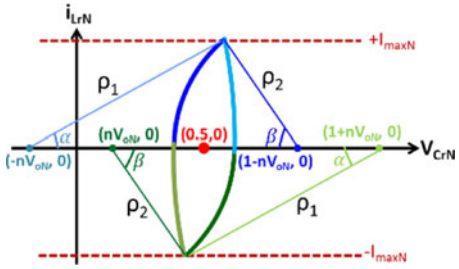

Fig. 9. f_S versus V_O table calculation for given V_O.

where $\omega_o = 1/\sqrt{L_r \cdot C_r}$. The values for ΔT_1, ΔT_2 ... ΔT_n are calculated step by step until it comes to the step at which V_{Cr} comes into the region around $V_{\rm in}/2$, which is the last switching action in Stage 1

$$\alpha_1 = \sin^{-1}\left(I_{\max N}/\rho_1\right) \tag{1}$$

$$\Delta T_1 = \alpha_1/\omega_o \tag{2}$$

$$\alpha_2 = \sin^{-1}\left(I_{\max N}/\rho_2\right) + \sin^{-1}\left(I_{{\rm Lm}N}/\rho_2\right) \tag{3}$$

$$\Delta T_2 = \alpha_2/\omega_o. \tag{4}$$

In Stage 2, f_S can be determined based on the precalculated f_S versus V_O table. This is because for a given $V_{\rm in}$ and V_O, f_S can be determined based on the i_{Lr} stress requirements when operating at above f_O. During start-up, $V_{\rm in}$ and V_O can be considered to be constant within several switching cycles because there is a large input capacitor for the hold-up time and a large output capacitor for the load transient. Under these conditions, the corresponding f_S can be obtained for different values of V_O to guarantee i_{Lr} is within $I_{\max}$ under the nominal input voltage $V_{\rm in\_nom}$ based on the corresponding trajectory shown in Fig. 9. The switching period is then calculated as (5), (6) to derive the f_S versus V_O table for Stage 2, which then linearized piece-wise and stored in the MCU

$$\alpha = \sin^{-1}\left(I_{\max N}/\rho_1\right);\ \beta = \sin^{-1}\left(I_{\max N}/\rho_2\right) \tag{5}$$

$$T_s = 2\left(\alpha+\beta\right)/\omega_o. \tag{6}$$

Stage 3 for this method is the same as that of the OTC for soft start-up, just decreasing f_S gradually until $V_O = 12$ V and then merging with closed-loop control.

In this method, the ΔT table and the f_S versus V_O table are calculated based on $V_{\rm in\_nom}$ and given *Lr* and *Cr* values, because different tables based on $V_{\rm in}$ will increase the memory requirement, and online measurement of *Lr* and *Cr* is not practical. Thus, the impact of variation of $V_{\rm in}$ and the tolerance of *Lr* and *Cr* need to be considered under such conditions. The impact of variation of $V_{\rm in}$ is analyzed as follows: $I_{\max}$ is determined using $V_{\rm in\_nom}$, the tables are calculated based on $I_{\max N}$ as expressed by (7). The same tables are applied under different $V_{\rm in}$ conditions, then the relationship between current stress $I_{\rm stress}$ and $V_{\rm in}$ is expressed as (8), which shows clearly that $I_{\rm stress}$ is proportional to $V_{\rm in}$. Since $V_{\rm in}$ is normally within a certain range ($\pm 5\%$), the variation of $I_{\rm stress}$ is also very small

$$I_{\max N} = \frac{I_{\max}}{V_{\rm in\_nom}/\sqrt{L_r/C_r}} \tag{7}$$

$$I_{\rm Stress}\left(V_{\rm in}\right) = I_{\max N} \cdot \frac{V_{\rm in}}{\sqrt{L_r/C_r}}. \tag{8}$$

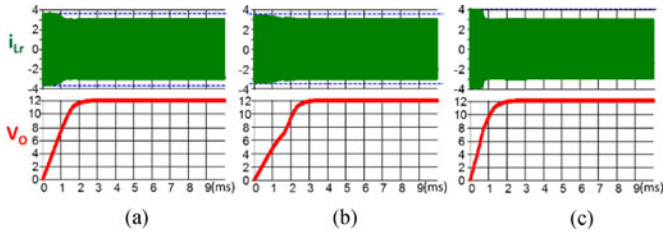

Fig. 10. Simulation of proposed method for soft start-up with *Lr*, *Cr* tolerance for 130 kHz *LLC*. (a) No tolerance. (b) +5% tolerance. (c) –5% tolerance.

The impact of the tolerance of *Lr* and *Cr* is estimated by simulation, as shown in Fig. 10. The start-up conditions are $V_{\rm in} = 390$ V and *load* = 25 A (full-load). The table is calculated based on $Lr = 60\,\mu$H and $Cr = 24$ nF. Fig. 10(a) shows the case without tolerance, and $I_{\rm stress} = 3.60$ A, compared to the full-load steady-state current stress of around 3 A. Fig. 10(b) shows the case with +5% tolerance for both *Lr* and *Cr*, and the $I_{\rm stress} = 3.40$ A, which is around 6% less than the nominal case. Fig. 10(c) is the case with –5% tolerance for both *Lr* and *Cr*, and the $I_{\rm stress} = 3.91$ A, which is around 9% higher than the nominal case. So the impact of the tolerance of *Lr* and *Cr* is small, because $\pm 5\%$ tolerance will result in less than 9% current stress variation.

This method is applicable to different load conditions because even under different loads, the output can still be considered as a constant voltage source within several switching cycles. The load conditions have an impact on the duration of the whole start-up process, but will not have an impact on i_{Lr} stress. While the table is derived for given power stage parameters and $V_{\rm in}$, it is still suitable for a given $V_{\rm in}$ range and is sufficiently robust for the tolerance of the resonant tank. It is worth noting that the parasitic has little impact on the proposed start-up using the f_S versus V_O table due to the following reasons: for *LLC* converters, parasitic may have large impact on the input/output gain at very light load conditions, but it has a very little effect on the input/output gain at the heavy load conditions [34], [35]; the proposed start-up controls the *LLC* converter with a current limiting band slightly larger than the full-load current stress, which means that during the whole start-up process, the converter's operation is always

TABLE I
SWITCHING INSTANTS FOR STAGE 1

Time interval	130-kHz *LLC* converter	500-kHz *LLC* converter
ΔT_1	808 ns	210 ns
ΔT_2	2096 ns	544 ns
$\Delta T_1 + \Delta T_2\ (f_S)$	2904 ns (344 kHz)	754 ns (1.33 MHz)
ΔT_3	1163 ns	302 ns
ΔT_4	1646 ns	428 ns
$\Delta T_3 + \Delta T_4\ (f_S)$	2809 ns (356 kHz)	730 ns (1.37 MHz)

equivalent to heavy load conditions; so the small error caused by the parasitic will only have very little impact on i_{Lr} majorly determined by the f_S versus V_O table during the start-up process. It is recommended to leave $+20\%$ margin for $I_{\max}$, so that the impact of parasitic and tolerance for start-up can be compensated to guarantee the converter can start-up under any conditions.

IV. SOFT START-UP FOR HIGH-FREQUENCY *LLC* CONVERTERS

The state-trajectory control is basically a cycle-by-cycle control, which means that the control cycle should be based on the switching cycle of the power stage, so that the controller can record the status of the resonant tank and integrate other state-trajectory control functions [28], [29], [30], [31]. In the proposed implementation with lookup tables, the switching times are controlled by the CPU of the MCU. Hence, there is a limitation in f_S with a given performance of the CPU if the control cycle is set to be equal to the switching cycle. The 60-MHz MCU TMS320F28027 selected in this paper is normally used to control the *LLC* converter with an f_O of around 70–130 kHz. The analysis below investigates how to use this MCU for the *LLC* converter with an f_O above 500 kHz. The control system is programed to fully utilize the controller resource. When the system is reset, the MCU generates ΔT_1, ΔT_2 ... ΔT_n subsequently for Stage 1. Since the code is optimized with the system initialization, it actually takes only a few CPU cycles (around 25 CPU cycles) to execute Stage 1 for each control cycle. In Stage 2, the MCU senses V_O through ADC and refers to the f_S versus V_O table to determine f_S for Stage 2, which takes around 130 CPU cycles to execute once. In Stage 3, it takes a few more CPU cycles than Stage 2 (around 180 CPU cycles to execute once) because the MCU needs to gradually merge with the closed-loop control.

The switching instants for Stage 1 is shown in Table I. These analyses are based on a 130-kHz 300-W *LLC* converter with Ln ≈ 5, as referred to above, and a 500-kHz 1-kW *LLC* converter with $Lr = 4.5\,\mu$H, $Cr = 22$ nF, and $Lm = 22\,\mu$H. The same methodology applies to the design of different power stages. Twenty five CPU cycles in a 60 MHz MCU is equivalent to 418 ns, so there is enough time for the MCU to update the PWM module, even for a 500-kHz *LLC* converter.

Since the maximum start-up frequency $f_{S\_\max}$ of Stage 2 is much higher than that of Stage 3, and it takes many more CPU cycles for Stage 2 than Stage 1, the limitation for the soft start-up is the beginning of Stage 2. To ensure that there is enough time for the MCU to update PWM, which takes around 130 CPU cycles, the PWM module can be configured to be updated every nth switching cycle (n $= 1, 2, 3 \ldots$). Then, $f_{S\_\max}$ must satisfy

$$\frac{n}{f_{S\_\max}} > \frac{130}{60\,\text{MHz}}. \tag{9}$$

TABLE II
F_{S_MAX} UNDER DIFFERENT PWM UPDATING SPEEDS

PWM updating speed	$f_{S\_\max}$
Every switching cycle	460 kHz
Every second switching cycle	920 kHz
Every third switching cycle	1.38 MHz

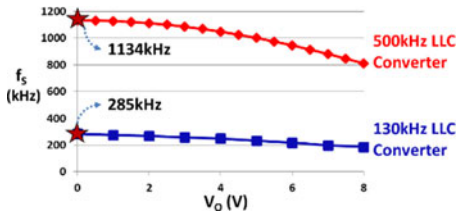

Fig. 11. f_S versus V_O for 400 V/12 V 130- and 500-kHz *LLC* converters.

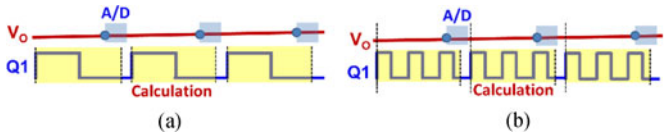

Fig. 12. Comparison between different PWM updating speeds. (a) Every switching cycle. (b) Every third switching cycle.

The summary for $f_{S\_\max}$ under different PWM updating speeds is listed in Table II, and the graph of f_S versus V_O for the 130-kHz *LLC* converter and the 500-kHz *LLC* converter is shown in Fig. 11. For the 130-kHz *LLC* converter, the maximum f_S is around 300 kHz, so the PWM can be updated every switching cycle. For the 500-kHz *LLC* converter, the maximum f_S is around 1.1 MHz, so the PWM is updated every third switching cycle.

Fig. 12 provides a comparison between PWM updating speeds of every switching cycle and every third switching cycle. For both cases, the sampling and A/D is at the end of the previous control cycle, and the calculation, which includes looking up the f_S versus V_O table and PWM update, starts at the beginning of each control cycle. A comparison has been made to verify V_O variation for different PWM updating speeds as shown in Fig. 13. The simulation is based on the 500-kHz *LLC* converter referred above with an output capacitor of 3 mF and under 80-A constant-current load. Slower updating speed will increase V_O variation, but due to the long start-up process, V_O variation between two consecutive PWM updates is still very smaller compared to nominal V_O, for example, the worst case is 70 mV, which is equivalent to around 0.6% of nominal V_O.

If f_S is further pushed to even higher, then either a higher performance MCU or a slower PWM update speed is needed.

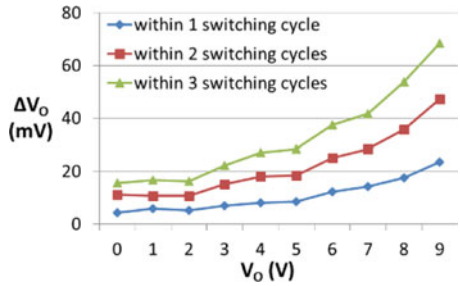

Fig. 13. Comparison of V_O variation under different PWM updating speeds

And V_O variation within one control cycle can be analyzed accordingly to guarantee that the proposed start-up is still valid for given parameters.

V. Short-Circuit Protection for High-Frequency *LLC* Converters

Short-circuit protection is very critical for front-end converters, especially when parallel operation is required. The converter is required to provide different output characteristics according to the load conditions: the converter should provide constant V_O from no load to full-load condition; if the load exceeds full-load power, the converter should be able to operate at constant power or constant current mode; furthermore, if V_O is shorted by a very small impedance under fault condition, the converter should be able to not only protect itself when V_O is shorted, but also start-up again after the short-circuit condition is removed. The transient from constant voltage mode to constant power mode or constant current mode is relatively slow, and its control can be inherently achieved by controlling f_S according to the f_S versus V_O table in Section III since V_O drops slowly and V_O variation is very small within two consecutive control cycles for the digital controller, meaning that the impact of digital delay is very small. As a comparison, under the protection mode, i.e., V_O is shorted by a very small impedance, V_O drops abruptly and it cannot be considered as stable over several switching cycles. Digital delay in the controller would have a significant impact since V_O may change greatly within two consecutive control cycles. And this effect will become more severe for the high-frequency *LLC* converters with low-cost digital controllers. It is of great meaning to investigate the impact of digital delay on the response of the converter under such abrupt short-circuit condition caused by a very small impedance, and figure out methods to minimize the digital delay impact.

The protection under short-circuit is normally tested by shorting V_O using a wire directly. The converter is tested as illustrated in Fig. 14; when V_O is shorted during the normal operation, the converter should be able to limit its stresses; and when the short-circuit condition is removed, the converter should be able to build up V_O again. It is worth noting that although Fig. 14 is a conceptual drawing, a converter satisfying the requirement in Fig. 14 is able to handle a varieties of real conditions, for example, a short-circuit could happen, then disappear, and then appear again. This is because if the converter is able to handle

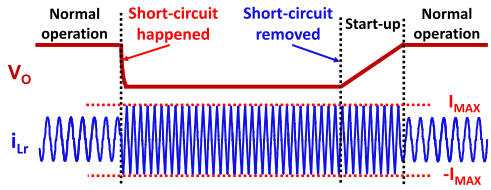

Fig. 14. Short-circuit protection test procedure.

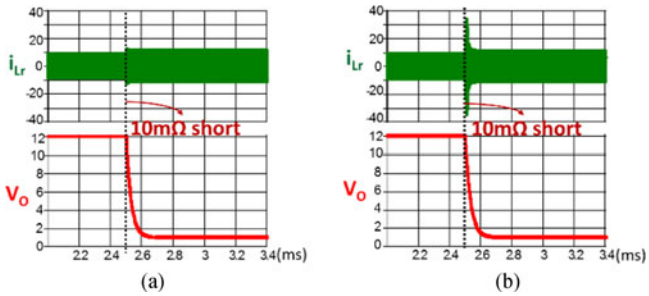

Fig. 15. Simulation of short-circuit protection using f_S versus V_O table for 500-kHz *LLC* converter. (a) No digital delay. (b) Digital delay of three switching cycles.

the transient between normal operation to short-circuit, it can handle the repetitive short-circuit conditions.

The analysis regarding the digital delay impact is verified by simulation as shown in Fig. 15, in which V_O is shorted by a 10 mΩ resistor during full-load steady-state operation. Fig. 15(a) is the case without digital delay, which shows little i_{Lr} stress increase compared to full-load stress after short-circuit occurs. Fig. 15(b) is the case with a digital delay of three switching cycles, which shows a significant i_{Lr} stress increase of up to three times the full-load current stress after short-circuit occurs.

Overcoming the limitations caused by digital delay in short-circuit protection using the f_S versus V_O table requires either a very fast digital controller or a very huge output capacitor. A very fast digital controller may limit the digital delay to a certain range that would minimize the digital delay impact but would also increase the cost significantly. A huge output capacitor may help slow down V_O drop when short-circuit occurs, but in order to limit the stress, the required capacitance would be much larger than the industrial practice, resulting in a larger footprint as well as a higher cost.

To solve this challenge in the short-circuit protection for the high-frequency *LLC* converters with low-cost digital controllers, this paper proposes a protection method based on load current i_{Load} that can be easily combined with the proposed soft start-up presented in Section III. Fig. 16 shows the proposed control scheme combining soft start-up and short-circuit protection. V_O is sensed for soft start-up, and i_{Load} is sensed to provide a fast response to short-circuit. Sensing i_{Load} is quite a common practice in power supplies for the IT industry due to the power management requirements. Advanced control methods such as SOTC already includes i_{Load} in the control system, as shown in Fig. 1, to achieve the benefit of fast transient response. The proposed control scheme is quite similar to that of SOTC, and thus

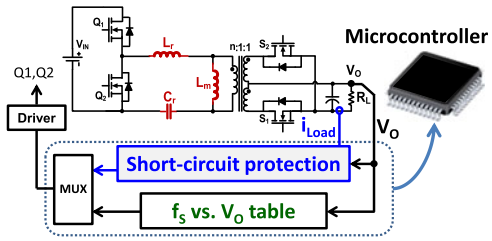

Fig. 16. Proposed control scheme for soft start-up and short-circuit protection.

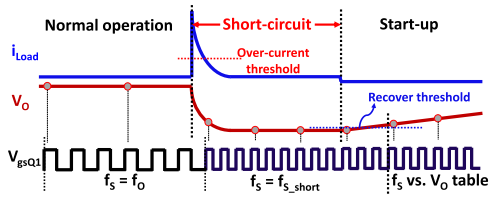

Fig. 17. Illustration of the proposed short-circuit protection method.

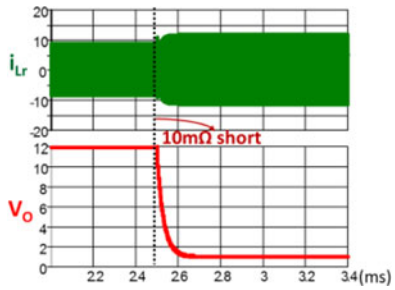

Fig. 18. Simulation of proposed short-circuit protection for 500-kHz *LLC* converter.

both methods can be integrated into the same digital controller without increasing the cost or adding an auxiliary circuit.

The basic control principle of the proposed short-circuit protection is illustrated in Fig. 17. During normal operation, the controller senses V_O and converts it through A/D for closed-loop control. Meanwhile, the controller senses $i_{\rm Load}$ and compares it with the preset overcurrent threshold. This comparison function could be implemented by the integrated comparator peripheral [36] within the digital controller or by an external comparator to minimize digital delay. When V_O is shorted, there would be a huge current drawn from the output capacitor, which would trigger short-circuit protection, and then the controller would set f_S to the predetermined short-circuit switching frequency $f_{S\_\rm short}$ to minimize the stresses. During the short-circuit conditions, the controller keeps monitoring V_O and compares it with a recover threshold. When the short-circuit condition is removed, V_O will increase gradually and the controller will begin the soft start-up process when V_O reaches the recovery threshold. The proposed short-circuit protection method is verified by simulation, as shown in Fig. 18. When V_O is shorted by a 10 mΩ resistor during full-load steady-state operation, the controller is able to respond very quickly to limit i_{Lr} stress.

TABLE III
SPECIFICATIONS OF THE 500-KHZ LLC CONVERTER

Component	Parameters
Resonant Frequency f_O	500 kHz
Dead Time	180 ns
Transformer turns ratio	16:1
Primary devices	IPW60R099P6
Secondary devices	BSC010N04LS
Primary Driver	ADuM4223
Secondary Drivers	FAN3122
Resonant Capacitor	22 nF
Resonant Inductance	4.5 uH
Magnetizing Inductance	21.6 uH

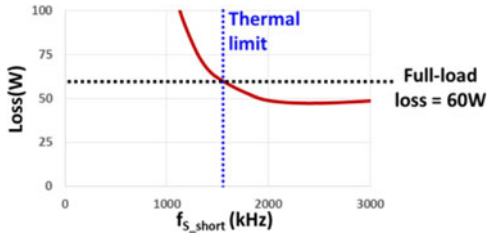

Fig. 19. Total loss versus $f_{S\_\rm short}$ under short-circuit for 500-kHz *LLC* converter.

Another important consideration for the short-circuit protection is to limit the system thermal stress. In order to not increase the cost for heat dissipation, the total loss under short-circuit conditions should be kept below the total loss under full-load condition in normal operation. Loss analysis under short-circuit condition has been made for a 1-kW 500-kHz 400-V/12-V *LLC* converter, whose specifications are listed in Table III. The primary is a half-bridge configuration, and the secondary consists of four sets of outputs. The total losses with different $f_{S\_\rm short}$ under short-circuit condition are shown in Fig. 19. The $f_{S\_\rm short}$ is selected as 1.6 MHz to fulfill the system thermal requirements.

It is worth noting that although the system total loss is less than the full-load loss, attention needs to be paid to the thermal limit of each component. Taking the converter referred to above as an example, when $f_{S\_\rm short}$ is very high, the primary driving loss would be very huge due to the large gate charge of the Si devices, and may exceed the thermal limit of the primary driver. Such limitations could be overcome by employing "hiccup" mode, meaning that the converter runs and stops alternatively. "Hiccup" mode is helpful to reduce thermal stress, but may result in a delayed response to the recovery if short-circuit condition is removed when the converter stops.

VI. EXPERIMENTAL RESULTS

The proposed soft start-up and short-circuit protection for the high-frequency *LLC* converters are implemented by a 60-MHz MCU TMS320F28027, and verified on a 1-kW 400-V/12-V 500-kHz *LLC* converter, whose parameters are listed in Table III of Section V. This high-frequency *LLC* converter is designed based on the matrix transformer for *LLC* converters in [16].

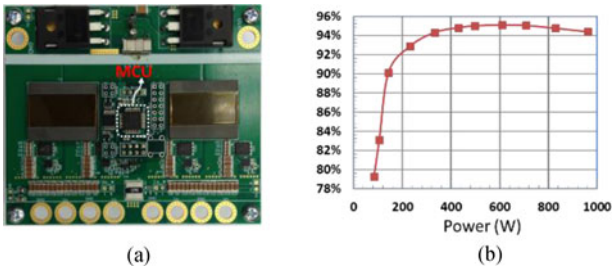

Fig. 20. MCU-controlled 1-kW 400-V/12-V 500-kHz *LLC* Converter. (a) Prototype. (b) Efficiency.

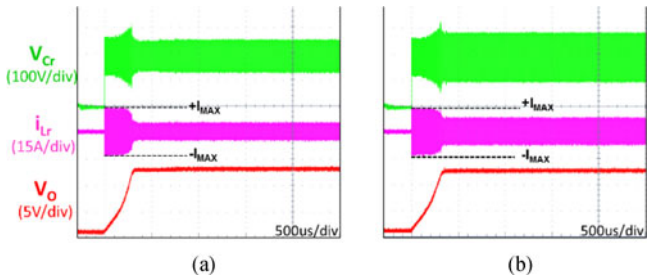

Fig. 21. Soft start-up under different resistive loads with $V_{\rm in} = 385$ V. (a) $Load = 0.35\,\Omega\,(40\%\,load)$. (b) $Load = 0.178\,\Omega\,(80\%\,load)$.

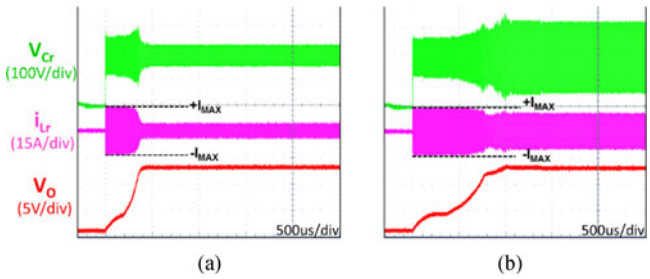

Fig. 22. Soft start-up under different constant-current loads with $V_{\rm in} = 385$ V. (a) $Load = 20\,{\rm A}\,(25\%\,load)$. (b) $Load = 80\,{\rm A}\,(full - load)$.

The prototype and the efficiency curve are shown in Fig. 20. The *LLC* converter has a power density of 207 W/in^3, a peak efficiency of 95.1%, and an output capacitor of 3 mF.

The 500-kHz *LLC* converter referred in Fig. 20 has a full-load steady-state i_{Lr} stress of around 10 A. Considering the impact of $V_{\rm in}$ variation and resonant tank tolerance, both of which contributes 10% i_{Lr} stress variation, 14 A current stress is selected as the current limiting band for calculating the f_S versus V_O table to ensure that the converter is able to start-up under any conditions. The experimental results of soft start-up with different resistive loads under $V_{\rm in} = 385$ V are shown in Fig. 21. Since the *LLC* converter works like a constant current source with the proposed control method during start-up, i_{Lr} stress for both cases are the same. Most of the output current charges the output capacitor while the rest is dissipated by the load, so it takes a little bit longer to finish the start-up process for the 0.178 Ω load conditions.

Fig. 22 shows the experimental results of soft start-up with different constant-current loads with $V_{\rm in} = 385$ V.

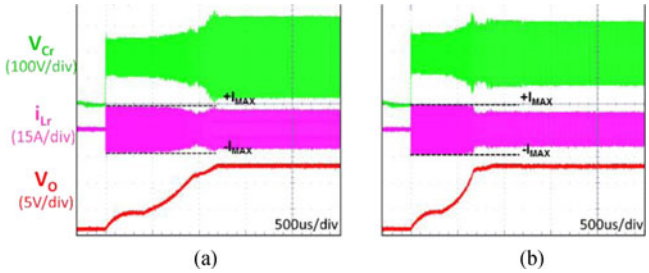

Fig. 23. Soft start-up under 80 A (full-load) constant-current loads with different $V_{\rm in}$. (a) $V_{\rm in} = 370$ V. (b) $V_{\rm in} = 400$ V.

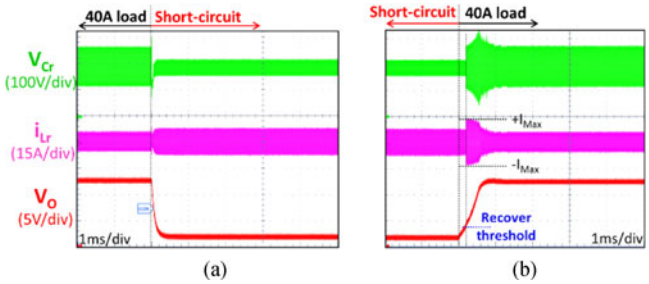

Fig. 24. Short-circuit protection and recovery. (a) Protection. (b) Recovery.

Electronic load RBL488 from TDI is used as the constant-current load. At the beginning of soft start-up, the slope of V_O is not as smooth as that of the resistive load, because the electronic load in constant-current mode is saturated at the beginning and extracts larger current than the programed value. An 80-A constant-current load is the worst case for the soft start-up, but even under such conditions the converter is able to limit i_{Lr} stress within the current-limiting band.

Fig. 23 shows the experimental results of soft start-up under 80 A constant-current load with different $V_{\rm in}$. With the proposed control method, i_{Lr} stress is proportional to $V_{\rm in}$, as discussed in Section III. Since $V_{\rm in}$ variation is kept relatively small to maintain a good efficiency, i_{Lr} stress variation is also small with the proposed control method.

The experimental results of the proposed short-circuit protection and its recovery are shown in Fig. 24. The short-circuit condition is emulated by the short-circuit function of the electronic load, and the total short-circuit resistance is around 10– 20 mΩ. In Fig. 24(a), the converter operates in the normal condition with 40-A load at the beginning. When short-circuit occurs, V_O drops to almost 0 V and the converter is able to limit i_{Lr} stress immediately. In Fig. 24(b), when short-circuit is removed, V_O starts rising; after V_O meets the recover threshold, the converter begins the soft start-up process and builds up V_O gradually to 12 V.

The experimental results of using "hiccup" mode to reduce the thermal stress during short-circuit conditions are shown in Fig. 25. In this case, the converter operates with an f_S of 1.6 MHz for around 6 ms, and stops for around 24 ms. The converter would repeat this process until the short-circuit condition is removed and the converter would recover to normal operation.

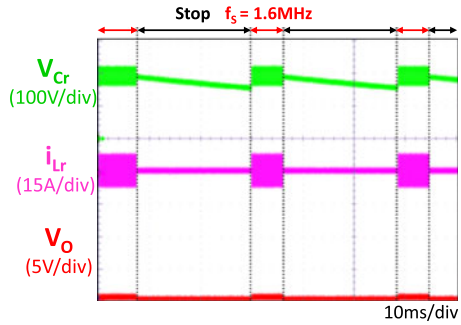

Fig. 25. "Hiccup" mode to reduce thermal stress during short-circuit condition

VII. Conclusion

This paper provides an investigation of OTC for soft start-up and the limitations of its MCU implementation. Digital delay has a significant impact on the stresses during start-up if directly employing the concept of OTC for soft start-up. An MCU-based implementation with lookup tables is proposed to overcome this challenge, which only requires sensing the output voltage. The lookup tables for different stages in the soft start-up are derived based on the concept of OTC for soft start-up and the state-plane analysis. The proposed method is then extended to high-frequency *LLC* converters without increasing the cost for the controllers. The method is proven by theoretical analysis and simulation to be robust enough to handle input voltage variations and resonant tank tolerances.

Based on the concept of SOTC, a short-circuit protection method is proposed that senses the load current to minimize the impact of digital delay. The total loss during the short-circuit condition under different switching frequencies is analyzed, and guidelines are provided to select a suitable switching frequency for short circuit. "Hiccup" mode is employed to further reduce the thermal stress. The proposed soft start-up and short-circuit protection have a control scheme which is similar to that of SOTC, and thus, they are suitable for integration with other SOTC control functions.

A 1-kW 500-kHz 400-V/12-V *LLC* converter is built and a 60-MHz MCU TMS320F28027 is used to implement the proposed soft start-up and short-circuit protection. The experimental results demonstrate that the proposed soft start-up is able to limit the stresses and optimize energy delivery under different load conditions and different input voltages, and the proposed short-circuit protection is able to limit the resonant current stress when abrupt short-circuit occurs and recover the output voltage when short-circuit conditions are removed.

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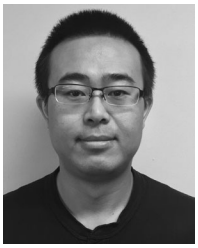

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