Design of a Highly Efficient (97.7%) and Very Compact (2.2 kW/dm^3) Isolated AC–DC Telecom Power Supply Module Based on the Multicell ISOP Converter Approach

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***Abstract*—The rising electricity demand of data centers has initiated a development trend toward highly efficient power supplies. Therefore, a multicell converter approach for a telecom rectifier module breaking through the efficiency and power density barriers of traditional single-cell converter systems is presented in this paper. The potential of the multicell approach for high efficiency is derived from fundamental scaling laws of different system performance aspects in dependence of the number of converter cells and the benefits of the interleaving technique. Based on the available degrees of freedom in the design of such a converter system, a comprehensive multiobjective optimization of the entire system with respect to efficiency and power density is performed with detailed component loss and volume models. In order to verify the analytical models and the design procedure, a hardware demonstrator of a 3.3 kW multicell 230 $V_{\rm AC}$/48 $V_{\rm DC}$ telecom power supply with $N_{\rm cells} = 6$ isolated converter cells in an input-series output-parallel arrangement is presented with measurement results indicating a maximum efficiency of $\eta = 97.7\%$ and a power density of $\rho = 2.2$ kW/dm^3 ($= 36$ W/in^3). Furthermore, different paths for future performance improvements of the multicell arrangement are outlined.**

***Index Terms*—AC–DC power converters, digital control, power MOSFETs.**

I. Introduction

DRIVEN by the increasing popularity of cloud-based internet services, the Internet-of-Things, and the trend around "big data," the electricity consumption of data centers has grown tremendously in the past decade and is projected to grow in the future even further, e.g., around 70% from 2013 to 2020 in the U.S. alone [1]. As a consequence, data centers are now one of the largest consumers of electricity and, therefore, also under a growing financial and political pressure to increase their energy efficiency.

State-of-the-art single-phase telecom power supply modules usually comprise a PFC rectifier stage and an isolated dc–dc converter output stage, usually generating a nominal output voltage of 48 V. The rectifier stage is typically a boost-type PFC rectifier that consists of a full-bridge diode rectifier in connection with a boost converter. Since the forward voltage drops of the diodes in the rectifier account for high conduction losses, alternative bridgeless topologies have gained significant interest over the past years [2], [3]. One example of a highly efficient single-phase bridgeless telecom rectifier is described in [4]. This is a triple-parallel-interleaved triangular current mode PFC rectifier system with a double-parallel-interleaved phase-shift full-bridge isolated dc–dc converter (rated power $P_{\rm out} = 3.3$ kW, rated output voltage $V_{\rm out} = 48$ V), which features a power density of $\rho = 3.3$ kW/dm^3 and an efficiency of $\eta = 97\%$ at half of the rated power. A new approach toward a hyperefficient and supercompact telecom rectifier design beyond the barriers of traditional converter concepts is presented in this paper. This approach is based on the employment of multiple low-power converter cells which are connected in series at the input terminals and in parallel at the output terminals (input series output parallel—ISOP). A multicell telecom power supply with this configuration can essentially be realized in three different ways, as shown in Fig. 1. Common to all three concepts is the application of multiple converter cells that equally share the input voltage and the output current, which requires a means of isolation between the individual series-stacked dc-link potentials from the common output potential. Therefore, in all three concepts, an isolated dc–dc converter stage is employed in each converter cell. The three concepts mainly differ concerning the rectification of the sinusoidal mains voltage. In Fig. 1(a), a full-bridge diode rectifier is utilized, similar to the structure of a conventional boost PFC rectifier, but with the difference that the boost stage is split up into multiple $|$ ac$|$–dc converter boost stages, which are located at the input of each converter cell. Since the diode full-bridge leads to significant conduction losses and synchronous rectification (SR) devices would have to be rated for the full peak input voltage, this concept will be

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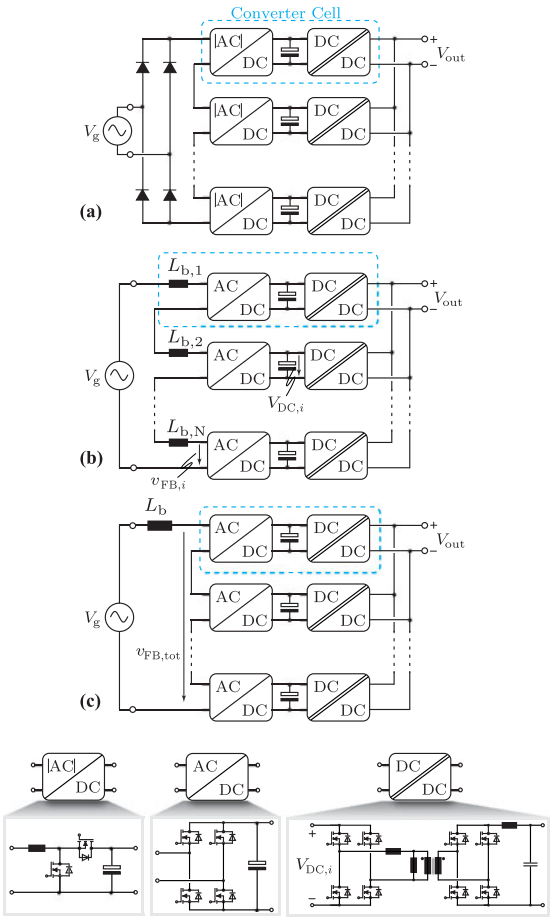

Fig. 1. Multicell telecom power supply module topologies in ISOP arrangement: (a) input-side diode rectifier with converter cells containing an | ac|-dc boost converter (processing a time-varying input voltage) and an isolated dc–dc converter connected in series; topologies where each cell contains an ac–dc rectifier input stage with (b) either a distributed line inductance or (c) a single line inductor, and an isolated dc–dc converter stage.

discarded. In Fig. 1(b) and (c), the diode bridge is omitted and, instead, a full-bridge synchronous rectifier is integrated in each converter cell, which only requires semiconductors which are rated for the dc-link voltage of a single cell. The boost inductor L_b can either be realized by distributed inductors where each inductor is associated with one converter cell [cf., Fig. 1(b)] similar to the distributed boost stages of Fig. 1(a), or can be realized by a single inductor for the whole converter system [cf., Fig. 1(c)]. The inductance value of the single inductor in the latter concept equals the sum of the distributed inductances of the former concept, for the assumption of the same input current ripple. Since the realization effort and the total volume is smaller for a single inductor than for distributed inductors,[1] the concept of Fig. 1(c) is selected in this paper.

[1]The area product of an inductor (defined as product of the winding area and the core area) scales with the required inductance and can be calculated as $A_\mathrm{w}A_\mathrm{c} = L \cdot I^2/(S \cdot k_\mathrm{fill} \cdot B_\mathrm{max})$, where S is the current density, k_fill is the filling factor of the winding area, and B_max the maximum flux density. The area product is proportional to the fourth power of the linear dimension l, whereas the volume is proportional to l^3. Thus, the volume of N inductors with each having an inductance of L/N is $\mathrm{Vol_{tot}} = N \cdot (A_\mathrm{w}A_\mathrm{c}/N)^{(3/4)} = N^{1/4}\mathrm{Vol_{single}}$, which is a factor of $N^{1/4}$ larger than the volume $\mathrm{Vol_{single}}$ of a single inductor with inductance L.

In the following sections, the benefits of the multicell converter approach, the optimization, the design, and the control of the multicell telecom rectifier system of Fig. 1(c) are analyzed. At first, in Section II, fundamental scaling laws of power electronic systems are described, which highlight the advantages of multicell converters for ac–dc conversion. The implemented control scheme for the ISOP multicell system with a master–slave regime is presented in Section III. In Section IV, the available degrees of freedom in the design of a multicell converter system are analyzed, the modeling of the losses and volumes of the employed components is outlined and the optimization results are discussed. Subsequently, in Section V, the design of the hardware demonstrated is shown and critical design aspects are analyzed. In order to verify the optimization results, different measurement results of the hardware demonstrator are presented in Section VI. In Section VII, possible paths to future performance improvements of the multicell telecom rectifier system are briefly discussed. Finally, conclusion is drawn in Section VIII.

II. AC–DC Converter Scaling Laws

The benefits offered by a multicell ac–dc rectifier system compared to its single-cell converter counterpart can be derived from fundamental scaling laws of interleaved converter cells. In [5], several scaling laws of parallel- and series-interleaved dc–dc converters have been derived that demonstrate the advantages of multicell systems in terms of the following.

1) Reduced conduction losses: The use of low-voltage semiconductors in series-connected converter cells effectively shifts the silicon limit toward lower specific on-state resistances, which is due to the scaling of the specific on-state resistance with the blocking voltage by $R_\mathrm{DS,on} \propto V_\mathrm{DS}^{2.5}$. This leads to the effect that N_cells in series-connected semiconductors with a blocking voltage of $V_\mathrm{DC}/N_\mathrm{cells}$ have a lower total $R_\mathrm{DS,on}$ than a single semiconductor with a blocking voltage of V_DC. For the case of equal total chip areas, a reduction of the total $R_\mathrm{DS,on}$ by a factor of $1/\sqrt{N_\mathrm{cells}}$ can be achieved.
2) Reduced current and voltage ripple: By interleaving the operation of the converter cells, the effective switching frequency of the system is a multiple of the switching frequency of a single converter cell [6]. In combination with the reduced voltage levels of the cells (in series interleaving) or increased boost inductance (in parallel interleaving for equal total stored energy), the current ripple reduces by $1/N_\mathrm{cells}^2$.
3) Reduced switching losses: By splitting the system into low power cells with low voltage and/or low current, the total switching losses reduce with $1/N_\mathrm{cells}^2$ for the case of equal current ripples (under the assumption of equal $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ rates of the multicell system and the single-cell system and that the switching losses are defined by the overlapping of voltage and current during the switching transition). For the case of equal switching losses, the effective switching frequency in the multicell system can be a factor of N_cells higher than in the single-cell system.
4) Reduced heat sink volumes: The reduction of the total switching and conduction losses combined with the

TABLE I
SCALING LAWS OF MULTICELL SYSTEMS WITH N_{CELLS} CELLS IN COMPARISON TO A SINGLE-CELL SYSTEM

System	Sw. Freq. per Cell	Eff. Sw. Freq.	Switching Losses	Curr. Ripple	Inductance	Stored Energy
Single-Cell	$f_{\text{sw},0}$	$f_{\text{sw},0}$	$P_{\text{sw},0}$	ΔI_0	L_0	$E_{L,0}$
Multicell (Series Interleaving)	$f_{\text{sw},0}$	$N_{\text{cells}} \cdot f_{\text{sw},0}$	$P_{\text{sw},0}$	$\Delta I_0/N_{\text{cells}}^2$	L_0	$E_{L,0}$
Multicell (Parallel Interleaving)	$f_{\text{sw},0}$	$N_{\text{cells}} \cdot f_{\text{sw},0}$	$P_{\text{sw},0}$	$\Delta I_0/N_{\text{cells}}^2$	$N_{\text{cells}} \cdot L_0$	$E_{L,0}$

In the parallel-interleaved multicell system, each converter cell has an inductor with the inductance specified in this table, and the current ripple is the total current ripple of the entire multicell system. The stored energy is the total energy stored in the inductors of each system and is calculated by considering only the average current through the inductors, i.e. neglecting the current ripple. Furthermore, it is assumed that the cells in the multicell systems are operated interleaved to each other with the optimal phase shift of $\delta = 2\pi/N_{\text{cells}}$.

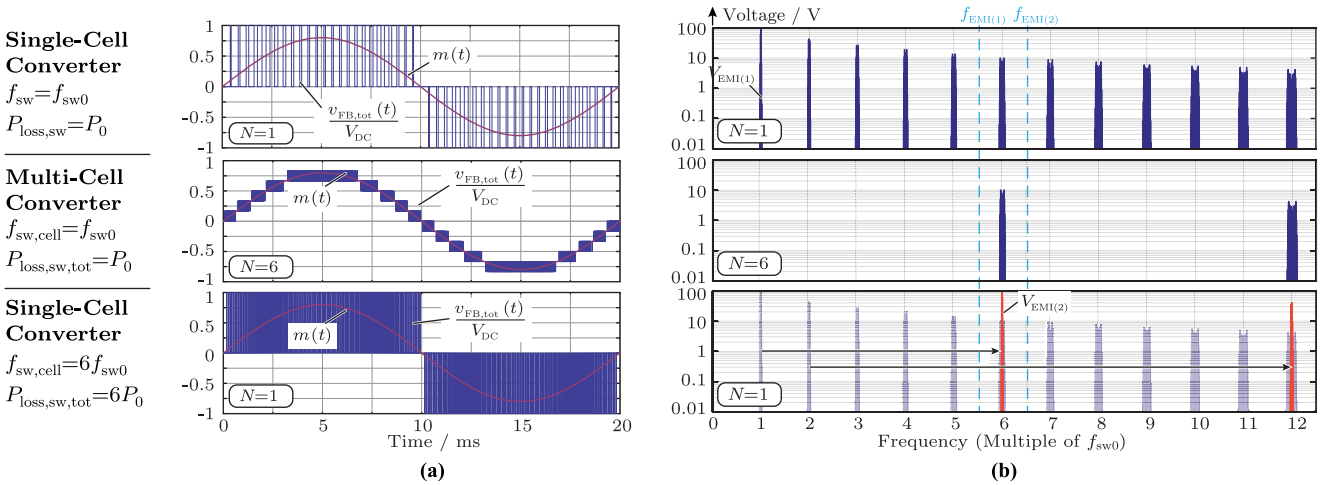

Fig. 2. Effect of multiple rectifier stages with phase-shifted modulation on the system behavior: (a) Comparison of the switched voltage waveform between (top) a single-cell converter system and (middle) a multicell converter system with six converter cells. Both systems feature the same switching losses (cf., Table I); (bottom) single-cell converter waveform with six times the switching frequency and also six times higher switching losses than the other two options; (b) corresponding harmonic spectra of the waveforms shown in (a). As a result, operating a single rectifier stage with six times the switching frequency does not yield the same harmonics (in amplitude) as the multicell converter system but creates six times higher switching losses. The cancelation of harmonics can lead to a reduction of the EMI filter volume if the EMI limited frequency range starts after the harmonic which is not canceled, i.e., $f_{\text{EMI(2)}}$. On the contrary, if the uncanceled harmonic is the first harmonic in the limited frequency range, i.e., $f_{\text{EMI(1)}}$, the EMI filter has to be designed with the same attenuation as for the single-cell system.

distribution of the losses among several semiconductors leads to smaller heat sinks or even completely eliminates the need for such.

5) Reduced magnetic component volumes: The parallel interleaving of converter cells leads to a reduction of the total energy stored in the inductors which correlates with a reduction of the total inductor volume for the same current ripple.

The above-mentioned benefits are summarized in Table I and can be leveraged in different dimensions. In Table I, the multicell systems are designed for the same switching losses and the same stored energy as the single-cell system, which results in a strong reduction of the current ripple (i.e., $1/N_{\text{cells}}^2$). Another possible design might be to operate the multicell systems with the same effective switching frequency of $f_{\text{sw},0}$ as the single-cell system (i.e., each cell operates with $f_{\text{sw},0}/N_{\text{cells}}$). This leads to reduced switching losses of $P_{\text{sw},0}/N_{\text{cells}}$ as well as a reduced current ripple of $\Delta I_0/N_{\text{cells}}$. Consequently, if the systems are designed for the same current ripple of ΔI_0, a reduction of the switching losses in the multicell systems by a factor of $1/N_{\text{cells}}^2$ can be gained.

It should be noted that the scaling laws are not only valid for dc–dc converter systems but also for ac–dc multicell converter systems, as will be shown in more detail in the following paragraphs.

Input Current Ripple and Harmonic Spectrum

The ac–dc conversion of the multicell telecom rectifier [cf. Fig. 1(c)] comprises multiple series-connected full-bridge switching stages that are advantageously operated with a phase-shifted (interleaved) modulation scheme considering a phase shift of $\delta_{\text{ph}} = 2\pi/N_{\text{cells}}$, with N_{cells} being the number of converter cells. In the simplest case, only one bridge leg of each cell is operated at switching frequency $f_{\text{sw,cell}}$, while the other bridge leg is operated at mains frequency f_g. This modulation method is commonly referred to as totem-pole modulation [7]. For a system with N_{cells} series-connected and interleaved full-bridge cells, this results in an effective switching frequency $f_{\text{sw,eff}}$ of the entire rectifier stage, which is N_{cells} times higher than the switching frequency $f_{\text{sw,cell}}$ of a single cell, i.e., $f_{\text{sw,eff}} = N_{\text{cells}} \cdot f_{\text{sw,cell}}$. Compared to the conventional single-cell topology where a

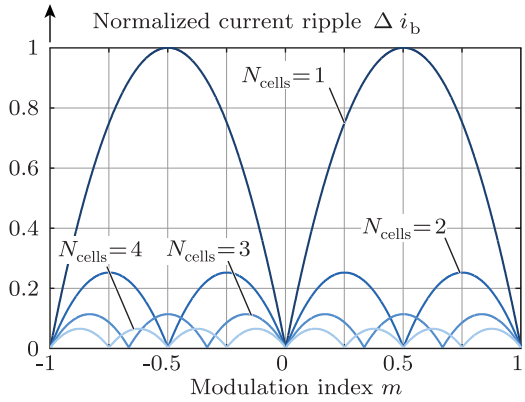

Fig. 3. Peak-to-peak current ripple reduction of the boost inductor current i_b (normalized to $V_{DC}/(4f_{sw}L_b)$) for different numbers of rectifier stages N_{cells} in dependence of the modulation index $m = v_{FB,tot}/V_{DC}$ for a given value of boost inductance L_b.

capacitor voltage V_{DC} is required for the operation of the PFC rectifier (i.e., sufficiently above the peak value of the mains voltage $\hat{V}_g$), in the multicell system this voltage is distributed among N_{cells} capacitors, i.e., each dc-link capacitor is charged to $V_{DC,i} = V_{DC}/N_{cells}$. As a result, the voltage $v_{FB,tot}$ (i.e., sum of all rectifier stage voltages $v_{FB,i}$) comprises $2 \cdot N_{cells} + 1$ voltage levels, as shown in Fig. 2(b).

Consequently, with a higher effective switching frequency and more voltage levels of the rectifier voltage $v_{FB,tot}$, the peak-to-peak current ripple Δi_b of the boost inductor current i_b decreases with increasing number of converter cells. The current ripple can be calculated in dependence of the modulation index m by introducing an effective modulation index $m_{eff} = (m \text{ modulo } 1/N_{cells})$, i.e., a modulation index that has values only between 0 and $1/N_{cells}$, with the relation of $v = L\mathrm{d}i/\mathrm{d}t$ as

$$\Delta i_b(m_{eff}) = \frac{V_{DC}}{f_{sw}L_b} \cdot m_{eff} \cdot \left(\frac{1}{N_{cells}} - m_{eff}\right) \tag{1}$$

(cf., [8]). This relation is shown in Fig. 3 normalized to the value of $V_{DC}/(4f_{sw}L_b)$. The maximum peak-to-peak value of the boost inductor current ripple can be found at $m_{eff} = 0.5/N_{cells}$ as

$$\Delta i_{b,max} = \frac{V_{DC}}{4N_{cells}^2 f_{sw}L_b}. \tag{2}$$

As a result, by increasing the number of cells N_{cells} with the same switching frequency, the current ripple of the boost inductor current decreases quadratically for a given boost inductance L_b.

The additional voltage steps of the converter voltage in combination with a higher effective switching frequency also lead to an improved electromagnetic interference (EMI) spectrum, as can be derived based on [9]. For a single full-bridge stage with a total dc-link voltage V_{DC}, the amplitude $\hat{V}_{FB,single(q)}$ of a harmonic with order q of the mains frequency $f_g = 1/T_g$ can

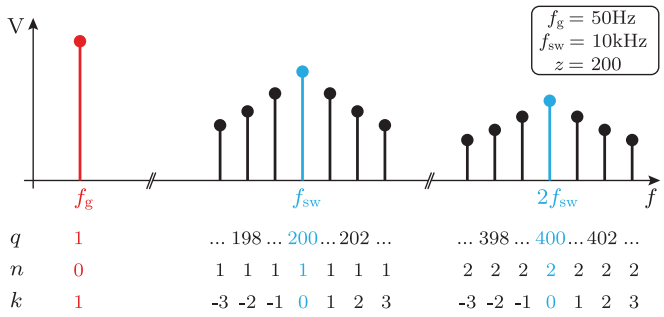

Fig. 4. Explanation of the nomenclature used to specify the order $q = n \cdot z + k$ of the harmonics at the example of $f_g = 50$ Hz and $f_{sw} = 10$ kHz.

be calculated for a modulation index $m(t) = v_{FB,tot}(t)/V_{DC}$ as

$$\hat{V}_{FB,single(q)} = \frac{-4 \cdot V_{DC} \cdot (1-(-1)^k)}{n\pi T_g} \cdot \int_0^{T_g/4} \cos(k \cdot \omega_g \cdot t) \cdot \sin(n \cdot \pi \cdot m(t))\, dt \tag{3}$$

with $q = n \cdot z + k$, where $z = f_{sw}/f_g$ and $|k| \le z/2$. Typically, n is referred to as the number of the harmonic of the switching frequency and k specifies the sideband ($n, k \in \mathbb{N}$), as visualized in Fig. 4 for the example of $f_g = 50$ Hz and $f_{sw} = 10$ kHz. In a system with N_{cells} rectifier stages, each cell emits harmonics where the amplitude of a harmonic with order q can be calculated according to (3) just with a lower dc-link voltage, i.e.,

$$\hat{V}_{FB,cell(q)} = \frac{\hat{V}_{FB,single(q)}}{N_{cells}}. \tag{4}$$

Since the cells are operated interleaved to each other, the time-dependent waveform of a harmonic with order q of the total multicell converter input voltage $v_{FB,tot}$ has to be expressed as a sum of voltages of all cells, taking into account the phase shift between the individual cells

$$\hat{V}_{FB,tot(q)}(t) = \sum_{i=1}^{N_{cells}} \frac{\hat{V}_{FB,single(q)}}{N_{cells}} \cdot \cos\left(q\left(2\pi f_g t + \frac{2\pi}{zN_{cells}}(i-1)\right)\right). \tag{5}$$

By assuming $z \to \infty$, (5) converges to the simplified expression of

$$\hat{V}_{FB,tot,(q)}(t) = \begin{cases} \hat{V}_{FB,single(q)} \cos(q2\pi f_g t), & \text{if } n = lN_{cells},\ l \in \mathbb{N} \\ 0, & \text{else.} \end{cases} \tag{6}$$

The amplitude of this time-dependent waveform is the amplitude of the considered harmonic. Consequently, the harmonic spectrum of the multicell system can be derived from the spectrum of a single-cell converter system by considering only the harmonics $q = n \cdot z + k$, where n is a multiple of the number of converter cells N_{cells}, i.e., $\hat{V}_{FB,tot,(q)} = \hat{V}_{FB,single(q)}$ for $n = l \cdot N_{cells}$, $l \in \mathbb{N}$, as visualized in Fig. 2(b). Thus, the interleaving of multiple low-voltage converter cells has the advantage of harmonic cancelation compared to a single-cell converter under the assumption of equal switching losses.

In order to quantify the effect of the harmonic cancelation on the EMI filter design and/or requirement, however, the relevant EMI standards have to be taken into account. In typical PFC applications, the conducted high-frequency harmonic noise emissions are restricted by EMI standards (e.g., CISPR Class A and B) which define absolute allowable emissions limits on harmonics in the frequency range of 150 kHz $\leq f \leq$ 30 MHz. Since the EMI filter attenuation has a roll-off slope of -40 dB/dec per filter stage and an EMI filter has typically two or more filter stages, the filter attenuation has a much steeper roll-off characteristic than the EMI standard with a roll-off slope of only -20 dB/dec (Class B) up to a frequency of 500 kHz. Therefore, typically only the first harmonic of the converter, which falls into the restricted EMI spectrum, has to be considered for the design of the EMI filter. As a result, the cancelation of harmonics in multicell converter systems is only offering benefits in terms of reduced EMI filtering efforts compared to single-cell systems if among the canceled harmonics of the single-cell system is also the first harmonic that falls into the limited EMI spectrum, which was previously determining the filter design in the single-cell converter. That means, e.g., in Fig. 2(b), the multicell converter with six converter cells would have the greatest reduction of the EMI filter volume if the restricted frequency band would start between the sixth and seventh harmonic (i.e., after a harmonic that is not canceled) of the single-cell system [cf., $f_{\mathrm{EMI(2)}}$ in Fig. 2(b)], e.g., if the sixth harmonic was at 140 kHz. On the contrary, however, if the sixth harmonic was the first harmonic in the EMI limited frequency band [cf., $f_{\mathrm{EMI(1)}}$ in Fig. 2(b)], e.g., at 150 kHz or above, then the interleaving of the converter with six cells would not result in EMI filter benefits since the sixth harmonic is not canceled, i.e., the harmonic which determines the filter design in the single-cell system is the same harmonic as in the multicell system.

Please note that the cancelation of harmonics in multicell systems is not equal to operating the single-cell system with N_{cells} times the switching frequency. This would (apart from a sixfold increase of switching losses) only shift the harmonics to higher frequencies but not additionally reduce the amplitude of the harmonics, as it is the case for the interleaved cell operation of a multicell system. The reason for this is that the single-cell converter would still switch the full dc-link voltage and not the low-voltage levels as in the staircase voltage waveform of the multicell system. This is visualized in Fig. 2(b) where the harmonic spectrum of $V_{\mathrm{EMI(2)}}$ is the spectrum of the single-cell converter with six times the switching frequency of the original system with spectrum $V_{\mathrm{EMI(1)}}$.

The boost inductor can also be considered as a part of the EMI filter since it provides attenuation to emitted harmonics of the converter, which offers a degree of freedom in the choice of the boost inductance and the attenuation of the remaining EMI filter. Instead of designing the multicell converter for the same maximum peak-to-peak current ripple $\Delta i_{\mathrm{b,max}}$ as the single-cell system, which would yield a boost inductance which is $1/N_{\mathrm{cells}}^2$ times smaller, a reduction of the boost inductance of, e.g., only $1/N_{\mathrm{cells}}$ might also be acceptable which in addition to a smaller boost inductance also leads to a lower current ripple. This would result for the multicell system in a lower attenuation requirement of the remaining EMI filter and, thus, in a smaller volume of this part of the EMI filter in addition to the smaller volume of the boost inductor than in the single-cell system.

III. ISOP Converter Control Concept

One of the main challenges regarding the control of multicell converters in general is the equal distribution of the current and/or voltage among the converter cells. In ISOP systems, the total dc-link voltage should be equally shared between the individual cells in order to avoid critical voltages above the component ratings of each cell. Furthermore, the output current and/or power should be equally split among the dc–dc converter stages such that no cell exceeds its power rating and the losses are evenly distributed between the cells.

A. Common-Duty Cycle Control

The most convenient way to operate an ISOP multicell system is to apply a common modulation index to all ac–dc rectifier stages and a common duty cycle (i.e., phase-shift for the phase-shifted full-bridge (PSFB) converters) to all converter cells. This operation scheme relies on the natural balancing behavior inherent to ISOP multicell converter systems [10]–[12].

1) Voltage and Current Balancing: For the case that all converter cell hardware realizations are exactly identical, the dc-link voltage and output currents are perfectly balanced since any deviation of the dc-link voltages from the balanced steady state leads to different output power levels which are counteracting the unbalance. Since this balancing method is not actively controlling the dc-link voltages and output currents, however, any mismatch between the converters, such as, e.g., slightly different transformer terminal behaviors, leads to unbalanced dc-voltage levels and output currents but not to a runaway situation [10]. The dc-link cell voltages $V_{\mathrm{DC},i}$ can be calculated for the case of different transformer turns ratios as

$$V_{\mathrm{DC},i} = V_{\mathrm{DC}} \frac{1}{\left(\sum_{k=1}^{N_{\mathrm{cells}}} \frac{1}{n_{\mathrm{k}}}\right) \cdot n_{\mathrm{i}}} \tag{7}$$

with n_k being the transformer turns ratio $N_{\mathrm{sec},k}/N_{\mathrm{prim},k}$ of cell k with $k \in [1, N_{\mathrm{cells}}]$. In the same way, the average steady-state output current $I_{\mathrm{out},i}$ of each converter cell can be calculated in dependence of the total output current $I_{\mathrm{out,tot}}$ as

$$I_{\mathrm{out},i} = I_{\mathrm{out,tot}} \frac{1}{\left(\sum_{k=1}^{N_{\mathrm{cells}}} \frac{1}{n_{\mathrm{k}}}\right) \cdot n_{\mathrm{i}}}. \tag{8}$$

As a consequence, the total power of the system is unequally shared among the converter cells, i.e.,

$$P_{\mathrm{cell},i} = P_{\mathrm{tot}} \frac{1}{\left(\sum_{k=1}^{N_{\mathrm{cells}}} \frac{1}{n_{\mathrm{k}}}\right) \cdot n_{\mathrm{i}}}. \tag{9}$$

Typically, the mismatch between the transformers of the different cells can be kept reasonably small with standard industrial manufacturing methods and/or before assembling a multicell converter only transformers with similar terminal characteristics can be selected.

2) Circulating Currents: Another issue of mismatch between the converter cells can arise from different dc-link capacitances. The employed capacitors in the dc links are usually electrolytic capacitors featuring a high energy density which is required to filter the power pulsation with twice the grid frequency, if not more advanced compensation techniques such as power pulsation buffers [13] are used. The electrolytic capacitors in the individual cells, however, might have different capacitance values either from the beginning due to manufacturing variance or after some time because of unequal aging processes which might lead to an uneven reduction of the capacitance values [14]. This difference in the dc-link capacitances can cause additional circulating currents between the ISOP-connected converter cells with the common-duty cycle control, which is analyzed in the following.

For the simplified case of only two converter cells with equal transformer turns ratios of $n = 1$ [cf., Fig. 5(a)], an equivalent circuit model can be derived [cf., Fig. 5(c)] for the analysis of the circulating currents that can occur with the common-duty cycle control. The output voltage is controlled to be a constant dc value which allows us to neglect the output capacitor in the analysis of the circulating ac currents. The ac–dc converter stages can be modeled as equal current sources, where only the ac component is of interest for the following analysis, which is

$$i_{\text{in,ac}} = \frac{P_{\text{sys}}}{V_{\text{DC}}} \cdot e^{j2\omega_g t} \tag{10}$$

under the assumption of negligible voltage ripples on the dc links. By applying the concept of superposition for the two current sources, the currents into the capacitors ($i_{c,1}$, $i_{c,2}$) and the ac components of the inductor currents ($i_{L,ac,1} = -i_{L,ac,2}$) can be found in dependence of the component impedance values, i.e.,

$$i_{c,1} = i_{\text{in,ac}} \cdot \frac{2 \cdot (Z_L + Z_{c,2})}{Z_{\text{tot}}} \tag{11}$$

$$i_{c,2} = i_{\text{in,ac}} \cdot \frac{2 \cdot (Z_L + Z_{c,1})}{Z_{\text{tot}}} \tag{12}$$

$$i_{L,ac,1} = i_{\text{in,ac}} \cdot \frac{Z_{c,1} - Z_{c,2}}{Z_{\text{tot}}} \tag{13}$$

with $Z_{c,1} = 1/(j2\omega_g C_1)$, $Z_{c,2} = 1/(j2\omega_g C_2)$, $Z_L = j2\omega_g L$, and $Z_{\text{tot}} = Z_{c,1} + Z_{c,2} + 2 \cdot Z_L$. The resulting voltage ripple on each capacitor can thus be calculated by

$$v_{c,i} = i_{c,i} \cdot Z_{c,i}. \tag{14}$$

As a result, the amplitude of the circulating current equals

$$\hat{i}_{L,\text{ac},1} = \frac{P_{\text{sys}}}{V_{\text{DC}}} \cdot \left| \frac{Z_{c,1} - Z_{c,2}}{Z_{\text{tot}}} \right|. \tag{15}$$

This analysis can be extended to ISOP systems with N_{cells} cells with the same methodology of superposition. For the case that only the first cell has a different dc-link capacitance value than the other cells ($Z_{c,1} \neq Z_{c,2} = \ldots = Z_{c,N} = Z_c$), the amplitude of the circulating current in the first cell can be derived as

$$\hat{i}_{L,\text{ac},1} = \frac{P_{\text{sys}}}{V_{\text{DC}}} \cdot \left| \frac{(N_{\text{cells}} - 1) \cdot (Z_{c,1} - Z_c)}{N_{\text{cells}} \cdot Z_L + (N_{\text{cells}} - 1) \cdot Z_{c,1} + Z_c} \right| \tag{16}$$

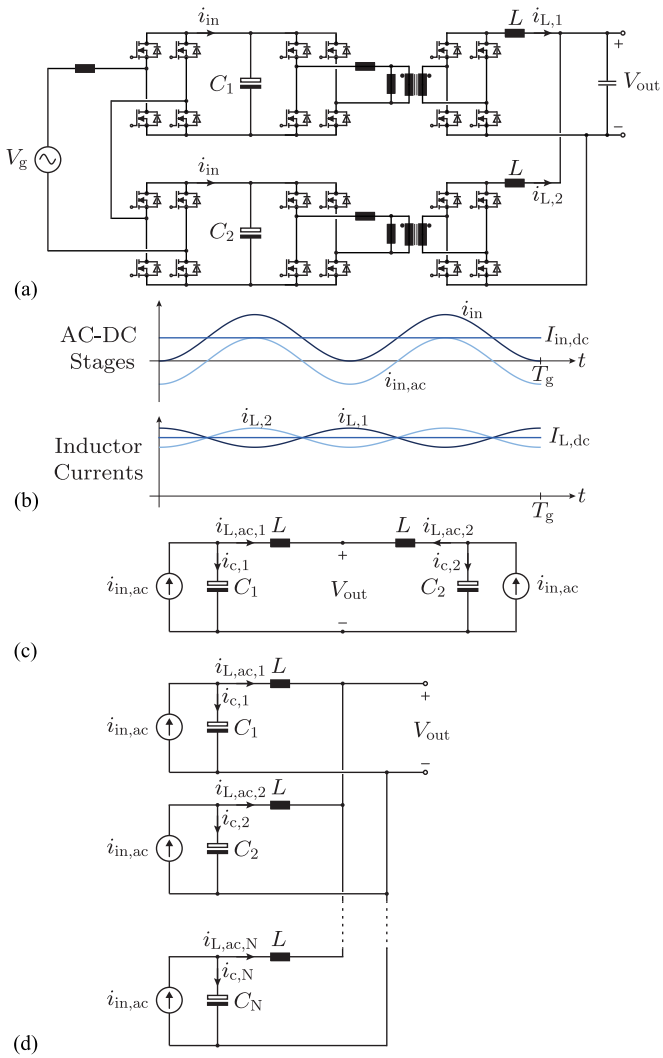

Fig. 5. Analysis of circulating currents in ISOP multicell systems with common-duty cycle control: (a) simplified ISOP ac–dc converter system with only two converter cells; (b) characteristic waveforms of the input currents and the circulating currents in the output inductors for the case where $C_1 > C_2$; (c) low-frequency ac-equivalent circuit of the two cell ISOP system. The ac–dc rectifier full bridges can be modeled as current sources where only the ac component is considered for the analysis of the circulating current. Since the output voltage is a controlled dc voltage, its capacitor can be regarded as an open circuit for the ac analysis; (d) generalized equivalent circuit with N_{cells} cells.

and in the remaining cells as

$$\hat{i}_{L,\text{ac},2} = \cdots = \hat{i}_{L,\text{ac},N} = \frac{\hat{i}_{L,\text{ac},1}}{(N_{\text{cells}} - 1)}. \tag{17}$$

Even though the circulating currents are not destabilizing the system operation, they are a source of additional conduction losses due to higher rms values of the currents conducted by the switches, transformers, and output inductors.

B. Active Balancing Control Schemes

In order to remedy the adverse effects associated with the mismatch in common-duty cycle control and to guarantee the

balanced operation, different active control strategies have been proposed for ISOP ac–dc converter systems [15]–[17]. The balancing of the dc-link voltages can be controlled either by the ac–dc rectifier stages (also termed cascaded H-bridges in [18]–[20]) and/or the isolated ISOP dc–dc converter stages, whereas the output current sharing is only controllable by the dc–dc stages where control concepts known from ISOP dc–dc conversion systems can be applied [21]–[24].

In [15], a voltage balancing control is presented which is based on modifying the common-duty cycle control (in dq-coordinates) for the ac–dc rectifier stages [17] in order to balance the dc-link voltages by allowing different duty cycles. Since this can only counteract limited power unbalances of the dc–dc converter stages, an additional power balancing control is also required for the dc–dc converters that are connected in parallel at their outputs.

In [16], the voltage of the dc links is balanced by operating the ac–dc rectifier stages with a mixture of low- and high-frequency PWM and the power transferred through the dc–dc converter stages is balanced by additional controllers. In the aforementioned methods, the voltage balancing is performed by a different stage than the power balancing.

In the selected control scheme, both the dc-link voltage balancing and the output current sharing are handled by the dc–dc converter stages, whereas the grid current is controlled by the ac–dc rectifier stages with a common-duty cycle control, as shown in Fig. 6. This control scheme contains a total dc-link voltage regulator on the rectifier side [cf., Fig. 6(a)] in order to obtain a constant total dc-link voltage (i.e., the sum of all dc-link voltages) with a superimposed 100 Hz ripple. The dc-link voltage regulator of the ac–dc rectifier stage consists of cascaded control loops where the outer control loop comprises a proportional-resonant voltage controller $G_{\mathrm{u},1}(s)$. This controller creates a current reference value $i_{\mathrm{g,ref}}$ of the input current by multiplying the controller output value (power reference value p^*) with the time-varying grid voltage value v_{grid} and a factor $k = 2/\hat{V}_{\mathrm{grid}}^2$. This current reference value is tracked by the inner proportional-integral (PI) current controller $G_{i,1}(s)$ which outputs the modulation index m that is given to all ac–dc stages.

Furthermore, the control scheme of the dc–dc converters contains a cascaded output voltage regulator [cf., Fig. 6(b)] consisting of the outer PI voltage controller $G_{\mathrm{u},2}(s)$, implemented on the master cell, and inner PI current controllers $G_{\mathrm{i},2}(s)$ which are implemented locally on each cell. By controlling the output current of each cell, circulating currents can be prevented. Since output current control alone is not leading to a stable operating of an ISOP system with balanced dc-link voltages [21], an additional dc-link voltage balancing control mechanism has to be implemented. For this reason, each cell also receives the value of the average dc-link voltage of all cells $V_{\mathrm{DC,ref}}$. Each cell can compare this value with its own dc-link voltage and based on that difference, the voltage controller $G_{\mathrm{u},2}(s)$ creates a current value i_{mod} which is added to $i_{\mathrm{out,ref}}$, the output of the voltage controller $G_{\mathrm{u},2}(s)$ of the master cell [21]. Thus, the system is driven back to the state where the output power and the total dc-link voltage are equally shared among the converter cells.

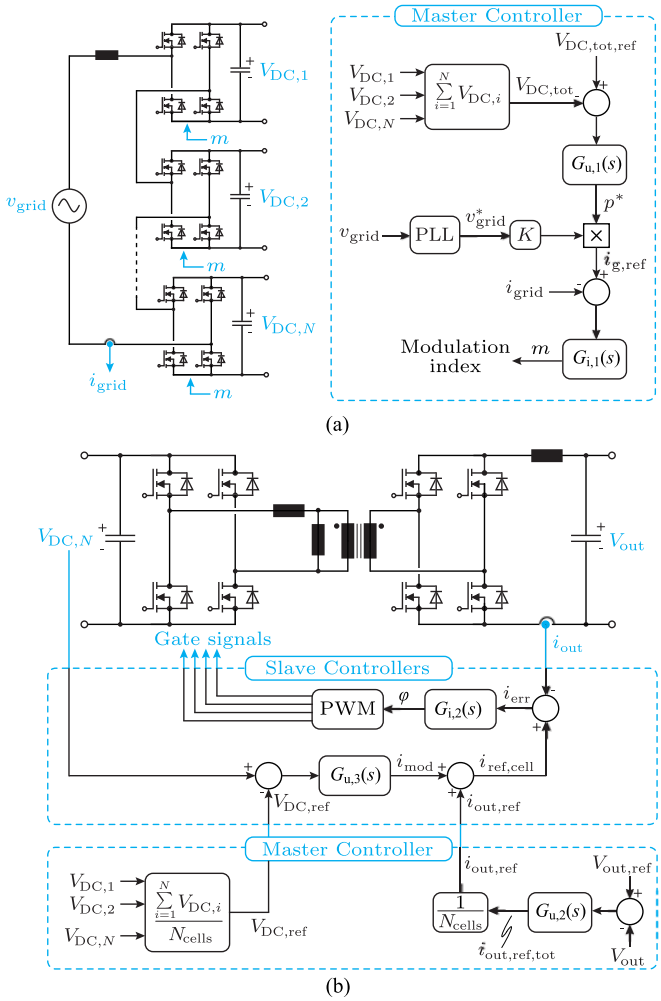

Fig. 6. Control implementation of the multicell telecom rectifier: (a) Total dc bus voltage controller and input current controller; (b) output current controller and dc-link voltage controller.

This control concept can be implemented as a master–slave control regime. The master cell measures the input current i_{grid}, the grid voltage v_{grid}, the output voltage V_{out}, and its own output current $i_{\mathrm{out},i}$. The slave cells, on the other hand, only need to measure their own dc-link voltage $V_{\mathrm{DC},i}$ and output current $i_{\mathrm{out},i}$. The slave cells transmit the value of the dc-link voltage $V_{\mathrm{DC},i}$ to the master cell and receive the modulation m index for the ac–dc stages, the output current reference value $i_{\mathrm{out,ref}}$ which they have to track, and the average value of the dc-link voltage of all cells $V_{\mathrm{DC,ref}}$.

IV. Converter Optimization

In order to identify the efficiency η versus power density ρ Pareto performance limit of the proposed multicell telecom power supply module (the full set of specifications can be found in Table II), a comprehensive converter optimization routine has to be performed. This routine takes all available degrees of freedom in the design of the converter into account, which constitutes the design space, and maps the design space into the performance space by means of a performance function, as

TABLE II
SPECIFICATIONS OF THE ISOP MULTICELL TELECOM RECTIFIER MODULE

Parameter	Variable	Value
Nominal grid voltage	$V_{\text{grid,RMS,nom}}$	230 V/50 Hz
Grid voltage range	$V_{\text{grid,RMS}}$	180–270 V
Rated output power	$P_{\text{sys,rat}}$	3.3 kW
Nominal output voltage	$V_{\text{out,nom}}$	48 V
Output voltage range	V_{out}	40–60 V
Hold-up time	T_{hold}	10 ms at rated power
Switching freq. per cell	f_{sw}	$\geq$ 18 kHz
EMI standards		CISPR Class A and B
Max. ambient temperature	T_{amb}	40 °C

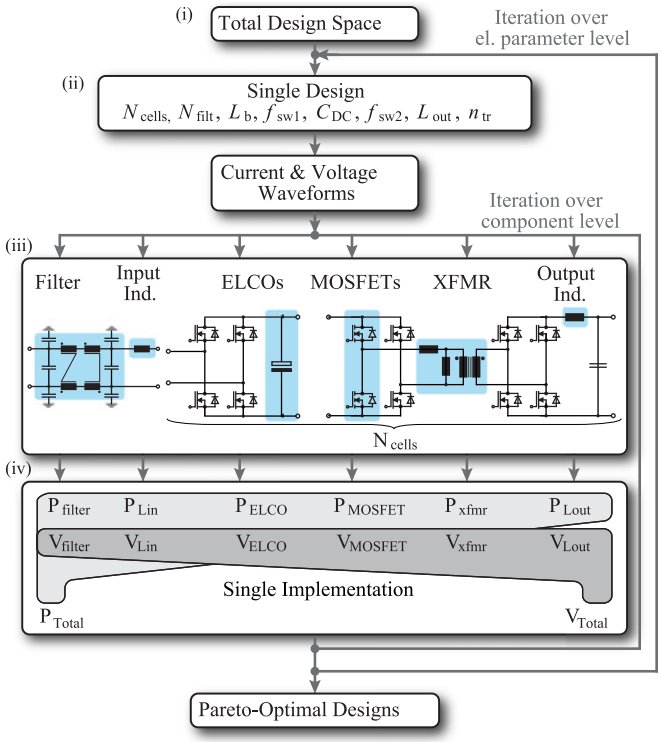

Fig. 7. Flowchart visualization of the η–ρ multiobjective optimization of the multicell telecom rectifier module.

visualized in Fig. 7. This allows us to compare all possible converter designs with respect to their efficiency and power-density [25], [26]. The performance function contains the converter behavioral models and analytical models of the losses and volumes of each type of component. The behavioral models allow to determine the conducted waveforms for each component at a given operating point, and thus to identify the electrical parameters of each component required for the loss and volume calculation, e.g., the rms values and peak values of voltages and currents and voltage–time areas seen by the components.

A. Design Space

The design space [cf., Fig. 7(i)] is comprised of different levels of available degrees of freedoms in the multicell converter design where the most basic level is the multicell topology itself, i.e., the interconnection of the converter cells such as ISOP, input-series output-series, input-parallel output-parallel, and input-parallel output-series (cf., [5]). In the case at hand, the ISOP structure is selected since it inherently provides a step-down voltage conversion ratio of $1/N_{\text{cells}}$, depending on the number of employed converter cells N_{cells}, as also utilized in [27] for a dc–dc power supply. As already mentioned, another benefit of the ISOP structure is that the input voltage and output current are already naturally balanced among the converter cells when operated with the same control parameters (cf., Section III) for the case of no mismatch between the cells.

The choice of the converter topologies for the ac–dc and the isolated dc–dc stages is an additional very basic level of degree of freedom. The selected topology of the ac–dc rectifier stages is a full-bridge rectifier operated with totem-pole modulation, which means that one bridge leg of the full bridge is operated with high frequency, whereas the other bridge leg is switched with line frequency. The totem-pole modulation reduces the high-frequency common-mode voltage spectrum compared to bipolar or unipolar modulation schemes [7], [28]. For the isolated dc–dc converters, a PSFB with a secondary side SR for higher efficiency is selected [29]. This topology has the advantage of an easy controllability with a single control parameter (i.e., phase shift value) and of a high efficiency due to ZVS where only a small circulating energy is required [30], [31]. The drawback of the PSFB converter is the overvoltage occurring at the secondary rectifier devices due to resonances between parasitic elements such that a snubber is required, as will be addressed later on. The *LLC* resonant converter [32] and the dual-active bridge converter (DAB) [33] have also been considered since they also allow to achieve high efficiencies over a wide power range. However, either they require unreasonable transformer designs (e.g., a leakage inductance in the same order of magnitude as the magnetizing inductance) for the specifications at hand in the case of the *LLC* converter or the control implementation for minimum conduction losses [34] mandates the employment of an FPGA on each cell with a high power consumption in the case of the DAB, which renders them unfeasible for the implementation in a multicell system. Furthermore, the system specification also requires a current and a voltage source characteristic of the power supply, which means it has to be able to control the output voltage and to limit the output current in case of a short circuit. This requirement is fulfilled by the PSFB converter.

The above mentioned basic levels of degrees of freedom are determined beforehand and are not part of the iteration in the optimization routine since this would lead to unreasonable computational and modeling efforts that are beyond the scope of this paper.

The next level of degrees of freedom is the abstract level of electrical parameters [cf., Fig. 7(ii)] which define a single converter design. The following is the most universal parameter.

1) *Number of converter cells N_{cells}:* With increasing number N_{cells}, the benefits of the scaling laws of [5] and Section II are leveraged to a larger extent. However, the communication overhead and the constant losses associated with each converter cell also increase. Thus, for the

optimization algorithm, the range for the number of cells is limited to $N_{\text{cells}} \in [3 \dots 10]$.

Additional electrical parameters that define a single converter design are associated with the ac–dc stages (including the EMI filter) and the isolated dc–dc converter stages.

2) AC–DC Rectifier Stages:

a) DC-link capacitance C_{DC}: The converter system and especially the energy stored by the dc-link capacitors have to be designed for the worst case operating point, which is given for the case of a grid outage during half a mains period (i.e., $T_{\text{hold}} = 10$ ms hold up time) when the system still has to supply the full amount of power to the load. This case inevitably leads to a voltage drop in the dc link, depending on the overall energy stored in the dc link. Thus, by specifying a maximum permissible drop of the dc-link voltage (i.e., $k_{\text{DC,drop}} \in [10\,\% \dots 40\,\%]$), the required capacitance value $C_{\text{DC,cell}}$ of the dc link in a cell can be determined as

$$C_{\text{DC,cell}} = \frac{2 \cdot N_{\text{cells}} \cdot P_{\text{sys,rat}} \cdot T_{\text{hold}}}{(2 - k_{\text{DC,drop}}) \cdot k_{\text{DC,drop}} \cdot V_{\text{DC}}^2}. \quad (18)$$

b) Switching frequency $f_{sw,1}$: The lower limit of the switching frequency of each cell is deduced from the audible frequency range and thus should not be lower than $f_{\text{sw,1}} \geq 18$ kHz. An upper boundary of the switching frequency is not inherently given; however, the CISPR EMI standards impose limits on the harmonics in the frequency range above $f_{\text{EMI}} = 150$ kHz [35]. Thus, an upper boundary of the switching frequency per cell can be derived as $f_{\text{sw,1}} < f_{\text{EMI}}/N_{\text{cells}}$, which allows to have the first harmonic below the EMI restricted frequency range.

c) Boost inductance L_b: The inductance of the boost inductor depends on the specified maximum allowable current ripple $\Delta i_{\text{b,max}}$ derived in (2) for a given number of cells and switching frequency. The maximum peak-to-peak current ripple is varied between $\Delta i_{\text{b,max}} \in [5\,\% \dots 30\,\%]$.

d) Input filter stages N_{filt}: The input filter, which is needed to suppress harmonics such that the EMI standards are fulfilled, can be designed with different numbers of stages $N_{\text{filt}} \in [1...3]$ and different filter component values

3) Isolated PSFB DC–DC Converters:

a) Switching frequency $f_{sw,2}$: The switching frequency is an important parameter for the design of the dc–dc converter as it influences the transformer design, the output inductor design, and also the losses in the MOSFETs (i.e., gate driver losses). The effective frequency at the output inductor is twice the switching frequency of the full-bridge rectification. The range of the switching frequency for the optimization is set to $f_{\text{sw,2}} \in [50 \dots] 300$ kHz.

b) Output inductance L_{out}: The required output inductance can be calculated for a defined switching frequency in dependence of the maximum peak-to-peak output current ripple, which is varied in the range of $\Delta I_{\text{out}} \in [5\,\% \dots 20\,\%]$.

c) Transformer turns ratio n_{tr}: The PSFB converter is a buck-type topology which is not able to boost the output voltage beyond $V_{\text{out}} = V_{\text{DC,cell}} \cdot n_{\text{tr}}$. Therefore, the minimum turns ratio is defined by the lowest dc-link voltage (during the hold-up time) and the maximum specified output voltage.

For a single converter design, there are still many available degrees of freedom on the component level, which are based on the various possibilities of how the physical components can be realized. Therefore, a Pareto front can be calculated for each component by sweeping through all possible combinations of a component implementation, as shown in Fig. 7(ii). Thus, the total Pareto front of a single converter design is obtained by combining the Pareto results of the individual components. The degrees of freedom in the component implementations are as follows:

1) *MOSFETs:* For MOSFETs, the technology (Si, GaN, or SiC) as well as the chip size can vary for a given voltage rating. For the optimization in this paper, Si is selected due to the broad availability of devices with different chip sizes. The chip size optimization allows to tradeoff conduction and switching losses and is performed in the range of $A_{\text{chip}} \in [5\ \text{mm}^2 \dots]\ 30\ \text{mm}^2$. Additionally, the junction temperature can also be varied ($T_{\text{j}} \in [70\ °\text{C} \dots 110\ °\text{C}]$) which enables the tradeoff between the heat sink volume and conduction losses (since the switching losses show a negligible temperature dependency).
2) *Magnetic components:* The magnetic components can be realized with a variety of different options. For the cores, all available E-cores and RM-cores of N87 and N97 ferrite material (TDK-Epcos) and AMCC cores of amorphous material 2605SA1 (Metglas) are considered. For the windings, litz wires with different wire diameters and strand numbers, solid round wire and foil winding are considered. Additionally, the winding number and the length of the air gap (in inductors) are further degrees of freedom.
3) *DC-link capacitors:* The required capacitance can be realized with different numbers of paralleled electrolytic capacitors. This allows to tradeoff the equivalent series resistance (ESR) related conduction losses with the leakage current losses.
4) *EMI filter:* For the EMI filter ring cores with T35 and T38 ferrite material (TDK-Epcos) with solid round wires are considered.

B. Mapping of Design Space Into Performance Space

In order to map the obtained design space with all possible implementations into the performance space, detailed component loss and volume models have to be applied to the aforementioned components.

1) MOSFETs: For performing a chip-size optimization, the conduction and switching losses of the MOSFETs have to be described in dependence of the chip size A_{chip}. For the ac–dc rectifier, the losses have to be calculated as an average value over a mains period. The conduction losses can be calculated with the rms current I_{RMS} of a MOSFET as

$$P_{\text{MOSFET,cond}}(T_{\text{jct}}, A_{\text{chip}}) = I_{\text{RMS}}^2 \cdot R_{\text{DS,on}}(T_{\text{jct}}, A_{\text{chip}}). \quad (19)$$

In the considered current range, the on-state resistance of the low-voltage MOSFETs is basically not dependent on the conducted current.

The switching losses of the MOSFETs of the ac–dc stage (the dc–dc converters are operated with ZVS) depend on the specific layout of the commutation loop (e.g., the parasitic loop inductance) and, thus, are difficult to precisely calculate. However, a fairly good approximation can be obtained by taking into account different loss mechanisms of the switching process, such as the stored charge in the parasitic drain–source capacitances Q_{oss}, the reverse recovery charge of the intrinsic body diodesQ_{rr}, and the gate drive losses in dependence of the chip size [36]. The energy lost in a hard switching transition of the ac–dc stages is at least

$$E_{\text{MOSFET,loss}} = V_{\text{DC}} \cdot (Q_{\text{oss}} + Q_{\text{rr}}) + V_{\text{gate}} \cdot Q_{\text{gate}}. \quad (20)$$

For the losses associated with the soft-switching transitions of the dc–dc stages, it is assumed that only gate driver losses occur and C_{oss}-related losses during ZVS [37] are not considered, as they are small for low-voltage Si MOSFETs. Since the hard- and soft-switching losses increase and the conduction losses decrease with larger chip size, an optimal value of the chip size leading to the lowest total losses can be found. The thermal resistance of the junction to the case is also influenced by the chip size. Thus, in the last step, the required heat sink can be calculated based on the total MOSFET losses and the specified junction temperature. By considering the cooling system performance index [38] of different types of heat sinks or by employing a more sophisticated cooling system design approach [39], the volume of a heat sink for a MOSFET can be calculated based on the required value of thermal resistance $R_{\text{Th,HS}}$. Since the PCB itself also functions as a heat spreader which helps to dissipate heat, there is no need for a heat sink if the required $R_{\text{Th,HS}}$ is below a certain threshold (e.g., 50 K/W for a board with a copper area of 6 cm^2 and copper thickness of 70 μm around the switch).

2) *Inductive components:* The losses of inductors and transformers can be divided into winding and core losses. The core losses (per unit volume) can be calculated for arbitrary waveforms of the flux with the improved generalized Steinmetz equation (iGSE) by

$$P_{c,\text{iGSE}} = k_i \cdot f_{\text{sw}} \cdot (\Delta B)^{\beta-\alpha} \cdot \int_0^{1/f_{\text{sw}}} \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} \mathrm{d}t \quad (21)$$

where ΔB is the local peak-to-peak flux density and

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} \, 2^{\beta-\alpha} \mathrm{d}\theta} \quad (22)$$

with α, β, and k being the material parameters. These can be deduced from data sheets of the manufacturer or by means of loss maps based on measurement values which also allow to incorporate dc offsets in the flux [40]. The winding losses consist of dc losses and ac current losses (skin and proximity effect), which can be calculated based on [41] and [42] for different winding types. For the calculation of the proximity losses, the external magnetic field strength on each conductor has to be known. This can be determined via one-dimensional (1-D) [43] or 2-D [44] modeling approaches or FEM simulations. A thermal impedance network [42] is applied to adequately model the heat transfer within an inductive component and to the ambience which also impacts the losses in both the core and the windings.

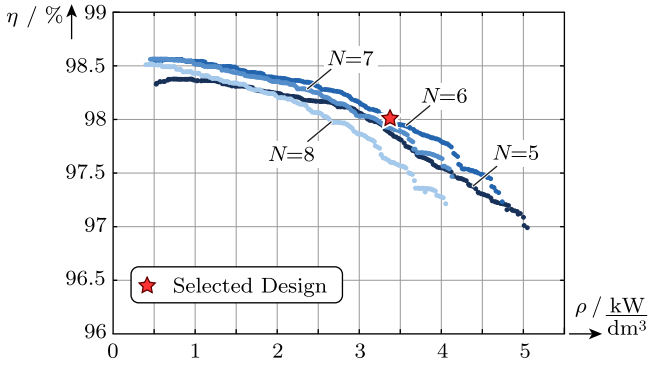

Fig. 8. Pareto-optimal (efficiency/power-density) designs of the multicell telecom power supply module for different numbers of converter cells and a drop of the dc-link voltage during the hold-up time of $k_{\text{DC,drop}} = 20\%$ for the operation at nominal voltages and $P_{\text{out}} = 80\% \cdot P_{\text{out,rat}}$.

3) *DC-link capacitors:* The electrolytic dc-link capacitors have to carry an rms current, which creates losses in connection with the ESR of the capacitors. Since the ESR is frequency dependent, the total losses are the sum of the losses at twice the fundamental frequency and at the switching frequency of the ac–dc stage. Furthermore, each capacitor exhibits a leakage current that has to be taken into account too. The total capacitor losses can be modeled in dependence of the number of paralleled capacitors n_{par} as

$$P_{\text{ELCO}} = \frac{(I_{\text{rms,100Hz}} \cdot R_{\text{ESR,100Hz}} + I_{\text{rms,fsw}} \cdot R_{\text{ESR,fsw}})}{n_{\text{par}}} + n_{\text{par}} \cdot V_{\text{DC,cell}} \cdot I_{\text{leak}}. \quad (23)$$

The volume of the capacitors in a single cell can be approximated with a fitting function, which was derived from more than 500 electrolytic capacitors of three different manufacturers (Panasonic, Rubycon, Epcos), in dependence of the required dc-link capacitance $C_{\text{DC,cell}}$ as

$$\mathrm{V}_{\text{ELCO}} = k_1 + k_2 \cdot C_{\text{DC,cell}} \cdot V_{\text{DC,cell}} + k_3 \cdot C_{\text{DC,cell}} \cdot V_{\text{DC,cell}}^2 \quad (24)$$

where $k_1 = 5.41 \cdot 10^{-7}$, $k_2 = 3.33 \cdot 10^{-5}$, and $k_3 = 5.5 \cdot 10^{-7}$ (all units are SI units).

4) *Input filter:* The volume of the input filter has been taken into the optimization by models which translate the required filter attenuation for different number of filter stages into component volumes [45].

5) *Auxiliary electronics:* For the losses attributed to auxiliary electronics (e.g., for a digital signal processor, voltage, and

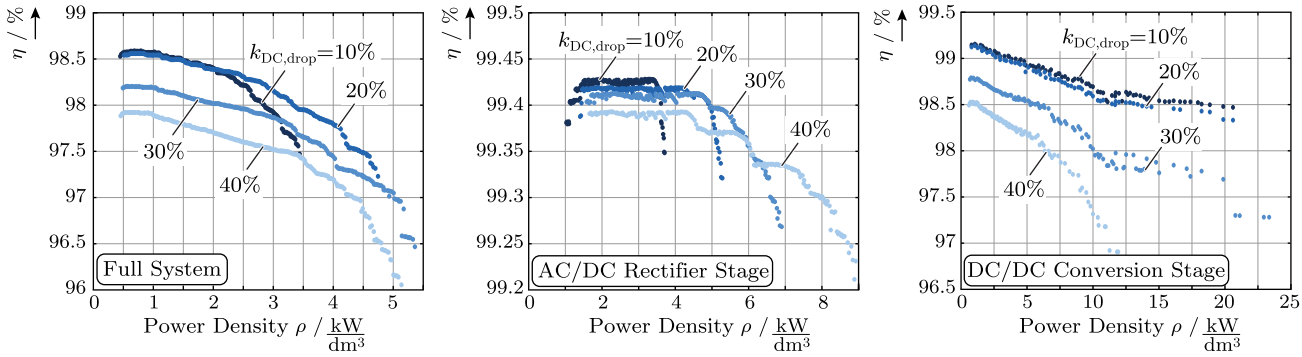

Fig. 9. Impact of different values of the maximum permissible drop of the dc-link voltage during the hold-up time on the achievable Pareto-optimal results of the entire system, the ac–dc rectifier stages and the dc–dc converter stages for $N = 6$ converter cells.

current sensing) on each slave converter cell constant losses of $P_{\text{slave,const}} = 800$ mW are estimated and for the master cell constant losses of $P_{\text{master,const}} = 2$ W are considered since this cell also has to operate the relay and additional sensors. It should be noted that the constant losses do not influence the choice of Pareto-optimal designs but only reduce the achievable efficiency of all designs.

C. Optimization Results

The η–ρ Pareto limits resulting from the optimization for the entire multicell converter system of Fig. 1(c) are depicted in Fig. 8 for the operation at $P_{\text{out}} = 80\% \cdot P_{\text{out,rat}}$ and nominal voltages for different numbers of converter cells and a maximum permissible drop of the dc-link voltage during the hold-up time of $k_{\text{DC,drop}} = 20\%$. It can be seen that the optimum number of converter cells is $N_{\text{opt}} = 6$ where a performance of $\eta = 98\%$ and $\rho = 3.3$ kW/dm^3 (calculated by summing up the boxed volumes of all components, i.e., not yet considering intermediate spaces between components of different shapes and sizes) can be achieved. In a real setup, the power density typically decreases by a factor of around $2/3$ compared to the calculation due to space between the components and other mechanical constraints.

An optimum value can also be found for the maximum permissible drop of the dc-link voltage during the hold-up time. In Fig. 9(a), the Pareto-optimal results are shown for the entire system for different values of $k_{\text{DC,drop}}$ for $N_{\text{cells}} = N_{\text{opt}} = 6$. The results are examined in greater detail in Fig. 9(b) and (c), which depicts the individual results for the ac–dc rectifier stage and the dc–dc conversion stage, respectively. Based on these results, an optimum value of $k_{\text{DC,drop,opt}} = 20\%$ can be deduced. The tradeoffs, leading to this optimal value, are described in the following.

1) AC–DC rectifiers: In the ac–dc rectifiers, the value of $k_{\text{DC,drop}}$ mainly influences the tradeoff between the losses and the size of the electrolytic dc-link capacitors. With a larger permissible voltage drop, lower capacitance values can be used within the cells. However, since the ESR of electrolytic capacitors increases with decreasing capacitance, the losses also increase.

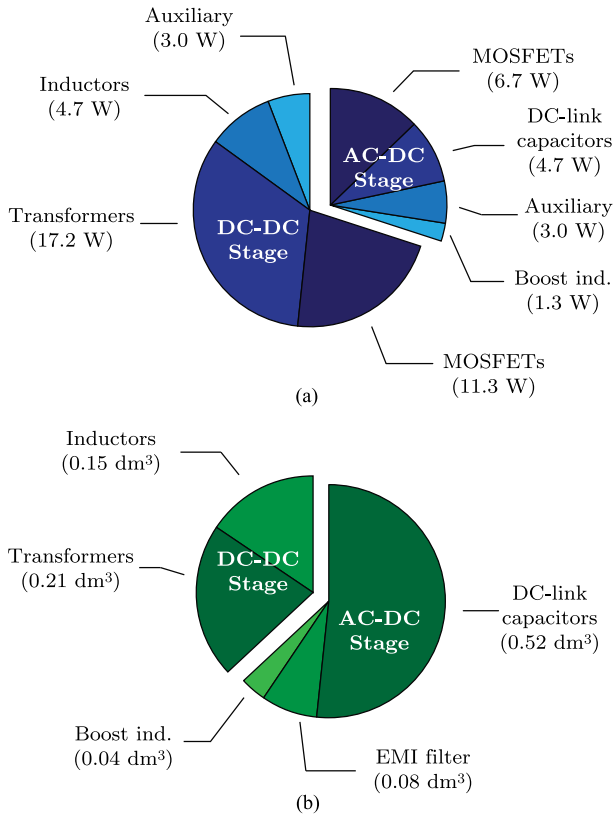

Fig. 10. (a) Breakdown of the losses and the (b) volume for the optimized converter design of the multicell telecom power supply module at $P_{\text{out}} = 80\% \cdot P_{\text{out,rat}}$ at nominal voltages for $N = 6$ converter cells.

2) DC–DC converters: The performance of the dc–dc converters deteriorates with larger values of $k_{\text{DC,drop}}$. This is due to the fact that the transformer turns ratio has to be adjusted according to the lowest dc-link voltage value. Thus, at the nominal operating point, a lower duty cycle of the dc–dc converter is required which results in larger rms current values in the transformer and the input full-bridge switches and, therefore, in higher losses if large values of $k_{\text{DC,drop}}$ are chosen.

In Fig. 10(a) and (b), a loss and volume breakdown, respectively, is provided for the selected design operating at $P_{\text{out}} = 80\% \cdot P_{\text{out,rat}}$ at nominal voltages. The main share of the

TABLE III
MAIN SYSTEM PARAMETERS OF THE SELECTED DESIGN FOR THE HARDWARE DEMONSTRATOR WITH $N = 6$ CONVERTER CELLS

AC–DC Rectifier	
Switching frequency	$f_{\text{sw,cell}} = 20$ kHz
Boost inductance	AMCC-4, 2605SA1, 25 μH, 7 turns
MOSFETs	2 × BSC040N10NS5G, 100 V, 4.0 mΩ
dc-link cap.	4 × Panasonic ECO-S1KA222CA, alum. elect., 80 V, 2.2 mF
EMI filter	3 stages, 2 × common mode chokes (EPCOS R40 cores T38, 10 turns), 3 × 680 nF
DC–DC Converter	
Switching frequency	$f_{\text{sw}} = 80$ kHz
Transformer	turns ratio 9:9, RM14, N97, EPCOS litz wire (420 × 71 μm)
Inductance	RM14LP, N97, EPCOS, 25 μH
Prim. MOSFETs	BSC040N10NS5G, 100 V, 4.0 mΩ
Sec. MOSFETs	BSC040N10NS5G, 100 V, 4.0 mΩ

(All values given per component of a cell, e.g., parallel MOSFETs, if not otherwise noted.)

losses is attributed to the dc–dc stages where the transformers and the output inductors account for half of the total converter losses. Regarding the volume distribution, it can be deduced that half of the total converter volume consists of dc-link capacitors. The second and third largest volume contributors are the transformers and output inductors, respectively, of the dc–dc converter stages. In summary, the converter losses and volume are dominated by the passive components, whereas the active components (i.e., semiconductors) contribute only around 30% of the losses and a negligible share of the overall volume due to an absence of heat sinks.

V. HARDWARE DEMONSTRATOR DESIGN

The design, which is selected for the hardware demonstrator with a calculated maximum efficiency of $\eta = 98\%$ at 80% of the rated output power and a power density of $\rho_{\text{calc}} = 3.3$ kW/dm^3, is marked in Fig. 8. The main system parameters of the selected design are listed in Table III and a picture of the assembled prototype is shown in Fig. 11. The hardware demonstrator features a volume of Vol = 30.4 cm · 4.5 cm · 11 cm= 1.504 dm^3 and, thus, an overall power density of $\rho_{\text{sys}} = 2.2$ kW/dm^3. This is in good agreement with the rule of thumb that the volume of the intermediate spaces between components amounts to around 30% of the total converter volume. The power density of the prototype is lower than the calculated value since the space between the components adversely affects the achievable power density and the volume of the PCB and the control boards have not been included in the calculations.

A. Phase-Shifted Full-Bridge Converter Design

As mentioned before, the PSFB converter with full-bridge SR is chosen for the isolated dc–dc converter stage since it allows to achieve a comparably high efficiency by operating the semiconductors under zero-voltage switching (ZVS) and still provides an easy way to control the power flow by means of the phase shift between the bridge legs on the primary side at a constant switching frequency. For a proper operation of

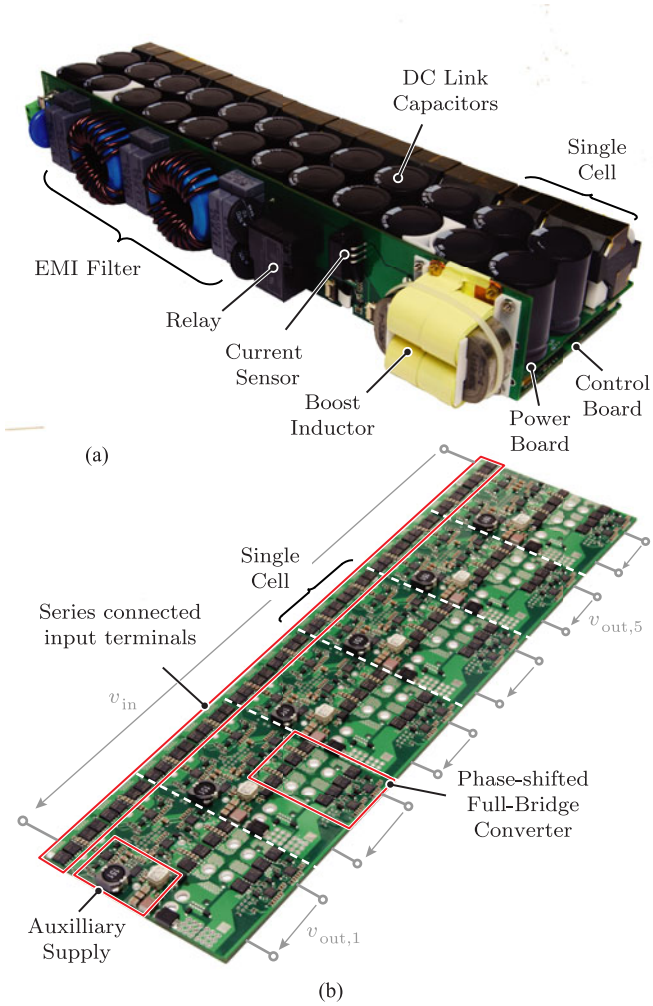

Fig. 11. Prototype of the multicell telecom rectifier with $N = 6$ converter cells according to the specification of Table III: (a) full system consisting of the power board, the control board, and the EMI filter board with the boost inductor. The power board is shown individually in (b) for a better visualization of the ISOP interconnection of the converter cells.

the converter, however, certain design guidelines have to be considered [46]. While ZVS can be achieved for the lagging leg of the primary full bridge easily by utilizing both, the energy stored in the output inductor and in the leakage inductor of the transformer, the operation of the leading leg with ZVS relies solely on the energy stored in the leakage inductance during the freewheeling phase

$$E_{\text{L}\sigma} = \frac{1}{2} L_\sigma \left(I_{\text{Load}} \cdot n_{\text{tr}} + I_{\text{mag}} \right)^2 . \tag{25}$$

This energy has to be sufficient to charge/discharge the parasitic output capacitances of the MOSFETs in the leading bridge leg. The energy analysis in [47] reveals that soft switching can only be achieved if the energy $E_{L\sigma}$ is larger than the energy which is fed back into the dc input voltage during discharge of the charge equivalent capacitance of a MOSFET, i.e.,

$$E_{C,\text{sw}} = C_{\text{oss},Q,\text{eq}} \cdot V_{\text{DC}}^2 = Q_{\text{oss}} \cdot V_{\text{DC}}. \tag{26}$$

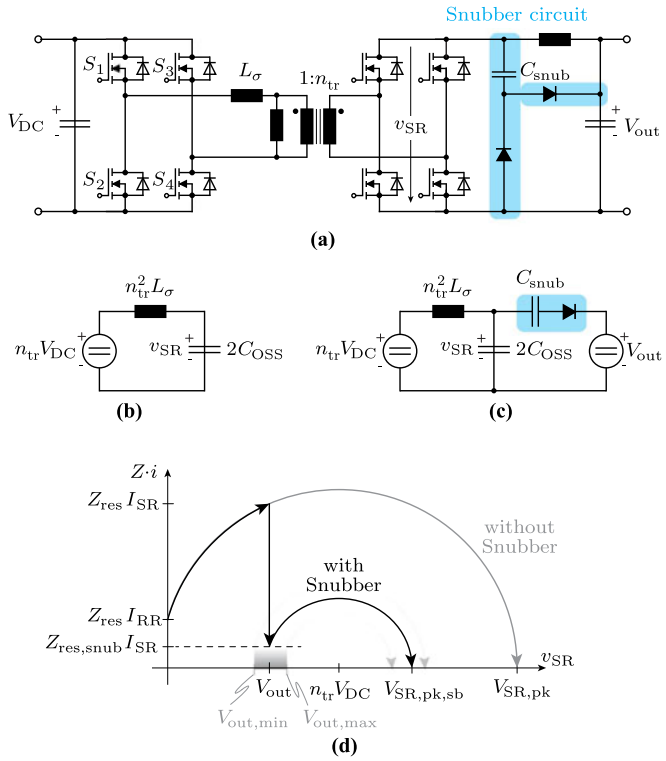

Fig. 12. Phase-shifted full-bridge converter with overvoltage limiting lossless snubber circuit [48] for the secondary rectifier MOSFETs: (a) application of the snubber circuit to the converter; (b) equivalent circuit of the resonant network for the case without snubber; (c) modified resonant network for the case with snubber elements; (d) comparison of the resonant trajectories for the cases with and without snubber elements and their resulting voltage peaks $V_{SR,pk,sb}$ and $V_{SR,pk}$, respectively.

In the prototype at hand, the leakage inductance of the transformer was selected to be $L_\sigma = 1\ \mu$H by adjusting the spacing between the primary and secondary winding. This allows us to achieve soft switching in the leading leg at levels of the output current above $I_{Load} \geq 3.4$ A (i.e., 30%) according to (25) and (26).

Increasing the leakage inductance even further in order to achieve soft switching for a broader range of load currents would introduce the drawback of a larger duty cycle loss caused by the time required to reverse the current in the leakage inductance from $(-I_{Load} \cdot n_{trafo})$ to $(+I_{Load} \cdot n_{trafo})$ or vice versa, and also to a larger ringing of the voltage at the SR MOSFETs (as described in the following paragraph), thus rendering it as an unpractical solution.

Another issue in the operation of the PSFB is the voltage ringing at the secondary rectifier MOSFETs after the freewheeling phase. The ringing is caused by the resonant circuit comprising the leakage inductance L_σ of the transformer and the parasitic capacitances of the rectifier MOSFETs $(2 \cdot C_{oss})$ since the voltage across the output rectifier is decoupled by the output inductor from the output voltage and therefore not clamped to a fixed voltage [cf., Fig. 12(b)]. The resonant frequency of this resonant circuit equals

$$\omega_{res} = 1/\sqrt{2C_{oss}L_\sigma n_{tr}^2} \tag{27}$$

and the characteristic impedance amounts to

$$Z_{res} = \sqrt{L_\sigma n_{tr}^2/(2C_{oss})}. \tag{28}$$

The voltage overshoot can reach the value of twice the transformed primary voltage $V_{SR,peak} = 2V_{sec} = 2n_{tr}V_{DC}$, as shown in Fig. 12(d). In the case at the hand, the dc bus voltage in each cell equals $V_{DC} = V_{DC,tot}/N_{cells} = 400$ V/6 $= 66$ V and with a transformer turns ratio of $n_{tr} = 1$, the voltage spike would reach around $V_{SR,peak} = 133$ V that would lead to the destruction of the SR MOSFETs with a voltage rating of $V_{DS,max} = 100$ V. Since the diodes in the rectifier MOSFETs are prone to reverse recovery effects, the voltage spike increases depending on the peak reverse recovery current I_{RR} and can be calculated as

$$V_{SR,pk} = V_{DC}n_{tr} + \sqrt{(V_{DC}n_{tr})^2 + (Z_{res}I_{RR})^2}. \tag{29}$$

In order to limit the voltage spike, a loss-less snubber circuit consisting of a snubber capacitor C_{Snub} and two diodes is added to the converter [48]. By introducing the snubber, the equivalent circuit of the resonant network changes as shown in Fig. 12(c) and the resonant frequency becomes

$$f_{res,snub} = 1/\sqrt{L_\sigma n_{tr}^2(2C_{oss} + C_{snub})} \tag{30}$$

while the resonant impedance becomes

$$Z_{res,snub} = \sqrt{L_\sigma n_{tr}^2/(2C_{oss} + C_{snub})} \tag{31}$$

after the voltage v_{SR} exceeds the level of the output voltage V_{out}. This is also depicted in Fig. 12(d) where the sudden change of the resonant impedance leads to a drop in the $v_{SR} - Z \cdot i$ plane. The maximum voltage spike can then be derived as a function of the output voltage to be

$$V_{SR,pk,sb} = V_{DC}n_{tr} + \sqrt{(V_{DC}n_{tr} - V_{out})^2 + (Z_{res,snub}I_{SR})^2} \tag{32}$$

where the value of I_{SR} can be found through geometrical considerations in the v-Zi plane as

$$I_{SR} = \sqrt{R^2 - (V_{DC}n_{tr} - V_{out})^2} \tag{33}$$

with $R = \sqrt{I_{RR}^2 + (V_{DC}n_{tr})}$. The value of the overvoltage depends on the output voltage V_{out} in which the worst case situation is obtained for low output voltages, as indicated in Fig. 12(d). The snubber capacitor is chosen to have a value of $C_{Snub} =$ 14 nF which limits the worst case voltage spike at the lowest output voltage of $V_{out,min} = 40$ V to $V_{SR,peak,snub} = 92$ V without considering the influence of the reverse recovery current. For the material of the ceramic snubber capacitors, the C0G (NP0) dielectric is chosen since it provides a stable capacitance value under varying temperature and voltage. In order to minimize the reverse recovery currents of the diodes, the conduction time of the diodes in the SR MOSFETs is kept to a minimum (around 10 ns) by adjustments of the timings of the gate signals [49].

Please note that the snubber capacitor also adversely affects (i.e., reduces) the current in the transformer leakage inductance during the freewheeling phase of the primary full bridge (cf., Fig. 13), which is required for soft switching of the lagging leg. In order to change from the active phase into the freewheeling

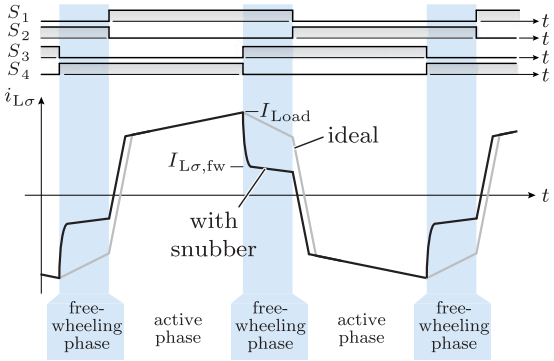

Fig. 13. Effect of a large snubber capacitor on the freewheeling current of the transformer leakage inductance.

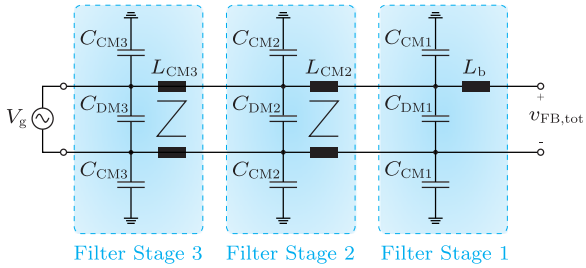

Fig. 14. Schematic of the employed three-stage common-mode and differential-mode EMI filter.

phase, the snubber capacitor C_{snub} has to be completely discharged. During the discharging process, which is dependent on the output current of the converter, the voltage of the snubber capacitor is opposing the leakage inductance and reducing its current level. In case the snubber capacitor is significantly larger than the parasitic capacitances of the employed primary and secondary MOSFETs (e.g., factor of 10), the current value of the leakage inductance after the transition from the active phase into the freewheeling phase can be approximated as

$$I_{L\sigma,\text{FW}} = n_{\text{tr}} \cdot \left(I_{\text{Load}} - V_{\text{DC}} \cdot \sqrt{\frac{C_{\text{snub}}}{L_\sigma}} \right) + I_{\text{mag}} \tag{34}$$

by considerations of the differential equations of the resonant network of L_σ and C_{snub} with an impressed output current I_{Load} of the output inductor. The energy in the leakage inductance, which is available for soft switching of the lagging leg, is then reduced to

$$E_{L\sigma} = \frac{1}{2} L_\sigma I_{L\sigma,\text{FW}} \tag{35}$$

which is lower than the value given for the ideal case of (25). This requires either to increase the leakage inductance value to obtain soft switching at the desired output power level or to take the additional losses resulting from incomplete soft switching into account based on [47].

B. EMI Filter Design

For the design of the EMI filter, the influences of the differential-mode and the common-mode noise have to be considered. The filter design can be performed individually for the common-mode and the differential-mode noise if the required attenuation for each case is calculated with a margin of around 16 dB to the limits, i.e., 6 dB for the worst case addition of the two noise signals and 10 dB to account for component tolerances.

In order to calculate the required attenuation for the differential-mode noise, the first harmonic that falls into the EMI constrained spectrum ($f_{\text{EMI}} \geq 150$ kHz) is considered, since the amplitude of the harmonic spectrum of square wave voltage decreases with -20 dB per frequency decade, whereas the filter attenuation increases with $-40 \cdot n_{\text{filt}}$ dB/dec with n_{filt} being the number of filter stages. For the case at hand, the first harmonic in the constrained frequency range is at twice the effective switching frequency $f_{\text{sw,eff}} = 120$ kHz of the interleaved ac–dc stages, i.e., $f_{\text{filt}} = 240$ kHz. The compliance with EMI standards is evaluated by determining the quasi-peak emission levels of the converter. The quasi-peak voltage of the harmonic at $f_{\text{filt}} = 240$ kHz is calculated by considering a 9 kHz band around that harmonic and by synthesizing a time-domain signal which is fed into the nonlinear quasi-peak detection network [9]. This results in a quasi-peak noise voltage of the converter at $f_{\text{filt}} = 240$ kHz of $V_{\text{filt,qp}} = 17.2$ V and/or a required attenuation of 92.8 dB including the margin previously mentioned. Following the filter volume optimization guidelines presented in [45], the number of filter stages for a minimum volume can be found at $n_{\text{filt}} = 3$, as shown in Fig. 14. The maximum value of the total differential mode capacitance is limited by the maximum allowable reactive power consumption of the filter. The limit was set such that a power factor of $\cos\phi = 0.9$ can be reached above 10% of the nominal power. This leads to a total differential mode capacitance of $C_{\text{DM,tot}} = 2\ \mu$F, which means each differential mode capacitance amounts to $C_{\text{DM}} = 660$ nF. This results in differential mode inductances of $L_{\text{DM}} = 18\ \mu$H in order to achieve the required attenuation in combination with the boost inductor L_{b}.

The precise modeling of the common-mode noise is challenging since it requires the exact knowledge of the stray capacitances of all electric nodes in the converter cells to the ground. Since this is practically impossible to determine for multicell converter systems, an approach as presented in [50] was followed that deduces an equivalent circuit for the common-mode noise. By applying a worst case approximation and neglecting small capacitances compared to larger ones, it can be found that due to the nature of the series connection of the converter inputs the measured common-mode voltage at the line impedance stabilization network (LISN) depends on which cell of the series stack is switching. So, for example, each time the lowest cell of the series stack switches, all upper cells are also moved with respect to their potential to ground. Since the cells are operated interleaved, the common-mode voltage resembles a staircase-like voltage waveform with the levels being

$$v_{\text{CM}}(i) = \frac{N_{\text{cells}} - i}{N_{\text{cells}}} \cdot V_{\text{DC}} \tag{36}$$

for $i \in [1, N_{\text{cells}}]$, where $i = 1$ means that the lowest cell of the stack is switched and $i = N_{\text{cells}}$ means the uppermost cell is

switched. Based on that voltage waveform, the quasi-peak voltage spectrum can be derived by means of simulations and the required common-mode filter attenuation can be determined to be 78 dB. The maximum allowable total common-mode filter capacitance is limited by the maximum total leakage current to earth (e.g., 3.5 mA rms), which leads to $C_{\mathrm{CM,tot}} = 36$ nF, and thus, the value for each common-mode capacitor is selected as $C_{\mathrm{CM}} = 4.7$ nF. Usually, the smallest common-mode filter volume is obtained by utilizing the maximum allowable amount of common-mode filter capacitance [51]. As a result, the common-mode inductances can be determined to be $L_{\mathrm{CM}} = 1.6$ mH. In the prototype, the leakage inductances of the common-mode chokes are utilized as differential-mode filter inductances.

VI. Measurement Results

In order to validate the operation of the multicell system and the result of the optimization routine, different measurements of the hardware demonstrator are shown in this section.

In Fig. 15, the measured waveforms of the converter input voltage $v_{\mathrm{FB,tot}}$ and the boost inductor current i_{b} are shown for different output power levels (i.e., $P_{\mathrm{out}} = 1.5$ kW and $P_{\mathrm{out}} = 2.5$ kW). The converter input voltage $v_{\mathrm{FB,tot}}$ exhibits multiple voltage levels, as was described in Section II. The boost inductor current i_{b} exhibits a sinusoidal shape in phase with the input voltage.

The proper operation of the overvoltage snubber (cf., Fig. 12) for the SR MOSFETs of the phase-shifted full-bridge dc–dc converters is demonstrated in Fig. 16 for nominal operating voltages. The selected snubber design allows to suppress the voltage overshoot to values below the rated drain–source voltage of $V_{\mathrm{DS,max}} = 100$ V. Since the MOSFETs are avalanche-rated, a short spike of voltage overshoot above the rated drain–source voltage will not lead to a destruction of the device but will introduce additional losses.

The conversion efficiency of the entire system has been measured with a single-phase grid emulator (SW 5250A/ELGAR), a high-precision power analyzer (WT3000/Yokogawa) and resistive loads. The measurement results for the full multicell system are depicted in Fig. 17 for different output power levels P_{out}. The measurement results include all losses associated with the system, i.e., also control losses, and the peak efficiency of $\eta_{\mathrm{max}} = 97.7\%$ is reached at an output power level of around $P_{\mathrm{out}} = 2.25$ kW. The measured power factor at nominal output power and nominal input voltage is $\lambda = 99.8\%$ and the THD of the input current is $\mathrm{THD_I} = 4.6\%$.

For a more detailed analysis, the efficiency of the dc–dc stage has also been measured independently. Based on this result and the efficiency characteristic of the entire system, the efficiency of the ac–dc stage (including the EMI filter) is calculated. The measurement results of the dc–dc stage and the calculated efficiency curve of the ac–dc stage are shown in Fig. 17.

The main deviations between the measured and the calculated efficiency (cf., Section IV-C) arise from nonidealities in the hardware setup that have not been considered in the optimization:

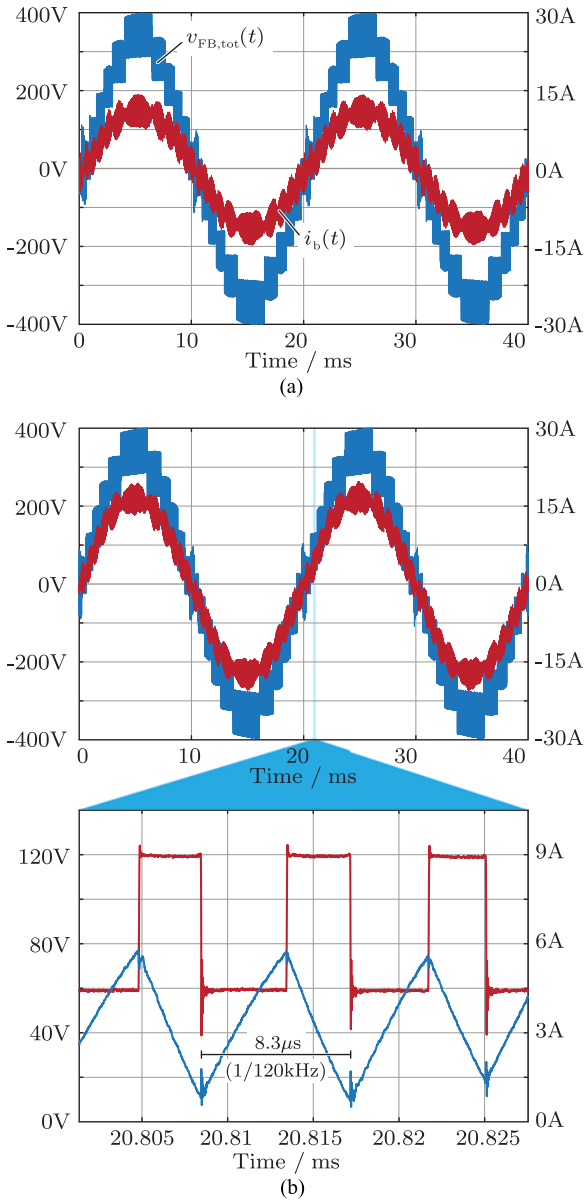

Fig. 15. Measured waveforms of the operation of the ac–dc stages of the multicell telecom rectifier with a grid voltage of $V_{g,\mathrm{RMS}} = 230$ V: (a) measurement of the converter input voltage $v_{\mathrm{FB,tot}}$ and the boost inductor current i_{b} for an output power of $P_{\mathrm{out}} = 1.5$ kW and (b) for an output power of $P_{\mathrm{out}} = 2.5$ kW with an enlarged view of some switching periods showing the effective switching frequency of $f_{\mathrm{sw,eff}} = 120$ kHz.

1) PCB losses: Even though the PCB containing the power electronic components and the EMI filter board are manufactured with a copper thickness of $d_{\mathrm{Cu}} = 70$ μm, additional conduction losses are generated. At the operating point of $P_{\mathrm{out}} = 2.25$ kW, these losses are estimated based on the converter layout to amount to almost $P_{\mathrm{PCB}} = 5$ W for the entire converter. This yields to a drop of the efficiency of around $\Delta\eta = -0.2\%$.
2) Thermal coupling: Due to the dense layout of the power stage, the components are no longer thermally decoupled. This means, that, e.g., the inductive components are transferring heat to the MOSFETs that leads to a junction

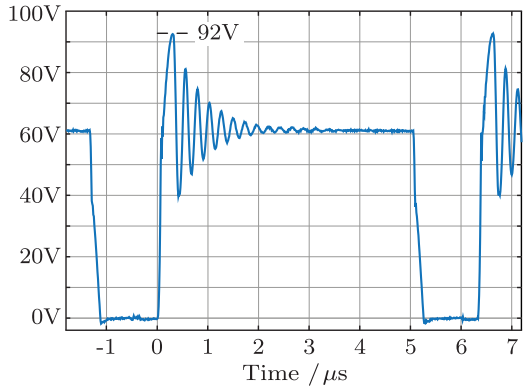

Fig. 16. Measurement of the voltage v_{SR} across the SR MOSFETs of the dc–dc converter stage for an output voltage of $V_{out} = 48$ V and an output power of $P_{out} = 2.5$ kW. The employed snubber is capable of limiting the voltage ringing to values below the maximum blocking voltage of $V_{DS,max} = 100$ V.

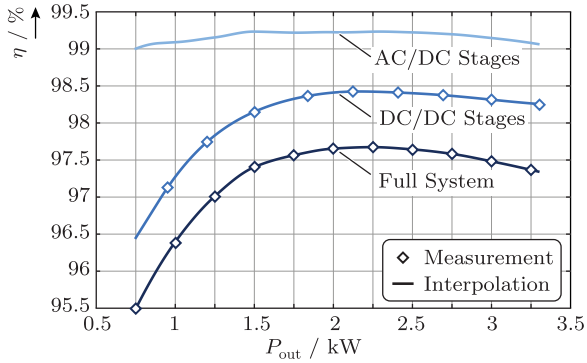

Fig. 17. Measurement of the conversion efficiency of the multicell telecom rectifier. The efficiency of the full system and the efficiency of the dc–dc stages have been measured with a power analyzer. Based on these measurements, the efficiency of the ac–dc stages was derived.

temperature which is larger than calculated. Since the $R_{DS,on}$ of the silicon MOSFETs is strongly dependent on the junction temperature, larger MOSFET conduction losses are created. An increase of the junction temperature, e.g., from $T_j = 80$ to 100 °C effects an increase of the $R_{DS,on}$ of around 15%.

3) Magnetic coupling: The close vicinity of the inductive components and the electrolytic capacitors as well as the PCB creates eddy currents in the capacitors and the PCB, which are induced by the stray fields of the inductive components. The precise dimension of this effect is difficult to quantify, though.
4) MOSFET switching losses: For the calculation of the switching losses, the parasitic capacitances of the PCB traces of the switch node have not been considered, which also contribute a small amount of losses. Furthermore, the dead time of the switches has been assumed to be ideal such that the conduction interval of the internal body diode of the MOSFETs is negligible.
5) Control, communication, and auxiliary electronics: The amount of losses attributed to control and auxiliary electronics (e.g., damping resistors of the EMI filter and power relay) has only been estimated by a fixed value of losses and thus leads to an additional deviation between the calculation and the measurements.

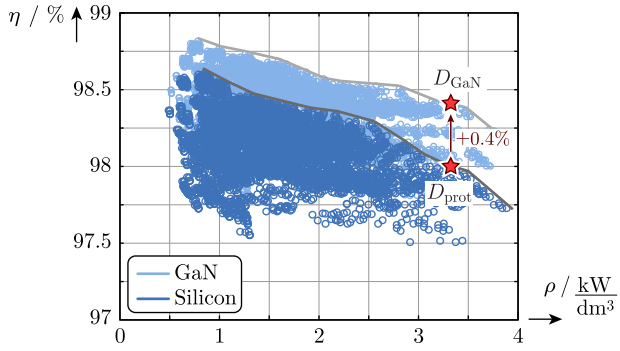

Fig. 18. Possible performance improvements by shifting from Si to GaN semiconductors as a result of η–ρ Pareto optimization. The efficiency of the prototype design D_{prot} can be increased by $\Delta\eta = +0.4\%$.

Since the exact layout of the components and the precise design of the converter are typically not known at the step of the optimization, it is very difficult to include the above-mentioned loss contributions in a meaningful way in the optimization.

A. Challenges in the Operation of Multicell Converters

Apart from the challenges in the design of the PSFB converter, such as the load current dependent ZVS range and the voltage ringing at the SR MOSFETs, additional issues have occurred during the commissioning of the hardware demonstrator.

1) *Common-Mode Currents:* As already mentioned in Section V-B and [5], the series connection of cells leads to increased common-mode currents since the potentials of the cells with reference to ground exhibit step changes every time any other cell in the stack below changes its switching state. The change of the potential drives a current through all parasitic common-mode capacitances, which includes the capacitances of the signal isolators, too. It was found that these currents disturb the SPI communication between the master and the slaves cells if not properly attenuated by common-mode chokes on the signal lines. Since a safe and faultless communication between the master and slaves is vital for the operation of the entire system, a CRC check is implemented in order to verify that the data transmission is not corrupted. Further methods of suppressing the common-mode currents suggest the application of common-mode chokes at the input terminals of each cells [52].
2) *System startup:* Due to the boost character of the ac–dc stages, the dc links are charged via a precharging circuit as soon as the converter is connected to the grid. Directly after the connection to the grid, the dc–dc stages are not operated, which means that the system can be regarded as a stack of series-connected capacitors and does not possess the natural balancing capability at this point which is inherent to ISOP systems. This requires some methods of balancing the voltages of the dc-link capacitors until the system is in normal operation.

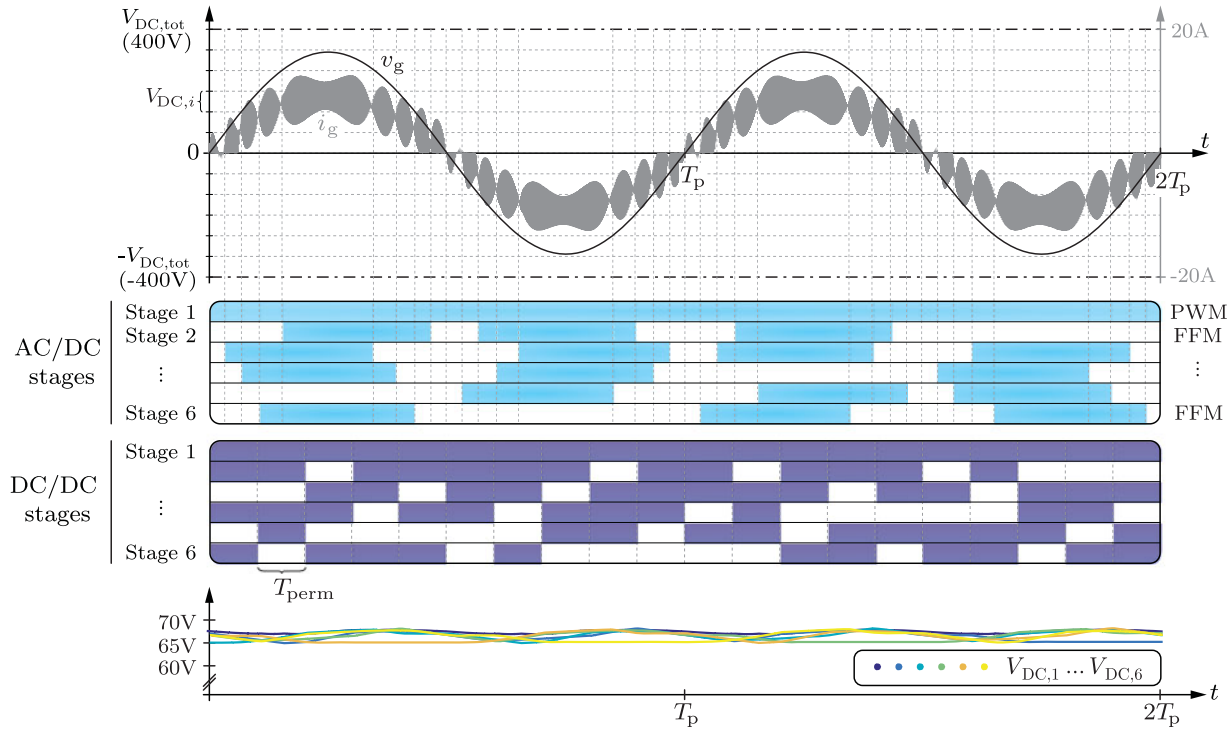

Fig. 19. Simulation results of the 4D-interleaving modulation of the ISOP multicell telecom rectifier system with $N = 6$ at the operating point of $P_{out} = 1.5$ kW. At the input side, only one ac–dc stage (Stage 1) is modulated with PWM, while the remaining five stages are operated with FFM. At the selected power level of $P_{out} = 1.5$ kW, the most efficient operation of the dc–dc stages is achieved with $N_{p,op} = 4$ active dc–dc stages. The balancing algorithm selects the active ac–dc and dc–dc stages based on the dc-link voltages of the cells. The permutation time interval for the dc–dc stages is chosen as $T_{perm} = 2$ ms.

3) *Reliability:* A common argument, which is often raised in the context of multicell converters, addresses the reliability of the entire system. As the system is constructed of several converter cells, the total number of employed components is increased compared to an equivalent single-stage converter system. This increases the probability of a failure of a component. However, in contrast to the single converter system, the failure of a single component is not necessarily leading to a failure of the entire multicell system since only one cell is affected. Depending on the operation of the multicell system, it might still be functional at a reduced power and/or voltage level. This might requires that the failed cell goes into a predefined state in case of failure, i.e., open- or short-circuit state. It, furthermore, has to notify the master cell about the occurrence of the failure such that the control loops in the master cell can be adapted to the new number of active cells.
The simplest and most effective way to increase the reliability of the multicell system is achieved by introducing redundancy by means of additional standby cells [53]. For an assumed failure in time (1FIT $= 1/10^9$ h) rate λ_{cell} of a single converter cell, the mean time to failure ($MTTF_{sys}$) for the entire system with N_{cells} can be derived as

$$\mathrm{MTTF}_{sys} = \frac{1}{N_{cells}\lambda_{cell}}. \tag{37}$$

The addition of k_{red} redundant cells allows us to achieve a redundancy, where the system is operational as long as at least N_{cells} cells are functional out of $N_{cells} + k_{red}$ total cells [54]. For the case that the redundant cells are just in standby, the total system MTTF has increased to

$$\mathrm{MTTF}_{sys} = \frac{k_{red} + 1}{N_{cells}\lambda_{cells}}. \tag{38}$$

The additional cost to achieve redundancy is only a fraction of the entire system cost, whereas a single converter system doubles in cost if it is made redundant.

VII. Future Performance Improvements

The multicell telecom power supply offers different paths for future performance improvements. This can either be achieved on the hardware level by shifting toward wide-bandgap semiconductors or on the software level by operating the system with a sophisticated 4D-interleaving control concept.

A. GaN Implementation

The superior figure-of-merit (FOM $= 1/\sqrt{R_{DS,on}C_{oss}}$ [4]) of GaN high-electron mobility transitors (HEMTs) compared to Si MOSFETs allows us to push the performance of the multicell system to higher levels. A multiobjective optimization (cf., Section IV) with GaN HEMTs (based on the $V_{DS} = 100$ V devices of EPC) reveals the achievable performance gain obtained by the shift toward wide-bandgap semiconductors. The optimization results are shown in Fig. 18 and indicate that the performance of the design of the prototype system D_{prot} can be increased by $\Delta\eta = +\ 0.4\%$ (D_{GaN}) without altering the power density.

B. 4D Interleaving

The multicell structure in combination with the time-varying value of the input voltage and the actual load current level, which can be lower than the rated output power, offer a new degree of freedom in the control of the system that can be leveraged in order to improve the performance of the entire system [55]. The 4D-interleaving modulation concept is based on a time-varying activation/deactivation of individual ac–dc rectifier stages and dc–dc converter stages of different cells. This operating concept utilizes the decoupling of the ac–dc and dc–dc stages provided by the dc-link capacitors. As a result, a very flat efficiency versus output power characteristic can be obtained for the parallel-connected dc–dc converter stages by operating only an optimum number of dc–dc converters depending on the output power level. Additionally, a smaller and more efficient rectifier input stage (losses: -17%, volume: -10%) can be designed for the operation of only one ac–dc rectifier stage with PWM and the remaining rectifier stages with fundamental frequency modulation (FFM). This leads to an efficiency increase of the entire system of around $\Delta\eta = +0.1\%$. In order to balance the dc-link voltages over a certain time period, a permutation of the active ac–dc and dc–dc stages can be implemented, as verified by simulation results in Fig. 19 for an output power level of $P_{\text{out}} = 1.5$ kW.

VIII. Summary and Conclusion

In this paper, a new approach toward a highly efficient and very compact single-phase telecom rectifier module is presented. The system is based on the multicell converter approach with series connection of the cells at the input and parallel connection of the cells at the output (ISOP). Each converter cell employs an ac–dc converter stage that consists of a full-bridge and an isolated dc–dc converter comprising a phase-shifted full-bridge converter.

Based on fundamental scaling laws, the benefits of a multicell converter system are derived in comparison to a single-cell ac–dc converter system. As a result from the increased effective switching frequency and the multilevel voltage waveform due to the interleaving of the series-connected ac–dc stages, the ripple of the boost inductor current is greatly reduced and a cancelation of harmonics occurs.

The degrees of freedom in the design procedure of the multicell telecom power supply module in ISOP configuration are outlined. Based on the degrees of freedom in the converter design, a multiobjective optimization is performed, which allows to map each converter's design into the performance space by use of analytical component loss and volume models. The optimization results show that a converter design with an efficiency of $\eta = 98\%$ and a power density of $\rho = 3.3$ kW/dm^3 can be achieved. The results also reveal an optimum value of $N = 6$ for the number of converter cells and an optimum maximum permissible drop of 20% the dc-link voltage during the hold-up time.

In order to validate the theoretical aspects of the multicell converter operation and the optimization results, a prototype system is designed and built up. Different critical design aspects such as the ZVS conditions and the snubber design of the dc–dc converter stage are analyzed in detail. The measurements results with a maximum efficiency of $\eta_{\max} = 97.7\%$ and a power density of $\rho = 2.2$ kW/dm^3 confirm the optimization results and show that this converter concept can achieve a very high conversion efficiency. The deviations between the measured and the calculated values originate from difficult-to-quantify loss contributions regarding the efficiency calculation and from intermediate spaces between components regarding the power density calculation. Additionally, several pitfalls and challenges in the operation and commissioning of the converter are highlighted.

Considering the increasing importance of high-efficiency telecom power supplies, the multicell converter approach offers an interesting path toward highly efficient and compact power supplies with future performance improvements provided by the shift toward wide-bandgap semiconductors and the implementation of an advanced 4D-interleaving control concept.

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