

Design and Experimental Testing of a Resonant DC–DC Converter for Solid-State Transformers

Gabriel Ortiz, *Member, IEEE*, Michael Georg Leibl, *Member, IEEE*, Jonas Emanuel Huber, *Student Member, IEEE*, and Johann Walter Kolar, *Fellow, IEEE*

Abstract—In the solid-state transformer (SST) concept, the key task of voltage adaptation and isolation is performed by a high-power dc–dc converter, which is operated in the medium-frequency range, hence enabling a reduction in size and weight of the converter’s reactive components. This dc–dc converter presents the main challenge in the implementation of the SST concept, given its operation at medium frequency together with the direct connection to medium voltage. This combination demands the utilization of dc–dc converter topologies that are able to operate in the soft-switching mode, whereby, given that typically insulated-gate bipolar transistor switches are used as power devices, zero-current switching modulation schemes become highly attractive and often mandatory in order to achieve the targeted efficiency goals. This paper describes in detail the analysis and design of a 166-kW/20-kHz dc–dc converter of the series-resonant type, which results to be particularly interesting for high-power applications, given its tight input-to-output transfer characteristics and its capability to ensure soft-switching transitions of all semiconductor devices. The main focus of this paper is to describe in detail the practical implementation of the aforementioned resonant dc–dc converter, where its main components, i.e., the medium- and low-voltage-side power bridges and the medium-frequency transformer, are described independently. The assembled prototype is presented together with the implemented testing strategy and the final experimental results.

Index Terms—DC–DC power conversion, power electronics, power transformers, resonant power conversion.

I. INTRODUCTION

AMONG modern trends in electrical power delivery, the implementation of solid-state transformer (SST) technologies results to be attractive for a number of applications, whereby traction and the smart grid can be highlighted. This concept is mainly characterized by the following: 1) operation at higher frequency of the power conversion unit, potentially enabling a considerable reduction of the system’s size/weight; and 2) the introduction of front- and load-end active power electronic circuits together with a low-voltage (LV) dc port, enhancing

considerably the functionality of the system concerning, e.g., reactive power compensation and operation as a UPS, given the available dc port. These two key features render the SST technology particularly interesting, but not limited to, traction and smart grid applications.

In traction, for example, the main indexes defining the propulsion system’s performance are its weight and efficiency [1]. Given the relatively low operating frequency of the overhead catenary lines [2], the weight of the system is, to a large extent, defined by the locomotive’s energy supply chain and, more specifically, by the step-down transformer responsible for the link between the medium-voltage (MV) level (15 or 25 kV [2]) and the LV rectifier supplying the dc bus, which feeds the drive system of the locomotive.

In order to reduce the size and, consequently, the weight of this energy supply chain, strong efforts are being placed by traction manufacturers to incorporate highly compact and efficient energy conversion chains based on SST technology into their high-performance solutions [1], [3]–[8]. By incorporating this SST technology, the traction solution can be greatly reduced while increasing the system’s efficiency, as proven by full-scale experimental prototypes [9].

On the other hand, SSTs are considered to be one of the key enabling technologies for the implementation of the future electric power system architecture: the smart grid [10]–[12]. This concept consists of an efficient distribution of electric energy, which is based on flexible routing mechanisms and comprehensive information availability about the end-user’s energy consumption, which ultimately facilitates the coordination and integration of renewable energy sources and energy storage systems into the current electrification network.

A possible implementation of this concept is clearly visualized in local microgrids [13], battery charging facilities, and data centers [14]. In this case, a set of different (ac and dc) loads, battery stacks, and renewable energy sources are interconnected within the local grid. With this arrangement, a flexible flow of electric power is achieved, effectively integrating renewable energy sources and powering loads of dc and ac nature. Here, the distribution of electrical energy is no longer done in LV ac, as would be the case in a traditional system architecture, but in the shape of LV dc [15]. The final conversion stage supplying the loads is now realized from LV dc into ac or other lower voltage dc values. Moreover, by utilizing a medium-frequency (MF)-operated dc–dc converter, the efficiency and power density of the solution can be increased [16].

Manuscript received September 9, 2016; accepted November 22, 2016. Date of publication December 8, 2016; date of current version May 9, 2017. Recommended for publication by Associate Editor J. H. R. Enslin.

M. G. Leibl, J. E. Huber, and J. W. Kolar are with the Power Electronic Systems Laboratory, ETH Zurich, 8092 Zürich, Switzerland (e-mail: leibl@lem.ee.ethz.ch; huber@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

G. Ortiz was with the Power Electronic Systems Laboratory, ETH Zurich, 8092 Zürich, Switzerland. He is now with ABB Corporate Research Center, Baden-Dättwil 5405, Switzerland (e-mail: gabriel.ortiz@ch.abb.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2016.2637827

As in traction solutions, this isolated dc–dc converter represents the key element in the modern microgrid arrangement, as it is now responsible for the input-to-output isolation and the required voltage adaptation from MV to LV. A well-known topology extensively utilized in low-power applications given its tight input-to-output voltage gain and soft-switching behavior over the whole operating range is the series-resonant converter (SRC) operated in the subresonant mode [17], [18]. The practical introduction of this converter in the higher power domain faces several shortcomings, which must be tackled in order to enable its implementation in the aforementioned applications. This paper is, therefore, intended to be utilized as reference for the practical design of dc–dc converters in this power/frequency class and specifically, but not limited to, converters of the resonant type.

Consequently, the practical design and experimental testing of an insulated-gate bipolar transistor (IGBT)-based 2-kV–400-V series-resonant dc–dc converter with a nominal power rating of 166 kW and a switching frequency of 20 kHz are covered in this paper. It should be noted that this frequency is comparatively high, given the power rating and the MV-side voltage range. To start, the converter's specifications are presented in Section II. The main part of the paper is dedicated to the implementation of this high-power dc–dc converter. The key practical aspects related to the semiconductor selection and their arrangement, busbar design including high-frequency finite-element method (FEM) simulations and cooling system dimensioning, among others, are covered in dedicated subsections for the MV- and LV-side power bridges. Moreover, an overview of the implemented water-cooled MF transformer, based on nanocrystalline core material, is also covered in a dedicated subsection. Finally, Section III presents the final mechanical assembly of the dc–dc converter and the obtained experimental results.

II. RESONANT CONVERTER DESIGN

As mentioned earlier, the operation under soft-switching conditions and the nearly fixed input-to-output voltage ratio renders the SRC operated in the subresonant mode very attractive for high-power dc–dc applications, since no feedback loops are required in order to maintain a good regulation of the output voltage, while ensuring that all switching transitions are performed under soft-switching conditions. Given the operation of this SRC under discontinuous current over one half switching cycle, it is often referred to as half-cycle discontinuous-conduction-mode SRC (HC-DCM-SRC) [18]. Fig. 1 shows the selected topology for the dc–dc converter, which comprises the MV-side NPC half-bridge, the LV-side full-bridge, and the MF transformer.

Utilizing the known formulas for the HC-DCM-SRC [17], [18], [20], the design parameters shown in Table I are calculated for a 166-kW/20-kHz HC-DCM-SRC prototype, whereby a detailed description of the converter's design is presented herein. Here, a practical approach for the description of the dc–dc converter's main parts, i.e., the MV-side NPC half-bridge, the LV-side full-bridge, and the MF transformer (cf., Fig. 1), will be followed, highlighting the key challenges in their respective realizations.

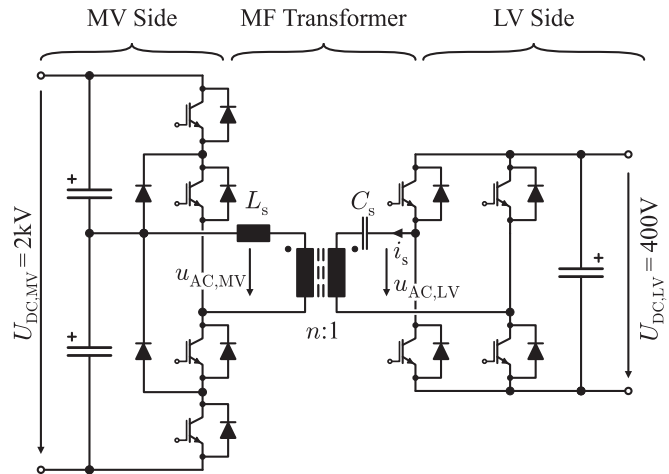


Fig. 1. Topology of the constructed SRC comprising MV-side NPC half-bridge, MF transformer, and LV-side full-bridge.

TABLE I
REFERENCE VALUES FOR THE DESIGN OF THE HC-DCM-SRC

Parameter	Value
Nominal power P_N	166 kW
Operating frequency f_s	20 kHz
MV-side voltage U_{MV}	2 kV
LV-side voltage U_{LV}	400 V
Turns ratio $n = N_{MV}/N_{LV}$	$(2 \text{ kV}/2)/400 \text{ V} = 5:2$
Series inductance L_s (MV side)	min.
Resonant frequency f_r	$\sim 22 \text{ kHz}$
MV-side peak current $\hat{I}_{s,MV}$	287 A
LV-side peak current $\hat{I}_{s,LV}$	654 A

A. MV-Side NPC Half-Bridge

The design of the MV-side power electronics is initiated with the estimation of the switching/conduction losses in the semiconductor devices. Given the aforementioned zero-current switching (ZCS) operation of the IGBT switches in the HC-DCM-SRC, the calculation of these losses cannot be realized by extraction of datasheet values, given the higher operating frequency and the rather long time constants associated with the stored charge dynamics of IGBT switches in this voltage class [21]. For this reason, the approach presented in [19], which utilizes the ZCS loss model and parameters obtained in [21], is used, whereby the utilized IGBT module is the FF450R17ME4.

For the loss calculation, an $f_r = 22 \text{ kHz}$ resonant pulse with a peak current of $\hat{I}_s = 287 \text{ A}$ is considered, whereby a peak magnetizing current of $\hat{I}_m = 40 \text{ A}$ is superimposed for ensuring soft-switching transitions of all IGBT switches [5], [21], [22]. It should be noted that this magnetizing current is supplied by the MV side when the power flow is from the MV to the LV side, and by the LV side when the power flow is from the LV to the MV side. With these parameters, the resonant pulse shape shown in Fig. 2 is fully defined, and the total switching losses in the MV-side NPC half-bridge, for the power flow from the MV to the LV side, can be calculated, reaching 942 W. In Fig. 3(a), the conduction losses based on the aforementioned

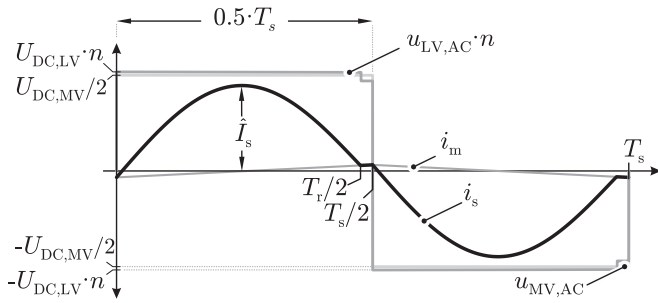


Fig. 2. Operation of the HC-DCM-SRC with increased magnetizing current in order to achieve soft-switching transitions, as explained in [19].

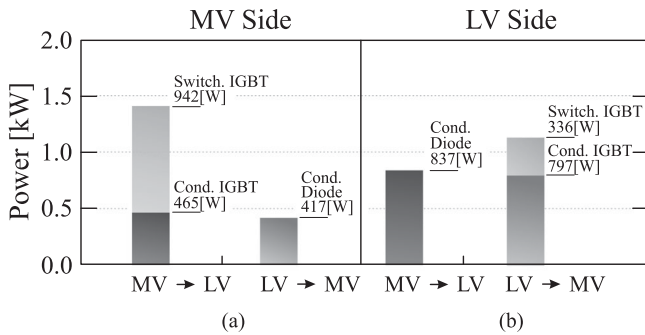


Fig. 3. Switching and conduction losses in the semiconductors for both power directions for (a) MV-side NPC half-bridge and (b) LV-side full-bridge.

resonant pulse parameters are calculated with the output and forward characteristics of the IGBT and diode, respectively, for the junction temperature of 120 °C.

The most thermally critical operating point occurs for the power flow from the MV to the LV side and reaches 1407 W, and it is for this power loss level at which the water-cooled heat sink is dimensioned. For this purpose, the MQT1914 commercial heat sink was selected, as it is capable of dissipating up to 3000 W at high water flow rates [23].

The IGBT modules comprise a pair of IGBT switches with their respective antiparallel diodes in the half-bridge configuration. In order to ensure the compatibility of the IGBTs and their complementary diodes, for the clamping diodes D_{c1} and D_{c2} , an extra IGBT module is utilized. The arrangement of these clamping diodes and the active IGBT switches is presented in Fig. 4(a) and (b). As shown in Fig. 4(a), the clamping diode D_{c1} is paired in module 1 with switch S_1 , since during a turn-off event, the current conducted by this last device would commutate to D_{c1} ; therefore, a low parasitic inductance loop is needed in the connection of these two devices. Analogously, module 3 integrates the clamping diode D_{c2} and switch S_4 . The arrangement is finalized with module 2, which integrates the inner IGBT switches of the NPC half-bridge structure.

A further interesting aspect to analyze in the construction of the NPC half-bridge is the arrangement of copper busbars used to interconnect the modules to each other and to the dc-link capacitors. These busbars are required to conduct the full peak currents at a switching frequency of 20 kHz, therefore potentially exciting high-frequency effects. For these reasons, the busbars conducting the nominal currents at operating

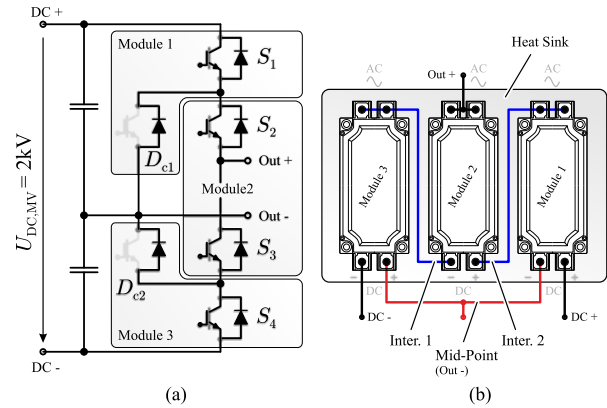


Fig. 4. (a) Assignment of the IGBT modules to switch pairs of the MV-side NPC half-bridge. This assignment ensures that all current commutations occur within the IGBT modules. The interconnections between these IGBT modules when placed on the heat sink are shown in (b).

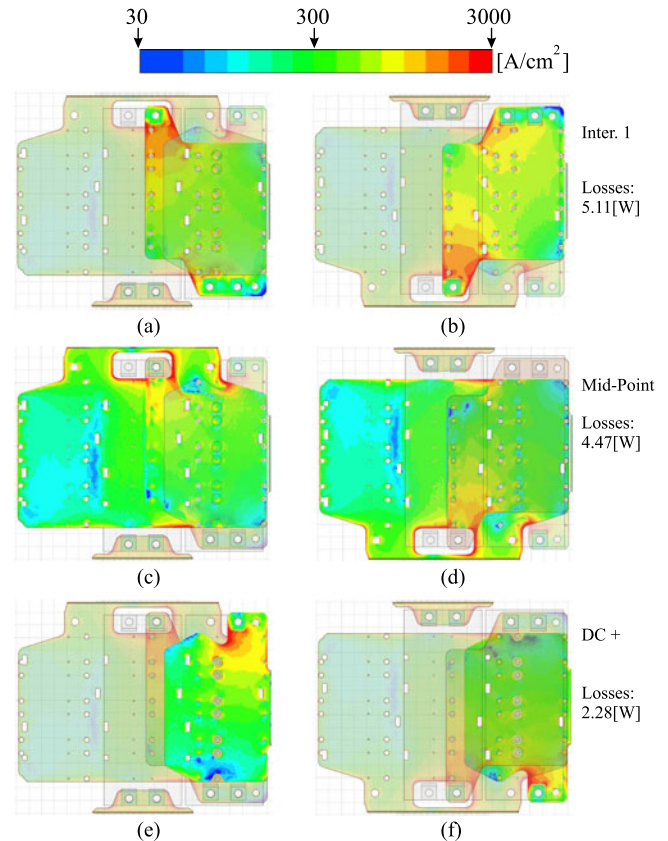


Fig. 5. FEM simulations for estimation of current densities and losses in the power busbars in Fig. 4. (a) Top view of interconnection 1 busbar. (b) Bottom view of the busbar in (a). (c) Top view of the mid-point busbar. (d) Bottom view of the busbar in (c). (e) Top view of positive busbars. (f) Bottom view of the busbar in (e).

frequency were arranged in a coplanar way and were simulated using FEM tools, with the results being shown in Fig. 5. The simulation considers the conduction of a sinusoidal current with the nominal RMS value of 191.9 A through all busbars involved in the conduction of a positive current from the plus dc-link capacitors into the transformer, i.e., busbars Inter. 1, mid-point, and DC+ in Fig. 4(b). The results for the current distribution

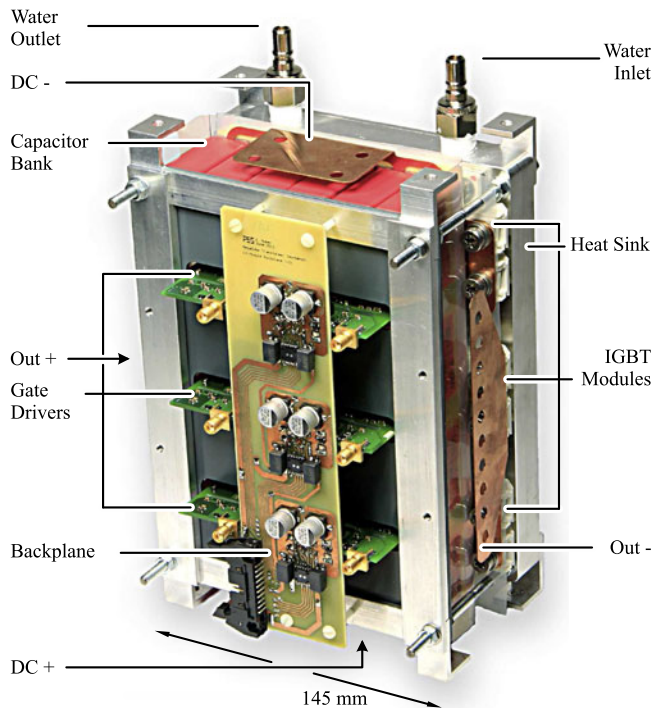


Fig. 6. Final assembly of the HC-DCM-SRC MV-side NPC half-bridge. Concerning labels DC+, DC–, Out+, and Out–, refer to Fig. 4.

and the simulated loss values are presented in Fig. 5 for the top and bottom faces of each of the involved busbars. As expected, the highest current concentration, reaching 30 A/mm^2 , is found to be close to the connection to the IGBT modules in all cases. The total losses were calculated based on the simulated current densities, giving a total of 13.2 W for all five power busbars. This is a comparatively low amount of losses, proving that the interconnection strategy reduces high-frequency effects in the busbars.

The final mechanical arrangement of the MV-side NPC half-bridge is presented in Fig. 6. The water-cooled heat sink's inlet and outlet face the top of the arrangement for easy connection of the cooling fluid. The dc link has a capacitance of $160 \mu\text{F}$ for each capacitor, which was designed to fulfill a 1% voltage ripple requirement while being able to handle a total of 112.8-A RMS current. The gate driver units for all three modules are interconnected by a common backplane and are inserted in between these dc-link capacitors, as shown in Fig. 6.

In analog fashion, the construction of the LV-side full-bridge will be discussed in the next section.

B. LV-Side Full-Bridge

The LV-side full-bridge feeds a 400-V dc link; thus, semiconductor devices of the 600-V class are suitable in this case. Accordingly, the FF600R06ME3 600-V/600-A power module is utilized for the construction of this full-bridge. As seen from Table I, this current rating is not sufficient if a single full-bridge is considered for the LV side. For this reason, two identical full-bridges are used in the LV side, each of them driving one LV winding of the MF transformer, as shown in Fig. 7(a).

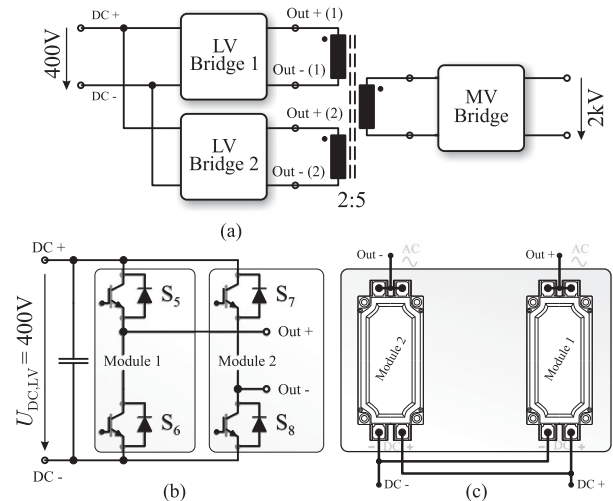


Fig. 7. (a) Splitting of bridges on the LV side of the converter. (b) Assignment of the IGBT modules to switch pairs of the LV-side HC-DCM-SRC full-bridge. The interconnections between these IGBT modules when placed on the heat sink are shown in (c).

Furthermore, as will be shown in Section II-C, this MF transformer comprises two parallel windings on the LV side; thus, the construction of the LV-side bridge with two identical full-bridges requires no special modification of the MF transformer.

Given the lower voltage-blocking capability and hence the smaller n-drift region of the bipolar junction in these IGBT switches [21], the dynamic effects of the charge carriers were neglected, whereby, for the calculation of losses, datasheet values for switching losses were considered. Here, the highest losses are generated when the power flow direction is from the LV to the MV side, since, in order to achieve soft-switching transitions, in this operating mode, the IGBT devices in the LV side switch the peak magnetizing current, which reaches $\hat{I}_m = 100 \text{ A}$. The total losses in the LV-side full-bridges including conduction losses for 120°C junction temperature and for both power directions are shown in Fig. 3(b), reaching in the worst case 1133 W. Consequently, the same heat sink as in the MV-side NPC half-bridge, the MQT1914 [23], is selected for the LV-side full-bridges.

Each of the two full-bridges utilized in the HC-DCM-SRC consists of two half-bridge IGBT modules. The construction of this bridge is, therefore, straightforward, since these modules are originally designed to operate in this configuration, reducing potential overvoltages during the switching transients. Fig. 7(b) shows the LV-side full-bridge circuit and the assignment of modules to both bridge legs. The selected water-cooled heat sink for these semiconductors is designed to cool three of these modules, whereby the two outermost positions are used, as shown in Fig. 7(c). Here, also the required busbars for connection to the dc-link capacitors as well as output terminals can be seen.

Due to the high currents and MF level, FEM simulations were conducted in order to quantify the losses in the aforementioned busbars, visualizing the current density distribution caused by high-frequency effects. The simulation consists of imposing a

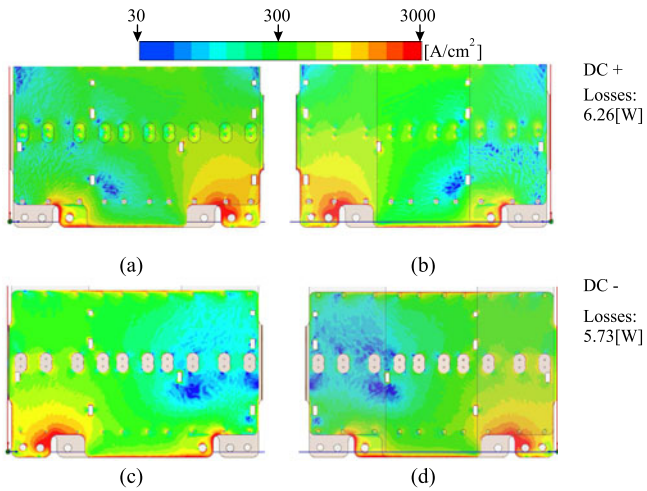


Fig. 8. FEM simulations for estimation of current densities and losses in the power busbars. (a) Top view of the positive busbar. (b) Bottom view of the busbar in (a). (c) Top view of the negative busbar. (d) Bottom view of the busbar in (c).

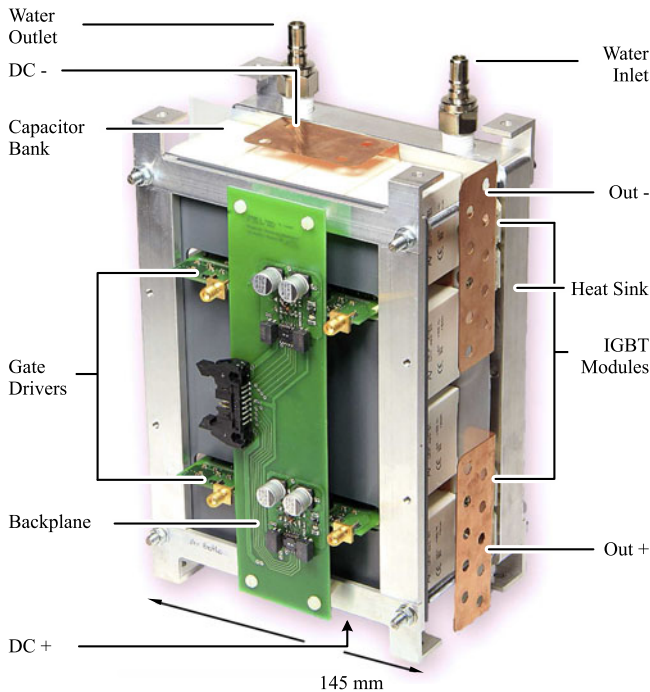


Fig. 9. Picture of the realized LV-side IGBT-based HC-DCM-SRC full-bridge. Concerning terminals Out+, Out-, DC+, and DC-, refer to Fig. 7(b).

rectified sinusoidal current with a peak value of the sine wave at nominal power, which amounts to 479.87 A. The results of this simulation are displayed in Fig. 8. As expected, in all cases, the highest current densities, with a peak value close to 3000 A/cm², are found in the vicinity of the modules' terminals. With the presented current distribution, a total of 6.26 and 5.73 W are generated as losses in the positive and negative dc-link busbars, respectively; thus, no further cooling of these parts is considered.

The final assembled HC-DCM-SRC LV-side bridge is shown in Fig. 9. As can be seen, a compact construction was achieved for this module, reaching a power density of 25 kW/L.

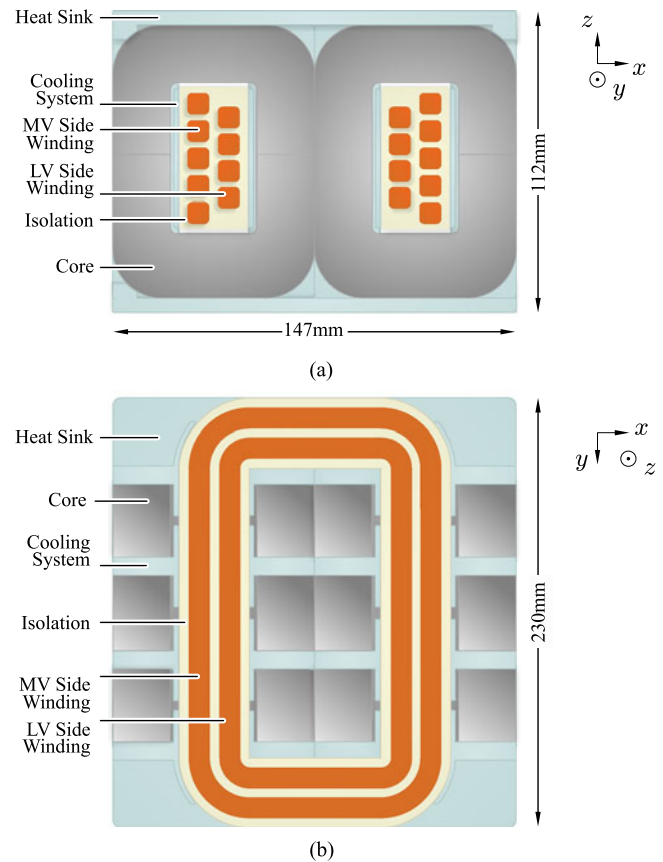


Fig. 10. MF transformer concept based on the shell-type core arrangement, nanocrystalline core material, and water cooling for heat extraction.

The construction resembles that of the MV-side bridge (cf., Fig. 6): top water-cooling inlet and outlet, top/bottom dc-link connections, compact dc-link capacitor bank with a capacitance value of 480 μ F (for a total of 0.4% voltage ripple and 320-A RMS current), vertically inserted gate drivers, and common signal distribution backplane. The main difference is presented by the output ac terminals, which are now placed on the same side of the module.

The linking component between the two previously presented converter parts is the MF transformer, which is responsible for the voltage adaptation and the isolation between the MV and LV sides. The optimization and construction of this transformer will be briefly discussed in the following.

C. MF Transformer

The constructed MF transformer concept and winding arrangement is shown in Fig. 10. As can be seen, this transformer follows a shell-type construction concept, i.e., it comprises magnetic cores in an E shape, in this case utilizing six pairs of U cores, as shown in Fig. 10(a) and (b). In addition, the windings are arranged concentrically, easing the task of isolation and the leakage inductance estimation, which is critical for the dynamic behavior of the converter [24].

The utilized core material is nanocrystalline 500 F, which is characterized by a high saturation flux density around 1.2 T and

comparatively low specific core losses. The windings in both LV and MV sides are based on a 9500-strand litz wire with $70\ \mu\text{m}$ per strand. The cooling concept consists of C-shaped aluminum pieces pressed against the winding and core for good thermal contact [cf., Fig. 10(b)], following the concept proposed in [25]. A layer of isolation based on a mica tape is placed between the LV winding and the MV winding. This material can isolate up to 13.8 kV and is originally designed for the isolation of MV electrical machines [26]. In addition to this isolation layer, the windings are initially covered with a semi-conductive tape in order to even out the electric field within the isolation.

This transformer was optimized, and its construction details can be found in [27]. Comparatively high power densities are achievable mainly due to the rather high switching frequency in combination with the core material selection and the cooling concept. For the realized design, the theoretical value of efficiency reaches 99.82% at a power density of 45 kW/L.

A further step in the construction of the HC-DCM-SRC is the design of the resonant capacitor bank. The leakage inductance measured from the LV side reaches $0.4\ \mu\text{H}$, whereby a resonant frequency f_r close to 22 kHz is desired. The required resonant capacitor C_r value is therefore [17]

$$C_r = \frac{1}{(2\pi f_r)^2 L_s} = 158.31\ \mu\text{F}. \quad (1)$$

This capacitor value was realized with 44 paralleled KEMET C4A-TGBW 4330A3EJ 450-V/3- μ F capacitors, reaching a total capacitance of $132\ \mu\text{F}$. With this capacitance value, the achieved resonance frequency is $f_r = 21.9\ \text{kHz}$, ensuring the subresonant operation of the HC-DCM-SRC. It should be noted that, in this topology, it is convenient to place the resonant capacitor on the LV side in order to avoid biased operation of the transformer's flux density due to possible dc components in the voltage applied from the power electronic bridges when the power flow direction is from the LV to the MV side. In the case when power flows from the MV to the LV side, the split dc-link arrangement ensures the unbiased flux-density operation of the transformer, and therefore, no additional benefits would be obtained by placing the resonant capacitor on the MV side.

The mechanical arrangement of the complete transformer comprising the aforementioned resonant capacitor bank is presented in Fig. 11(a). In order to realize a compact transformer design, this capacitor bank possesses equal length and width as the transformer's heat sinks. This way, the top face of the capacitors can be attached to the cover of one water-cooled heat sink. Moreover, the magnetic cores are placed in between the C-shaped cooling pieces utilized to extract the heat from the cores and winding, as explained earlier. These C-shaped pieces conduct the heat to top/bottom water-cooled heat sinks, whereby the water inlet and outlet are conveniently positioned at the top of the assembly. The power terminations for the MV side are placed on one of the transformer's faces, whereas for the LV side, these terminals are placed on top of the capacitor bank, as shown in Fig. 11(a).

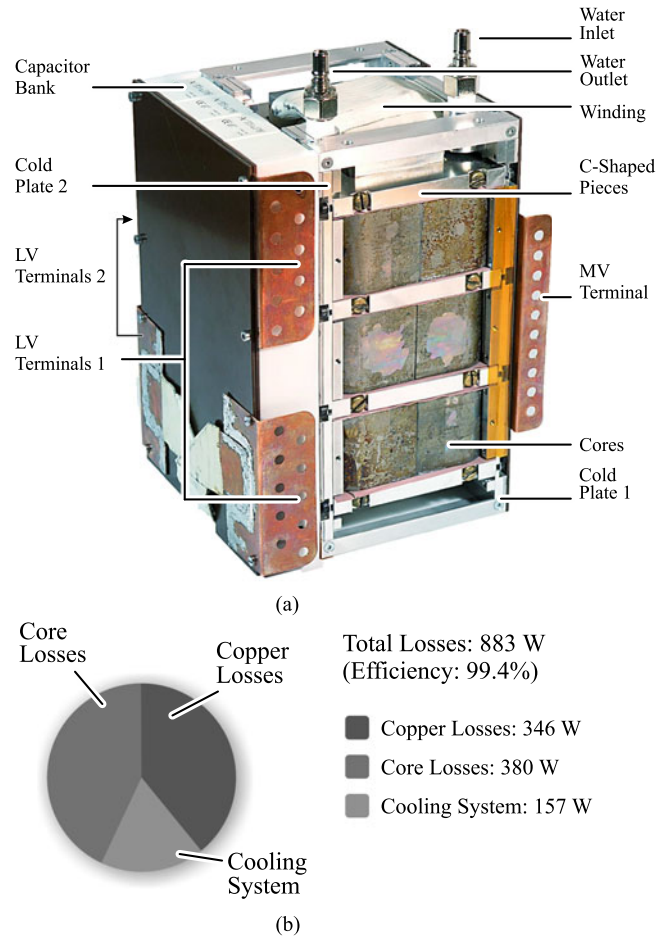


Fig. 11. (a) Final mechanical assembly of the nanocrystalline transformer utilized in the dc–dc converter prototype. (b) Breakdown of losses at nominal power in the MF transformer.

This transformer was experimentally tested in order to verify the theoretically calculated loss values for core, copper, and cooling system losses. Here, several phenomena such as uneven current distribution in the litz wire bundles, asymmetric loss distribution in the transformer cores (which comprise an air-gap of $100\ \mu\text{m}$), and additional unaccounted losses in the water-cooling system increased significantly the value of these losses. These are summarized in Fig. 11(b), where it is possible to see the considerable losses generated in the cooling system, which were analyzed in more detail in [27]. Nevertheless, this 166-kW/20-kHz nanocrystalline water-cooled transformer achieves a 99.4% efficiency at rated power with a power density of 32.7 kW/L (including resonant capacitors).

All details about the aforementioned optimization procedure together with a comprehensive overview of previously reported transformer concepts and extensive experimental results about this nanocrystalline water-cooled transformer prototype can be found in [15] and [27].

This transformer is now combined with the designed MV-side NPC half-bridge and the LV-side full-bridges to assemble and experimentally test the complete HC-DCM-SRC prototype in the following section.

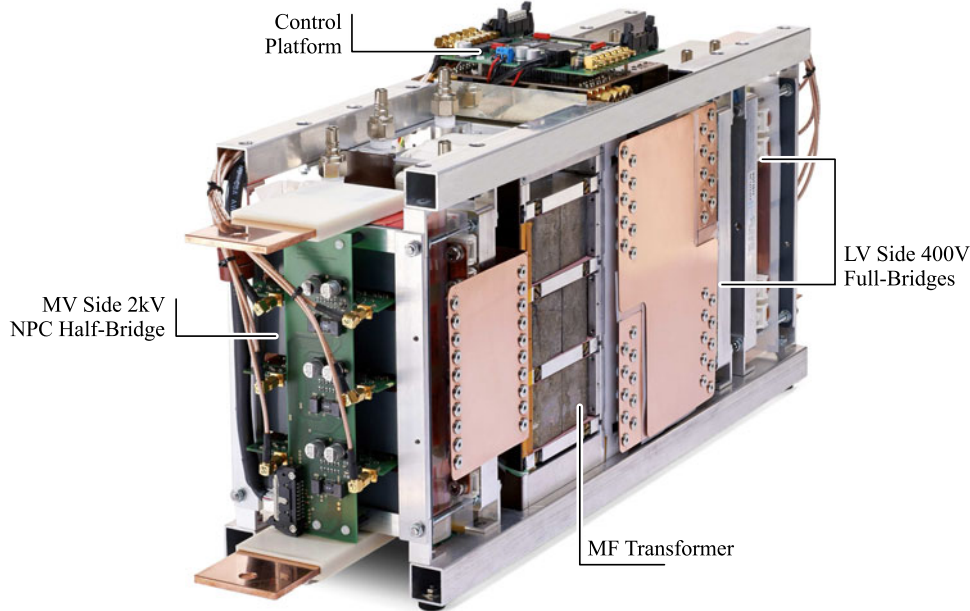


Fig. 12. Finally assembled 166-kW/20-kHz HC-DCM-SRC prototype comprising 2-kV IGBT-based NPC half-bridge on the MV side, 400-V IGBT-based full-bridge on the LV side, and nanocrystalline water-cooled MF transformer.

III. CONVERTER PROTOTYPE AND EXPERIMENTAL TESTING

The HC-DCM-SRC comprising the LV-side bridge, the MV-side bridge, the MF transformer, and the control platform is shown in Fig. 12. This control platform comprises the TMS320F28335 floating point DSP from TI and the LFXP2-5E-T144/TN144 FPGA from Lattice.

The converter is arranged with the two LV bridges in the back, followed by the MF transformer and the MV bridge in the front. Since all bridges and the MF transformer were designed with equal height and depth, they can all be fitted within an aluminum frame serving also as chassis in order to achieve a high mechanical stability. The ac power connections from the MV and LV bridges to the transformer are done with respective 0.5-mm copper plates, which are placed at the sides of the converter. The dc-link connections are placed on the top and bottom for both MV- and LV-side bridges. Additionally, all water-cooling connections are accessible from the top, leading to an easy connection of the hoses carrying the cooling fluid.

Given the rather high power rating of the designed converter, in order to perform full power experimental testing of the system, a second converter, which is based on a triangular-current-mode dual-active bridge (TCM-DAB) [15], is designed for equal power and input/output voltages.

The concept of the test setup is shown in Fig. 13. This arrangement, known as back-to-back connection, is based on a direct connection of the MV- and LV-side dc links of the two converters. One converter, e.g., the HC-DCM-SRC, transfers power from the LV to the MV side, therefore charging the MV-side dc link. On the other hand, the TCM-DAB is adjusted to transfer power from the MV to the LV side, i.e., charging back the common LV-side dc link. Furthermore, an external power

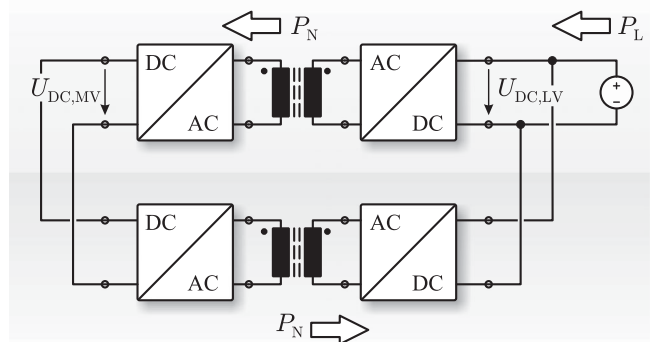


Fig. 13. Concept of the back-to-back assembly. The HC-DCM-SRC is utilized to fix the LV- and MV-side voltages (without control of power flow), while the TCM-DAB controls the amount of power transferred between the MV- and LV-side dc links.

supply is utilized to provide the losses of the system, which in this case at nominal conditions are about $P_L = 8$ kW. With this setup, the nominal power P_N circulates via the two converters, while only a small portion must be externally provided by the power supply, enabling the experimental testing in a standard laboratory environment, as also demonstrated in [28].

With the aforementioned test concept, the high power testing of the system was performed. In Fig. 14(a), the ac-link quantities of the designed converter operating at 50 kW are shown. Here, the resonant pulse combined with the magnetizing current can be seen in the ac-link current i_s . It should be noted that, given the comparatively low amount of transferred power, the magnetizing current, utilized to

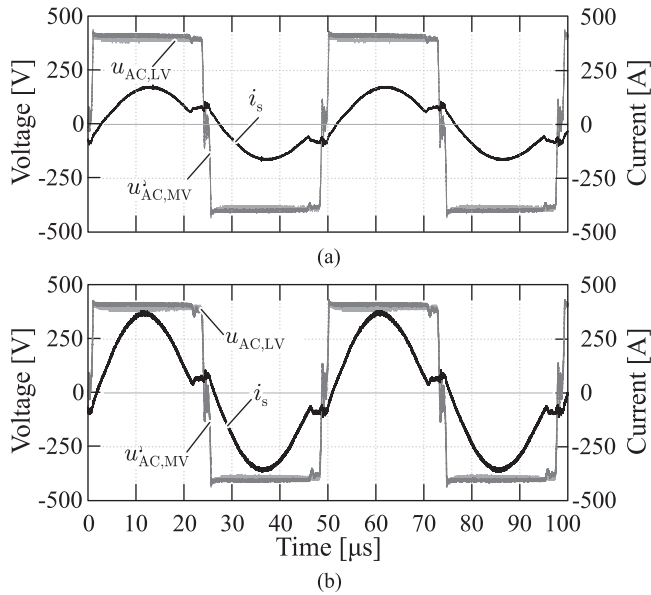


Fig. 14. Continuous test of the HC-DCM-SRC. (a) Transferred power of 50 kW. (b) Transferred power of 80 kW.

TABLE II
TOTAL INPUT POWER FROM EXTERNAL POWER SUPPLY AND OVERALL
BACK-TO-BACK SYSTEM EFFICIENCY

Parameter	Transferred Power	
	50 kW	80 kW
Total back-to-back system power losses	4.3 kW	5.6 kW
Total back-to-back system efficiency	91.4%	93.0%

reduce switching losses in the IGBT switches, represents a large part of the total current. Additionally, the small difference between the reflected MV-side voltage $u'_{AC,MV,S}$ and the LV-side voltage $u_{AC,LV,S}$ is visible, which corresponds to the voltage difference required to transfer the specified power of 50 kW.

For this power level, the total input power from the external 400-V supply is 4.3 kW, corresponding to a total system efficiency of 91.4% (cf., Table II). It should be noted that this efficiency corresponds to the total back-to-back system efficiency and not to the individual (HC-DCM-SRC and TCM-DAB) converters' efficiency. Nevertheless, an improvement is achieved when operating at higher transferred power, as will be visible when the power level is increased in the next test.

The next measurement was done at the transferred power of 80 kW, with the results being shown in Fig. 14(b). As can be seen, the HC-DCM-SRC features a higher current amplitude with respect to the operation at 50 kW, which reflects the higher amount of power transfer. It should be noted that, in comparison to the waveform in Fig. 14(a), the applied ac voltages remain virtually unchanged in spite of the higher transferred power, proving the capability of the HC-DCM-SRC to operate with a nearly constant input-to-output voltage transfer ratio.

The total power delivered by the external 400-V power supply is 5.6 kW, corresponding to a total back-to-back system efficiency of 93% (cf., Table II). This efficiency represents an important improvement with respect to the value achieved at the transferred power of 50 kW, showing the tendency of the system to higher efficiencies when operated at higher power levels.

Overall, the back-to-back testing of the converters shows a good performance. The sinusoidal pulse superimposed with the transformer's magnetizing current can be seen, and the natural adjustment of this pulse's amplitude, and therefore of the transferred power, is visible when the power level is increased, while the MV-side voltage is kept nearly unchanged. This behavior proves the capability of the HC-DCM-SRC to operate with fixed voltage transfer ratio, while achieving soft switching in all semiconductor devices.

It is worth to point out that the HC-DCM-SRC does not possess the capability to limit its output power due to its uncontrolled operation. In order to include protection features into the converter, pre- or postregulation nonisolated converters (e.g., buck or boost type) are typically implemented. Other protection mechanisms can be built in the converter by clamping the series-resonant capacitor voltage, hence limiting resonant current amplitude and, therefore, the output power.

IV. SUMMARY/CONCLUSION

Given its operation at near-resonant switching frequency that ensures ZCS transitions of all semiconductor devices while keeping a good regulation of the output voltage without the requirement of feedback control loops, the HC-DCM-SRC results to be highly attractive for high-power isolated dc–dc converter applications, where a simple and reliable converter construction is among the main requirements.

This paper focused on practical details of the converter implementation, e.g., the power electronic bridges' mechanical construction, whereby a coplanar busbar construction was selected in order to minimize the losses associated with high-frequency effects, which were confirmed by respective FEM simulations. Moreover, water cooling was selected for heat extraction, enabling a compact and low parasitic converter module design for both the MV and LV sides of the dc–dc converter. These LV and MV sides are linked by an MF transformer based on nanocrystalline core material, which also utilizes water cooling for heat extraction, leading to a transformer prototype, which achieves 99.4% efficiency and 32.7-kW/L power density. These three basic converter components, the MV and LV power bridges together with the MF transformer, were electrically and mechanically coupled in order to build a converter prototype utilized for the experimental testing.

For the testing of the dc–dc converter prototype, a back-to-back strategy was implemented, which enabled the verification of the converter's operation in a standard laboratory environment. With this testing strategy, the key features of the HC-DCM-SRC were verified at high-power operation, proving the feasibility of this converter topology for isolated high-power dc–dc systems to be utilized in SST applications.

REFERENCES

- [1] D. Dujic, F. Kieferndorf, and F. Canales, "Power electronics transformer technology for traction applications—An overview," in *16th Int. Symp. Power Elect.*, Novi Sad, Serbia, Oct. 26–28, 2012, pp. 1–7.
- [2] A. Steimel, "Power-electronic grid supply of ac railway systems," in *Proc. Optim. Elect. Electron. Equipment*, Brasov, Romania, 2012, pp. 16–25.
- [3] B. Engel, M. Victor, G. Bachmann, and A. Falk, "15 kV/16.7 Hz energy supply system with medium frequency transformer and 6.5 KV IGBTs in resonant operation," in *Proc. Eur. Conf. Power Electron. Appl.*, Toulouse, France, 2003, pp. 2–4.
- [4] J. Taufiq, "Power electronics technologies for railway vehicles," in *Proc. Power Convers. Conf.*, Nagoya, Japan, 2007, pp. 1388–1393.
- [5] H. Reinold and M. Steiner, "Characterization of semiconductor losses in series resonant DC-DC converters for high power applications using transformers with low leakage inductance," in *Proc. Eur. Conf. Power Electron. Appl.*, Lausanne, Switzerland, 1999, pp. 1–10.
- [6] L. Heinemann, "An actively cooled high-power, high frequency transformer with high insulation capability," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Dallas, TX, USA, 2002, pp. 352–357.
- [7] H. Hoffmann and B. Piepenbreier, "High voltage IGBTs and medium frequency transformer in DC-DC converters for railway applications," in *Proc. Symp. Power Electron., Elect. Drives, Autom. Motion*, Pisa, Italy, 2010, pp. 744–749.
- [8] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *Proc. Eur. Conf. Power Electron. Appl.*, Aalborg, Denmark, 2007, pp. 1–10.
- [9] C. Zhao *et al.*, "Design, implementation and performance of a modular power electronic transformer (PET) for railway application," in *Proc. Eur. Conf. Power Electron. Appl.*, Birmingham, U.K., 2011, pp. 1–10.
- [10] "UNIFLEX," 2013. [Online]. Available: www.eee.nott.ac.uk/uniflex/Project.htm
- [11] M. Simoes *et al.*, "Smart-grid technologies and progress in Europe and the USA," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, Sep. 2011, pp. 383–390.
- [12] L. Heinemann and G. Mauthe, "The universal power electronics based distribution transformer, a unified approach," in *Proc. IEEE Power Electron. Spec. Conf.*, Vancouver, BC, Canada, 2001, pp. 504–509.
- [13] T. Dragicic, J. C. Vasquez, J. M. Guerrero, and D. Skrlac, "Advanced LVDC electrical power architectures and microgrids: A step toward a new generation of power distribution networks," *IEEE Electr. Mag.*, vol. 2, no. 1, pp. 54–65, Mar. 2014.
- [14] B. Hafez, H. S. Krishnamoorthy, P. Enjeti, S. Ahmed, and I. J. Pitel, "Medium voltage power distribution architecture with medium frequency isolation transformer for data centers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, 2014, pp. 3485–3489.
- [15] G. Ortiz, "High-power DC-DC converter technologies for smart grid and traction applications," Ph.D. dissertation, Swiss Federal Inst. Technol. Zurich, Zurich, Switzerland, 2014.
- [16] J. Huber and J. Kolar, "Volume/weight/cost comparison of 1MVA 10 kV/400 V solid-state and conventional low-frequency distribution network," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 4545–4552.
- [17] R. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–182, Apr. 1988.
- [18] W. C. Ho, "Design and analysis of discontinuous mode series resonant converter," in *Proc. Int. Conf. Ind. Technol.*, Guangzhou, China, 1994, pp. 486–489.
- [19] J. Huber, G. Ortiz, F. Krismer, N. Widmer, and J. Kolar, " η - ρ Pareto optimization of bidirectional half-cycle discontinuous-conduction-mode series-resonant DC/DC converter with fixed voltage transfer ratio," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, 2013, pp. 1413–1420.
- [20] V. Vorperian and S. Cuk, "A complete DC analysis of the series resonant converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Cambridge, U.K., 1982, pp. 85–100.
- [21] G. Ortiz, H. Uemura, D. Bortis, J. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of IGBTs in high-power high-efficiency dual-active-bridge DC/DC converters," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 587–597, Feb. 2012.
- [22] L. Lindenmuller, R. Alvarez, and S. Bernet, "Optimization of a series resonant DC/DC converter for traction applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Raleigh, NC, USA, 2012, pp. 2201–2208.
- [23] "MAX Q Technologies," 2015. [Online]. Available: www.maxqtechnology.com
- [24] A. Esser and H. Skundenly, "A new approach to power supplies for robots," *IEEE Trans. Ind. Appl.*, vol. 27, no. 5, pp. 872–875, Sep./Oct. 1991.
- [25] M. Pavlovsky, S. de Haan, and J. Ferreira, "Design for better thermal management in high-power high-frequency transformers," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Hong-Kong, 2005, pp. 2615–2621.
- [26] "VonRoll," 2013. [Online]. Available: <http://www.vonroll.ch>
- [27] G. Ortiz, M. Leibl, J. W. Kolar, and O. Apeldoorn, "Medium frequency transformers for solid-state-transformer applications—Design and experimental verification," in *Proc. IEEE 10th Int. Conf. Power Electron. Drive Syst.*, Apr. 2013, pp. 1285–1290.
- [28] D. Dujic *et al.*, "Experimental characterization of LLC resonant DC-DC converter for medium voltage applications," in *Proc. Eur. Conf. Power Electron. Appl.*, Birmingham, U.K., 2011, pp. 3–8.



Gabriel Ortiz (M'10) received the M.Sc. degree in electronics engineering from Universidad Técnica Federico Santa María, Valparaíso, Chile, and the Ph.D. degree in electrical engineering from the Power Electronic Systems Laboratory, ETH Zürich, Zürich, Switzerland, in 2008 and 2013, respectively.

The focus of his Ph.D. research project was on solid-state transformers for future smart grid implementations and traction solutions. Specifically, his Ph.D. research dealt with the modeling, optimization, and design of high-power dc-dc converters operated in the medium-frequency range with a focus on modeling of soft-switching processes in insulated-gate bipolar transistors and medium-frequency transformer designs. In 2014, he supervised Ph.D. research projects at the Power Electronic Systems Laboratory, ETH Zurich, Zürich, Switzerland, as a Postdoctoral Research Fellow, with a focus on silicon carbide for solid-state transformer applications and isolation issues of medium-frequency transformers. He is a Research Scientist at ABB Corporate Research Center, Baden-Dättwil, Switzerland.



Michael Georg Leibl (M'12) received the B.Sc. degree from Vienna University of Technology, Vienna, Austria, in 2010, and the M.Sc. degree from ETH Zurich, Zürich, Switzerland, in 2012, both in electrical engineering. He is working toward the Ph.D. degree with the Power Electronic Systems Laboratory, ETH Zurich.

His research interests include the optimized design of inductive components, in particular modeling high-frequency winding loss, high-power three-phase power factor correction rectifiers, and isolated dc-dc converters.



Jonas Emanuel Huber (S'11) received the M.Sc. degree in electrical engineering from ETH Zurich, Zürich, Switzerland, in 2012, where he is working toward the Ph.D. degree with the Power Electronic Systems Laboratory.

His research interests include solid-state transformers, focusing on the analysis, optimization, and design of high-power multilevel converter systems, reliability considerations, control strategies, and applicability aspects, among others.



Johann Walter Kolar (F'10) received the M.Sc. degree in industrial electronics and control engineering and the Ph.D. degree (*summa cum laude*) in electrical engineering from Vienna University of Technology, Vienna, Austria, in 1997 and 1999, respectively.

He is a Full Professor and the Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zürich, Switzerland. He has proposed numerous novel pulse width modulation converter topologies and modulation and control methods (e.g., the Vienna rectifier, the sparse matrix converter, and the SWISS rectifier). He has supervised more than 60 Ph.D.s and has authored or coauthored more than 750 scientific papers in international journals and conference proceedings and has filed more than 140 patents. His current research interests include ultracompact and ultraefficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, as well as ultrahigh-speed and ultralight-weight drives, bearingless motors, and energy harvesting.

Dr. Kolar received 25 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award, and the ETH Zurich Golden Owl Award for excellence in teaching.