Cascaded Dual-Buck AC–AC Converter With Reduced Number of Inductors

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***Abstract*—This paper proposes a new type of cascaded ac–ac converter with phase-shift control and reduced number of inductors. It can attain high voltage levels by using standard low-voltage rating semiconductor devices. The proposed converter is resistant to current shoot-through and does not require pulse-width modulation (PWM) dead-time; these lead to greatly enhanced system reliability and effective utilization of PWM voltages. Moreover, it does not require current/voltage polarity sensors, lossy snubbers, or dedicated PWM strategies for commutation. These features make it possible to design the converter with reduced control complexity, and obtain output voltage with less distortion. The cascaded units in the proposed converter share the inductors; therefore, number of inductors, inductors footprints, and magnetic volume can be reduced. The phase-shift PWM control is also presented. It increases the effective frequency of the converter by the number of cascaded units, which decreases the size of the passive components and/or the current and voltage ripples. In order to demonstrate the advantages of the proposed converter, detailed comparative simulations and experimental results of the proposed 2-unit, 3-unit, and 4-unit cascaded converters are provided.**

***Index Terms*—AC–AC converter, cascade, dual-buck, high voltage level, multilevel, phase-shift, reliability.**

I. Introduction

FOR voltage regulation only, direct pulse-width modulation (PWM) ac–ac converters are widely used. The research on the direct PWM ac–ac converters mainly focuses on single-phase [1]–[4], [28], [31] and three-phase low-voltage applications [5]–[7]. The traditional two-level buck-type ac–ac converter is depicted in Fig. 1(a). It has a simple structure and produces an output voltage lower than the input voltage. However, it has commutation problem due to the delayed response of electronic circuits and semiconductor switching devices [2], [7], [28]. It is also susceptible to electromagnetic interference noise's misgating-ON or -OFF. The commutation problem arises when an instant of dead or overlap time occurs in the gate signals. The unwanted overlap or dead time in the gate signals causes high current and voltage spikes, respectively, which are major failure of traditional ac–ac converters. In addition, when implemented with MOSFET, this converter has reverse recovery issues of MOSFET body diode especially at high voltage. As an alternative to the converter in Fig. 1(a), a new type of two-level buck-type converter without the commutation problem is proposed in [2] [see Fig. 1(b)]. The inductors $L_1 - L_4$ in this converter split the phase legs; therefore, the converter has no overlap time problem, which is observed in the traditional converters. In this converter, the body diodes of MOSFETs do not conduct, thus, eliminates their reverse recovery issues. The leg capacitors C_1 and C_2, while serving as lossless snubbers, provide safe path for the inductor currents during the dead time.

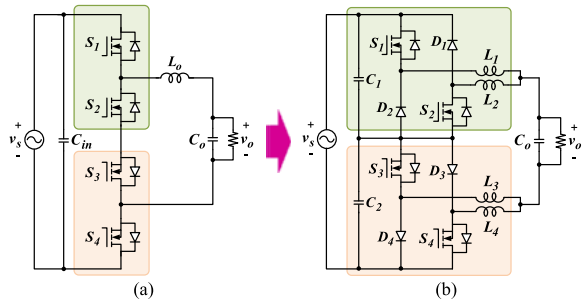

Fig. 1. Single-phase buck-type ac–ac converters. (a) Traditional. (b) Buck-type in [2].

Similar to dc–ac inverters, ac–ac converters are also widely used in high-voltage and high-power applications, but the two-level converters in Fig. 1 can hardly be used for such applications. For this reason, multilevel converters have been considered as a viable solution for high-voltage applications. For the dc–ac power conversion, neutral-point-clamped inverter [8], flying-capacitor (FC) inverter [9], and cascaded H-bridge inverter [10] are the prominent multilevel topologies. The attractive features of multilevel converters are as follows:

1) they can produce output voltages with low distortion;
2) they can generate high output voltages using standard low-voltage rating semiconductor devices;
3) they can operate at low switching frequencies.

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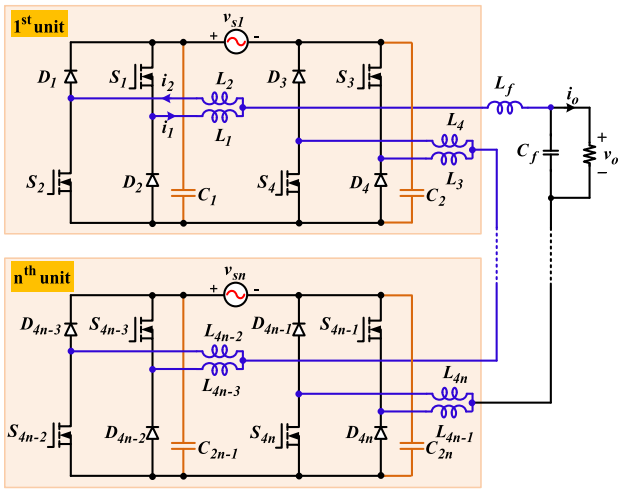

Fig. 2. Proposed type-I cascaded dual-buck ac–ac converter with n-unit cells.

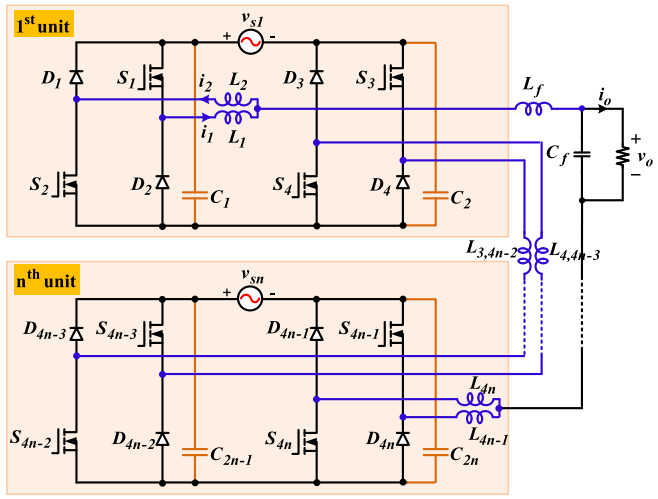

Fig. 3. Proposed type-II cascaded dual-buck ac–ac converter with n-unit cells.

Multilevel direct PWM ac–ac converters (MPACs) using the concept of the FC-type multilevel topologies in [11]–[14] can obtain high output voltages using low voltage rating devices. They have the voltage balancing issues of the FCs, and require control techniques for voltage balancing of FCs. The control techniques become more challenging as the number of levels of the output voltage increases. In addition, the MPACs using FCs have short-circuit risk.

A cascaded multilevel ac–ac converter can be obtained through the series connection of a number of single-phase converters with separate ac sources. It is necessary to connect many single-phase converters in series to attain high voltage levels. Cascaded converters are highly modular because all the single-phase units have similar structures, controls, and operations. Therefore, maintenance is easy and the faulty unit can be easily replaced and corrected. The faulty unit can also be bypassed without disturbing the circuit operations of the healthy units. The cascaded converter based on the converter in Fig. 1(a) has the commutation problem for each unit. For this reason, in the literature, the traditional cascaded ac–ac converters have not been well supported with phase-shift PWM control. Phase-shift PWM control is widely used for the cascaded converters, where the gate signals of the cascaded units are phase shifted. The phase-shift control can increase the effective frequency of the passive components by the number of cascaded units. Because of this, the volume of the passive components and/or the current and voltage ripples can be reduced greatly.

A reliable cascaded multilevel ac–ac converter was proposed in [27] and it requires extra coupled inductors for each unit. The coupled inductors in this converter are used to limit the circulating currents only and do not serve as filter inductors. In addition, the phase-shift control in [27] can reduce the sizes of the input and output filters, but the magnetic volume of the coupled inductors cannot be reduced with the phase-shift PWM control as the effective switching frequency of the coupled inductors remain the same as the converter switching frequency.

Cascaded dc–ac and ac–ac converters can be used for reactive power compensation in high-voltage applications [15]. In such

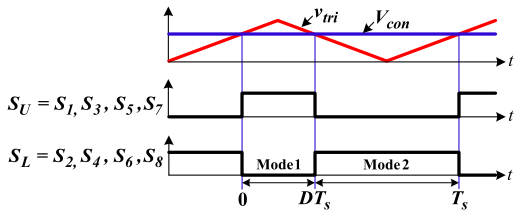

Fig. 4. Gate signals of the 2-unit cascaded converter without phase-shift control.

applications, the ac–ac converter is a viable solution to replace the sizeable dc–ac inverter solution by both reducing the power loss and saving bulky dc-link capacitors [16]. Dynamic voltage restorers (DVRs) based on ac–ac converters [17]–[24] can compensate voltage sags and swells. DVRs based on the cascaded converters [25], [26] are more practical for applications where both voltage and power are high.

This paper proposes a cascaded dual-buck ac–ac converter with reduced number of inductors. It can attain high voltage levels by using low voltage rating switching devices. In the proposed converter, the cascaded units share the inductors; thus, the number of inductors, inductors footprints, circuit layout complexity, and magnetic volume can all be reduced. The proposed converter has no misgating-ON or -OFF related problem in any unit. It does not sense the polarity of current or voltage for the commutation of the switches, therefore, control complexity can be reduced. Phase-shift PWM control is presented for the proposed converter and it increases the equivalent switching frequency of passive components. The topology derivation, operation, detailed circuit analysis, phase-shift control, and inductor current ripple analysis are presented. Finally, detailed simulation and experimental results of the proposed 2-unit, 3-unit, and 4-unit cascaded converters are presented.

II. Proposed Cascaded Dual-Buck AC–AC Converters

In this paper, two types of converters are proposed as follows.

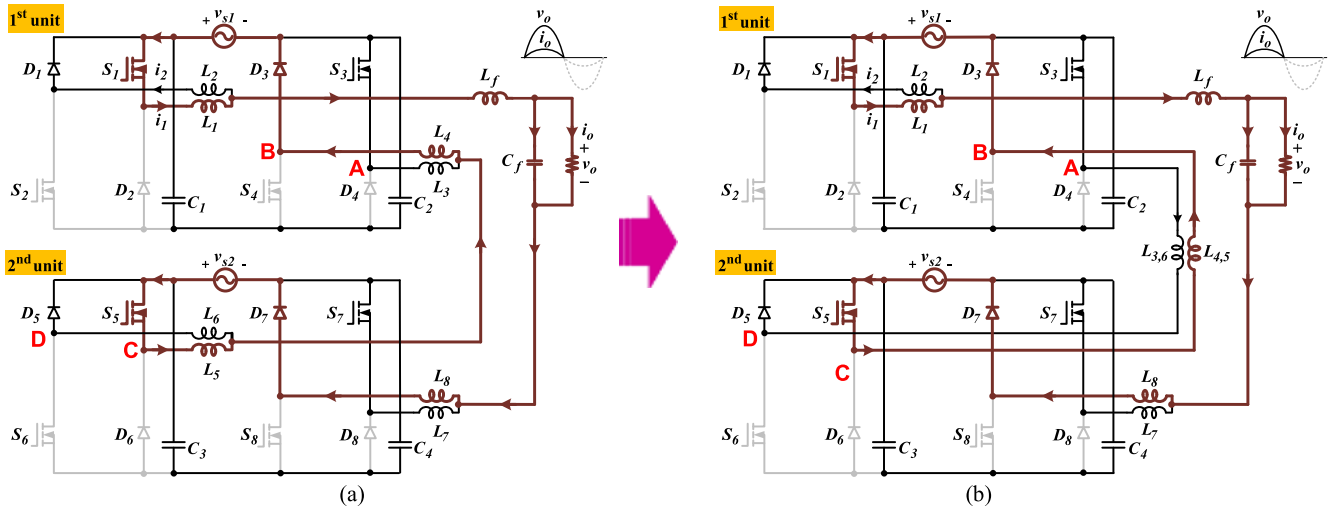

Fig. 5. Operation of the proposed 2-unit cascaded converters in mode 1 (S_U are ON and S_L are OFF). (a) Type-I. (b) Type-II.

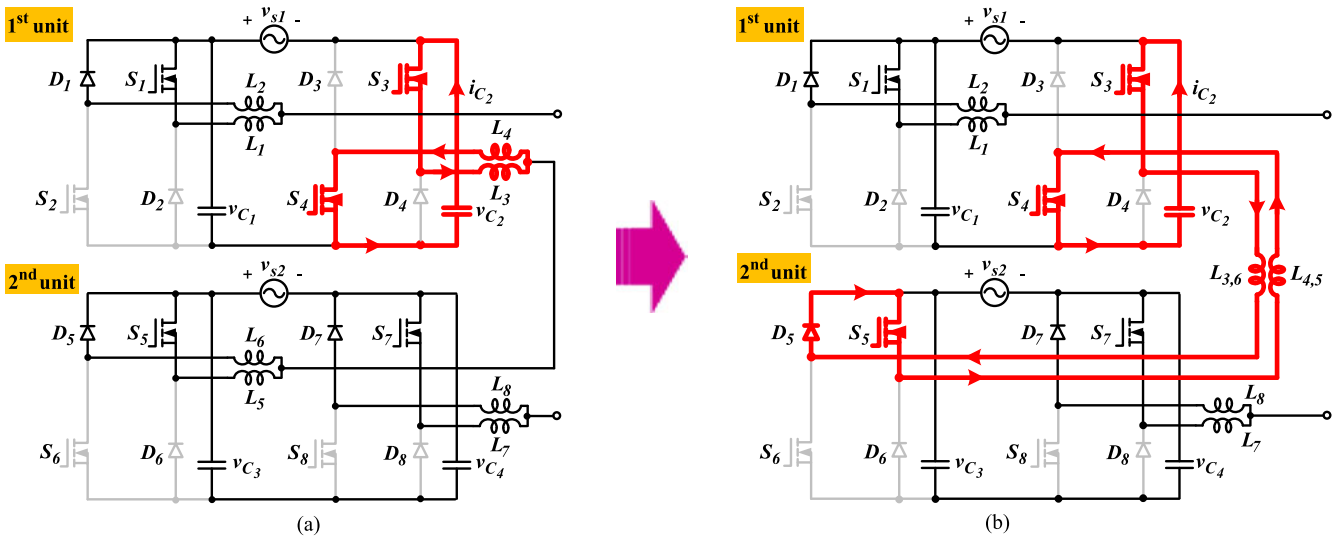

Fig. 6. Opposition to shoot-through current. (a) Type-I. (b) Type-II.

A. *Type-I*

Fig. 2 shows the proposed type-I converter, where i_1 and i_2 represent inductor currents of L_1 and L_2, respectively. The inductors $L_1 - L_{4n}$ limit the shoot-through current when the upper and lower switches in each unit are turned ON simultaneously. They also serve as filter inductors as will be explained later. The proposed converter, similar to the dual-buck inverters [29]–[31], needs a compromise between magnetic volume and converter reliability as follows:

1) by increasing the inductances of $L_1 - L_{4n}$, reliability of the converter can be improved greatly, however, the magnetic volume will be increased;
2) by decreasing the inductances of $L_1 - L_{4n}$, magnetic volume can be reduced, but the converter reliability will be decreased.

The leg capacitors ($C_1 - C_{2n}$) provide safe paths for inductor currents when the upper and lower switches in each unit are turned OFF simultaneously. They also serve as both snubber and input filter capacitors.

B. *Type-II*

Fig. 3 shows the proposed type-II converter. In the type-I n-unit converter, the inductors L_{4x-3} and L_{4x} flow the output current for $i_o > 0$, and the inductors L_{4x-2} and L_{4x-1} flow the output current for $i_o < 0$, where x (=1, ..., n) represents the number of unit in the n-unit cascaded converter. Therefore, the inductors L_3 and L_{4n-2} in the type-I converter can be integrated into one inductor $L_{3,4n-2}$ as depicted in the type-II converter. Similarly, the inductors L_4 and L_{4n-3} in the type-I converter can be integrated into one inductor $L_{4,4n-3}$ in the type-II converter.

The proposed converters are similar in the structure to the conventional cascaded H-bridge inverter. Thus, the input voltages in each unit cell are supplied by separate ac sources, which

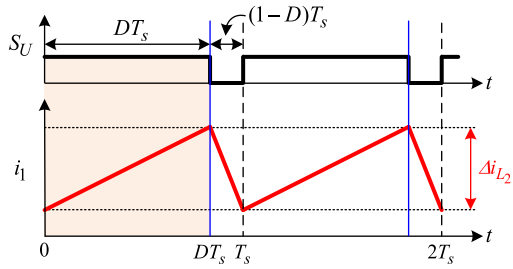

Fig. 7. Gate signals and inductor current ripple of the 2-unit cascaded converter without phase-shift control.

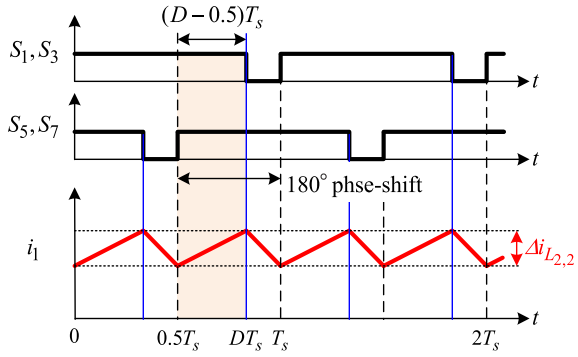

Fig. 8. Gate signals and inductor current ripple of the 2-unit cascaded converter with phase-shift control for $0.5 \leq D \leq 1$.

are provided by a multiwinding transformer. The transformer also provides galvanic isolation. Ideally, each voltage source has the same phase and magnitude, but practically small mismatch can occur. The proposed converters have equivalently parallel-input–series-output structure. Thus, no voltage-balancing problem exists for small mismatches among the unit cells, and does not require dynamic balancing control strategies [14]. The dynamic balancing control strategy is used for multilevel dc–ac or ac–ac converters having voltage-balancing problems [11]–[13].

MOSFETs have fast switching, low switching loss, and nearly resistive conduction voltage drop; thus, MOSFETs allow higher switching frequency than the insulated-gate bipolar transistor. However, the reverse recovery of the MOSFET body diode is poor. Therefore, MOSFETs are normally not suggested for the traditional hard-switching converters, especially at high voltages. In the proposed converters, the body diodes of MOSFETs do not conduct; therefore, the aforementioned benefits of MOSFETs can be obtained without the reverse recovery issues of body diode. For the freewheeling of inductor current, externally selected diodes having good reverse-recovery features and low forward-voltage drops can be used. Thus, the proposed converters can improve the efficiency by using MOSFETs and external diodes. In addition, higher switching frequency can be used to reduce the volume of passive components. Due to the absence of current shoot-through related problems in the proposed converters, the PWM dead times can be removed or minimized as well. For this reason, lossy snubbers are not required and the duty ratio can be pushed to the theoretical limit, and the output voltage and current waveforms can be obtained with less distortion. Furthermore, the current/voltage sensors for mode detection are not required; thus, control complexity can be reduced.

III. Operation of the Proposed Dual-Buck AC–AC Converters

The gate signals of the 2-unit cascaded converter without phase-shift control are shown in Fig. 4. S_U and S_L represent the upper (S_{4x-3} and S_{4x-1}) and lower switches (S_{4x-2} and S_{4x}) in each unit and they are complementary. The ON time of S_U is defined as the duty ratio (D) of the converter. Ideally, the proposed converters have two continuous conduction modes as discussed below.

A. Mode 1 $[0 - DT_s]$

In mode 1, as shown in Fig. 5, S_U are ON and S_L are OFF. In this mode, the inductors store energy from the source.

B. Mode 2 $[DT_s - T_s]$

In mode 2, S_U are OFF and S_L are ON. The inductor current freewheels through external diodes during this mode.

Using the flux (volt-sec) balance condition on inductors, voltage gain of the proposed n-unit cascaded converter can be calculated as [27]

$$\frac{v_o}{v_s} = nD. \tag{1}$$

Equation (1) shows that by increasing the number of cascaded units n, the output voltage v_o can be increased while switch voltage stresses remain at the input voltage v_s.

Fig. 5 shows the operation of the 2-unit cascaded converters in mode 1 for $i_o > 0$. As shown in Fig. 5(a), L_4 and L_5 conduct the same current for $i_o > 0$ and are observed to be in series during the conduction; therefore, they are integrated into one inductor $L_{4,5}$ in the type-II converter shown in Fig. 5(b). Similarly, L_3 and L_6 of the type-I converter are integrated into $L_{3,6}$ in the type-II converter.

IV. Reliability and Magnetic Volume Comparison of Type-I and Type-II Converters

A. Reliability Comparison

Ideally, dead and overlap times do not occur in gate signals, but they could occur in practice. Fig. 6 shows the operation in mode 1 when an overlap between S_3 and S_4 occurs. When an overlap occurs in the type-I converter [see Fig. 6(a)], L_3 and L_4 limit the shoot-through current. In addition to the inductors, the voltage drops of the semiconductor devices also oppose the shoot-through current. By defining $L = L_3 = L_4$, the rise in the shoot-through current Δi_{C_2} flowing through S_3 and S_4 can be expressed as

$$\Delta i_{C_2} = \frac{v_{C_2} - 2V_{\mathrm{ds.on}}}{2L} t_o \tag{2}$$

where v_{C_2} is the voltage of capacitor C_2, $V_{\mathrm{ds.on}}$ is the conduction voltage drop of MOSFET, and t_o is the overlap interval between S_3 and S_4. Fig. 6(b) shows the opposition to the shoot-through

TABLE I
INDUCTOR CURRENT RIPPLES

Unit (n)	Current ripple ($\Delta i_{L_{n,N}}$)			
1	$v_o\frac{\left(\frac{1}{D}-1\right)DT_s}{2L+L_f}$, $N=1, 0\le D\le 1$			
2	$v_o\frac{\left(\frac{1}{2D}-1\right)DT_s}{3L+L_f}$, $N=1, 0\le D\le \frac{1}{2}$	$v_o\frac{\left(\frac{1}{D}-1\right)\left(D-\frac{1}{2}\right)T_s}{3L+L_f}$, $N=2, \frac{1}{2}\le D\le 1$		
3	$v_o\frac{\left(\frac{1}{3D}-1\right)DT_s}{4L+L_f}$, $N=1, 0\le D\le \frac{1}{3}$	$v_o\frac{\left(\frac{2}{3D}-1\right)\left(D-\frac{1}{3}\right)T_s}{4L+L_f}$, $N=2, \frac{1}{3}\le D\le \frac{2}{3}$	$v_o\frac{\left(\frac{1}{D}-1\right)\left(D-\frac{2}{3}\right)T_s}{4L+L_f}$, $N=3, \frac{2}{3}\le D\le 1$	
4	$v_o\frac{\left(\frac{1}{4D}-1\right)DT_s}{5L+L_f}$, $N=1, 0\le D\le \frac{1}{4}$	$v_o\frac{\left(\frac{2}{4D}-1\right)\left(D-\frac{1}{4}\right)T_s}{5L+L_f}$, $N=2, \frac{1}{4}\le D\le \frac{2}{4}$	$v_o\frac{\left(\frac{3}{4D}-1\right)\left(D-\frac{2}{4}\right)T_s}{5L+L_f}$, $N=3, \frac{2}{4}\le D\le \frac{3}{4}$	$v_o\frac{\left(\frac{1}{D}-1\right)\left(D-\frac{3}{4}\right)T_s}{5L+L_f}$, $N=4, \frac{3}{4}\le D\le 1$

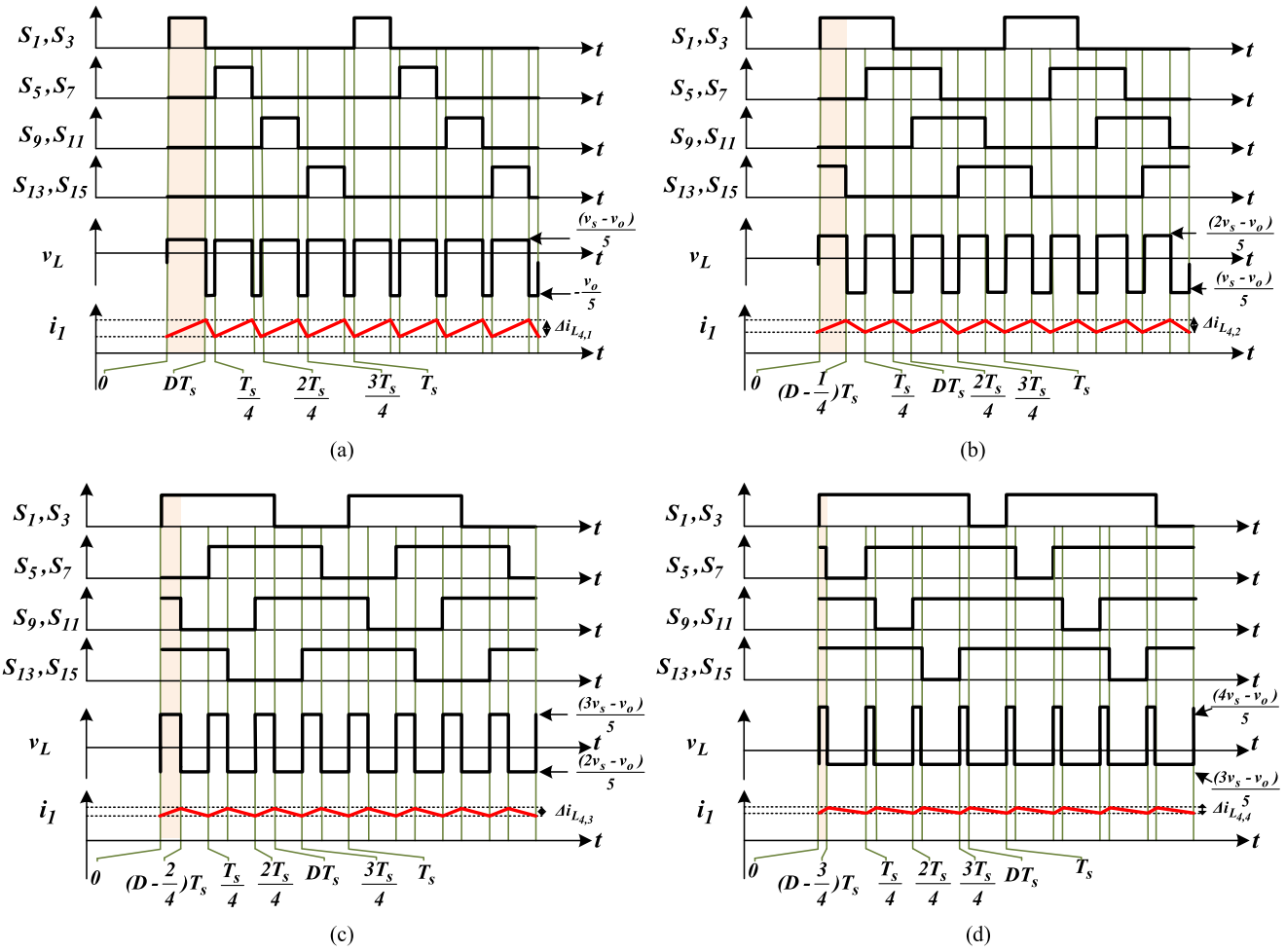

Fig. 9. Key waveforms of the 4-unit cascaded converter with phase-shift control. (a) $0 \le D \le 0.25$. (b) $0.25 \le D \le 0.5$. (c) $0.5 \le D \le 0.75$. (d) $0.75 \le D \le 1$.

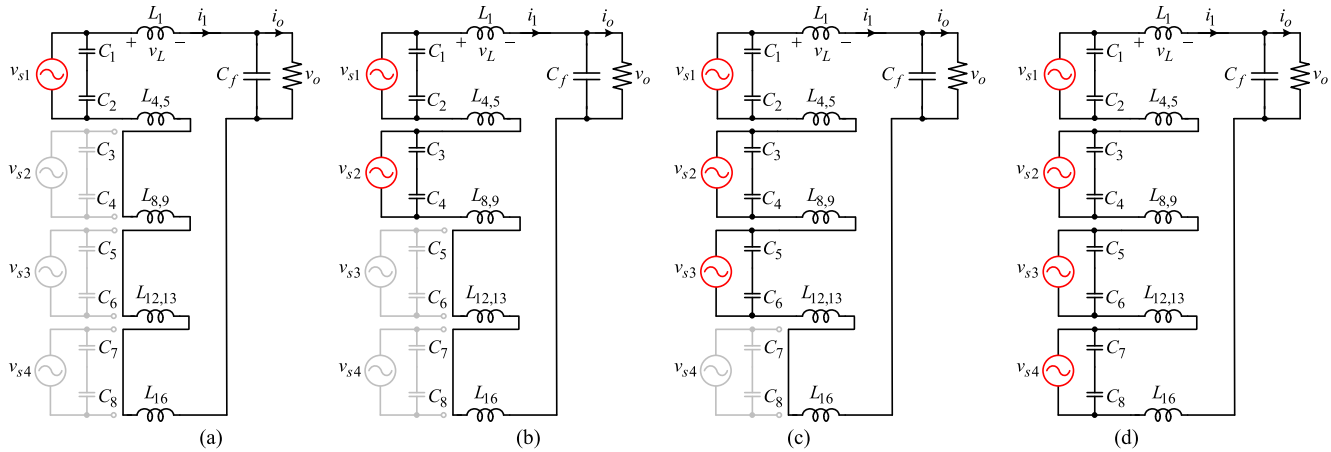

Fig. 10. Equivalent circuit diagrams of the 4-unit cascaded converter with phase-shift control for $i_o > 0$. (a) DT_s interval during $0 \le D \le 0.25$. (b) $(D-0.25)T_s$ interval during $0.25 \le D \le 0.5$. (c) $(D-0.5)T_s$ interval during $0.5 \le D \le 0.75$. (d) $(D-0.75)T_s$ interval during $0.75 \le D \le 1$.

TABLE II
ELECTRICAL SPECIFICATIONS

Output voltage	2-unit	352 Vrms/60 Hz
	3-unit	528 Vrms/60 Hz
	4-unit	704 Vrms/60 Hz
Input voltage		220 Vrms/60 Hz
Output power	2-unit	0.75 kW
	3-unit	1.7 kW
	4-unit	3 kW
Switching frequency		50 kHz
MOSFET		47N60CFD
Diode		RHRG3060
Inductor		100 μH
Leg capacitor		1.5 μF
Output capacitor		0.47 μF

current in the type-II converter. As explained, the inductors $L_{3,6}$ and $L_{4,5}$ are the combination of inductors L_3 and L_6, and L_4 and L_5, respectively. Therefore, the inductance of each integrated inductor $L_{3,6}$ and $L_{4,5}$ is 2*L*. From Fig. 6(b), the rise in the current can be expressed as

$$\Delta i_{C_2} = \frac{v_{C_2} - 3V_{\text{ds.on}} - V_d}{4L} t_o \tag{3}$$

where V_d is the voltage drop of diode.

From (2) and (3), it is evident that the type-II converter can provide more opposition to the shoot-through current than the type-I converter.

B. Magnetic Volume Comparison

The type-II converter requires (*2n–2*) less inductors than the type-I converter. As given by (2), in the type-I converter, *2L* inductance opposes the rise in the shoot-through current, while in the type-II converter, *4L* inductance opposes the rise in the shoot-through current. Therefore, for the same opposition to the shoot-through current, the inductance of each integrated inductor in the type-II converter can be reduced to the same inductance of separate inductor (shoot-through limiting inductors) in the type-I converter. Thus, the overall magnetic volume can be reduced significantly with the type-II converter.

In this paper, the type-II cascaded converter is considered because of its obvious advantages over the type-I converter, and all the shoot-through-limiting inductors are assumed to have the same inductance value of *L*.

V. PHASE-SHIFT CONTROL AND CURRENT RIPPLE ANALYSIS

A. Inductor Current Ripple Without Phase-Shift Control

Fig. 4 shows the gate signals of the 2-unit converter and Fig. 5(b) shows the operation during the DT_s interval. Fig. 7 shows the inductor current ripple Δi_{L_2}. As shown in Fig. 5(b), the inductors L_1, $L_{4,5}$, L_8, and L_f are in series for $i_o > 0$, and the inductors L_2, $L_{3,6}$, L_7, and L_f are in series for $i_o < 0$. Therefore, Δi_{L_2} without phase-shift control can be expressed as

$$\Delta i_{L_2} = \frac{(2v_s - v_o)}{3L + L_f} DT_s = \frac{(1-D)}{3L + L_f} v_o T_s. \tag{4}$$

Similarly, the inductor current ripple Δi_{L_n} of the *n*-unit cascaded converter can be expressed as

$$\Delta i_{L_n} = \frac{(1-D)}{(n+1)L + L_f} v_o T_s. \tag{5}$$

From (5), it is found that all the shoot-through-limiting inductors serve as filter inductor. Thus, the output filter inductor L_f can be removed if n or L is large enough, and (5) can be rewritten as

$$\Delta i_{L_n} = \frac{(1-D)}{(n+1)L} v_o T_s. \tag{6}$$

B. Inductor Current Ripple With Phase-Shift Control

With the phase-shift control, the gate signals in the *n*-unit cascaded converter are phase-shifted by 360°/*n*. Fig. 8 shows the gate signals and the inductor current ripple ($\Delta i_{L_{2,2}}$) of the

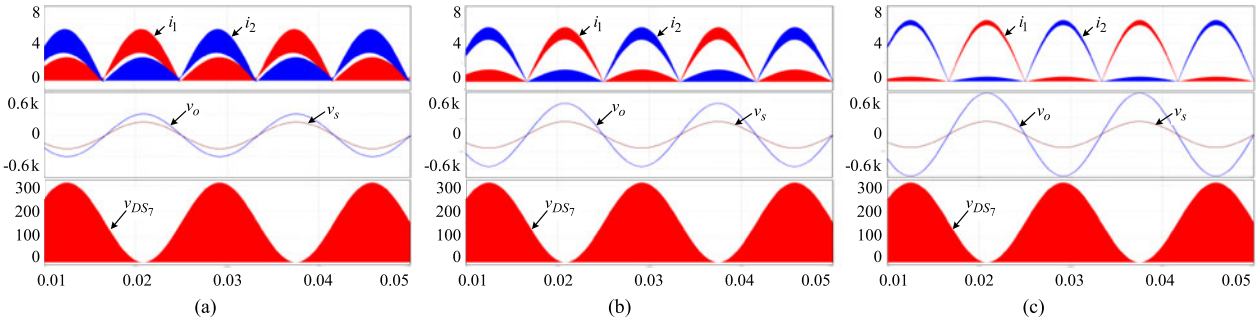

Fig. 11. Simulation results of the proposed cascaded converter. (a) 2-unit. (b) 3-unit. (c) 4-unit.

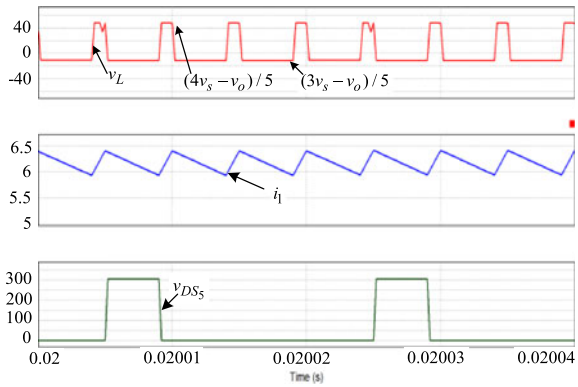

Fig. 12. Inductor voltage and current ripple of the 4-unit cascaded converter in switching cycle.

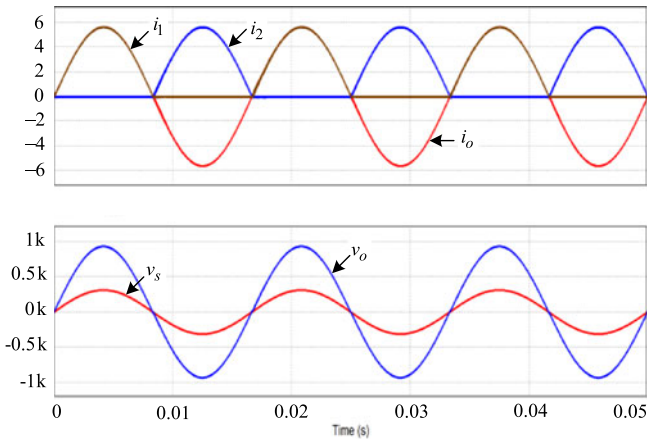

Fig. 13. Simulation results of the 4-unit cascaded converter with partially inductive load when $D = 0.75$.

2-unit cascaded converter. The gate signals are phase-shifted by 180°. The shaded portion of Fig. 8 corresponds to the rise of i_1 shown in Fig. 5(b). The inductor current ripple is significantly reduced with the phase-shift control as observed from Figs. 7 and 8. From Figs. 5(b) and 8, $\Delta i_{L_{2,2}}$ can be derived as

$$\Delta i_{L_{2,2}} = \frac{\left(\frac{1}{D} - 1\right)\left(D - \frac{1}{2}\right)}{3L + L_f} v_o T_s. \tag{7}$$

The n-unit cascaded converter has n different inductor current ripples and each inductor current ripple is represented by N

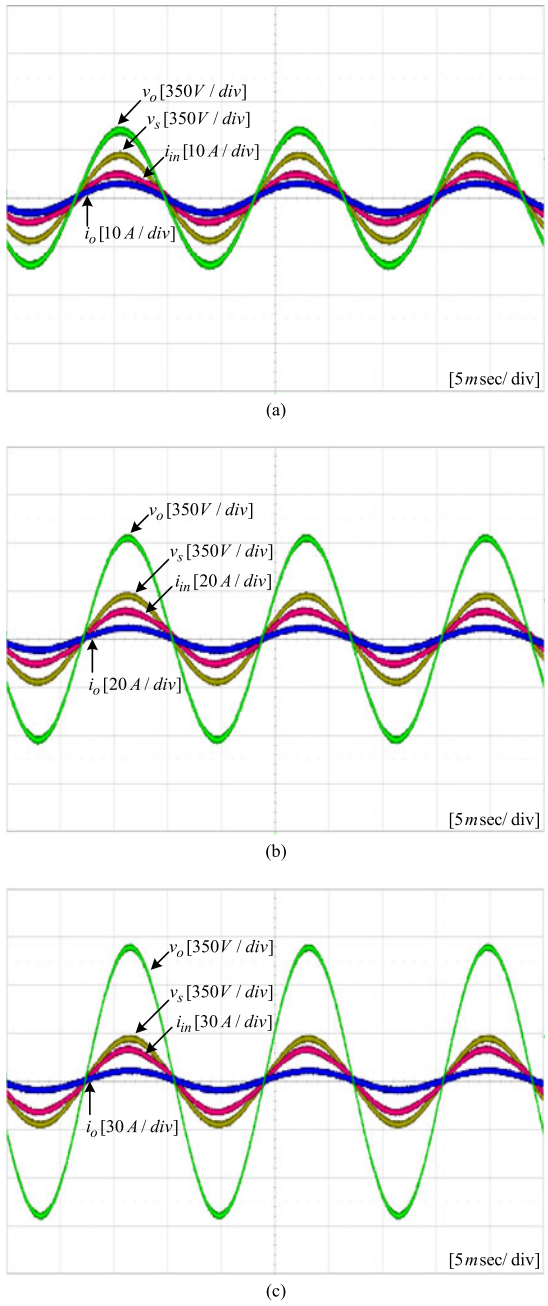

Fig. 14. Input and output voltages and currents waveforms. (a) 2-unit (Po = 0.75 kW). (b) 3-unit (Po = 1.7 kW). (c) 4-unit (Po = 3 kW).

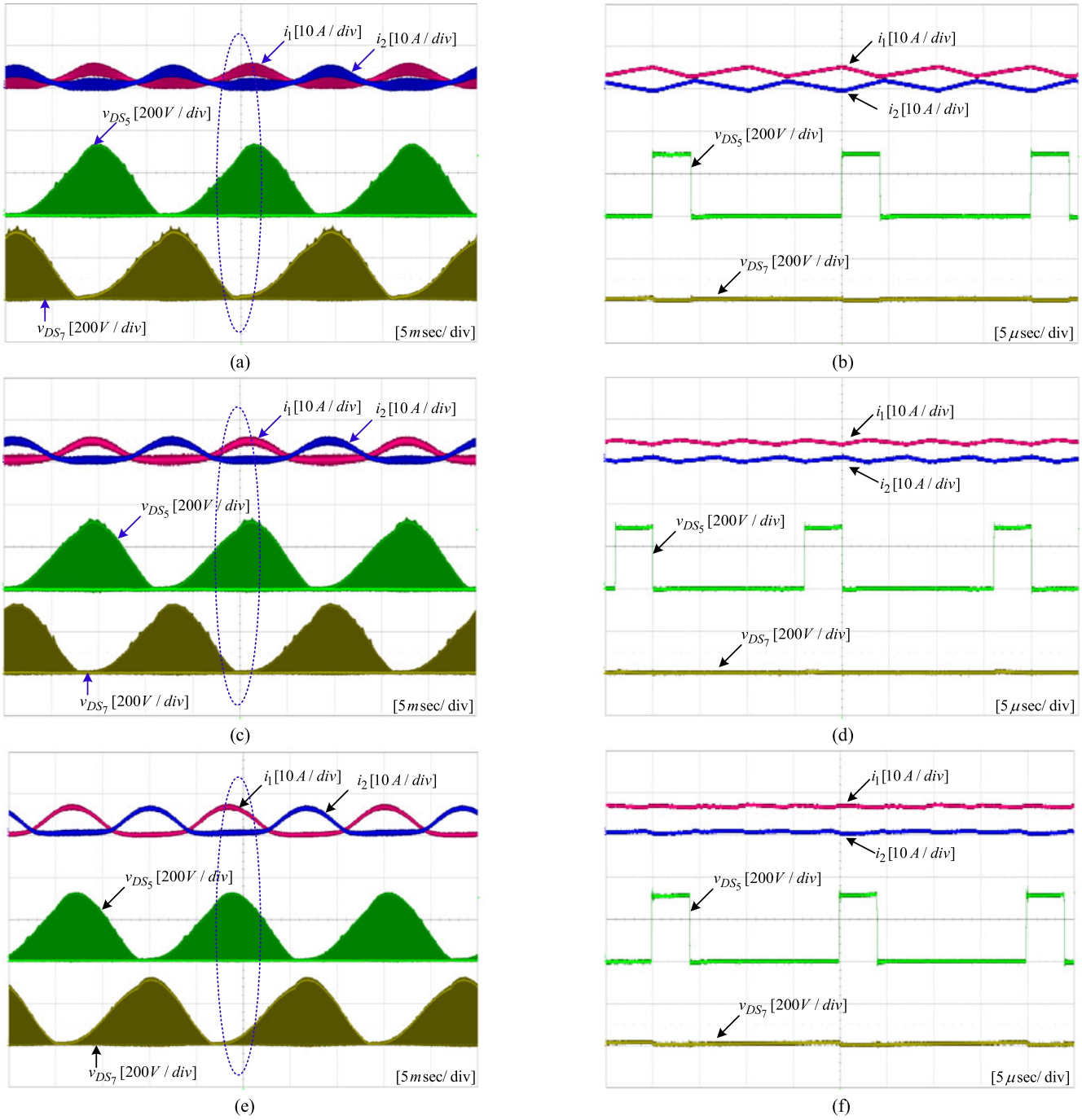

Fig. 15. Inductor currents and drain–source voltage waveforms of the proposed converter. (a) 2-unit (Po = 0.75 kW). (b) Expanded waveforms of (a). (c) 3-unit (Po = 1.7 kW). (d) Expanded waveforms of (c). (e) 4-unit (Po = 3 kW). (f) Expanded waveforms of (e).

in this paper as given in Table I. The first inductor current ripple is defined within the interval $0 \le D \le 1/n$. The second one is defined within the interval $1/n \le D \le 2/n$, and so on. The generalized inductor current ripple $\Delta i_{L_{n,N}}$ of the n-unit cascaded converter can be obtained as

$$\Delta i_{L_{n,N}} = \frac{\left(\frac{N}{nD} - 1\right)\left(D - \frac{N-1}{n}\right)}{(n+1)L + L_f} v_o T_s. \tag{8}$$

For example, the 4-unit cascaded converter has four different inductor current ripples as given in Table I. The first inductor current ripple $\Delta i_{L_{4,1}}$ is obtained by substituting $n = 4$ and $N = 1$ in (8), the second one $\Delta i_{L_{4,2}}$ is obtained by substituting $n = 4$ and $N = 2$, and so on.

Each inductor current ripple becomes maximum when v_o is the maximum and D is mean value during the corresponding interval. For the n-unit cascaded converter, the inductor current

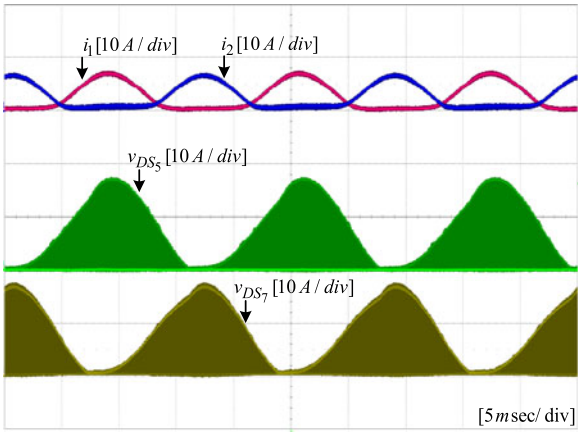

Fig. 16. Inductor currents and drain–source voltage waveforms of the 4-unit cascaded converter at 3 kW when $D = 0.75$.

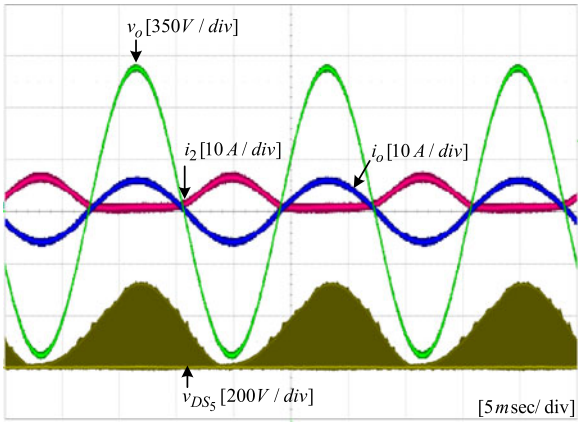

Fig. 17. Experimental waveforms of the 4-unit cascaded converter using a partially inductive load ($R_L = 165\,\Omega,\ L = 10$ mH) at 3 kW when $D = 0.8$.

ripple becomes zero at n different values of D for $0 \le D \le 1$, which are $D = 1/n$, $D = 2/n$, $\ldots$, $D = (n-1)/n$, $D = 1$.

C. Inductor Current Ripple Analysis of the 4-Unit Cascaded Converter

The key waveforms for different values of D are shown in Fig. 9, and the equivalent circuit diagrams during the rise time of inductor current are shown in Fig. 10. The four different inductor current ripples ($\Delta i_{L_{4,1}}$, $\Delta i_{L_{4,2}}$, $\Delta i_{L_{4,3}}$, and $\Delta i_{L_{4,4}}$) shown in Fig. 9 can be derived as given in Table I. The maximum inductor current ripples occur when D is equal to mean values of the corresponding interval, i.e.,$(0 + 0.25)/2$, $(0.25 + 0.5)/2$, $(0.5 + 0.75)/2$, and $(0.75 + 1)/2$. On the other hand, the inductor current ripples become zero when D is equal to 0.25, 0.5, 0.75, and 1. Considering $L_f = 0$, during the DT_s interval in $0 \le D \le 0.25$, the inductor voltage v_L is $(v_s - v_o)/5$ instead of $(v_s - v_o)$[see Fig. 9(a)]. This is because the five inductors are always in series and they share the voltage as shown in Fig. 10. Similarly, as shown in Fig. 10, for $0.25 \le D \le 0.5$, $0.5 \le D \le 0.75$, and $0.75 \le D \le 1$, v_L is $(2v_s - v_o)/5$, $(3v_s - v_o)/5$, and $(4v_s - v_o)/5$, respectively.

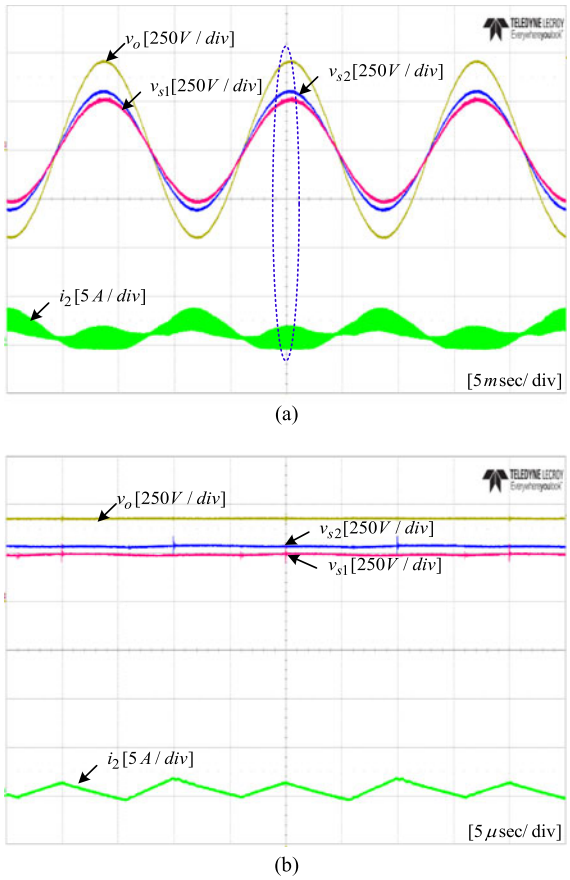

Fig. 18. Experimental results of the 2-unit cascaded converter with inconsistent input voltages. (a) Input and output voltages, and inductor current. (b) Expanded waveforms of (a).

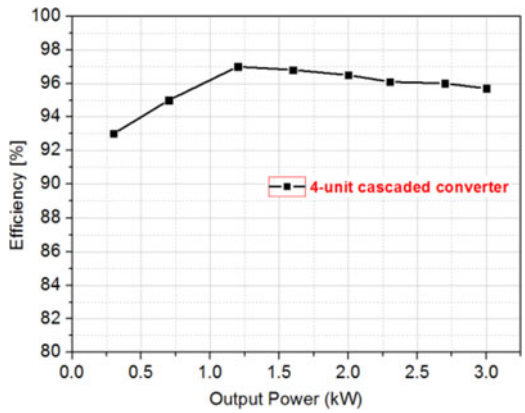

Fig. 19. Measured efficiency of the proposed 4-unit cascaded converter.

VI. Comparative Simulation Results

The electrical specifications of the proposed type-II converter are given in Table II. The input ac voltages in cascaded units are supplied by a multiwinding transformer. The shoot-through-limiting inductors serve as filter inductors; therefore, L_f is not used. The load resistance in each case is 165 Ω. Fig. 11(a) shows waveforms of the inductor currents i_1 and i_2, input voltage v_s, output voltage v_o, and drain–source

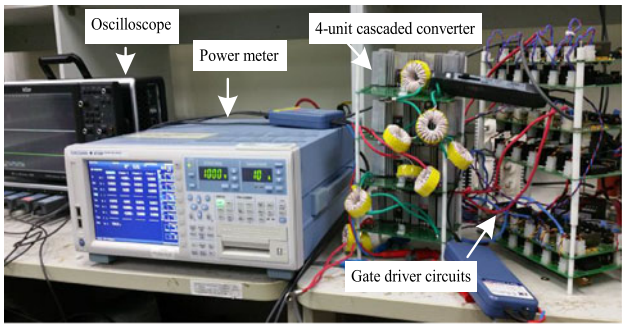

Fig. 20. Experimental setup.

voltage v_{DS_7} of switch S_7 in the 2-unit cascaded converter when $D = 0.8$.

Fig. 11(b) and (c) shows the same waveforms for 3-unit and 4-unit cascaded converters, respectively. The output power and v_o increase with the number of cascaded units, but the switch voltage stresses are always equal to the input voltage for all three cases. It is evident from Fig. 11 that the inductor current ripples of the 4-unit cascaded converter are significantly smaller than those of the 2-unit and 3-unit cascaded converters.

Fig. 12 shows the maximum and minimum inductor voltages and they are close to the theoretical values in Fig. 9(d).

As expected, the effective switching frequency of the 4-unit cascaded converter is increased to 200 kHz, which is four times of the actual switching frequency of the converter.

Fig. 13 shows the simulation results of the 4-unit cascaded converter with partially inductive load ($R_L = 165\,\Omega$, $L_L = 10\,\mathrm{mH}$) and $D = 0.75$. Both the inductor and output current ripples are zero due to the interleaving (or phase-shifting) effect explained in Section IV.

VII. Comparative Experimental Results

To prove the validity and advantages of the proposed type-II converter with phase-shift control, detailed experimental results of the 2-unit, 3-unit, and 4-unit cascaded converters are presented and compared in this section. Similar to the simulations results, ac voltages are supplied from a multiwinding transformer and L_f is not used. The PWM signals are generated using a DSP TMS320F28335.

Fig. 14 shows waveforms of i_o, v_o, v_s, and input current of ac source i_{in} when $D = 0.8$. For each additional unit, converter output voltage increases by 176 Vrms. Therefore, v_o of the 2-unit, 3-unit, and 4-unit cascaded converters are 352, 528, and 704 Vrms, respectively.

The output waveforms have low distortion because of the absence of lossy snubber circuits and dedicated PWM strategies.

Fig. 15 shows the comparative experimental results of the inductor currents and the drain-source voltages v_{DS_5} and v_{DS_7} of switches S_5 and S_7 when $D = 0.8$. The expanded waveforms of Fig. 15(a), (c), and (e) are shown in Fig. 15(b), (d), and (f), respectively. The effective switching frequencies of the 2-unit, 3-unit and 4-unit cascaded converters are 100, 150, and 200 kHz, respectively. The inductor current ripple comparison in Fig. 15 shows that the current ripples of the 4-unit converter are significantly smaller than those of the 2-unit and 3-unit converters.

Fig. 16 shows the experimental results when $D = 0.75$ and they are experimental verification of the simulation results in Fig. 13. Due to the phase-shifting (or interleaving) effect, inductor current ripples are almost zero. Fig. 17 shows the experimental results of the proposed 4-unit cascaded converter with a partially inductive load when $R_L = 165\,\Omega$ and $L_L = 10\,\mathrm{mH}$. All the experimental waveforms are clean and there is no apparent current or voltage spike.

Fig. 18 shows the experimental results of the 2-unit cascaded converter for the inconsistent sources. For the inconsistent sources, the inductor current ripple has changed slightly. However, the phase-shift control is still valid, and the converter has no balancing problem because of input-parallel and series-output connection.

The measured efficiency of the proposed 4-unit cascaded converter for $D = 0.8$ is shown in Fig. 19. Fig. 20 shows the experimental setup of the proposed converter.

VIII. Conclusion

This paper presented a new series of highly reliable cascaded ac–ac converters that produce high output voltages using standard low-voltage rating semiconductor devices. The risks of failure due to high *dv*/*dt* and *di*/*dt* can be solved with the proposed converter. Furthermore, MOSFETs can be used as switching devices without the risk of device failure, and the use of current/voltage polarity sensors and lossy snubbers can be avoided.

The cascaded units in the proposed converter shared inductors, which decreased the total number of inductors. To further decrease magnetic volume of the proposed converter, phase-shift control was presented. It increased the equivalent switching frequency of the converter by the number of cascaded units. The topology derivation, detailed circuit analysis, phase-shift control, and inductor current ripple analysis was presented. To prove the advantages of the proposed topology, hardware prototypes of 2-unit, 3-unit, and 4-unit cascaded converters were fabricated and tested at different powers. By comparing the simulation and experimental results of the 2-unit, 3-unit, and 4-unit cascaded converters, the advantages and benefits of the proposed cascaded converter were validated.

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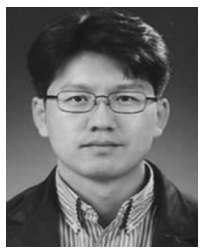

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