An Investigation of Temperature-Sensitive Electrical Parameters for SiC Power MOSFETs

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***Abstract*—This paper examines dynamic temperature-sensitive electrical parameters (TSEPs) for SiC MOSFETs. It is shown that the switching rate of the output current (dI_{DS}/dt) coupled with the gate current plateau (I_{GP}) during turn-ON could be an effective TSEP under specific operating conditions. Both parameters increase with the junction temperature of the device as a result of the negative temperature coefficient of the threshold voltage. The temperature dependency of dI_{DS}/dt has been shown to increase with the device current rating (due to larger input capacitance) and external gate resistance (R_G^{EXT}). However, as dI_{DS}/dt is increased by using a small R_G^{EXT}, parasitic inductance suppresses the temperature sensitivity of the drain and gate current transients by reducing the "effective gate voltage" on the device. Since the temperature sensitivity of dI_{DS}/dt is at the highest with maximum R_G^{EXT}, there is a penalty from higher switching losses when this method is used in real time for junction temperature sensing. This paper investigates and models the temperature dependency of the gate and drain current transients as potential TSEPs for SiC power MOSFETs.**

***Index Terms*—Power MOSFETs, power semiconductor devices, switching transients, temperature measurement.**

I. Introduction

CONDITION monitoring of power electronic devices involves ascertaining the state of health of the devices during field operation. This can be used, through lifetime estimation and operational management, for prolonging the service of the converter and minimizing the damage. The junction temperature of the power device is often used as an indicator of device condition [1]. Devices that have been subjected to numerous power and temperature cycles typically exhibit higher junction-to-case thermal resistances resulting from solder cracks, die attach voiding and may also exhibit higher source and gate contact resistance [2]. This is due to the constant thermo-mechanical stresses resulting from the mismatch in the coefficients of thermal expansion at critical interfaces like the semiconductor/die-attach/substrate interfaces or the wirebond/source metal interface. The most effective and direct way of sensing the condition of the device is to integrate temperature and current sensors directly with the chip. This is usually done for industrial organizations using custom made power devices fabricated specifically for targeted applications; hence, such design solutions are usually not available for generic power devices. Another effective method of condition monitoring is using temperature-sensitive electrical parameters (TSEPs) to estimate the junction temperature indirectly through the known temperature dependence of an electrical parameter. Using TSEPs, the temperature can be estimated during online operation and off-line operation. This is a wide area of research, with several TSEPs proposed and evaluated [3]. In [4]–[7], the threshold voltage is proposed as a TSEP by using the known negative temperature coefficient of the threshold voltage to estimate the junction temperature during device switching. However, the time resolution required by the measurement instruments coupled with the background noise makes this a difficult technique to implement especially since two sensors are needed. Other reports have cited the IGBT on-state voltage drop as a TSEP at both low and high currents [8]–[10] and results have shown that it can be an effective way for monitoring the degradation of the power module [11]. In [12], the discharge time of the Miller capacitance is used as a TSEP and a circuit capable of detecting its temperature dependency is presented. However, using the Miller capacitance discharge time in silicon carbide (SiC) is complicated by the fact that SiC devices typically have significantly smaller parasitic capacitance than silicon IGBTs/MOSFETs because of the smaller die size. Furthermore, this technique is difficult to implement in SiC MOSFETs since the turn-OFF dV/dt is not as temperature sensitive as it is in silicon IGBTs [13]. The fast switching rate in SiC MOSFETs coupled with parasitic inductances induces electromagnetic oscillations in the voltage and current characteristics [14]. Furthermore, oscillations in the drain-source voltage resulting from source inductance are transmitted back to the gate voltage characteristics through the Miller capacitance [15]; hence, monitoring the gate transient as a TSEP is complicated. In [16], harmonic analysis of an IGBT converter output is used as a TSEP, whereas in [17] and [18], the temperature dependency of the gate current in MOSFETs and IGBTs has been used as a TSEP for condition monitoring with promising results demonstrated. In the case of Si MOSFETs, the switching rate during turn ON was evaluated as a TSEP in [19]. The characteristics of SiC MOSFETs suggest that the

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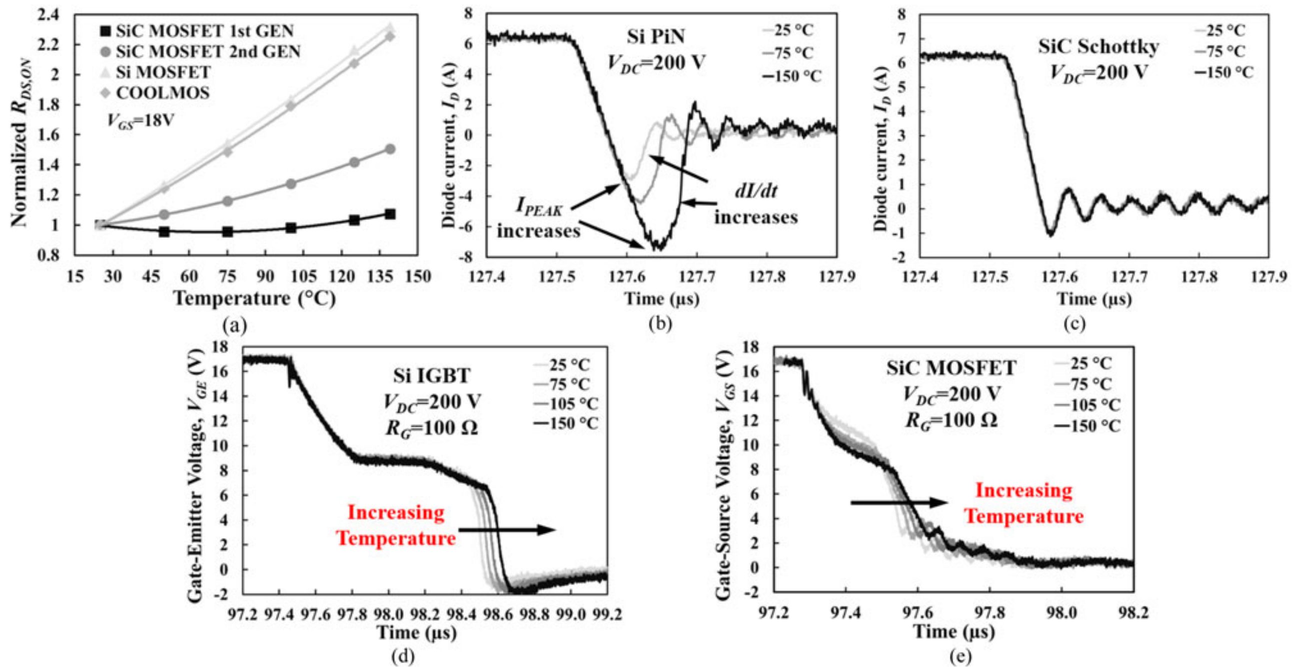

Fig. 1. (a) ON-state resistance as a function of temperature for different MOSFET technologies; (b) silicon PiN diode reverse recovery characteristics at different temperatures; (c) SiC Schottky diode turn-OFF characteristics at different temperatures; (d) silicon IGBT gate voltage during turn OFF at different temperatures, and (e) SiC MOSFET gate voltage during turn OFF at different temperatures.

dynamic properties of SiC during turn ON can be a suitable TSEP [20]–[22].

SiC MOSFETs have demonstrated higher energy conversion efficiency and power density through reduced conduction and switching losses based on the material properties of SiC [23]. SiC devices are gaining popularity and if their potential is to be maximized, the question of condition monitoring will become an important topic. Due to the wide bandgap in SiC (∼3.3 eV), the intrinsic carrier concentration is lower and more thermal energy is needed to excite carriers across the bandgap. As a result, SiC devices allow operation at high temperature exceeding 200 °C. This fact makes condition monitoring of SiC MOSFETs using TSEPs a challenging task. The temperature dependency of the on-state resistance in SiC is not linear [24] and is low. Fig. 1(a) shows the measured ON-state resistances of different MOSFET technologies at different temperatures including two 1.2 kV SiC MOSFETs (from Cree/Wolfspeed with datasheet reference CMF10120D and C2M0160120D), a 1.2 kV silicon MOSFET (from IXYS with datasheet reference IXFX20N120P) and a 900 V CoolMOS device (from Infineon with datasheet reference IPW90R340C3). It can be seen that the SiC MOSFETs show the lowest temperature sensitivity as far as the ON-state resistance is concerned, with the Cree/Wolfspeed second generation device showing higher temperature sensitivity than the first generation. Fig. 1(b) shows the reverse recovery characteristics of a silicon PiN diode during turn OFF at different temperatures where it can be seen that the reverse recovery charge increases with temperature [25]. This is due to the positive temperature coefficient of minority carrier lifetime which has the effect of increasing the stored charge in the diode drift region. Fig. 1(c) shows the turn-OFF transient of the SiC Schottky diode at different temperatures where it can be seen that there is no noticeable temperature sensitivity in the switching transients. Fig. 1(d) presents the gate voltage (V_{GE}) turn-OFF transient of a 1.2 kV Si IGBT, where the temperature sensitivity of the discharge of the Miller capacitance can be easily observed, especially when a large gate resistance is used. The temperature sensitivity of the IGBT V_{GE} turn-OFF transient results from the bipolar nature of the device since minority carrier lifetime increases with temperature and the rate of the V_{CE} transient depends on the lifetime. In the case of SiC MOSFETs, as shown in the turn-OFF V_{GS} transient in Fig. 1(e), the significantly faster V_{DS} transient resulting from a much lower Miller capacitance results in a nonflat Miller plateau [20]. Furthermore, the unipolar nature of the device means there is less temperature sensitivity since there are no minority carriers.

The switching energy in SiC actually reduces as the temperature increases, thereby causing the device to dissipate less power during operation [21]. Hence, using the losses as a TSEP is therefore not straightforward in SiC MOSFETs. In this paper it is shown that the temperature dependency of the current commutation rate (dI_{DS}/dt) and the gate current plateau I_{GP} can be the effective TSEPs. However, this becomes more challenging at high current commutation rates because parasitic inductances affect the temperature sensitivity of the gate and drain current transients. This paper will show that the temperature dependency of dI_{DS}/dt and the gate current depends on the current rating (the die size) of the device as well as the external gate resistance. This dependency is based on the device capacitances and internal gate resistances which affect dI_{DS}/dt and its temperature sensitivity through parasitic inductance. Section II analyses the gate/drain current and its temperature dependency through

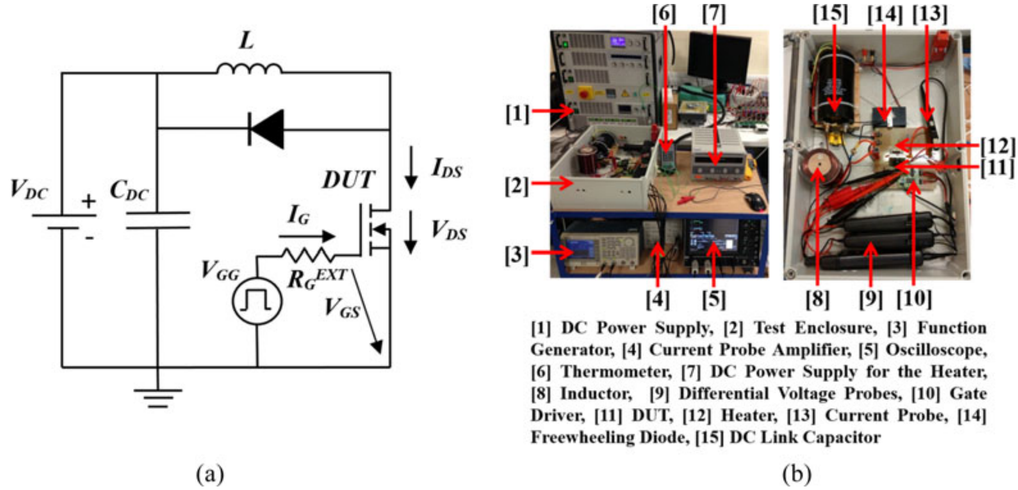

Fig. 2. (a) Electrical schematic of the experimental setup and (b) experimental setup.

analytical modeling and experimental measurements. Section II also discusses and models the impact of parasitic inductance on the temperature sensitivity of the $I_{\rm DS}$ turn-ON transient. Section III discusses the load current and dc-link voltage dependency of $dI_{\rm DS}/dt$ and the gate current plateau ($I_{\rm GP}$) and shows how it can be decoupled from its temperature sensitivity while Section IV concludes the paper.

II. Analytical Modeling of the Gate and Drain Current Temperature Sensitivity

The double pulse test setup shown in Fig. 2 has been used for characterizing the turn-ON transient of SiC power MOSFETs at different temperatures, using a small temperature-controlled heater attached to the discrete device. A 2 mH inductor L, a 470 μF dc-link capacitor $C_{\rm dc}$, and a 1.2 kV SiC Schottky diode with datasheet reference C4D10120A from Cree/Wolfspeed are the other elements of the test configuration. The electrical schematic and the test rig used are presented in Fig. 2(a) and (b), respectively. The measurements were performed at a dc-link voltage $V_{\rm dc} = 200$ V, load current $I_{\rm DS} = 9$ A, gate driver voltage $V_{\rm GG} = 0/18$ V, and a range of external gate resistances from $R_G^{EXT} = 10{-}220\ \Omega$. A Tektronix current probe model TCP312 in conjunction with a Tektronix probe amplifier model TCPA300 were used for measuring the current. The current rating of the probe is 30 A dc, with a bandwidth of 100 MHz and a rise time of 3.5 ns. The oscilloscope used for capturing the data was a Lecroy Wavesurfer 104MXs-B, with a bandwidth of 1 GHz and a rise time of 300 ps.

It is a general observation that the current commutation rate ($dI_{\rm DS}/dt$) increases with temperature during the turn-ON transient of SiC power MOSFETs [20], [21] however what has not been adequately investigated is the impact of temperature on the gate current plateau and how this, together with the turn-ON $dI_{\rm DS}/dt$ can be used as a TSEP for junction temperature sensing in SiC power MOSFETs. The turn ON of a MOSFET is described in [26]–[28]. The idealized plots of the gate current (I_G), the drain-source current ($I_{\rm DS}$), and the gate-source voltage ($V_{\rm GS}$) transients for an SiC MOSFET during turn ON at a low (25 °C) and high (150 °C) junction temperatures are shown in Fig. 3(a). Fig. 3(b) shows experimental measurements for a 1.2 kV/42 A SiC MOSFET from Cree/Wolfspeed with datasheet reference CMF20120D. As can be seen from the measurements, the turn ON $dI_{\rm DS}/dt$ increases with temperature, the gate-current plateau ($I_{\rm GP}$) increases with temperature and the gate voltage plateau ($V_{\rm GP}$) reduces with increasing temperature. During the turn-ON transient of the SiC MOSFET, the total gate current supplied by the gate driver is given by the time dependent combination of three stages described by (1), where I_G is the total gate current, $C_{\rm GS}$ is the gate source capacitance, $C_{\rm GD-HV}$ is the Miller capacitance at high drain voltage, $C_{\rm GD-LV}$ is the Miller capacitance at low drain voltage, $V_{\rm GG}$ is the gate drive voltage, $R_G^{\rm EXT}$ is the external gate resistance, $R_G^{\rm INT}$ is the internal gate resistance, and $V_{\rm GP}$ is the plateau voltage, see (1) shown at the bottom of this page.

Assuming that the MOSFET gate is triggered at time t_0 according to Fig. 3(a), between time t_0 and t_1, the gate current charges the input capacitance $C_{\rm ISS}$, which is given by the sum

$$I_G = \begin{cases} \dfrac{C_{\rm GS}}{(C_{\rm GS}+C_{\rm GD-HV})}\dfrac{V_{\rm GG}}{(R_G^{\rm INT}+R_G^{\rm EXT})}e^{-\frac{t-t_0}{(R_G^{\rm INT}+R_G^{\rm EXT})(C_{\rm GS}+C_{\rm GD-HV})}} & \text{for } t_0 < t < t_1 \\ \dfrac{V_{\rm GG}-V_{\rm GP}}{R_G^{\rm INT}+R_G^{\rm EXT}} & \text{for } t_1 < t < t_2 \\ \dfrac{C_{\rm GS}}{(C_{\rm GS}+C_{\rm GD-LV})}\dfrac{V_{\rm GG}-V_{\rm GP}}{(R_G^{\rm INT}+R_G^{\rm EXT})}e^{-\frac{t-t_2}{(R_G^{\rm INT}+R_G^{\rm EXT})(C_{\rm GS}+C_{\rm GD-LV})}} & \text{for } t_2 < t < t_3 \end{cases} \quad (1)$$

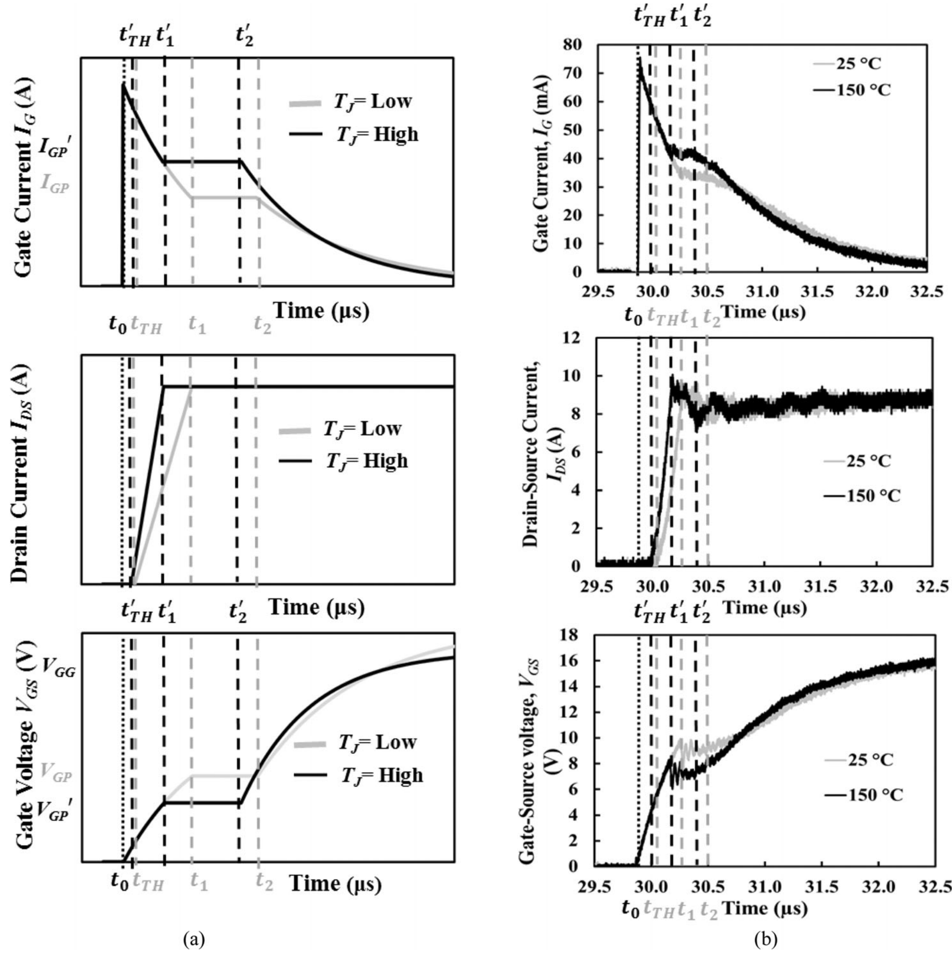

Fig. 3. (a) Idealized I_G, I_{DS}, and V_{GS} turn-ON transients for an SiC MOSFET at different temperatures; (b) measured I_G, I_{DS}, and V_{GS} turn-ON transients for an SiC MOSFET at different temperatures.

of the gate-source capacitance (C_{GS}) and the Miller capacitance (C_{GD})

$$C_{\mathrm{ISS}} = C_{\mathrm{GS}} + C_{\mathrm{GD}}. \tag{2}$$

Depending on the *RC* time constant of the gate transient, V_{GS} will reach V_{TH} at time t_{TH}, which is between t_0 (when the gate is triggered) and t_1 (when $V_{\mathrm{GS}} = V_{\mathrm{GP}}$). The load current starts to rise at time t_{TH} and reaches its maximum at t_1, causing V_{DS} across the MOSFET to fall to its on-state value thereby charging the Miller capacitance between t_1 and t_2. The threshold voltage and time it takes for V_{GS} to rise to V_{TH} ($t_{\mathrm{TH}} - t_0$) have been presented as TSEPs for silicon MOSFETs [19]. Equation (3) models t_{TH}

$$\begin{aligned} t_{\mathrm{TH}} - t_0 &= (R_G^{\mathrm{INT}} + R_G^{\mathrm{EXT}}) C_{\mathrm{ISS}} \ln\left(\frac{V_{\mathrm{GG}}}{V_{\mathrm{GG}} - V_{\mathrm{TH}}}\right) \\ &= (R_G^{\mathrm{INT}} + R_G^{\mathrm{EXT}}) C_{\mathrm{ISS}} \\ &\quad \times \ln\left(\frac{\mathrm{V_{GG}}}{\mathrm{V_{GG}} - \left(\mathrm{V_{TH}}|_{25^\circ\mathrm{C}} - \left|\frac{\mathrm{dV_{TH}}}{\mathrm{dT}}\right| (\mathrm{T_j} - 25)\right)}\right) \end{aligned} \tag{3}$$

As I_{DS} reaches the load current, V_{GS} reaches its plateau value (V_{GP}) and the gate current reaches its plateau value (I_{GP}). The gate voltage plateau (V_{GP}) is given by

$$V_{\mathrm{GP}} = V_{\mathrm{TH}} + \sqrt{\frac{I_{\mathrm{LOAD}} L_{\mathrm{CH}}}{\mu C_{\mathrm{OX}} W_{\mathrm{CH}}}} \tag{4}$$

where μ is the effective mobility, W_{CH} the MOSFET channel width, C_{OX} the gate oxide capacitance density and L_{CH} the MOSFET channel length. The two temperature-sensitive parameters that determine the value of V_{GP} in (4) are the threshold voltage (V_{TH}) and the effective mobility of the electrons in the channel of the MOSFET (μ). V_{TH} reduces with temperature as a result of temperature induced bandgap narrowing, which increases the intrinsic carrier concentration of the semiconductor thereby making the channel easier to invert [26]. The temperature dependency of V_{TH} is given by

$$\frac{dV_{\mathrm{TH}}}{dT} = \frac{d\psi_B}{dT}\left(2 + \frac{1}{c_{\mathrm{OX}}}\sqrt{\frac{\varepsilon_{\mathrm{SiC}} q N_A}{\psi_B}}\right) \tag{5}$$

where

$$\frac{d\psi_B}{dT} \approx \frac{1}{T}\left[\frac{E_g(0)}{2q} - |\psi_B|\right] \tag{6}$$

Ψ_B is the potential difference between the Fermi level and the intrinsic Fermi level, $\varepsilon_{\mathrm{SiC}}$ the dielectric constant of SiC,

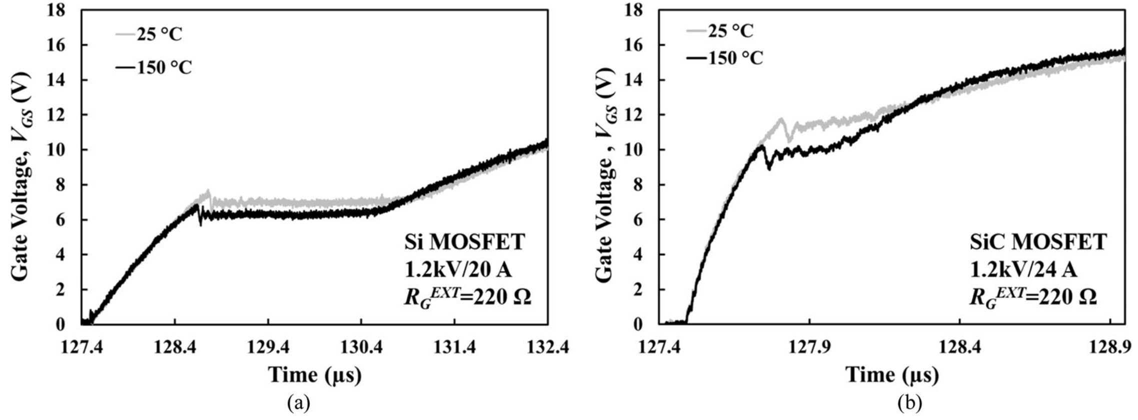

Fig. 4. (a) $V_{\rm GS}$ turn-ON transient for the Si MOSFET at 25 and 150 °C. (b) The $V_{\rm GS}$ turn-ON transient for the SiC MOSFET at 25 and 150 °C.

N_A the doping density, q the electron charge, and $E_g(0)$ is the band-gap energy at $T = 0\,\rm K$. According to the datasheets and previously presented measurements [29], [30] the threshold voltage is higher for Si MOSFETs however, both SiC and Si MOSFETs have a similar $dV_{\rm TH}/dT$. The effective mobility (μ) also reduces with temperature as a result of increased phonon scattering reducing the relaxation time between carrier-to-lattice scattering events. The negative temperature coefficient of $V_{\rm TH}$ will reduce $V_{\rm GP}$ while the negative temperature coefficient of μ will increase $V_{\rm GP}$. Hence, assuming a constant load current, the more dominant parameter will determine the temperature behavior of $V_{\rm GP}$ with temperature. $V_{\rm GP}$ reduces with temperature in SiC MOSFETs while it is less temperature sensitive for Si MOSFETs.

Fig. 4(a) shows the $V_{\rm GS}$ turn-ON transient for a 1.2 kV/20 A Si MOSFET, while Fig. 4(b) shows the same measurements for a 1.2 kV/24 A SiC MOSFET. These measurements where performed with a low $dI_{\rm DS}/dt$ corresponding to an $R_G^{EXT} = 220\,\Omega$. In this figure, some of the characteristics that define the switching of SiC MOSFETs [20] are clearly identified, namely: 1) the higher value of the gate voltage plateau ($V_{\rm GP}$) caused by a lower transconductance compared to the silicon MOSFET; 2) a nonflat Miller plateau compared to the silicon MOSFET; and 3) a significantly reduced $V_{\rm GS}$ transient duration in the SiC MOSFETs as a result of the lower input capacitance compared to the silicon MOSFET. It should, however, be noted that at high $dI_{\rm DS}/dt$, the presence of parasitic inductance in the path of $I_{\rm DS}$ masks the changing behavior of $V_{\rm GP}$ with temperature since the oscillations in I_G, $V_{\rm GS}$, and $V_{\rm DS}$ dominate the measured transient characteristics.

Referring back to Fig. 3, between time t_1 and t_2, the Miller capacitance is charged and the $V_{\rm DS}$ transient occurs. At the end of t_2, the $V_{\rm DS}$ transient is complete and $V_{\rm GS}$ resumes its exponential rise to $V_{\rm GG}$ but with a larger time constant since the Miller capacitance has increased due to its dependency on $V_{\rm DS}$. At higher temperatures, due to the lower threshold voltage, the turn-ON transition times $t_{\rm TH}$', t_1' and t_2' are shifted in time as shown in Fig. 3, indicating that the device turns on sooner. Between time t_0 and t_1 corresponding to the idealized switching transients shown in Fig. 3(a), the gate voltage ($V_{\rm GS}$) and its time derivative is given, respectively, by (7) and (8)

$$V_{\rm GS} = V_{\rm GG}\left(1 - e^{-\frac{t-t_0}{(R_G^{\rm INT}+R_G^{\rm EXT})C_{\rm ISS}}}\right) \quad (7)$$

$$\frac{dV_{\rm GS}}{dt} = \frac{V_{\rm GG}}{(R_G^{\rm INT}+R_G^{\rm EXT})C_{\rm ISS}}e^{-\frac{t-t_0}{(R_G^{\rm INT}+R_G^{\rm EXT})C_{\rm ISS}}} \quad (8)$$

When the gate voltage reaches the threshold voltage $V_{\rm TH}$, the current starts to flow. Between time instants $t_{\rm TH}$ and t_1, assuming the MOSFET drain current is in saturation, the drain-source current ($I_{\rm DS}$) and its time derivative is given by (9) and (10), respectively

$$I_{\rm DS} = \frac{\beta}{2}(V_{\rm GS} - V_{\rm TH})^2 \quad (9)$$

$$\frac{dI_{\rm DS}}{dt} = \beta(V_{\rm GS} - V_{\rm TH})\frac{V_{\rm GG}}{(R_G^{\rm INT}+R_G^{\rm EXT})C_{\rm ISS}} \times e^{-\frac{t-t_0}{(R_G^{\rm INT}+R_G^{\rm EXT})C_{\rm ISS}}} \quad (10)$$

The temperature dependency of the current commutation rate ($dI_{\rm DS}/dt$) during turn ON can be calculated by taking the derivative of (10) with respect to temperature and is given by

$$\frac{d^2 I_{\rm DS}}{dt\cdot dT} = \frac{V_{\rm GG}\,e^{-\frac{t-t_0}{(R_G^{\rm INT}+R_G^{\rm EXT})C_{\rm ISS}}}}{(R_G^{\rm INT}+R_G^{\rm EXT})C_{\rm ISS}} \times\left(\beta\left|\frac{dV_{\rm TH}}{dT}\right| - (V_{\rm GS}-V_{\rm TH})\left|\frac{d\beta}{dT}\right|\right) \quad (11)$$

Given the temperature characteristics of different power MOSFETs, (11) can be used to identify the temperature sensitivity of the switching rate as a potential TSEP for condition monitoring. The switching rate of different MOSFET technologies has been measured and shown as a function of the external gate resistance ($R_G^{\rm EXT}$) in Fig. 5 for 25 and 150 °C measurements. By comparing the switching rate measured at both temperatures, it can be seen that the switching rate of the silicon MOSFET is temperature invariant while that of the SiC MOSFETs increases with temperature for larger $R_G^{\rm EXT}$. The three factors affecting $dI_{\rm DS}/dt$ and its temperature sensitivity, namely, device technol-

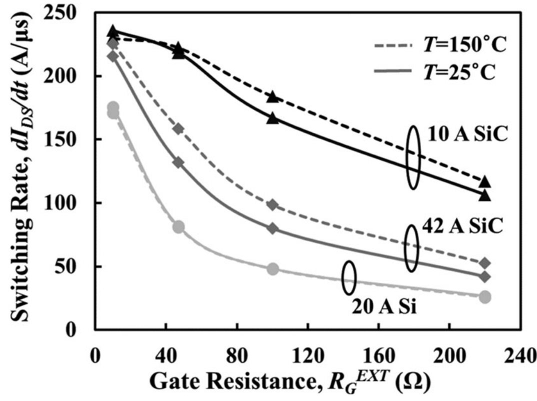

Fig. 5. Measured switching rate as a function of R_G^{EXT} for the different technologies at 25 and 150 °C.

ogy, current rating, and external gate resistance, are evaluated in the following sections.

A. Impact of Device Technology on dI_{DS}/dt as a TSEP

Equation (11) applies to all MOSFET technologies; however, the behavior of dI_{DS}/dt with respect to temperature differs according to the device technology, as the measurements on Fig. 5 show. Measurements from literature and datasheets show that for SiC MOSFETs, the turn-ON dI_{DS}/dt increases with temperature [21], [29], [31], while for silicon MOSFETs devices [32], the turn-ON dI_{DS}/dt is either temperature invariant or decreases with temperature. The reason for this is due to $d\beta/dT$, which is very low in SiC MOSFETs but is negative in silicon MOSFETs. β is dependent on temperature through the effective channel mobility which decreases as temperature increases but can be considered approximately constant for SiC MOSFETs due to its wide bandgap characteristics [33].

Fig. 6(a) and (b) shows the turn-ON drain-source (I_{DS}) and gate (I_G) current transients for a 1.2 kV/ 24 A SiC MOSFET. The measurements were done using an external gate resistance R_G^{EXT} of 220 Ω and it can be seen that the turn-ON dI_{DS}/dt and the gate current plateau both increase with temperature. In the case of silicon and SiC MOSFETs, the drain current transient shifts leftwards in time as the temperature is increased due to the negative temperature coefficient of the threshold voltage causing the device to switch sooner at higher temperatures. In the case of silicon MOSFETs, dI_{DS}/dt does not increase with temperature so the current transients are approximately parallel, since $d\beta/dT$ counteracts dV_{TH}/dT [32], thereby making dI_{DS}/dt less temperature sensitive. However, in SiC MOSFETs, $d\beta/dT$ can be neglected over the temperature range selected [33]; hence, dI_{DS}/dt increases with temperature due to dV_{TH}/dT.

B. Impact Impact of Device Current Rating on dI_{DS}/dt as a TSEP

The turn-ON current commutation rate of the SiC MOSFET has been identified as a potential TSEP. However, the temperature sensitivity of dI_{DS}/dt in SiC power MOSFETs needs to

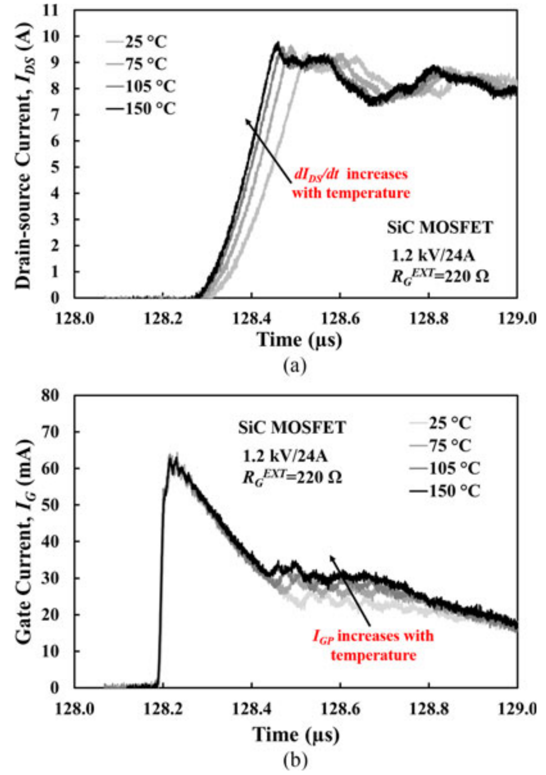

Fig. 6. (a) Drain-source current (I_{DS}) for a 24 A SiC MOSFET during turn-ON at different temperatures. (b) Gate current (I_G) for a 24 A SiC MOSFET during turn-ON at different temperatures.

be investigated as a function of the device current rating. Fig. 7(a) shows the drain-source and gate current transient during turn ON for a 1.2 kV 42 A SiC MOSFET while Fig. 7(b) shows similar measurements for the 1.2 kV/ 10 A SiC MOSFET. In both measurements the external gate resistance used is 220 Ω. It can be seen by comparing Fig. 7(a) and (b) that the temperature sensitivity of dI_{DS}/dt is smaller for the 10 A SiC power MOSFET compared to the 42 A SiC MOSFET. The temperature sensitivity of the gate current plateau (I_{GP}) is also higher for the 42 A MOSFET. Due to the fact that the 10 A die is physically smaller compared to the 42 A die, it has a smaller switching time constant which can be expressed as the product of the total input resistance and the total input capacitance i.e., $(R_G^{\mathrm{EXT}} + R_G^{\mathrm{INT}})C_{\mathrm{ISS}}$. According to the datasheets, the 10 A SiC MOSFET has an input capacitance of 0.259 nF while the 42 A device has an input capacitance of 1.915 nF. The result is significantly higher dI_{DS}/dt in the 10 A MOSFET compared to the 42 A SiC MOSFET, as can be seen in Fig. 5. It can also be seen from Fig. 5 that at low R_G^{EXT}, the temperature sensitivity of dI_{DS}/dt reduces for both SiC MOSFETs. A large external gate resistance of 220 Ω was used in these measurements, partially to limit the impact of the internal gate resistance (which is 5 Ω for the 42 A SiC MOSFET and 11.4 Ω for the 10 A device) and to improve the time resolution of the gate current plateau. However, in practical applications where there is a need to minimize switching losses and expedite the fast switching potential of SiC MOSFETs, a smaller gate resistance is preferable. As

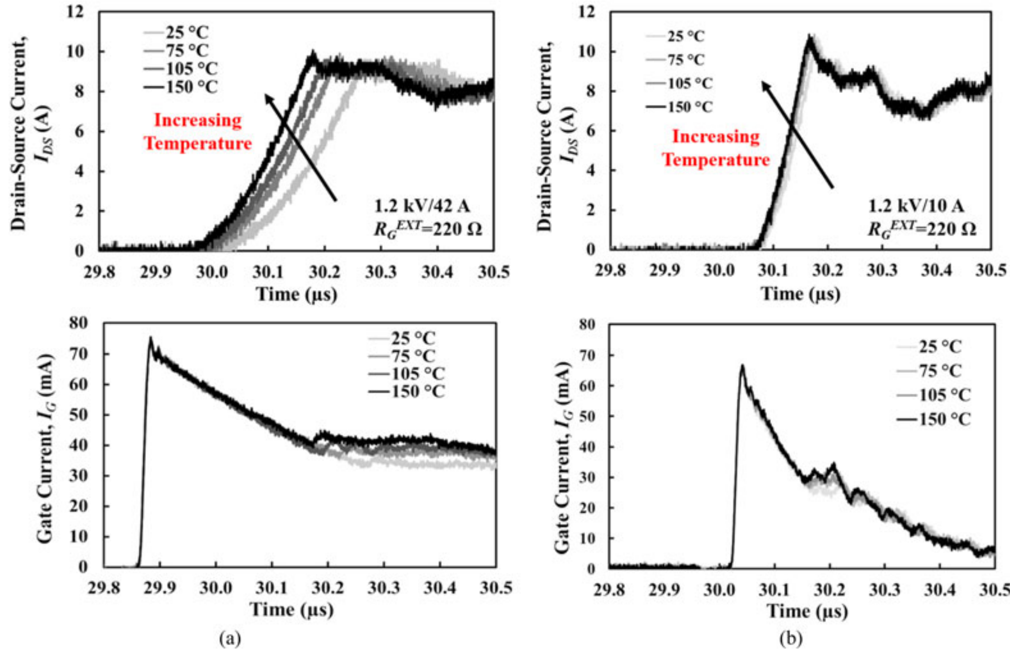

Fig. 7. (a) Drain-source current ($I_{\rm DS}$) and gate current (I_G) for the 1.2 kV/42 A SiC MOSFET during turn-ON at different temperatures. (b) Drain-source current ($I_{\rm DS}$) and gate current (I_G) for the 1.2 kV/10 A SiC MOSFET during turn-ON at different temperatures.

TABLE I
SWITCHING RATE DURING TURN ON FOR THE EVALUATED 1.2 KV SIC MOSFETS AT DIFFERENT TEMPERATURES AND EXTERNAL GATE RESISTANCES

Device	10 A SiC MOSFET (C2M0280120D)				24 A SiC MOSFET (CMF10120D)				42 A SiC MOSFET (CMF20120D)			
$(R_G^{\rm INT} + R_G^{EXT})C_{\rm ISS}$ (ns)	5.5	15.1	28.9	59.9	21.9	56.2	105.4	216.8	28.7	99.6	201.1	430.9
$dI_{\rm DS}/dt,_{T\ =25\,^{\circ}{\rm C}}$ (A/μs)	235.8	218.3	167.3	106.6	223.9	138.9	90.1	51.1	215.5	132.0	80.0	42.1
$dI_{\rm DS}/dt,_{\ T\ =75\,^{\circ}{\rm C}}$ (A/μs)	234.0	222.1	173.8	112.1	228.8	153.7	101.3	57.6	219.7	145.1	88.9	47.0
$dI_{\rm DS}/dt,_{\ T\ =105\,^{\circ}{\rm C}}$ (A/μs)	231.6	227.2	179.5	116.6	229.9	161.2	106.3	60.7	224.0	151.6	92.5	49.7
$dI_{\rm DS}/dt,_{\ T\ =150\,^{\circ}{\rm C}}$ (A/μs)	229.9	222.3	184.1	116.9	231.2	168.0	112.9	64.6	225.4	158.4	98.4	52.4

will be shown later, this increases the impact of the parasitic inductance which affects the effectiveness of $dI_{\rm DS}/dt$ as a TSEP in SiC MOSFETs.

C. Impact of the External R_G on $dI_{\rm DS}/dt$ as a TSEP

In this section, the effectiveness of the turn-ON $dI_{\rm DS}/dt$ as a TSEP in SiC MOSFETs is investigated over a range of external gate resistance for devices of three different current ratings. $dI_{\rm DS}/dt$ was calculated as the slope of the linear regression of the drain current for the three SiC MOSFETs (10, 24, and 42 A), and the results are presented in Table I. In this table, the switching time constant, which is given by $(R_G^{\rm EXT} + R_G^{\rm INT})C_{\rm ISS}$ is used to compare the switching rates of the different devices. Fig. 8(a) and (b) shows the graphical representation of the plots presented in Table I. Fig. 8(a) shows the switching rate as a function of the *RC* constant for the three SiC MOSFETs (10, 24, and 42 A) evaluated at a temperature of 25 °C. It can be observed that the three devices have similar maximum switching rates for the smaller *RC* constants, but in the case of the 10-A SiC MOSFET, $dI_{\rm DS}/dt$ is limited by the impact of the inductance on the load path. Fig. 8(a) shows that the MOSFET with a higher transconductance will exhibit a higher switching rate compared to a MOSFET with a lower transconductance even if both are switched with the same *RC* time constant. Hence, in Fig. 8(a), the 42-A MOSFET switches with the highest switching rate because the transconductance increases with the current rating through increased die area. Fig. 8(b) shows the measured $dI_{\rm DS}/dt$ as a function of the *RC* constant for the 42 A SiC MOSFET at 25 and 150 °C, where the reduced temperature sensitivity at lower *RC* constants, i.e., lower $R_G^{\rm EXT}$, can be seen. Fig. 9(a), (b), and (c) shows the normalized $dI_{\rm DS}/dt$ as a function of temperature for different external gate resistances ($R_G^{\rm EXT}$) in the 10-, 24-, and 42-A SiC MOSFETs, respectively. The results here generally show that the temperature sensitivity of $dI_{\rm DS}/dt$ decreases with the external gate resistance as well as with the current rating, i.e., to use $dI_{\rm DS}/dt$ as a TSEP, the SiC MOSFET must be driven with a large external gate resistance and the technique is most effective when the device current rating is high.

To understand the reduction of temperature sensitivity of $dI_{\rm DS}/dt$ at small $R_G^{\rm EXT}$ and at smaller current ratings, it is important to rederive the equations of $dI_{\rm DS}/dt$ and its temperature sensitivity with the added effect of the parasitic source

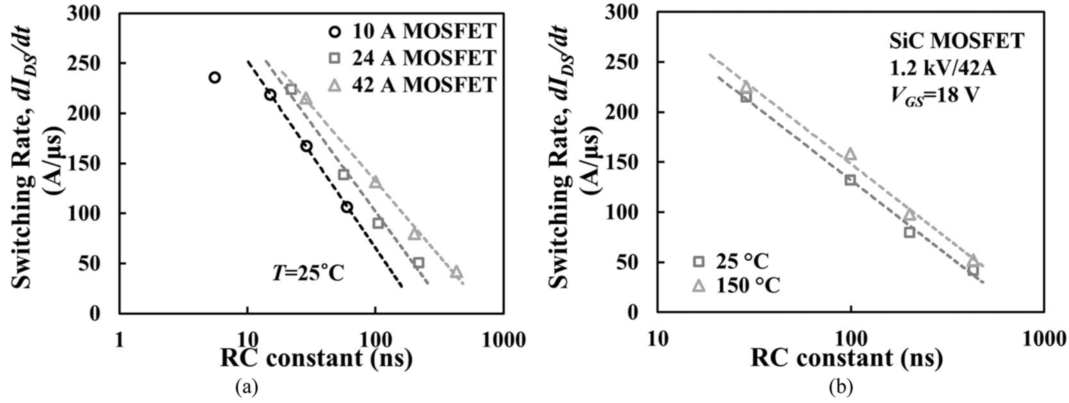

Fig. 8. (a) Measured turn-ON dI_{DS}/dt as a function of the *RC* constant for the evaluated SiC MOSFETs at 25 °C. (b) The measured turn-ON dI_{DS}/dt as a function of the *RC* constant for 42 A SiC MOSFETs at 25 and 150 °C.

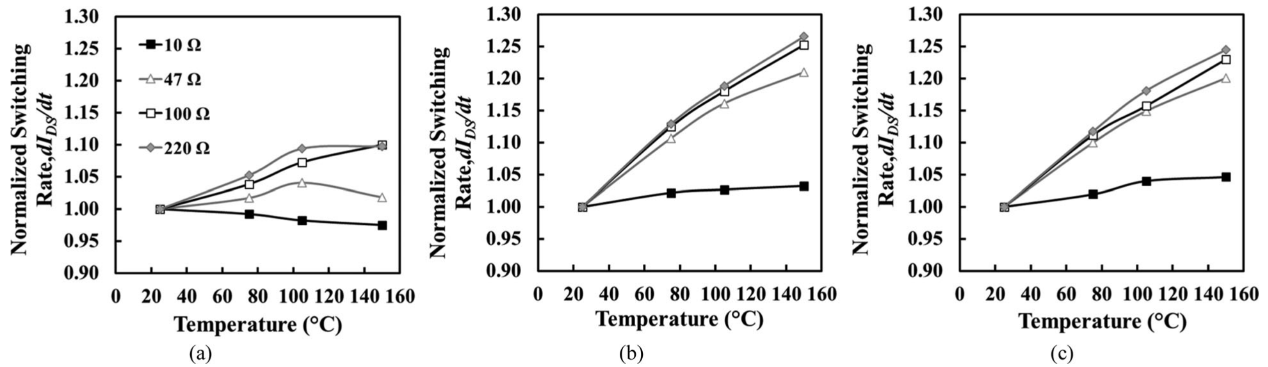

Fig. 9. (a) Normalized dI_{DS}/dt as a function of temperature for different R_G^{EXT} in the 1.2 kV/10 A SiC MOSFET. (b) Normalized dI_{DS}/dt as a function of temperature for different R_G^{EXT} in the 1.2 kV/24 A SiC MOSFET. (c) Normalized dI_{DS}/dt as a function of temperature for different R_G^{EXT} in the 1.2 kV/42 A SiC MOSFET.

inductance (L_S) [34], [35]. Equations (12) and (13) model the turn-ON I_{DS} for the MOSFET and its time derivative, respectively. However, the presence of the source inductance means that the source voltage can no longer be assumed to be zero but instead is given as the product of the source inductance and dI_{DS}/dt

$$I_{\mathrm{DS}} = \frac{\beta}{2}(V_G - V_S - V_{\mathrm{TH}})^2, \text{ where } V_S = L_S \frac{dI_{\mathrm{DS}}}{dt} \quad (12)$$

$$\frac{dI_{\mathrm{DS}}}{dt} = \beta \left(V_G - L_S \frac{dI_{\mathrm{DS}}}{dt} - V_{\mathrm{TH}}\right)\left(\frac{dV_G}{dt} - L_S \frac{d^2 I_{\mathrm{DS}}}{dt^2}\right) \quad (13)$$

Equation (13) is a second-order ordinary differential equation (ODE) that can be simplified by assuming a constant dI_{DS}/dt whose derivative ($d^2 I_{\mathrm{DS}}/dt^2$) is therefore zero. This assumption does not reduce the accuracy of the proposed model as will be seen later. Hence, the turn-ON dI_{DS}/dt can be expressed using (14)

$$\frac{dI_{\mathrm{DS}}}{dt} = \frac{\beta\,(V_G - V_{\mathrm{TH}})\left(\frac{dV_G}{dt}\right)}{1 + \beta L_S\left(\frac{dV_G}{dt}\right)} \quad (14)$$

When (14) is combined with (8), the resultant equation is given by

$$\frac{dI_{DS}}{dt} = \frac{\beta\,(V_G - V_{\mathrm{TH}})\left(\frac{V_{\mathrm{GG}}}{(R_G^{\mathrm{INT}}+R_G^{\mathrm{EXT}})(C_{\mathrm{ISS}})} e^{-\frac{t-t_0}{(R_G^{\mathrm{INT}}+R_G^{\mathrm{EXT}})(C_{\mathrm{ISS}})}}\right)}{1 + \beta L_S\left(\frac{V_{\mathrm{GG}}}{(R_G^{\mathrm{INT}}+R_G^{\mathrm{EXT}})(C_{\mathrm{ISS}})} e^{-\frac{t-t_0}{(R_G^{\mathrm{INT}}+R_G^{\mathrm{EXT}})(C_{\mathrm{ISS}})}}\right)} \quad (15)$$

Fig. 10(a) and (b) shows the gate current measurements for the 42 A SiC MOSFET using a $R_G^{\mathrm{EXT}} = 10\,\Omega$ and a $R_G^{\mathrm{EXT}} = 220\,\Omega$, respectively. It can be seen from Fig. 10 that the temperature dependency of the gate current plateau is higher for the large external gate resistance and the impact of the oscillations has also been minimized.

Equation (15) is useful for understanding how the current commutation rate is determined by the external gate resistance and temperature in the presence of parasitic inductance in the source-drain current path. It is well understood that reducing R_G^{EXT} increases dI_{DS}/dt; however, the rate at which this occurs also depends on the parasitic capacitances, the internal gate resistance, the parasitic inductance and temperature. Us-

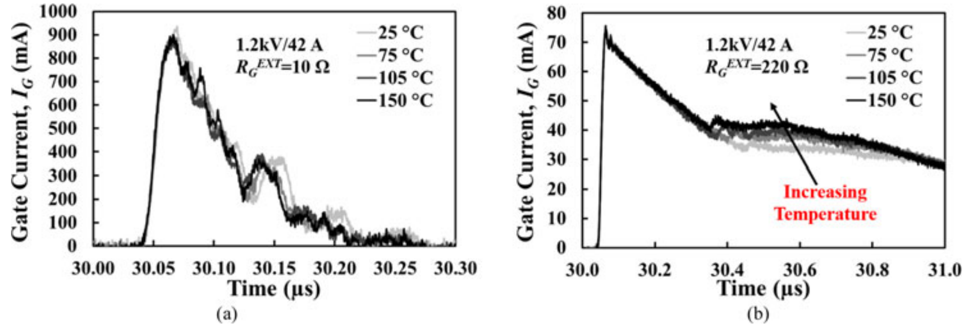

Fig. 10. (a) Measured turn-ON gate current for the 42 A SiC MOSFET at different junction temperatures with $R_G^{\mathrm{EXT}} = 10\,\Omega$. (b) The measured turn-ON gate current for the 42 A SiC MOSFET at different junction temperatures with $R_G^{\mathrm{EXT}} = 220\,\Omega$.

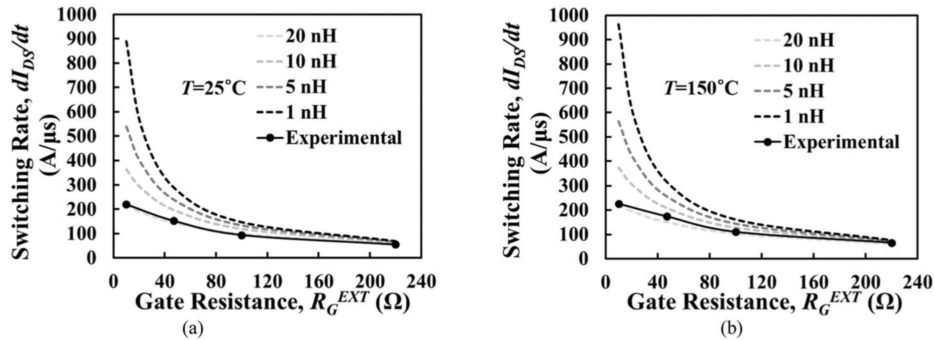

Fig. 11. (a) Modeled and measured turn-ON dI_{DS}/dt for the 42 A SiC MOSFET showing the impact of parasitic inductance at 25 °C. (b) The modeled and measured turn-ON dI_{DS}/dt for the 42 A SiC MOSFET showing the impact of parasitic inductance at 150 °C.

ing (15), dI_{DS}/dt has been calculated for the 1.2 kV/42 A SiC MOSFETs for different external gate resistances, temperatures and parasitic inductances. dI_{DS}/dt has been calculated for a load current I_{DS} of 9 A and assuming a constant mobility for the SiC MOSFET as has been discussed in Section II-A. Datasheet parameters were used in (15), and these include C_{ISS} being 1.915 nF, V_{GG} being 18 V, the internal gate resistance R_G^{INT} being 5 Ω, and the threshold voltage being 3.2 V at 25 °C and 2.3 V at 150 °C. Fig. 11(a) shows the results of the model for different R_G^{EXT} and parasitic inductance together with experimental measurements at 25 °C, while Fig. 11(b) shows similar modeling and measurement results at 150 °C. It can be seen that the model and measurements agree at large R_G^{EXT}; however, as R_G^{EXT} is reduced and dI_{DS}/dt is increased, the model matches the measurements when parasitic inductance is accounted for. The model shows that the parasitic inductance is within the range of 15−20 nH. By comparing the modeled and measured dI_{DS}/dt at the different temperatures for the different R_G^{EXT}, it was observed that the positive temperature coefficient of dI_{DS}/dt reduced with decreasing R_G^{EXT} as a result of the parasitic inductance. And this effect was more apparent at high dI_{DS}/dt, which explains why the 10-A SiC MOSFET (with significantly reduced input capacitance) exhibited a dI_{DS}/dt that was temperature insensitive at low R_G^{EXT}. Hence, this shows that the parasitic inductance reduces the temperature sensitivity of dI_{DS}/dt. It is important to mention that the impact of the parasitic inductance L_S not only limits the temperature sensitivity of dI_{DS}/dt as shown in this paper, but it can also be used as a temperature sensor if there is an additional terminal connected to the internal source of the power module so that the voltage drop across the parasitic inductance can be sensed. This method of using internal terminals across the stray inductance has been proposed for identifying the turn-OFF delay in IGBTs [36]. Equation (12) suggests that the voltage across the stray inductance can be used for identifying dI_{DS}/dt and junction temperatures in SiC MOSFETs.

III. Results for Condition Monitoring Implementation

If the switching rate is to be used as a TSEP for condition monitoring in SiC power MOSFETs, then its relationship with other parameters like load current and dc-link voltage must be calibrated. Any load current and/or voltage dependency of dI_{DS}/dt should be decoupled from its temperature dependency so that it can be used for junction temperature sensing. The measurements and analysis presented in Section II were performed using a dc-link voltage of 200 V, which is well below the 1200 V rated blocking voltage of the devices studied. Considering an application point of view, dc-link voltages of 300−600 V are widely used in applications like automotive drivetrains [37]; hence, the evaluation of dI_{DS}/dt and its temperature sensitivity at those voltage levels should be investigated. The dependency of the switching rate on the dc-link voltage and temperature has been investigated by experimental measurements. The results are shown in Fig. 12(a) where the turn-ON current transient has been shown for different dc-link voltages for the 42-A SiC power MOSFET at a temperature of 25 °C switched with

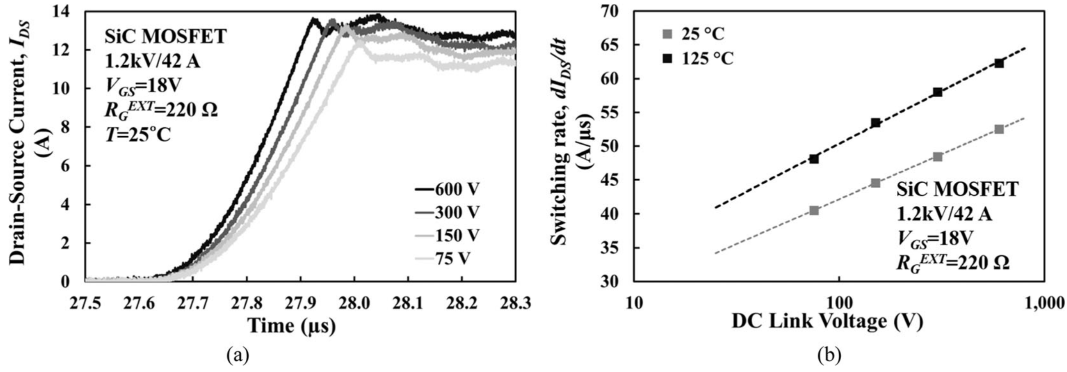

Fig. 12. (a) Drain-source ($I_{\rm DS}$) for the 42 A SiC MOSFET during turn-ON for different dc-link voltages; (b) $dI_{\rm DS}/dt$ for the 42 A SiC MOSFET during turn-ON as a function of the dc-link voltage at 25 and 125 °C.

$R_G^{\rm EXT} = 220\,\Omega$. The dc-link voltage values ($V_{\rm dc}$) are 75, 150, 300, and 600 V. Fig. 12(b) shows the measured $dI_{\rm DS}/dt$ characteristics as a function of the dc-link voltage for two temperatures, namely, 25 and 125 °C.

It can be seen from Fig. 12(a) that the turn-ON switching rate is increasing with the supply voltage. This is due to the fact that the input capacitance reduces with increasing dc supply voltage as a result of the voltage-dependent Miller capacitance. The Miller capacitance is comprised of a series combination of an oxide capacitance and a voltage dependent depletion capacitance that increases as the supply voltage reduces. Increasing the supply voltage increases the depletion width and hence reduces the Miller capacitance [26]. Hence, at low $V_{\rm dc}$, the high Miller capacitance slows down the MOSFET. Since the dc-link voltage is usually held constant in voltage source converter applications, the dependency of $dI_{\rm DS}/dt$ on $V_{\rm dc}$ is not critical in its use as a TSEP. In addition, by analyzing the switching rate as a function of the supply voltage for two temperatures presented in Fig. 12(b), it can be seen that the temperature sensitivity of the switching rate is constant for the different dc voltages evaluated. As the dc voltage is increased from 75 to 600 V, $dI_{\rm DS}/dt$ increases with temperature by 20%. However, as the nominal switching rate is affected by the dc-link voltage value, the use of $dI_{\rm DS}/dt$ as TSEP would require an initial calibration.

The impact of the load current on the switching transient is presented in Fig. 13. Fig. 13(a) shows the turn-ON drain-source current characteristics of the 42 A SiC power MOSFET switched with $R_G = 220\,\Omega$ for three different load currents namely, 5, 13, and 21 A at 25 °C. Fig. 13(b) shows the corresponding gate current characteristics of the SiC MOSFET during turn ON. These characteristics are repeated at 125 °C as can be seen in Fig. 14(a) and (b) where the turn-ON $I_{\rm DS}$ and I_G transients are shown at a higher temperature. It can be seen from Figs. 13 and 14 that the instantaneous switching rate of $I_{\rm DS}$ is independent of the load current while the gate current plateau is inversely proportional to the load current. Since the gate current plateau occurs at the time instant that $I_{\rm DS}$ reaches the load current, then for the same switching rate, the gate current plateau will increase with decreasing load current. This is due to the fact that the transition point of the gate current from the $C_{\rm GS} + C_{\rm GD-HV}$ (high Miller capacitance) charging phase to the $C_{\rm GS} + C_{\rm GD-LV}$ (low Miller capacitance) charging phase occurs after the full load current has been reached.

In the case of the gate current plateau, if the load current is known, the junction temperature can be deduced from the plateau value, especially when a high $R_G^{\rm EXT}$ is used as shown by the results in Figs. 13(b) and 14(b). If the load current is changing, using the gate current plateau as a TSEP will require separating the effect of the load current change from the effect of the junction temperature. As can be seen in Figs. 13(b) and 14(b), it is possible to measure the same gate current plateau at 2 different junction temperatures and load currents. For example, a gate current plateau of 30 mA results from a load current of 21 A at 125 °C, while the same gate current plateau also results from a load current of 13 A and a junction temperature of 25 °C.

The gate current plateau ($I_{\rm GP}$) can be calculated from the gate current characteristics shown in Fig. 3(a) at the time instant when the gate current transits from the gate-source capacitance charging component to the Miller capacitance charging component and it can be expressed as

$$I_{\rm GP} = \frac{C_{\rm GS}}{(C_{\rm GS} + C_{\rm GD-HV})} \cdot \frac{V_{\rm GG}}{(R_G^{\rm INT} + R_G^{\rm EXT})} \cdot e^{-\frac{t_1 - t_0}{(R_G^{\rm INT} + R_G^{\rm EXT})(C_{\rm GS} + C_{\rm GD-HV})}} \tag{16}$$

where t_1 is the time when $V_{\rm GS}$ becomes equal to $V_{\rm GP}$. The time $t_1 - t_0$ can be expressed as the sum of the current rise time and the time it takes for $V_{\rm GS}$ to reach $V_{\rm TH}$

$$t_1 - t_0 = t_{\rm rise} + (t_{\rm TH} - t_0) = \frac{I}{(dI_{\rm DS}/dt)} + (t_{\rm TH} - t_0) \tag{17}$$

where the current rise time is given by the ratio of the current to the switching rate. Hence, $I_{\rm GP}$, according to the earlier equations, will increase with decreasing load current and increase with junction temperature.

Using the switching rate as a TSEP requires the ability to measure high $dI_{\rm DS}/dt$. Recent power modules include current sensors embedded; hence, the evaluation of these sensors for measuring temperatures in SiC power MOSFETs could be the next step. In addition, intelligent gate drivers with closed loop control and dI/dt feedback and control have been presented

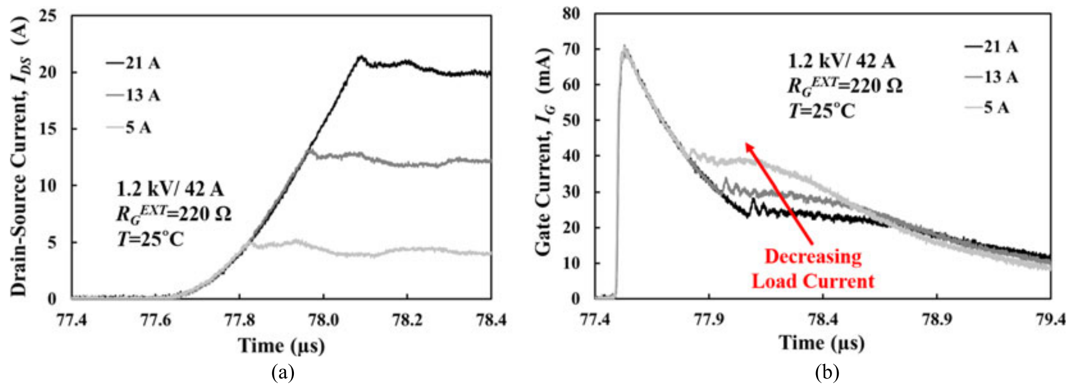

Fig. 13. (a) Measured $I_{\rm DS}$ turn-ON current transients for different load currents in the 1.2 kV/42 A SiC MOSFET at 25 °C. (b) The measured I_G turn-ON current transients for different load currents in the 1.2 kV/42 A SiC MOSFET at 25 °C.

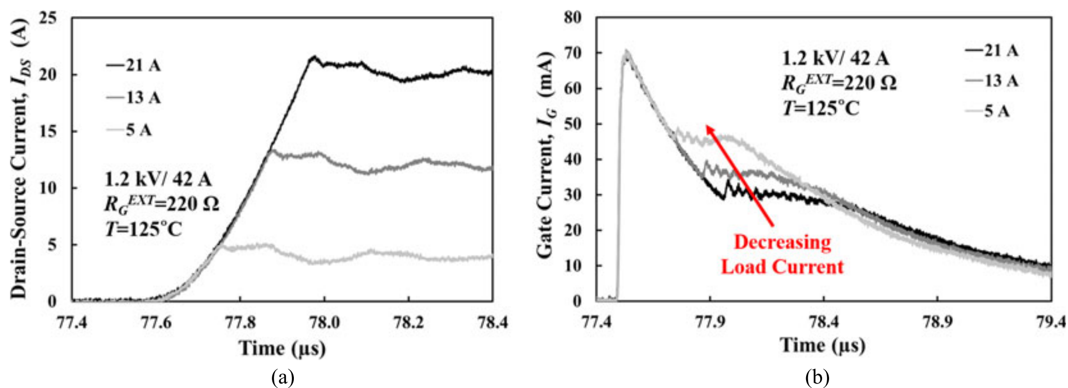

Fig. 14. (a) Measured $I_{\rm DS}$ turn-ON current transients for different load currents in the 1.2 kV/42 A SiC MOSFET at 125 °C. (b) The measured I_G turn-ON current transients for different load currents in the 1.2 kV/42 A SiC MOSFET at 125 °C.

and evaluated for IGBTs. Here, the voltage across the parasitic inductance of the power module is used for measuring the switching rate [38], [39], thus requiring an auxiliary emitter connection. Recent advances in current sensors like Rogowski coils with high dI/dt detection [40] or magnetoresisitive current sensors [41] suggest that the identification of the temperature by means of the switching rate can be feasible.

The ability to change the gate drive resistance during operation [42], by using an intelligent programmable gate driver [43], [44], could also enable this technique of junction temperature sensing without suffering the penalty of increased switching losses. The devices will be driven at high switching rates (using reduced gate drive resistances) and at the occasional instants when junction temperature sensing becomes necessary, a higher gate resistance is used momentarily for monitoring the temperature dependent switching parameters. Hence, the device switching rate will only be slowed down when junction temperature sensing is required, which will be occasional. Slowing down the switching transients for improving the sensitivity of a TSEP can have an impact in the operation of a converter, if the temperature is to be estimated online. Slowing down the turn-OFF transient can improve the temperature sensitivity of the turn-OFF delay of IGBTs and MOSFETs, as it was shown in Fig. 1(d) and (e), but it could affect the operation of the converter in the case that fixed dead times are implemented. In the case of slowing down the turn ON for enabling the junction temperature measurement, if the turn OFF of the transistor is done at the nominal switching rate, the use of fixed dead times would not be affected.

IV. Conclusion

The junction temperature of SiC power MOSFETs can be measured for online condition monitoring using the turn-ON current switching rate ($dI_{\rm DS}/dt$) and the gate current transient. The turn-ON $dI_{\rm DS}/dt$ and the gate current plateau both linearly increase with temperature. Using device mathematical models, it has been demonstrated that the negative temperature coefficient of the threshold voltage and the temperature invariance of the channel mobility are the reason behind the positive temperature coefficient of $dI_{\rm DS}/dt$ in SiC MOSFETs. In silicon MOSFETs, the negative temperature coefficient of threshold voltage is balanced by the negative temperature coefficient of the channel mobility; hence, $dI_{\rm DS}/dt$ is temperature invariant. However, the temperature sensitivity of $dI_{\rm DS}/dt$ and $I_{\rm GP}$ is reduced by high speed switching due to the presence of parasitic inductance. The parasitic source inductance has the effect of slowing the device down and reducing the temperature sensitivity of the turn-ON $dI_{\rm DS}/dt$. Dynamic models have been presented which correctly predict how the parasitic inductance

limits the temperature sensitivity of dI_{DS}/dt. The switching rate increases with the dc-link supply voltage and it will require an initial calibration to be used as a TSEP; however, the temperature sensitivity is approximately the same for the dc-link voltages evaluated. In the case of the gate current plateau, it depends on both temperature and load current, hence it needs decoupling. For both TSEPs, reducing the switching rate improves the temperature sensitivity. However to exploit the benefits of SiC power devices, fast switching is recommended for reducing the switching losses although this will be at the expense of effective junction temperature sensing using the TSEPs identified in this paper. Hence, either the device is slowed down at the expense of higher switching losses or intelligent gate drivers with the capability of variable gate drive impedance are used. These have been demonstrated in recent research, together with fast sensors for dI_{DS}/dt control. In this case, the device would be slowed down occasionally to measure the junction temperature whenever the information is needed.

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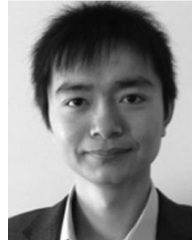

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