An Asymmetric Half-Bridge Resonant Converter Having a Reduced Conduction Loss for DC/DC Power Applications With a Wide Range of Low Input Voltage

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***Abstract*—A new asymmetric half-bridge (HB) resonant converter for dc/dc power system with a wide range of low input voltage is proposed in this paper. The proposed converter is easily derived based on the switch integration technique, merging a buck–boost, which is the same with the active-clamp forward's primary circuit, and the HB LLC resonant converter. By adopting the buck–boost circuit in front of the HB LLC resonant converter, higher input voltage of LLC resonant converter stage can be achieved. As a result, the primary conduction loss can be significantly reduced. In addition, to cover wide input voltage range, an asymmetric pulse width modulation control is applied. It can mitigate the design limitation for a high efficiency. Moreover, the proposed converter can achieve not only the small conduction loss and the optimal design for high efficiency, but also high power density and low cost due to the switch integration technique. The validity of the proposed converter is confirmed by the experimental results of a prototype converter with 36–72 $V_{\rm DC}$ input and 300 W (12 V/25 A) output.**

***Index Terms*—Asymmetric half-bridge (HB) resonant converter, dc/dc power applications, high voltage gain, LLC resonant converter, wide range of low input voltage.**

I. Introduction

THE dc/dc applications with low input voltage such as 48 *V* direct current (dc) power system based on 48 $V_{\rm DC}$ battery system has many advantages. First of all, since 48 $V_{\rm DC}$ power supplies are connected in parallel with 48 $V_{\rm DC}$ battery system, the power system has many strengths such as high reliability and easy maintenance [1]–[4]. Therefore, 48 $V_{\rm DC}$ system has been widely applied in many applications [1]–[8]. In the data center, 48 $V_{\rm DC}$ system shows high overall system efficiency because it can simplify the transmission stage compared with the ac system [5], [6]. Recently, 48 $V_{\rm DC}$ system has expanded to small electrical vehicle such as electric bike [8].

In these applications with a low-to-medium power capability in 48 $V_{\rm DC}$ power system, the single stage power systems, which consist of only one topology, are very widely applied due to the simple structure with small component count [7], [17], [29]–[31]. Among them, the half- bridge (HB) LLC resonant converter has been widely used due to many advantages such as a simple structure, wide zero-voltage-switching (ZVS) capability, and low secondary voltage stress as shown in Fig. 1(a) [9], [10]. However, this converter shows design limitations for 48 V power system having wide range of the low input voltage. First, the requirement to operate with a wide input voltage range (36–72 $V_{\rm DC}$) comes from a consideration of the dynamic battery voltage [1]–[4]. In the operating range, the highest efficiency at 48 $V_{\rm DC}$ called as nominal input voltage ($V_{\rm nom}$) is specially required because 48 $V_{\rm DC}$ power system mostly operates at $V_{\rm nom}$. However, due to the wide input voltage range, it is hard to achieve the optimized efficiency at $V_{\rm nom}$. Moreover, due

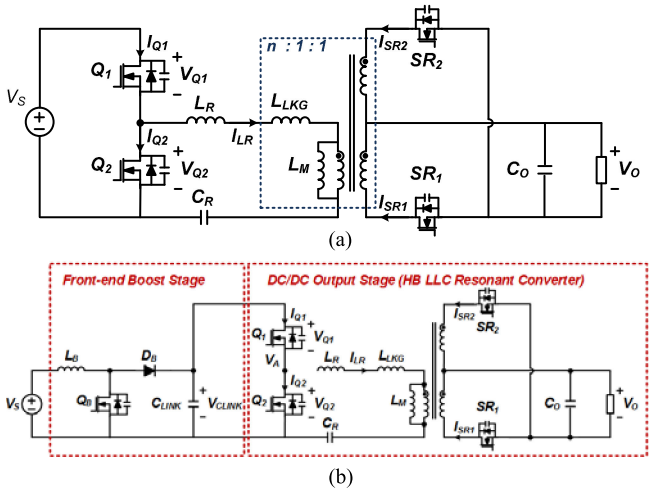

Fig. 1. Conventional dc/dc power system: (a) single-stage LLC resonant converter; and (b) conventional two-stage converter adopting boost converter and LLC resonant converter.

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to low-input voltage and restrictive voltage gain, the transformer ratio is also limited, and it causes a large reflected current in the primary side. As a result, the primary conduction loss becomes large, thus this converter shows low efficiency.

To cover the design limitation of the single-stage converter, many approaches have been proposed. Among them, the two-stage approach, which consists of the front-end boost converter stage and dc/dc output stage, is known as the suitable and practical converter as shown in Fig. 1(b) [6]. By applying the front-end boost converter, V_{CLINK}, which is the input voltage of the HB LLC resonant converter, can be increased. Therefore, the primary conduction loss in the post LLC stage can be reduced by the small reflected current from the secondary side due to larger voltage gain and transformer turns ratio. In addition, optimal design of the HB LLC resonant converter can be easily achieved because of the narrow voltage range of V_{CLINK} regulated by the front-end boost converter. Although the two-stage approach shows high performance, it has some severe drawbacks:

1) high cost;
2) low power density;
3) large additional conduction loss in the front-end boost converter;
4) large start-up current caused by an additional front-end boost converter.

To overcome the abovementioned problems of the two-stage approach, the asymmetric half-bridge resonant converter (AHBRC) is proposed in this paper. By simply integrating a buck–boost circuit, which is from the active-clamp forward, to HB LLC resonant converter, high power density and low cost can be easily achieved, and the additional conduction losses on additional switches in the two-stage approach and large start-up current can be removed. In addition, the proposed converter maintains same advantages of the two-stage approach such as small primary conduction loss and optimal design for a high efficiency at nominal input voltage. This paper is the improved version of the paper reported in [28]. Compared to the previous paper, the analysis and experimental results are newly added, and the overall contents were improved. The operation and performance of the proposed converter are verified by a prototype with 36–72 V_{DC} input and 300 W (12 V/25 A) output.

II. Concept and Operational Principle of the Proposed Converter

A. Derivation of the Proposed Converter

As mentioned before, when the single-stage HB LLC resonant converter is utilized in low input voltage applications with wide range, it has large primary conduction loss due to the large reflected current. On the other hand, the two-stage converter can reduce large primary conduction loss of the single-stage HB LLC resonant converter by increasing transformer turns ratio. However, it causes the low power density and high cost. Therefore, to have a large input voltage of the HB LLC resonant converter without any degradation of power density and cost, employing the primary-side circuit of the buck–boost converter is considered. The buck–boost circuit has a stacked-capacitor structure that V_{CB} is added on the top of the input voltage (V_S)

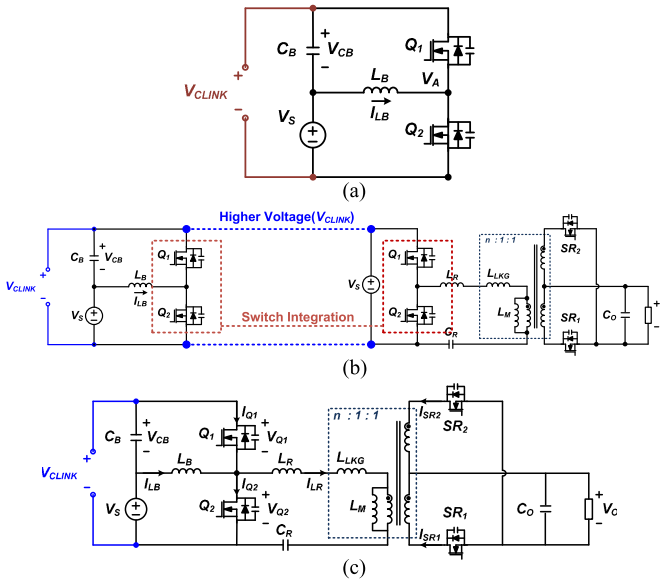


Fig. 2. Topology derivation of the proposed converter: (a) the buck–boost converter in primary side; (b) the integration process; and (c) circuit diagram of the proposed converter.

as shown in Fig. 2(a) [11], [12]. The increased voltage, V_{CLINK}, can be applied as the input voltage of the HB LLC resonant converter. The integration process is shown in Fig. 2(b). To integrate two converters, first, V_{CLINK} of the buck=-boost converter is connected to the input of the HB LLC resonant converter. In addition, since the two switches in the buck–boost converter and the HB LLC resonant converter complementarily operates, the two switches can be shared in the two converters. By merging two switches of two stages, the proposed converter can be derived as shown in Fig. 2(c). In summary, the proposed converter is derived based on the switch integration technique to reduce the number of the components, and high performance can be achieved by the higher input voltage, simultaneously. Moreover, since the buck–boost circuit is directly connected with the input stage with the buck–boost characteristics, the start-up current is significantly reduced compared with the conventional two-stage structure.

B. Duty-Cycle Control Scheme to Cover Wide Input Voltage Range

In the conventional LLC resonant converter, the output voltage (V_O) is regulated by the pulse frequency modulation (PFM) control with symmetric duty ratio ($D = 0.5$). In the proposed converter, the PFM control is basically used for the output voltage regulation. However, when the symmetric duty ratio is applied, the input voltage range is still wide, and it can be a burden on the design for high efficiency. Therefore, to alleviate the design limits from wide input voltage range, the APWM control [15]–[18], [31] is applied in the proposed converter according to the input voltage variation. According to the input voltage, since V_{CB} is changed, i.e., $V_{\mathrm{CB}} = DV_S/(1-D)$ by the APWM control, the input voltage range can be compensated. At nominal input where a high efficiency is required, V_{CB} is the same

as the input voltage because the proposed converter operates with symmetric duty ratio. When the input voltage is larger than $V_{\rm nom}$, $V_{\rm CB}$ is decreased by applying the narrower duty ratio than 0.5. On the other hand, when the input voltage is smaller than $V_{\rm nom}$, $V_{\rm CB}$ can be increased by the wider duty ratio than 0.5. Consequently, since the input voltage of the HB LLC resonant converter, i.e., $V_{\rm CLINK}$, can be expressed as the sum of V_S and $V_{\rm CB}$ in the proposed converter, the range of $V_{\rm CLINK}$ can be narrowed by the APWM control.

C. Operational Principles

To facilitate the explanation of the mode operation, Figs. 3 and 4 show topological states and key waveforms of the proposed converter, respectively. The buck–boost stage and the HB LLC resonant converter can independently operate except for the integrated switches. The operation of the buck–boost stage is totally same to the convention converters [11], [12], and the operation of the HB LLC resonant stage is so different due to the APWM control. This paper only describes the case with $D \le 0.5$, which is almost the same as the operation except for the current and applied voltage across the resonant tank at $D > 0.5$. In steady state, the operation of the proposed converter is separated into six different modes as shown in Fig. 3. The analysis is based on the assumptions as follows:

1) all active power devices are ideal switches with parallel body diodes and parasitic capacitors C_{OSS};
2) additional capacitor (C_B) of the buck–boost stage are large enough to be constant.

Mode 1 [$t_0 \sim t_1$]: At t_0, mode 1 begins when Q_2 is turned ON. In Q_2, the combined current of the buck–boost inductor current $I_{\rm LB}(t)$ and resonant inductor current $I_{\rm LR}(t)$ flows due to the integration technique, and the power is transferred to the output through SR_2. In the buck–boost stage, the input voltage (V_S) is applied to the buck–boost inductor (L_B), and reflected output voltage (nV_O) is applied across the primary side of the transformer. In the HB LLC stage, its operation is the same as the above operation with small duty ratio (D) [9], [10].

Mode 2 [$t_1 \sim t_2$]: After Q_2 is turned OFF at t_1, the energy stored in L_B and L_R charges a parasitic capacitor of Q_2 (C_{OSS2}) and discharges a parasitic capacitor of Q_1 (C_{OSS1}). In this mode, since $I_{\rm LR}$ is a negative value, the energy for the ZVS operation is the sum of the energy stored in L_B and L_R.

Mode 3 [$t_2 \sim t_3$]: After finishing the commutation of two switches' the voltage across C_{OSS1} and C_{OSS2}, the power to the secondary side is still carried out through SR_2. This mode is continuously maintained until the current of SR_2 reaches zero.

Mode 4 [$t_3 \sim t_4$]: Mode 4 begins when Q_1 is turned ON, the deducted current of $I_{\rm LB}$ and $I_{\rm LR}$ is flowing through Q_1. In the secondary side, only SR_1 is conducting in the secondary stage in order to transfer the power to the output. In the buck–boost stage, $I_{\rm LB}$ is decreased because $V_{\rm CB}$ is applied across L_B as the opposite polarity. In the HB LLC stage, due to large duty ratio, the below mode operation is shown [9], [10].

Mode 5 [$t_4 \sim t_5$]: Mode 5 also operates with below mode operation in an LLC resonant converter [9], [10]. At t_4, the power transfer is finished, and mode 5 starts. Since there is no clamped voltage of L_M, L_M is participated to resonant operation with L_R and C_R, namely it operates with $\omega_o\ (= 1/((L_R + L_M)C_R)^{0.5})$, which large frequency compared with $\omega_r\ (= 1/(L_R C_R)^{0.5})$ in Mode 1, 3, and 4.

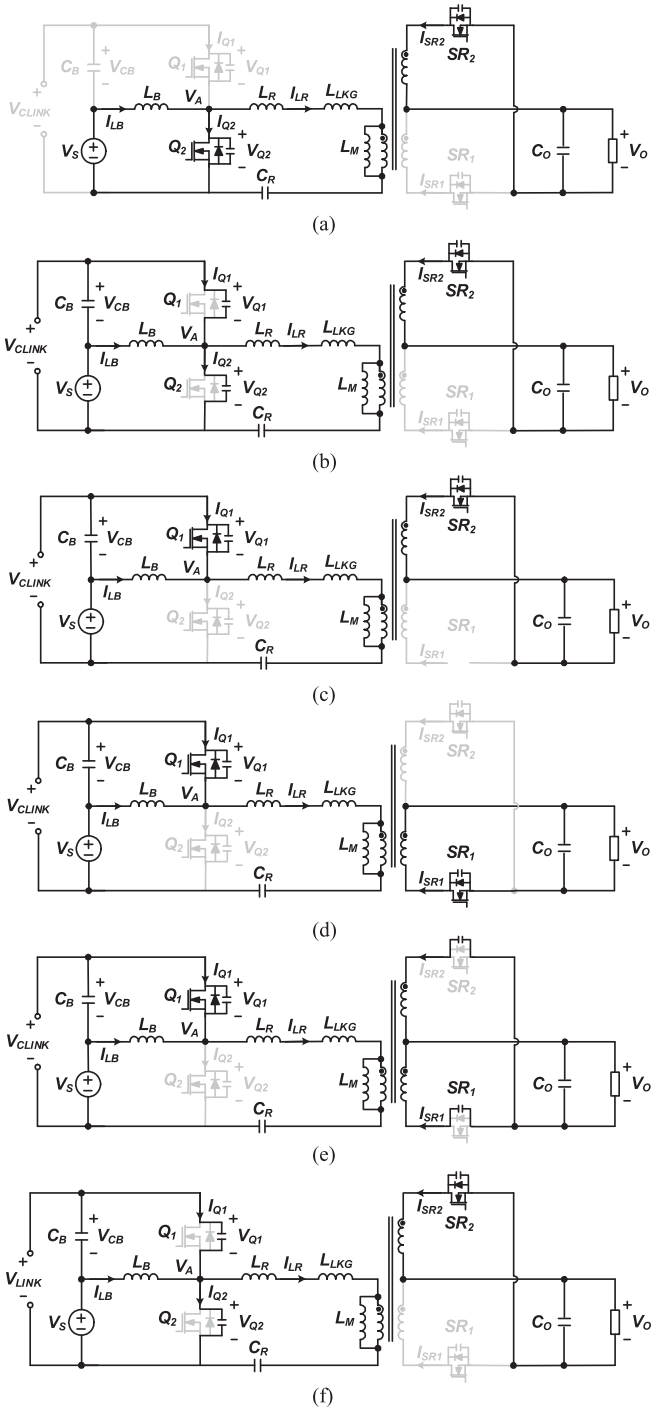


Fig. 3. Operating circuits of the proposed converter for each operational mode: (a) Mode 1 ($t_0 \sim t_1$); (b) Mode 2 ($t_1 \sim t_2$); (c) Mode 3 ($t_2 \sim t_3$); (d) Mode 4 ($t_3 \sim t_4$); (e) Mode 5 ($t_4 \sim t_5$); and (f) Mode 6 ($t_5 \sim t_6$).

Mode 6 [$t_5 \sim t_6$]: At t_3, Q_1 is turned off, C_{OSS2} is discharged, and C_{OSS1} is simultaneously charged. Since the ZVS operation of Q_2 is achieved by the current, which is the difference between $I_{\rm LM}$ and $I_{\rm LB}$, the ZVS energy of Q_2 is relatively smaller than that of Q_1.

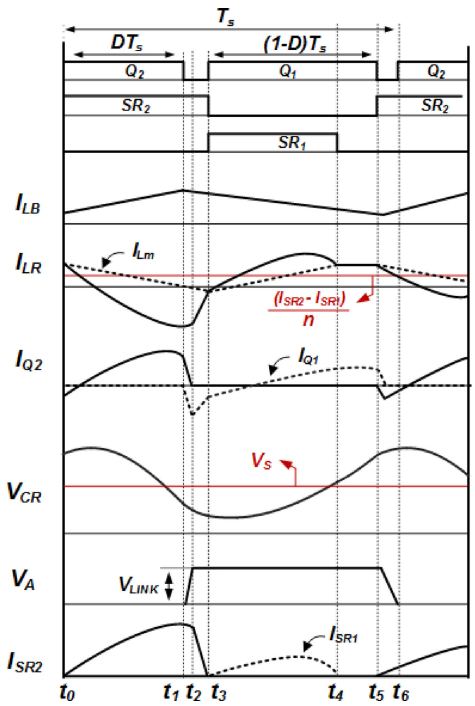


Fig. 4. Key waveforms of the proposed converter (at D < 0.5).

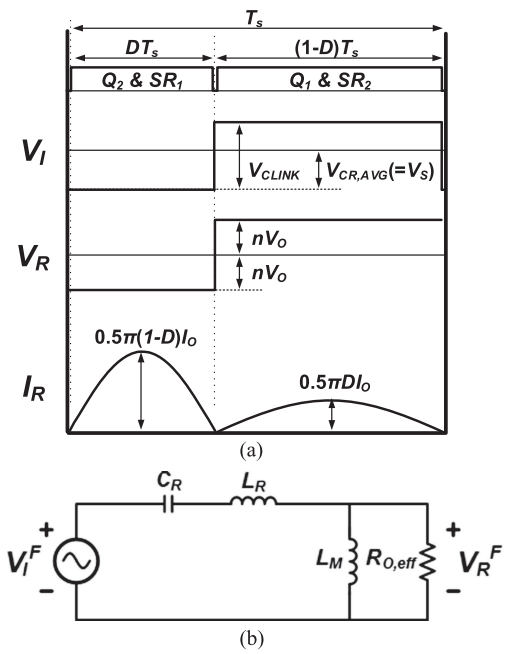


Fig. 5. (a) Simplified waveforms of LLC stage in the proposed converter. (b) Equivalent circuit of (a).

III. Analysis of the Proposed Converter

In this paper, the analysis, design, and experimental results of the proposed converter are mainly described except for the conduction loss comparing with the two-stage approach because the two-stage converter already shows higher performance than the single-stage HB LLC resonant converter.

A. DC Conversion Ratio

In the symmetric control ($D = 0.5$), the dc conversion ratio of the proposed converter is the same as the full-bridge LLC resonant converter, which is the twice of the conventional HB LLC resonant converter as follows [9], [10]:

$$M_{\mathrm{SYMM}}(f_{SW}, R_O) = \frac{nV_O}{V_S} = \frac{1}{\sqrt{\left[1+\frac{1}{k}\left\{1-\left(\frac{f_R}{f_{sw}}\right)^2\right\}\right]^2 + \left\{\frac{\pi^2}{8n^2R_O}\sqrt{\frac{L_R}{C_R}}\left(\frac{f_R}{f_{sw}}-\frac{f_{sw}}{f_R}\right)\right\}^2}} \quad (1)$$

where $k = L_M/L_R$, $f_R = 1/(2\pi(L_RC_R)^{0.5})$, and V_S, V_O, R_O, $n\,(= N_P/N_S)$, and f_{sw} are the input voltage, output voltage, output load resistance, the transformer turns-ratio, and the switching frequency, respectively. ‘

It notes the proposed converter can have twice the voltage gain compared with the HB LLC resonant converter, and it allows to increase the transformer turns ratio.

In the asymmetric control ($D< 0.5$ or $D > 0.5$), the voltage gain is changed. First of all, to simplify the analysis of the voltage gain, the voltage variation across C_R is neglected. In addition, in the LLC resonant converter with double-ended rectifier, since the power capability of each end are independent, it can be assumed that the current of each end are $(1-D)I_O$ and DI_O. The simplified waveforms of the LLC stage in the proposed converter are also presented in Fig. 5(a), and Fig. 5(b) presents the ac equivalent circuit based on the assumption and waveforms. Since only fundamental components of the applied input voltage to LLC resonant tank (V_I) and the reflected output voltage across transformer (V_R) involve in the power transfer, the asymmetric square-waves' fundamental components (V_I^F and V_R^F) are calculated, and the effective output load resistance ($R_{O,}$ eff) can be also derived as follows:

$$V_I^F = \frac{V_S}{\pi(1-D)}\sqrt{2(1-\cos(2\pi D))}\,\sin(\omega t+\alpha), \quad (2)$$

$$V_R^F = \frac{2V_O}{\pi}\sqrt{2(1-\cos(2\pi D))}\,\sin(\omega t+\alpha), \quad (3)$$

$$R_{O,\mathrm{eff}} = \frac{4n^2R_O}{\pi A}\frac{1-\cos(2\pi D)}{\sin(2\pi D)} \quad (4)$$

where $\alpha = \frac{1+\cos(2\pi D)}{\sin(2\pi D)}$, $A = \frac{-2(4D^2-4D+3)}{(1-4D^2)(3-2D)}$.

From (2)–(4), the voltage gain of the proposed converter (M_{ASYM}) can be expressed as follows:

$$M_{\mathrm{ASYM}} = \frac{nV_O}{V_S} = \frac{1}{2(1-D)} \times \frac{1}{\sqrt{\left[1+\frac{1}{k}\left\{1-\left(\frac{f_R}{f_{sw}}\right)^2\right\}\right]^2 + \left\{\frac{1}{R_{O,\,\mathrm{eff}}}\sqrt{\frac{L_R}{C_R}}\left(\frac{f_R}{f_{sw}}-\frac{f_{sw}}{f_R}\right)\right\}^2}}. \quad (5)$$

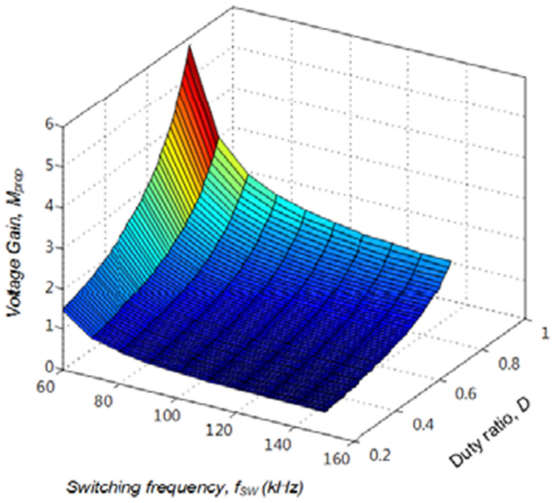


Fig. 6. Voltage gain (*Mprop*) according to *fSW* and *D* in 100% load conditions.

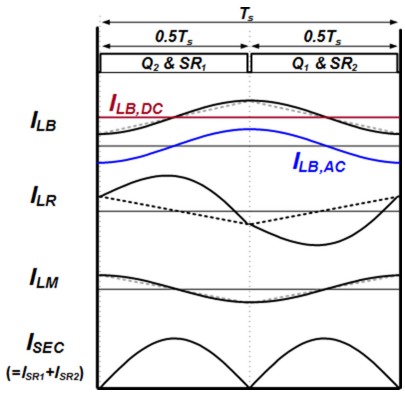


Fig. 7. Simplified waveforms for current stress.

By using (5), according to D and f_{SW}, the voltage gain of the proposed converter with APWM can be obtained as shown in Fig. 6. It can be seen that M_{ASYM} is proportional to D_{eff}, and it is inversely proportional to f_{SW}.

B. Primary Conduction Loss

In the dc/dc power system with a low input voltage, the primary conduction loss occupies a great part of total losses. Therefore, the efficiency can be estimated through the comparison on the primary conduction loss. Moreover, the conduction loss is basically analyzed at the nominal input voltage (V_{nom}) because the highest efficiency is required at V_{nom} based on the operating time of 48 V_{DC} power systems.

To analyze the conduction loss, the current stress should be first calculated. To easily get the current equations, the simplified current waveforms in the proposed converter are presented as shown in Fig. 7(a). Based on the fundamental harmonic approximation, the SRs' currents can be assumed as the rectified sinusoidal current source. I_{LM} and I_{LB} are assumed as the sinusoidal current waveforms with the different phase, which is same with the cosine wave. In addition, I_{LB} can separate the cosine wave ($= I_{\mathrm{LB,AC}}$) and the dc value ($= I_{\mathrm{LB,DC}}$). The waveforms can be described as follows:

$$I_{\mathrm{LB}} = I_{LB,\mathrm{DC}} + I_{LB,\mathrm{AC}} = \frac{V_O I_O}{\eta V_S} - \frac{V_S}{4 f_{SW} L_B} \cos(\omega t), \quad (6)$$

$$I_{\mathrm{LM}} = \frac{n V_O}{4 f_{SW} L_M} \cos(\omega t), \quad (7)$$

$$I_{\mathrm{SEC}} = \frac{\pi I_O}{2} |\sin(\omega t)|, \quad (8)$$

$$I_{\mathrm{LR}} = I_{\mathrm{LM}} + \frac{I_{\mathrm{SEC}}}{n}. \quad (9)$$

In the proposed converter, the currents on the primary switches (I_{Q1} and I_{Q2}) can be expressed as the subtraction between I_{LR} and I_{LB}, and the current flows through the channel resistor of the primary switches. Therefore, the conduction losses of the primary switches can be calculated as follows:

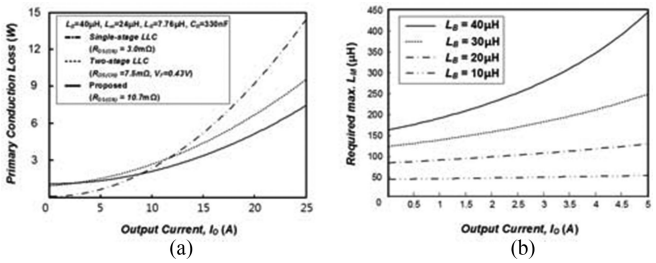
$$\begin{aligned} P_{\mathrm{Cond\_pri}} &= R_{\mathrm{DS(ON),\,prop}} \cdot (I_{Q1,RMS}^2 + I_{Q2,RMS}^2) \\ &= R_{\mathrm{DS(ON),\,prop}} \cdot \left\{ \left(\frac{V_O I_O}{\eta V_S} \right)^2 \right. \\ &\quad \left. + \left[\frac{1}{4\sqrt{2} f_{SW}} \left(\frac{n V_O}{L_M} + \frac{V_S}{L_B} \right) \right]^2 + \left(\frac{\pi I_O}{2\sqrt{2} n} \right)^2 \right\} \end{aligned} \quad (10)$$

where $R_{\mathrm{DS(ON),prop}}$ is the turn-ON resistance of the primary switches in the proposed converter.

On the other hand, the conduction losses of the conventional two-stage converter can be expressed by using three switches and one diode because there are a MOSFET and a diode in the preregulator stage, and the HB LLC stage has two switches, which is the same as the conventional single-stage converter. The conduction losses in the conventional converter can be calculated as follows:

$$\begin{aligned} P_{\mathrm{Cond\_pre-reg}} &= \frac{1}{T_S} \int_{D_B T_S}^{T_S} V_F I_{LB,\,\mathrm{Conv}}(t) dt \\ &\quad + R_{\mathrm{DS(ON),\,QB}} \frac{1}{T_S} \int_0^{D T_S} I_{\mathrm{LB}}^2(t) dt \\ &= V_F \cdot \frac{V_O I_O (1 - D_B)}{\eta V_S} + R_{\mathrm{DS(ON),QB}} \\ &\quad \cdot D_B \left[\left(\frac{V_O I_O}{\eta V_S} \right)^2 - \left(\frac{V_S D_B}{2 f_{B,SW} L_B} \right)^2 \right. \\ &\quad \left. + \frac{V_S D_B}{3 f_{B,SW} L_B} \right], \end{aligned} \quad (11)$$

$$\begin{aligned} P_{\mathrm{Cond\_LLC}} &= R_{\mathrm{DS(ON),conv}} \frac{1}{T_S} \int_0^{T_S} I_{\mathrm{LR}}^2(t) dt \\ &= R_{\mathrm{DS(ON),\,conv}} \left[\left(\frac{n_{\mathrm{conv}} V_O}{4\sqrt{2} f_{SW} L_M} \right)^2 \right. \\ &\quad \left. + \left(\frac{\pi I_O}{2\sqrt{2} n_{\mathrm{conv}}} \right)^2 \right] \end{aligned} \quad (12)$$



(a) (b)

Fig. 8. Design examples: (a) conduction loss comparison between two conventional converters and proposed converter; and (b) required maximum magnetizing inductance for ZVS operation according to the L_B.

where $D_B, V_F, R_{\mathrm{DS(ON)}}, _{QB}, R_{\mathrm{DS(ON),conv}}$, and $f_{B,SW}$ are the duty ratio of the preregulator, forward voltage of a diode, channel resistance of the switch in preregulator, channel resistance of the switch in the HB LLC resonant converter, and switching frequency in the preregulator.

Fig. 8(a) presents the comparison for the conduction losses of switches from (10)–(12) and one of the magnetics' winding in the primary side, which can be easily calculated based on (6)–(9). In the conventional single-stage and two-stage converter, the switches with lower channel resistance in the HB LLC stage can be selected due to lower voltage stresses. However, since the primary current is too large, it can show large conduction losses and low efficiency. Especially, since the single-stage converter has extremely large conduction losses, the practical application is difficult regardless of high light-load efficiency. In addition, the conventional two-stage converter rather has much larger conduction losses due to numerous components including three switches and one diode. On the other hand, in the proposed converter, in spite of larger $R_{\mathrm{DS(ON)}}$ caused by higher voltage stresses, the primary conduction losses can be significantly reduced compared to two conventional converters.

C. ZVS Operation

In the HB LLC stage of the conventional two-stage approach, the ZVS operation can be easily achieved under the entire load range because of large ZVS energy of L_M. On the other hand, in the proposed converter, the ZVS conditions are changed because the currents on Q_1 and Q_2 are different and uneven due to the switch integration. As shown in Fig. 4, in a case of Q_1, since the HB LLC stage operates in the above region and the direction of I_{LB} and I_{LR} is opposite, the ZVS conditions can be expressed as follows:

$$C_{OSS}V_{\mathrm{CLINK}}^2 < \frac{1}{2}L_B I_{\mathrm{LB}}^2(t_1) + \frac{1}{2}L_R I_{\mathrm{LR}}^2(t_1). \tag{13}$$

It notes that the ZVS energy becomes the sum of the energy stored in L_B and L_R, and the ZVS capability of Q_2 can be easily achieved with large I_{LB} and I_{LR}.

In case of Q_2, the ZVS equation can be expressed as follows:

$$C_{OSS}V_{\mathrm{CLINK}}^2 < \frac{1}{2}L_M I_{\mathrm{LM}}^2(t_5) - \frac{1}{2}L_B I_{\mathrm{LB}}^2(t_5). \tag{14}$$

To satisfy the ZVS condition in nominal input voltage with $D = 0.5$, when the offset current of the transformer is zero and I_{LB} is operating in a continuous current mode with assuming input power is same with the output power, then

$$L_M < \frac{(nV_O DT_S)^2}{2C_{OSS}V_{\mathrm{LINK}}^2 + L_B\left(\frac{P_O}{V_S} - \frac{V_S DT_S}{2L_B}\right)^2}. \tag{15}$$

In (15), according to L_B, which is designed by considering the ripple current of I_{LB}, the required maximum L_M can be decided as shown in Fig. 8(b). It shows larger L_B can make the ZVS operation be easy due to the small $I_{\mathrm{LB}}(t_5)$ in (14), and larger load current also help to achieve ZVS operation. Therefore, to achieve ZVS operation on the entire load range, L_B should be selected as larger also considering the power density. It makes the large L_M acceptable. It results in high efficiency due to the small magnetizing current and small turn-OFF switching loss.

D. Start-Up Current

The conventional two-stage converter including the boost converter can have severe start-up current because V_{CLINK} is under V_S. High current stress occurs, and it can be a burden of the switch stress when the components are selected [21]–[25]. To solve the problems, in the boost converter, some schemes and additional components are required. However, since the proposed converter can have inherently small start-up current due to the buck–boost characteristics, the start-up current can be considerably reduced compared with the conventional converter.

IV. Design Guideline of the Proposed Converter

A. Design Guideline of Minimum Duty Ratio (D_{min})

In the proposed converter, the asymmetric duty ratio is applied according to the input voltage to compensate $\Delta V_{\mathrm{CLINK}}$, i.e., $V_{\mathrm{CLINK}} = V_S + V_{\mathrm{CB}}$, which is the input voltage of the HB LLC stage. When the proposed converter operates over the nominal input (V_{nom}), D is controlled under 0.5. On the other hand, under V_{nom}, the proposed converter can increase V_{CB}, i.e., $V_{\mathrm{CB}} = DV_S/(1-D)$ by operating with $D > 0.5$. Therefore, APWM control can be set to minimize $\Delta V_{\mathrm{CLINK}}$ for design optimization for high efficiency.

To design the asymmetric control, there are two considerations which are maximum voltage stress ($V_{\mathrm{DS,\,max}}$) of the primary switches and transformer offset current (I_{OFFSET}). As for $V_{\mathrm{DS,max}}$, first, $V_{\mathrm{DS,max}}$ is the same as maximum V_{CLINK}, which is the sum of maximum V_{S} and minimum V_{CB}, and it can be expressed as follows:

$$V_{DS,\,\mathrm{max}} = V_{\mathrm{CLINK}} = V_{S,\,\mathrm{max}}\left(\frac{1}{1-D_{\mathrm{min}}}\right). \tag{16}$$

In (16), $V_{\mathrm{DS,\,max}}$ can be changed according to D_{min}. Since the switch with low voltage rating has generally small $R_{\mathrm{DS(ON)}}$, the proposed converter should consider applying minimized voltage rating with small $R_{\mathrm{DS(ON)}}$ for high efficiency. Fig. 9(a) shows $V_{\mathrm{DS,\,max}}$ on the primary switches according to D_{min}, which are in proportion to $V_{\mathrm{DS,\,max}}$. It notes that high efficiency with low voltage stress rating and low $R_{\mathrm{DS(ON)}}$ can be achieved by selecting small D_{min}.

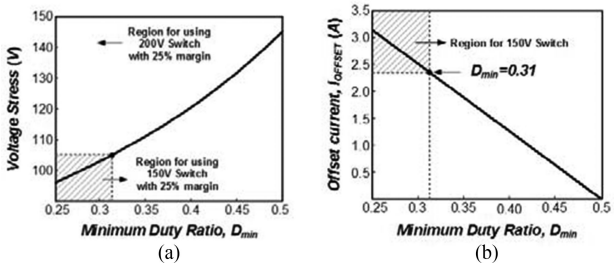


Fig. 9. Minimum duty ratio characteristics according to: (a) maximum voltage stress; and (b) transformer offset current.

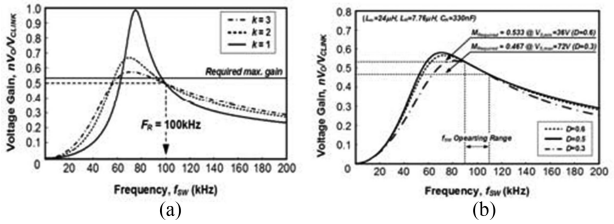


Fig. 10. Design example of the LLC resonant converter: (a) according to the *k* factor; and (b) according to the duty ratio at 100% load conditions.

Although the severe asymmetric control with small $D_{\min}$ can have small RDS(ON) of switches, it has some drawback such as the reduced voltage gain in (5) and the large transformer size due to the transformer offset current (IOFFSET) [26], [27]. In the proposed converter, IOFFSET can be simply expressed as follows:

$$I_{\mathrm{OFFSET}} = \frac{I_O(1-2D)}{n}. \tag{17}$$

The offset current, which is inversely proportional to $D_{\min}$ as shown in Fig. 9(b), affects the transformer size, power density, and efficiency. However, the efficiency is already considered by operating with the resonant frequency and the symmetric duty cycle at the nominal input voltage, which is mostly operated in 48 V_{DC} power systems. Therefore, to minimize the transformer size, $D_{\min}$ should be selected as large as possible. Under the conditions that the primary switch with 150 V voltage rating is selected, it is desirable that $D_{\min}$ is chosen as its maximum value, i.e., $D_{\min} = 0.31$.

B. Design Guideline of HB LLC Resonant Tank

The design of the HB LLC resonant tank is almost the same as the conventional design. Before the resonant tank design, the transformer turns-ratio should be selected for optimal design at V_{nom} and the turns-ratio is determined as 4 in the proposed converter. After then, the required maximum voltage gain ($M_{\max}$) is calculated at the minimum input voltage as follows:

$$M_{\max} = \frac{nV_O}{V_{\mathrm{CLINK,\,min}}} = \frac{nV_O}{V_S}(1-D_{\max}) = 0.533. \tag{18}$$

In Fig. 10(a), to obtain high voltage gain satisfying $M_{\max}$ with considering 5% voltage gain loss, the designed resonant tank parameters are presented as follows: $k = 3$, $Q = 0.78$, $L_R = 7.76\ \mu$H, $C_R = 330$ nF, $f_r = 100$ kHz, and $L_M = 24\ \mu$H.

In addition, Fig. 10(b) presents the voltage gain curves with the designed resonant tank according to the input voltage variation. It notes the required voltage gain range is narrower due to applying asymmetric control. Moreover, the operating switching frequency range is relatively narrow, which is around 20 kHz range. It can help to relieve the design burden of the transformer size.

C. Selection of Primary Switches

To select primary switches in the proposed converter, the maximum voltage and current stress are considered. From (10) and (16), the voltage and current stress can be rewritten with the worst conditions as follows:

$$\begin{aligned} V_{DS,\,\max} &= V_{S,\,\max}\left(\frac{1}{1-D_{\min}}\right) = 72\cdot\frac{1}{1-0.31} \\ &= 104.35[V] \end{aligned} \tag{19}$$

$$\begin{aligned} I_{Q2,\,\mathrm{MAX}} &= \sqrt{\int_0^{DT_S}(I_{\mathrm{LR}}(t)-I_{\mathrm{LB}}(t))^2dt} \\ &= 10.57[A]. \end{aligned} \tag{20}$$

From (19) and (20), Q_1 and Q_2 are selected as IPP110N 20N3G ($I_D = 88$ A, $V_{\mathrm{DS}} = 200$ V, $R_{\mathrm{DS(ON)}} = 10.7$ mΩ).

D. Additional Capacitor (C_{B})

For generally designing the capacitors, the ripple current and maximum voltage stress across the capacitor should be considered. As for the ripple current, the additional capacitor(C_B) in the proposed converter has the same current with Q_1. On the other hand, in the conventional two-stage converter, the ripple current is calculated in connection with an output current in the preregulator stage and a current of Q_1 as follows:

$$\begin{aligned} I_{\mathrm{CB,\,prop.}} &= \sqrt{\frac{1}{T_S}\int_{DT_S}^{T_S}(I_{\mathrm{LR}}(t)-I_{\mathrm{LB}}(t))^2dt} \\ &= 6.3[A] \end{aligned} \tag{21}$$

$$\begin{aligned} I_{\mathrm{CLINK,\,conv}} &= \sqrt{\frac{1}{T_S}\int_{D_BT_S}^{T_S}(I_{\mathrm{DB}}(t)-I_{\mathrm{LR}}(t))^2dt} \\ &= 7.6[A]. \end{aligned} \tag{22}$$

As for the maximum voltage stress of capacitors, the proposed converter has lower voltage stress than the conventional converter. Since V_{CB} subtracts V_S from V_{CLINK}, V_{CB} in the proposed converter can be considerably reduced compared with V_{CLINK} in the conventional two-stage converter. From two considerations, additional capacitors can be selected by using the capacitors with the same size and different voltage rating. In the conventional converter, the capacitors need to employ 6EA capacitors (ZLH, 220 μF, $V_{\max} = 100$ V, $I_{\mathrm{RMS}} = 1.62$ A) in order to meet the required large ripple current. On the other hand, the proposed converter can use only 4EA (ZLH, 470 μF, $V_{\max} = 63$ V, $I_{\mathrm{RMS}} = 1.99$ A) due to the reduced the voltage stress and ripple current. Therefore, the size of capacitors in the

TABLE I
COMPONENTS LIST OF PROTOTYPE

Stages	Components		Conventional (Single-stage LLC)	Conventional (Two-stage LLC)	Proposed
Pre-stage	Switch (Q_B)			IPP075N15N3G (150V/100A/7.5mΩ)	-
	Diode (D_B)			VF40120 (120V/40A/0.43V_F)	-
	Inductor (L_B)			L_B=40μH Core : PQ2620 (A_e=119mm^2) Wire : 0.1mm x120, 12T	
LLC Stage	Switches (Q_1 and Q_2)		IPP030N10N3G (100V/100A/3mΩ)	IPP075N15N3G (150V/100A/7.5mΩ)	IPP110N20N3G (200V/88A/10.7mΩ)
	Main Trans.	Core & Wire	L_M=23μH Core : EI3023 (Ae=190mm^2) N_P : 0.1mm x180, N_{S1} & N_{S2} : 0.1mm x240	L_M=23μH Core : EI3023 (Ae=190mm^2) N_P : 0.1mm x120, N_{S1} and N_{S2} : 0.1mm x180	
		Turns-ratio	Turns-ratio (N_P:N_{S1}:N_{S2}) = 4 : 3 : 3	Turns-ratio (N_P:N_{S1}:N_{S2}) = 7 : 2 : 2	Turns-ratio (N_P:N_{S1}:N_{S2}) = 8: 2 : 2
	L_R		L_R=7.7μH Core : PQ3220 (Ae=169mm^2) Wire : 0.1mm x240, 12Ts	L_R=7.7μH Core : PQ2020 (Ae=62.6mm^2) Wire : 0.1mm x120, 12Ts	
	C_R		330nF		
	f_r		100kHz		

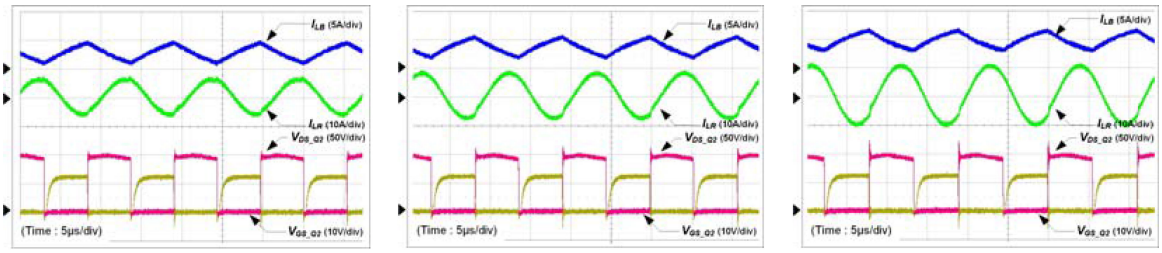


Fig. 11. Experimental waveforms of the proposed converter at nominal voltage ($= 48\ V_{\mathrm{DC}}$): (a) 20%; (b) 50%; and (c) 100% load conditions.

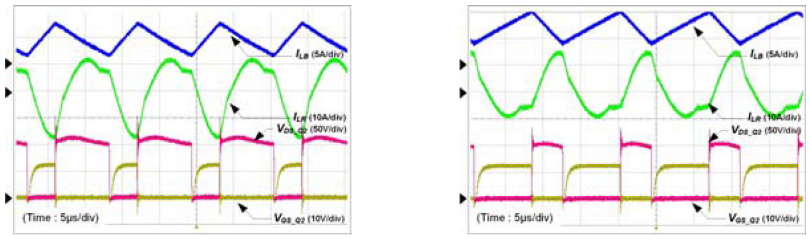


Fig. 12. Experimental waveforms of the proposed converter with the APWM duty control at 100% load conditions:(a) at $V_{S,\,\mathrm{min.}}\,(= 36\ V_{\mathrm{DC}})$; and (b) at $V_{S,\,\mathrm{max.}}\,(= 72\ V_{\mathrm{DC}})$.

proposed converter can be reduced about 33%, and high power density and low cost are achieved.

V. EXPERIMENTAL RESULTS

The feasibility of the proposed converter was verified with a 300 W prototype of dc/dc server power system. Design specification is as following: input voltage = 36–72 V_{DC}, output voltage = 12 V, and rated output power = 300 W. The detailed components' list is described in Table I.

Fig. 11 shows experimental waveforms at V_{nom} according to the load conditions, 20%, 50%, and 100%. As mentioned before, since efficiency at V_{nom} is very important, the proposed converter at V_{nom} should be optimally designed for high

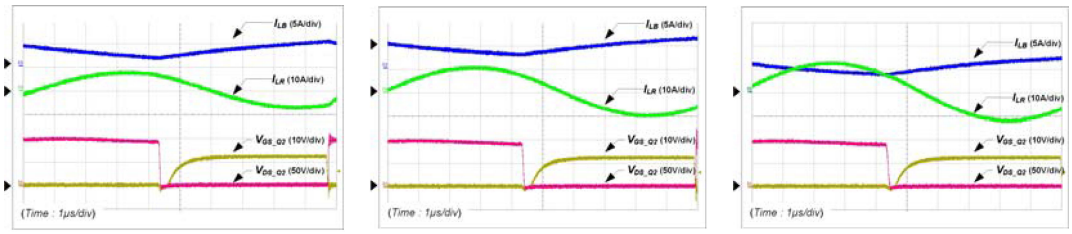


Fig. 13. ZVS waveforms at nominal voltage ($= 48V_{\rm DC}$): (a) 20%; (b) 50%; and (c) 100%.

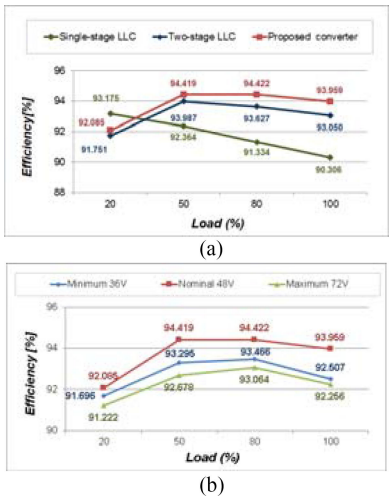


Fig. 14. Measured efficiency: (a) efficiency comparison of the conventional and proposed converter at nominal input voltage ($= 48V_{\rm DC}$); and (b) according to the input voltage.

efficiency, and the waveforms prove the optimal design by showing to operate with the resonant frequency and the symmetric ($D = 0.5$) duty ratio. Therefore, the proposed converter can show high efficiency because of the no circulating current by operating with the resonant frequency and the low RMS current by the zero offset current. In Fig. 12, the asymmetric duty ratio operations are presented in the wide input voltage range. The minimum duty ratio design selected by (16), (17) can be proved in Fig. 12(a) at $V_{S,\ \rm max}$. At $V_{S,\ \rm min}$, the proposed converter operates with $D_{\rm max}$ as shown in Fig. 12(b). Fig. 13 shows that the ZVS operation of the proposed converter can be surely achieved according to the load conditions, which are 20%, 50%, and 100% load conditions. Fig. 14 shows the measured efficiency results. In Fig. 14(a), the efficiency of the proposed converter at $V_{\rm nom}$ compared with the conventional two-stage converter is presented. The proposed converter has higher efficiency under entire load conditions because the proposed converter significantly reduces the primary conduction loss by removing large conduction loss of the additional switches in the front-end boost converter. Moreover, by reducing the reflected primary current, which can cause large conduction losses, the conduction loss of additional components such as transformer and inductors is also reduced. In addition, Fig. 14(b) presents the efficiency of the proposed converter according to the input voltage variation. It notes the highest efficiency can be achieved at the nominal input voltage by operating the resonant frequency and symmetric duty ratio.

VI. Conclusion

An asymmetric HB resonant converter for the dc/dc power system with wide range of low input voltage such as 48 $V_{\rm DC}$ battery system has been proposed in this paper. The proposed converter is derived from the switch integration technique, which merges the buck–boost stage and the HB LLC resonant converter, and the proposed converter has many advantages such as small conduction loss and small start-up current compared with the two-stage power systems. Moreover, high power density and low cost with small component counts and the optimized design for high efficiency can be simultaneously achieved. The verification of the proposed converter is proved with the prototype with $36 - 72V_{\rm DC}$ input voltage and 300 W (12 V/25 A) output capability. As shown in the curve of the measured efficiency, the proposed converter increases the efficiency about 0.43% at the half-load conditions and 0.91% at the full-load conditions compared with the conventional two-stage approach. Therefore, the proposed converter is expected to be very attractive for a high efficiency of 48 $V_{\rm DC}$ power system with a wide range of low input voltage.

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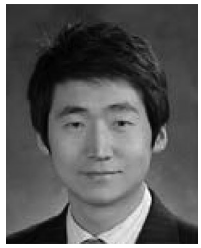

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