A PV Power Conditioning System Using Nonregenerative Single-Sourced Trinary Asymmetric Multilevel Inverter With Hybrid Control Scheme and Reduced Leakage Current

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***Abstract*—A power conditioning system (PCS) using multiple module-integrated converters and a single sourced 27-level asymmetric cascaded H-bridge multilevel inverter (MLI) without regeneration for photovoltaic (PV) applications is proposed. A newly suggested hybrid-switching closed-loop strategy is proposed to enable the use of a 27-level inverter in PV systems. The suggested hybrid-switching strategy implements fundamental line-frequency switching in the main H-bridge to ensure a high efficiency and low leakage current operation. Furthermore, high-frequency switching is used in the auxiliary H-bridge cells to achieve a higher bandwidth control loop. A cost-effective unidirectional single-ended 1-kW dc–dc module based on a boost coupled inductor and charge-pump circuits is proposed to achieve a single PV source per module for a multistring configuration. To couple the unidirectional converters with the central inverter, a jumping element in the hybrid switching strategy is introduced to enable an optimal nonregenerative operation. The proposed PCS with the control scheme is analyzed and verified using hardware results in a grid connected mode of operation.**

***Index Terms*—Asymmetric cascaded H-bridge, hybrid-switching strategy, photovoltaic (PV) applications, regeneration, trinary inverter.**

I. Introduction

DUE to the requirement of higher power, voltage, and efficiency for renewable energy power conditioning systems (PCS), several multilevel inverter (MLI) based power conversion systems have been proposed in recent years [1]–[6]. Multilevel inverters offer inherent advantages such as high power quality, low voltage stress on power electronic devices, reduction in filter size, and boosted output voltage. Although MLI were traditionally designed for high voltage industrial applications, they have also been gradually extended to small scale and residential photovoltaic (PV) applications [3]–[7].

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Among the several types of multilevel inverters, cascaded H-bridge (CHB) type of inverters have been preferred in PV systems [8]–[12]. CHB inverters are typically classified into two types: Symmetric and Asymmetric. Asymmetric CHB inverters provide a higher number of voltage levels compared to symmetric CHB inverters that have the same number of H-bridge cells. Furthermore, higher efficiency could be achieved with Asymmetric CHB because large amount of power passes through the main H-bridge with line frequency switching. The asymmetric CHB inverters can be further categorized based on their dc-link voltage ratios such as binary and trinary.

CHB-based PV systems have been proposed using PV string as a source for every individual H-bridge cell [13]–[14]. However, the partial shading phenomenon and requirement of maximum power point tracking (MPPT) in PV systems leads to a voltage imbalance between the H-bridge cells. qZC-CHB topologies have been proposed in previous literature to maintain voltage balancing among the H-bridge cells during MPPT operation [15], [16]. However, qZC-CHB topologies are not suitable for asymmetric CHB inverters that operate in low switching frequencies. qZC-CHB inverters require high frequency pulse width modulation (PWM), thereby limiting their application to symmetric CHB MLI. To overcome the aforementioned issue, the use of single sourced CHB inverters is the optimal solution.

Previous single sourced implementations have been proposed in the literature for other applications [17]. While line frequency transformer isolation is a solution, it renders the system bulky, reducing the efficiency and increasing the overall cost of the system. Another solution based on a high-frequency link (HFL) has been applied in traction applications [18]. Although the size and cost of the system was improved compared to the previous implementations, the topology proposed in [18] still requires additional switches and diodes used for the square-wave generator and the rectifier circuits.

In this paper, a modular single-ended dc–dc boost converter coupled with two charge pump circuits is proposed to provide the main dc link and the two auxiliary dc links (see Fig. 1). The 27-level MLI is used as a central inverter, while the single-ended dc–dc stages are connected in parallel to the dc-bus bars as a multistring configuration. In the proposed topology, the voltage gain of the charge pump is independent of the load current; therefore, the voltage balance is maintained even during light

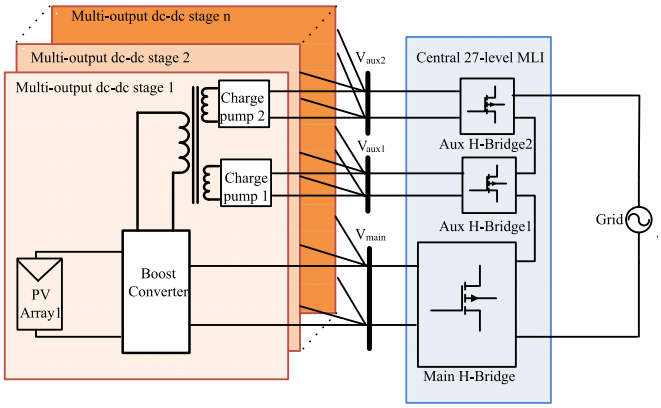


Fig. 1. Block diagram of the proposed trinary asymmetric inverter with single-ended preregulator in multistring configuration.

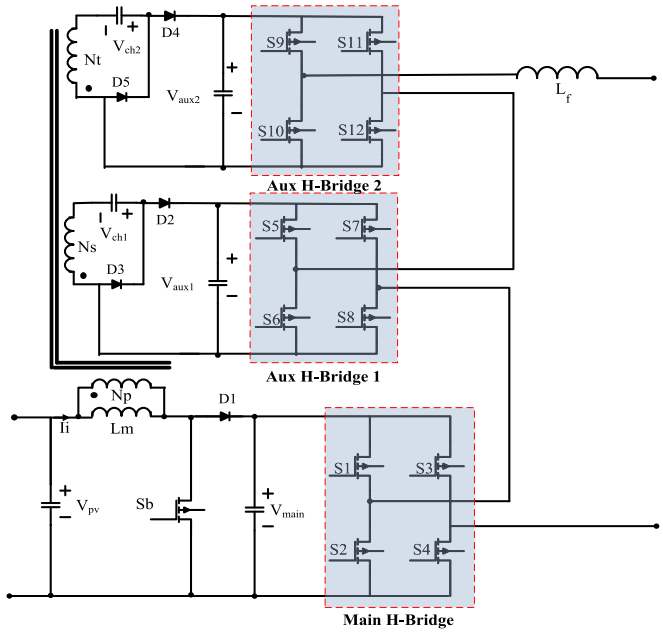


Fig. 2. Circuit diagram of proposed PCS with trinary asymmetric inverter and single-ended multioutput preregulator in grid connection.

load conditions. Additionally, soft switching is achieved in the charge-pump circuit by calculating the capacitor and switching frequency values in the design procedure. Moreover, since the transformer used for galvanic isolation in the charge-pump output is coupled with the boost inductor, the magnetic utilization ratio of the single core is enhanced and the size and cost are reduced.

Conventionally, the nearest level modulation (NLM) scheme has been applied for asymmetric CHB topologies of MLIs [19]. However, the low-frequency switching of NLM limits the design of the higher band width controllers that are required for PV grid-tied PCS. Furthermore, the auxiliary H-bridge cells have a regenerative power flow which is not applicable for unidirectional dc/dc converters.

A solution proposed in the literature is to apply PWM for both the high voltage main cell and the auxiliary lower voltage cells. However, this increases the undesirable common-mode leakage current in the system and reduces the overall efficiency of the inverter [20]–[23]. In the case of inverter topologies with leakage currents above the permissible limits, galvanic isolation between the grid and the inverter is required. However, isolation using a transformer would increase the cost and size of the PV PCS.

A modified hybrid-switching strategy is proposed to enable transformerless implementation of a trinary asymmetric inverter in grid-tied PV systems. The solution is based on a strategy using 60-Hz switching for the main H-bridge cell and high-frequency PWM for the auxiliary H-bridge cells. This basic hybrid-switching strategy results in loss of smooth tracking of the sine reference. The duration of this period, where the reference tracking is lost, is extremely short compared to the duration of the total fundamental period. Hence, it results in a negligible increase in THD compared to PWM in all H-bridge cells. However, this loss in reference tracking significantly affects the closed-loop operation of the grid connected controller. The saturation during the aforementioned period leads to controller instability. Therefore, an external zero-error signal is added to the hybrid control scheme to remove saturation in the period and achieve smooth grid current injection with low THD. However, the regenerative power in the auxiliary cells still needs to be resolved.

As mentioned previously, the single ended unidirectional dc/dc module requires the removal of the regenerative power flow. In previous literatures, solutions have been proposed including the design of specific firing angles or the addition of level jumping to remove negative power flow. However, calculating firing angles is not desirable for the proposed PWM-based control strategy, as discussed above. Furthermore, jumping in both auxiliary H-cells leads to a drastic increase of THD in the output [24], [25]. In this paper, jumping is only applied for an auxiliary two H-bridge cell to minimize the effect on THD.

Section II of this paper explains the operating principle of the proposed PCS in detail and Section III shows the procedure of the controller design and simulation results for the proposed PCS. Section IV explains the details of the hardware prototype implementation, while Section V concludes the paper.

II. The Proposed Single Sourced PV PCS

Fig. 1 depicts the complete architecture of the proposed PV PCS. According to the literature, the PV inverters are classified into three types:

1) centralized inverter;
2) multistring inverter;
3) module-integrated inverter or microinverter.

Since the trinary CHB inverter is applicable for high-power applications, centralized inverter architecture is chosen for the PV system. A multiple number (n) of PV strings with their individual dc–dc stages to implement MPPT operation are connected to the three dc-link bus bars. The proposed two-stage single-sourced PV PCS consists of a single ended boost converter coupled with two isolated charge-pump outputs, and a 27-level asymmetric CHB inverter. The complete circuit diagram of the PCS under grid-connection mode is illustrated in Fig. 2. The single sourced single ended boost dc/dc stage is cost effective because it is a single switch converter with a single core coupling the main boost stage to the other two auxiliary H-bride

circuits. The proposed PV PCS is also highly efficient, particularly when a small amount of power passes through the charge pump and auxiliary H-bridge circuits. However, the asymmetric 27-level MLI has a regenerative power flow in the auxiliary H-bride cells which is not suitable for uni-directional power flow. Therefore, a modified hybrid switching scheme is proposed, taking into account a reduced common mode leakage current. Section II-A describes the MLI power distribution and removal of the regenerative power flow. Section II-B describes the functioning and design of the single ended dc/dc stage.

A. 27-Level Asymmetric MLI

The trinary 27-level MLI consists of three H-bridge cells: the main and auxiliary 1 and 2 H-bridge cells. In the higher modulation index (m_a) regions (> 0.9), above 80% of the total power is processed by the main inverter. Hence, operating the main inverter under the fundamental line frequency ensures high efficiency. One of the inherent issues with the 27-level MLI is the presence of regenerative power flow in the auxiliary H-bridge cells, which can be eliminated by a jumping scheme in the PWM strategy.

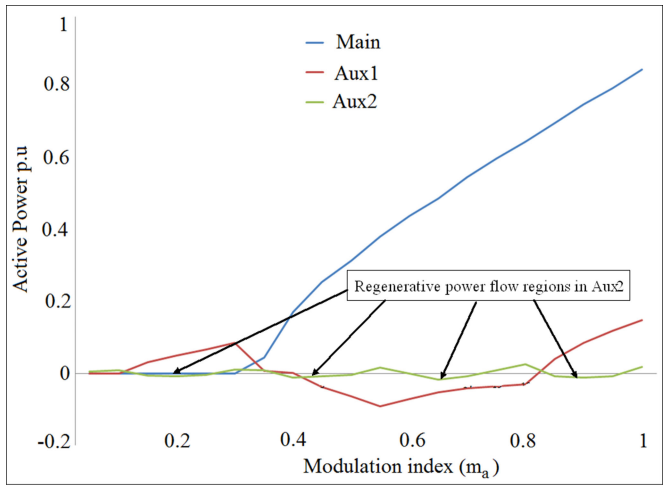
PWM with jumping has been used to eliminate regeneration in electric motor drive applications [25]. Negative power flow is restricted by calculating the inhibit negative current (INC) function for the auxiliary H-bridge cells and jumping the voltages for both auxiliary H-bridge cells. A modified version of the PWM method is proposed in this paper in response to the inherent changes present in PV applications compared to electric motor drives. One of the major differences in PV PCS is that the dc-link voltage for the centralized inverter is fixed. Hence, the inverter can be operated in fixed m_a regions with negligible variations. Also, the size of the grid-side filter is one of the major factors contributing to the size and cost of the PCS; therefore, it is advisable to operate the inverter in a high m_a region to obtain the maximum number of voltage levels in the output. From Fig. 3(a), it can be seen that only the auxiliary H-bridge-2 operates in regenerative mode at higher m_a values (above 0.8).

Hence, in the proposed PCS, the modulation strategy focuses on eliminating the regenerative mode in the auxiliary H-bridge-2. In grid-connected applications, the PCS operates in nearly unity power-factor conditions, which enables the regeneration to be eliminated by jumping the negative regions in the positive half cycle of the output voltage for the aux2 and vice-versa. Table I illustrates the parts where the aux2 output is jumped to 0 from –1. The per-unit power distribution for this modification can be derived from conventional NLM equations [19]. The reference for the sinusoidal signal is given by

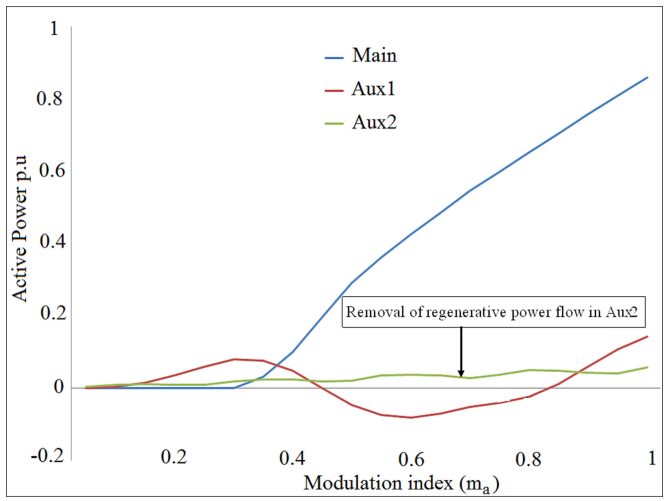
$$V_{\text{ref}} = m_a \sin(\omega t). \tag{1}$$

The fundamental output voltages of the main H-bridge and the auxiliary 1 are identical to the conventional NLM strategy without jumping. The fundamental output voltage to the aux2 is given by

$$V_{r3} = V_{r2} - 2c_2 s_2 \tag{2}$$



(a)



(b)

Fig. 3. Power distribution in the trinary inverter according to varying m_a (a) in conventional NLM and (b) with jumping applied to aux2.

TABLE I
LEVEL JUMPING IN AUX2 H-BRIDGE CELL (L: LEVEL, M: MAIN H-BRIDGE, A1: 1ST AUXILIARY, A2: 2ND AUXILIARY)

L	M	A1	A2	L	M	A1	A2
0	0	0	0	7	1	–1	1
1	0	0	1	8	1	0	–1 → 0
2	0	1	–1 → 0	9	1	0	0
3	0	1	0	10	1	0	1
4	0	1	1	11	1	1	–1 → 0
5	1	–1	–1 → 0	12	1	1	0
6	1	–1	0	13	1	1	1

where, V_{r2} is the reference voltage for aux1 and s_2 is the switching pattern for aux1 and $c_2 = (9/26)$. From Table I, the switching pattern for aux2 should satisfy the following:

$$S_3 = \begin{cases} 0 < s_3 = ((v_{r2} > c_2) - (v_{r2} < -c_2)) & V_{\text{ref}} > 0 \\ 0 > s_3 = ((v_{r2} > c_2) - (v_{r2} < -c_2)) & V_{\text{ref}} < 0 \end{cases}.$$

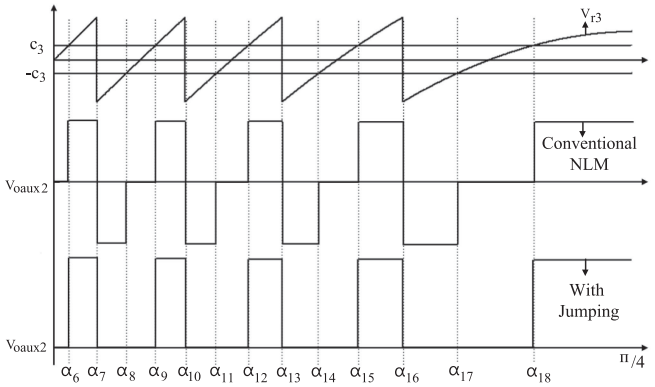


Fig. 4. Reference and output voltage for aux2 with conventional NLM scheme and jumping scheme.

Fig. 4 shows the fundamental output for auxiliary 2 H-bridge with the conventional NLM scheme and with the proposed jumping scheme. In the case of the jumping scheme, switching intervals for $\alpha_7, \alpha_{10}, \alpha_{13}$, and α_{16} has been used to obtain zero output voltage instead of negative output. The resulting fundamental output for auxiliary 2 is given by

$$\begin{aligned} V_{0\text{aux2}} &= V_{\text{aux2}}(s_3) \\ s_3 &= \frac{4}{n}(\cos(\alpha_6) - \cos(\alpha_7) + \cos(\alpha_9) - \cos(\alpha_{10}) \\ &\quad + \cos(\alpha_{12}) - \cos(\alpha_{13}) + \cos(\alpha_{15}) - \cos(\alpha_{16}) \\ &\quad + \cos(\alpha_{18}))\,. \end{aligned} \tag{3}$$

The power distribution curve for the individual H-bridge cells in the trinary inverter with jumping is shown in Fig. 3(b). It can be seen that there is no regenerative power in the aux2 H-bridge due to the elimination of the negative voltage output. The PWM strategy is based on the combination of left and right-justified timer scheduling [26]. One of the key advantages of this strategy is the accurate tracking of nonsinusoidal references in the H-bridge cells. While implementing the PWM strategy in the trinary inverter with jumping, the variation in the floor and ceiling voltages during each level caused by jumping should be taken into consideration. Duty-cycle calculation during each voltage level with and without jumping in the rising slope of the reference is given by

$$\text{Duty}-\text{cycle}_{(\text{no}-\text{jumping})} = \left(1 - \left(\frac{\text{ref} - \text{floor}}{V_{\text{aux2}}}\right)\right) \tag{4}$$

$$\text{Duty}-\text{cycle}_{(\text{with}-\text{jumping})} = \left(1 - \left(\frac{\text{ref} - \text{floor}}{2V_{\text{aux2}}}\right)\right) \tag{5}$$

where "ref" refers to the sinusoidal reference obtained from the controller and "floor" refers to the value of the voltage level immediately below the sine reference value. Fig. 5 shows the removal of negative power in the aux2 H-bridge cell with the jumping-PWM strategy applied to the trinary inverter compared to the PWM without jumping for $m_a = 0.9$. In Fig. 5(a), the average current from aux2 is negative, whereas it is positive in Fig. 5(b). In the proposed modulation scheme, the maximum

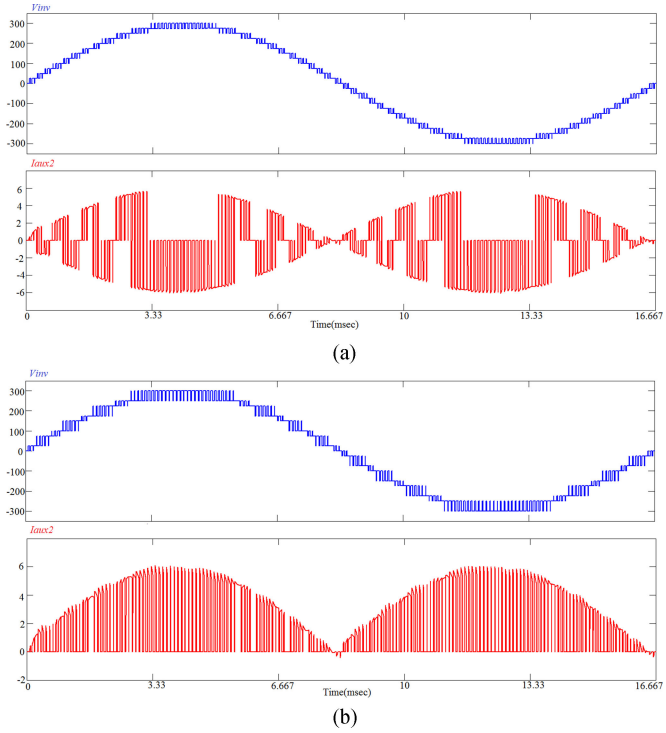


Fig. 5. Trinary inverter output voltage and current from the aux2 H-bridge cell, inverter output voltage (blue), auxiliary two dc-link capacitor current (red) for $m_a = 0.9$. (a) No jumping with 25 levels. (b) 17-levels with jumping.

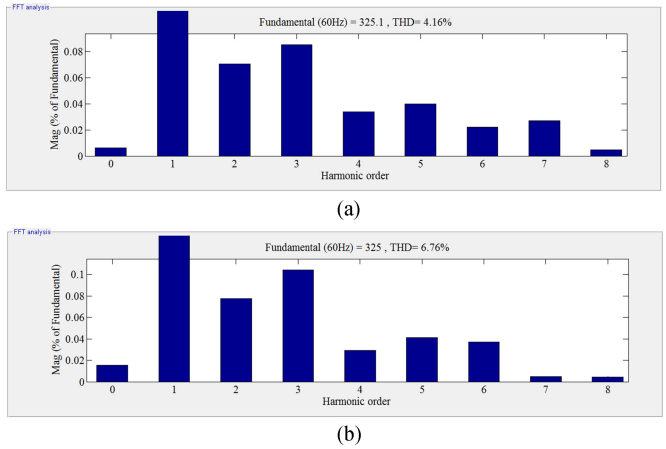


Fig. 6. Total THD and magnitude of individual harmonic orders up to 8. (a) Conventional PWM and (b) proposed PWM with jumping

available output voltage level has been reduced from 27 to 19 due to the jumping levels. Furthermore, the proposed jumping strategy occurs in only one H-bridge cell compared to two H-bridge cells in [25], therefore, a better waveform quality is achieved compared to the jumping performed in the motor drive applications.

The frequency spectrum and THD for the previous conventional scheme and the proposed scheme with jumping to prevent regeneration are shown in Fig. 6. It can be seen that the THD increased from 4.16% to 6.76% in the proposed scheme. This increase in THD is the result of jumping in the voltage levels,

which reduces the maximum output voltage level from 27 to 19. However, the magnitude of individual harmonic orders close to the fundamental frequency is critical, since it cannot be eliminated by the output filter inductor. From Fig. 5, it can be seen that the increase harmonics is very small due to the jumping scheme.

B. Boost Converter With Isolated Multioutput Charge Pump

The proposed newly organized dc/dc converter module consists of a single ended boost converter coupled with charge pump circuits (see Fig. 2). Traditionally, charge pump-based converters have been used as microinverters for lower power applications [27]–[32]. However, the auxiliary H-bridge cells in the 27 MLI process a small fraction of the total power. For example, in the case of the 1 kW dc/dc stage module, less than 200 W of power is processed by the charge pumps. Since the largest portion of the power is processed by the higher efficiency boost converter, the proposed dc–dc stage is suitable for this topology. The charge pump output voltages follow the boost converter output irrespective of the load condition. In this section, the steady-state voltage gain equations and the average, rms, and peak value equations for input current (I_i) are derived. The design procedure for soft switching and minimized switching losses operation is described.

The steady-state continuous conduction mode (CCM) voltage gains for both charge-pump outputs are given below

$$\frac{V_{\text{aux1}}}{V_{\text{pv}}} = \frac{1}{(1-D)}\left(\frac{N_s}{N_p}\right)$$
$$\frac{V_{\text{aux2}}}{V_{\text{pv}}} = \frac{1}{(1-D)}\left(\frac{N_t}{N_p}\right). \tag{6}$$

As shown in the equations, balancing between the main and auxiliary dc links can be obtained regardless of the duty-cycle D by adjusting the turn ratios.

Since the output power of the PV modules depends on the irradiance and temperature conditions, the PCS should also be able to operate under light load conditions in discontinuous conduction mode (DCM). The output voltage of the charge-pump circuit is directly dependent on the turns ratio (n) and the output voltage of the boost converter in the proposed PCS. Since the boost converter output is fixed under grid connection by the MLI dc-link controller, the charge-pump output voltage should also be matched by the transformer turns ratio (N). Fig. 7 shows the current flow for the boost converter and charge pump circuit during ON/OFF conditions. It can be seen that the energy is stored in the boost inductor and the charge pump capacitor when the switch (S_b) is turned ON [see Fig. 5(a)]. During the operation, we know the charge-pump capacitor is maintained at

$$V_{\text{ch}} = (V_{\text{pv}})\left(\frac{N_s}{N_p}\right). \tag{7}$$

Similarly, the stored energy is discharged when the switch is turned OFF. Fig. 5(b) indicated the output capacitor of the charge-pump circuit is charged. During the operation, the charge-pump

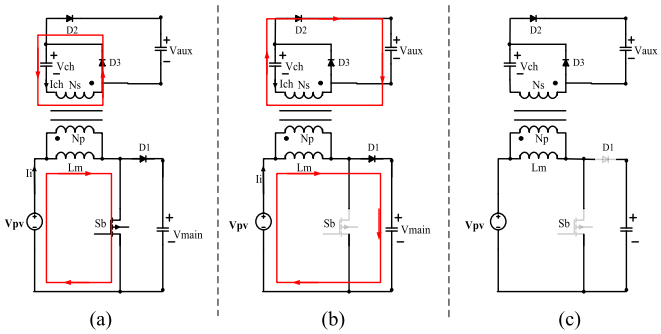


Fig. 7. DCM current flow for the boost and charge pump circuit. (a) Switch ON. (b) Switch OFF. (c) Diode OFF.

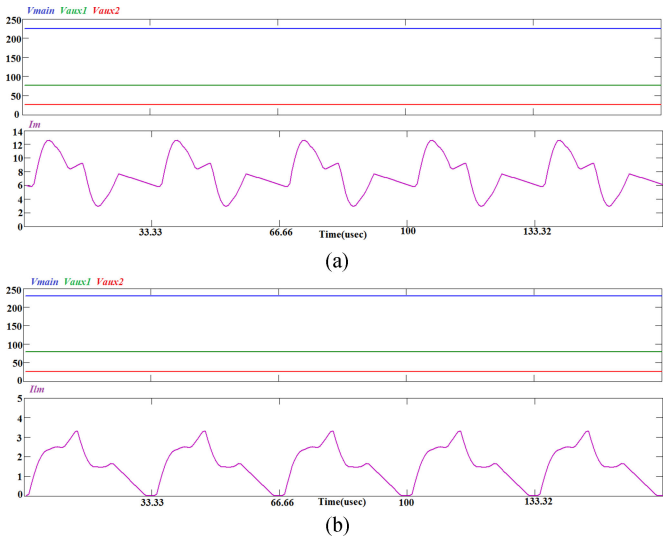


Fig. 8. Validation of the voltage balance during CCM/DCM in the PCS. (a) CCM mode. (b) DCM mode.

output capacitor voltage is given by

$$V_{\text{aux}} = (V_{\text{main}} - V_{\text{pv}})\left(\frac{N_s}{N_p}\right) + V_{\text{ch}} \tag{8}$$

where

$V_{\text{aux}} =$ Charge-pump output voltage.
$V_{\text{main}} =$ Boost converter output voltage.

From (7) and (8), the relationship between the charge-pump output voltage and the boost converter output voltage is derived as

$$V_{\text{aux}} = (V_{\text{main}})\left(\frac{N_s}{N_p}\right). \tag{9}$$

In the same manner, the tertiary output can be demonstrated. Fig. 8 shows the simulation results during the CCM and DCM operating modes, it can be seen that the voltage balance among the three H-bridge dc-links is maintained. Therefore, the balancing operation is achieved without any active switches and the controllers in the secondary and tertiary sides. This method ensures cost effectiveness by reducing the number of sensors, switches, and magnetic devices.

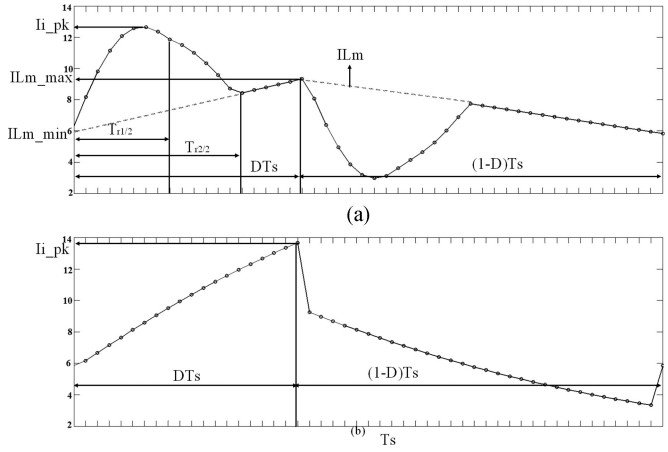


Fig. 9. Waveform for the input current I_i (a) with ZCS in charge pump; (b) without ZCS in charge pump.

The values of the charge-pump components can be designed to optimize the efficiency of the PCS. Since an inherent leakage inductance is present in the transformer, secondary in series with the charge-pump capacitor $C_{\rm ch}$, ZCS during turn-OFF is ensured for diode D3 by designing the capacitor $C_{\rm ch}$. ZCS in D3 also reduces the peak and rms values of the input current (I_i) in the primary side of the transformer, thereby reducing the conduction losses in the transformer primary and the conduction losses in switch S_b. The condition for ensuring ZCS in diode D3 is that the resonant frequency (f_r) of the charge-pump LC circuit should be greater than the critical resonant frequency ($f_{\rm rc}$) [27]. The critical resonant frequency is determined by

$$I_{\rm aux} = (1-\mathrm{D})\, V_{\rm aux} \left(\frac{2\sin(\omega_{\rm rc} T_s D)}{\sqrt{L_{\rm lk}/C_{\rm ch}}} - \frac{DT_s}{2N^2 L_m} \right) \quad (10)$$

where, $I_{\rm aux}$ is the average current charging the dc-link capacitor of the auxiliary H-bridge cell. Fig. 9(a) shows the waveform for the input current I_i with ZCS for both charge-pump circuits and Fig. 9(b) shows the waveform for $I_{\rm i}$ without ZCS in the charge-pump diodes. In the case of ZCS, the diode current charges the capacitor and reaches zero during its half-resonant period ($T_r/2$). Since the period ($T_r/2$) is less than the turn-ON time (DT_s), the peak of the diode current appears before the peak of the magnetizing current of the boost inductor (I_{Lm}), thereby reducing the peak of the input current (I_i) compared to the charge-pump circuit operating without ZCS.

The rms value for the input current I_i is derived below for the single charge-pump circuit for simplification. The maximum value of the diode current $I_{\rm max}$ can be derived as

$$\begin{aligned} I_{\rm av} &= \frac{1}{T_s} \int_0^{T_r/2} I_{\rm max} \sin(\omega_r t)\ dt \\ I_{\rm av} &= \frac{I_{\rm max} T_{r/2}}{T_s n} \\ I_{\rm max} &= \frac{n f_r P}{V f_{\rm sw} N} \end{aligned} \quad (11)$$

where P is the power delivered to the auxiliary H-bridge and the resonant frequency of the charge-pump circuit is given as

$$f_r = \frac{1}{2n\sqrt{L_{\rm lk} C_{\rm ch}}}. \quad (12)$$

The magnetizing current for the boost inductor during turn-ON is then

$$i_{\rm Lm+} = m_1 \mathrm{t} + I_{\rm Lm\_min} \quad (13)$$

where the positive slope (m_1) of the inductor current is given as

$$m_1 = \frac{I_{\rm Lm\_max} - I_{\rm Lm\_min}}{DT_s}. \quad (14)$$

Similarly, the magnetizing current for the boost inductor during turn-OFF is given as

$$i_{\rm Lm-} = I_{\rm Lm\_max} - m_2 t \quad (15)$$

where the negative slope (m_2) of the inductor current is given as

$$m_2 = \frac{I_{\rm Lm\_max} - I_{\rm Lm\_min}}{(1-D)T_s}. \quad (16)$$

The equation for the charge-pump current with the resonant frequency f_r is given by

$$i_{\rm ch} = I_{\rm max} \sin(\omega_r t)\,. \quad (17)$$

From (13), (15), and (17), the rms value for the input current I_i can be derived as

$$\begin{aligned} I_{i\_\rm rms}^2 &= \frac{1}{T_s} \\ &\left[\int_0^{T_{r/2}} (i_{\rm ch} + i_{\rm Lm+})^2 dt + \int_{T_{r/2}}^{DT_s} i_{\rm Lm+}^2\, dt + \int_{DT_s}^{DT_s+T_{r/2}} \right. \\ &\left. \times (i_{\rm Lm-} - i_{\rm ch})^2 dt + \int_{DT_s+T_{r/2}}^{T_s} i_{\rm Lm-}^2\, dt \right] \end{aligned} \quad (18)$$

$$\begin{aligned} I_{i\_\rm rms}^2 &= I_{\rm Lm\_rms}^2 + I_{\rm ch\_rms}^2 + \frac{2}{T_s} \\ &\left[\int_0^{T_{r/2}} (m_1 t + I_{\rm Lm\_min}) I_{\rm max} \sin(\omega_r t)\, dt \right. \\ &\left. - \int_{DT_s}^{DT_s+T_{r/2}} (-m_2 t + I_{\rm Lm\_max})\, I_{\rm max} \sin(\omega_r t)\, dt \right] \end{aligned} \quad (19)$$

where the boost inductor rms current is given by

$$I_{\rm Lm\_rms}^2 = \left(\frac{I_{\rm Lm\_max} + I_{\rm Lm\_min}}{2} \right)^2 + \frac{(I_{\rm Lm\_max} - I_{\rm Lm\_min})^2}{12} \quad (20)$$

and the charge-pump rms current is given by

$$I_{\rm ch\_rms}^2 = \frac{T_r I_{\rm max}^2}{4T_s} + \frac{I_{\rm max}^2}{T_s} \left(\frac{t_2}{2} - \frac{t_1}{2} + \frac{\sin(2c_1)}{4\omega_r} - \frac{\sin(2c_2)}{4\omega_r} \right). \quad (21)$$

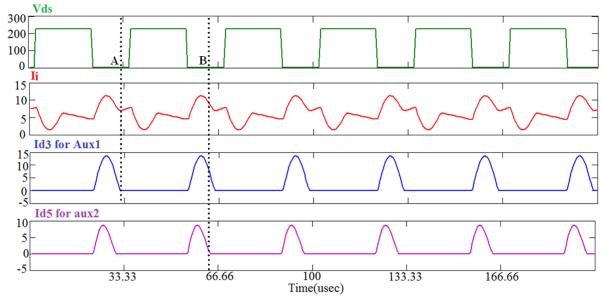


Fig. 10. Simulation waveform showing the ZCS for I_{D3} and I_{D5} for the designed charge-pump capacitor values.

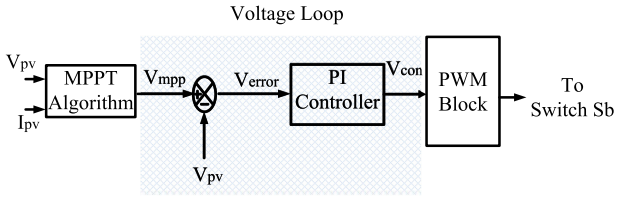


Fig 11. Control scheme for the multioutput dc–dc converter.

Using (11), (13), (14), (15), (16), and (19)

$$I_{i\_\mathrm{rms}}^2 = I_{\mathrm{Lm\_rms}}^2 + I_{\mathrm{ch\_rms}}^2 + \left(\frac{I_{\max}\left(mT_r + 4I_{\mathrm{Lm\_min}}\right)}{T_s\omega_r}\right) + \left(\frac{2mI_{\max}}{T_s\omega_r^2}\left(\sin(c_2) - c_2\cos(c_2) - \sin(c_1) + c_1\cos(c_1)\right) - \frac{2I_{\mathrm{Lm\_max}}I_{\max}}{T_s\omega_r}\left(\cos(c_2)\right) - \cos(c_1)\right) \quad (22)$$

where $t_1 = DT_s$, $t_2 = DT_s + T_{r/2}$, $c_1 = \omega_r t_1$, and $c_2 = \omega_r t_2$, respectively.

The charge-pump capacitor values are designed to achieve ZCS turn-OFF in the diodes using (10). Eqs. (21) and (22) are used to design the coupled inductor. After the coupled inductor was designed, the leakage inductance measured in the transformer secondary and tertiary were found to be around 2.7 and 0.58 μH, respectively. Hence, for a switching frequency of 30 kHz, the charge-pump capacitances of the auxiliary 1 and auxiliary 2 charge-pump circuits were chosen to be 3 and 5 μF, respectively. Fig. 10 shows the simulation waveforms for ZCS turn-OFF in diodes D3 and D5. Both the diodes reach zero current before switch turn-OFF and points A and B refer to the half-resonant period in the charge-pump circuits for auxiliary 1 and auxiliary 2, respectively.

The control scheme for the dc/dc converter stage is simplified as the charge pump output voltages follow the output of the main boost converter. The control signal for the boost converter switch (S_b) is used to realize the MPPT operation (see Fig. 11). The MPPT controller uses a conventional perturb-and-observe (P&O) algorithm. The variable PV voltage is perturbed with a specific step voltage (ΔV) during a time step (ΔT). The variation of the power (ΔP) is calculated, and accordingly the direction of ΔV is decided to track the MPP. This algorithm ensures a high efficiency of energy conversion, irrespective of the atmospheric conditions. For implementing the step change in the PV voltage, the transfer function of the control-to-input voltage (G_{vpvd}) is used to design the controller. The transfer function for G_{vpvd} is derived for the boost controller as shown below

$$G_{\mathrm{vpvd}} = \frac{\hat{V}_{\mathrm{pv}}}{\hat{d}} = \frac{-V_{\mathrm{main}}}{s^2 L_m C + \frac{sL_m}{R_s} + 1}. \quad (23)$$

III. Proposed Hybrid Switching and Control Scheme for the MLI

Conventional PWM techniques to implement transformerless operation in PV systems manipulate the switching to eliminate leakage current. In this paper, since the auxiliary H-bridge cells have a coupled inductor transformer, the leakage current is reduced by operating the main H-bridge in fundamental frequency instead of the high switching frequency, thereby eliminating the requirement of isolation transformer. One of the functions of the hybrid PWM strategy is to recognize the levels in which a high-frequency PWM is needed in the main H-bridge to track the reference sine waveform and inhibit the high-frequency switching during that level. The inherent advantage of using such strategy is that the operating modes requiring high-frequency PWM are only the main-inverter transition (0 to 1) periods. In the case of trinary asymmetric MLI, the high-frequency operating region for the main H-bridge cell can be tracked from the switching states as a transition from level 4 to level 5 (see Table I). Since PWM is only inhibited in this level, the effect in the THDs is quite small. The block diagram for the modified PWM strategy is shown in Fig. 12 and explained below.

1) The sine reference signal is sampled with a fixed sampling time in the digital signal processor.
2) The modulation s_1 for the main H-bridge is identical to the NLM technique, where the switch is turned ON when the reference crosses $c_1 = (9/26)$ for 27-level MLI.
3) The reference for the auxiliary H-bridge cells is derived by subtracting the main H-bridge output s_1 from the sine reference.
4) From the reference in step 3, the slope, floor, and ceiling values are calculated to implement the left and right-justified timer algorithm as shown in [26].
5) The switching frequency is fixed by the selected carrier wave frequency, and the modulated voltage output is then obtained.
6) The PWM inhibition is performed for main H-bridge by limiting the level 4 to 5 in the signal.
7) A Look-up table is used to obtain the switching states for aux 1 and 2 H-bridge cells for the respective levels.
8) One of the additional proposals in the controller design is the zero-error signal method. Since the hybrid PWM strategy has inhibition modes, an external signal is used to hold the error signal at zero in order to avoid control voltage saturation during the inhibition modes. The influence of the proposed scheme will be shown in Section IV.

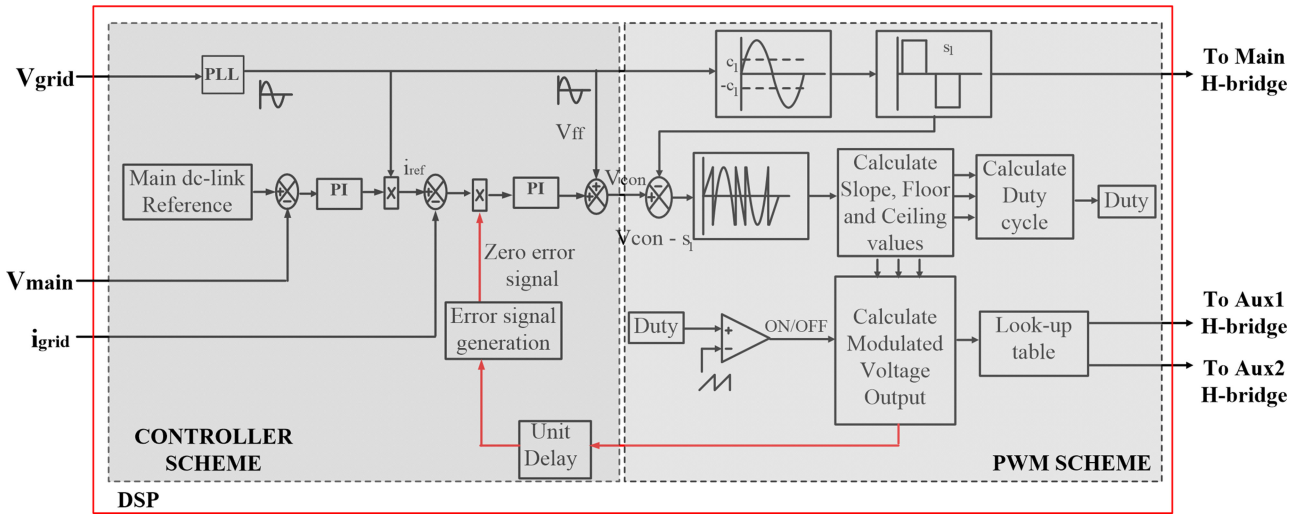


Fig. 12. Block diagram for the hybrid PWM strategy with control scheme for the 27-level inverter.

Fig. 13 depicts the simulation results to show the reduction of the leakage current in the proposed hybrid-switching scheme compared to the conventional PWM scheme for the three-level H-bridge and trinary asymmetric inverter. The leakage current is reduced from 756 mA rms in the three-level H-bridge to 243 mA rms in the 27-level inverter, and finally up to 92 mA rms in the proposed hybrid-switching scheme with a 100 nF parasitic capacitance and 1-kW output power.

Digital PI controllers have been previously used in MLI-based PV PCSs [33]–[37]. Fig. 12 shows the two-loop control scheme for the grid-connected 27-level inverter. The outer voltage loop is implemented to control the dc-link voltage of the main H-bridge cell, since the charge-pump circuits will fix the other dc-link voltage for the auxiliary H-bridge cells. Additionally, an inner current loop is used to maintain a unity power factor and the permissible THDs for the current injected to the grid. Hence, it is essential to derive transfer functions for both loops. From Table I, it can be seen that with the inclusion of jumping modulation, there are only ten operating modes for the inverter. The state equations for modes 1 and 2 can be derived as

$$L = \frac{di_L}{dt} = -V_o \qquad \text{(mode1)}$$
$$L = \frac{di_L}{dt} = -V_o \qquad \text{(mode2).} \tag{24}$$

By considering the step change in the voltage between 0 and V_{aux2}, the inverter model can be simplified as

$$\frac{\hat{i}_L}{\hat{V}_{\text{con}}} = \frac{V_{\text{aux2}}}{sL}. \tag{25}$$

It should be noted that during the jumping intervals, the voltage across the inductor becomes twice the auxiliary-2 dc-link voltage (V_{aux2} in Fig. 2).

The control-to-v_{main} transfer function should be derived for the controller design of the outer voltage loop. For an ideal 27-level inverter, the input power is equal to the output power.

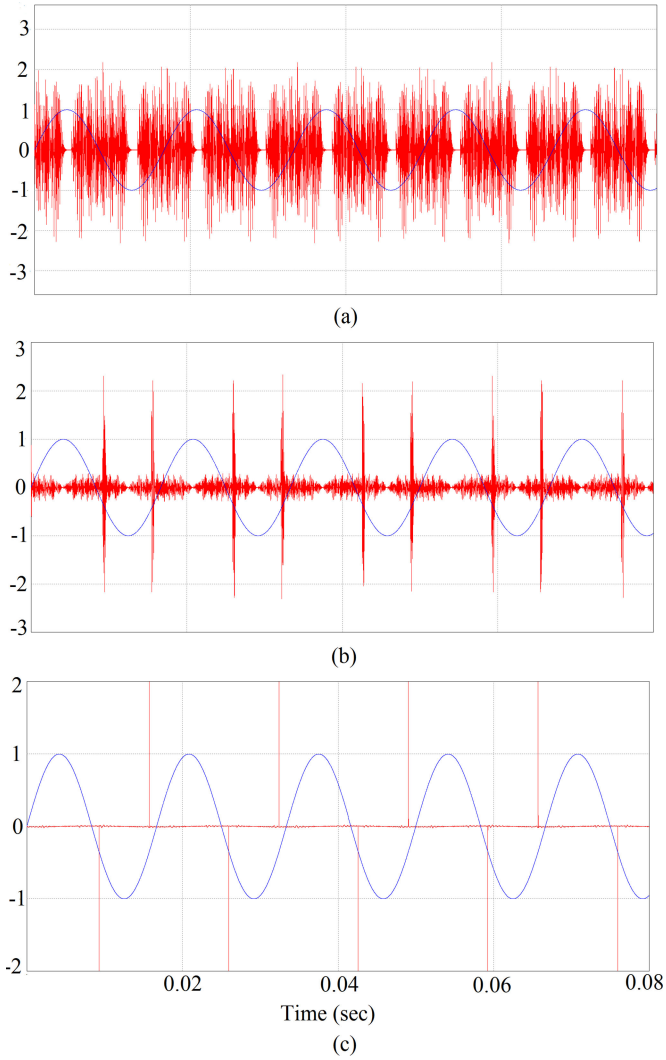


Fig. 13. Simulation waveform of the leakage current under a sine reference for (a) 3-level inverter (756 mA_{rms}), (b) conventional 27-level PWM case (243 mA_{rms}), and (c) proposed hybrid-switching scheme (92 mA_{rms}).

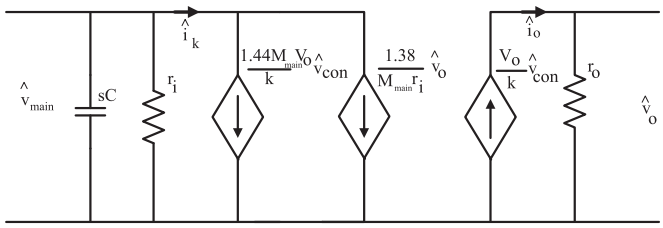


Fig. 14. Small-signal circuit diagram of the 27-level inverter.

We then have

$$(v_{\rm main}\, i_{\rm main}) + (v_{\rm aux1} i_{\rm aux1}) + (v_{\rm aux2} i_{\rm aux2}) = v_o i_o \quad (26)$$

$$v_{\rm main}(i_{\rm main} + i_{\rm aux1} + i_{\rm aux2}) = v_o i_o \quad (27)$$

$$v_{\rm main} i_k = v_o i_o \quad (28)$$

where $v_{\rm main}$ and i_k are the input dc quantities and v_o and i_o are the output rms values. On the assumption that the current injected to the grid tracks the reference well without errors, the output current is equal to the current-loop reference determined by multiplying from the phase-locked loop (PLL) block output multiplied with the voltage loop output

$$i_o = \left(\frac{v_o}{k}\right) v_{\rm con} \quad (29)$$

where *k* is the sensor ratio, from (28) and (29)

$$\frac{v_o^2}{k} v_{\rm con} = v_{\rm main} i_k. \quad (30)$$

From the above equations, the value of the modulation index in relation to $v_{\rm main}$ can be derived as

$$M_{\rm main} = \frac{V_{\rm grid}}{V_{\rm main}} = \frac{1}{1.444}\sqrt{\frac{k}{(v_{\rm con} r_i)}} \quad (31)$$

where r_i is the input small-signal resistance. Using the state-space averaging technique in (30) and (31), we have

$$\hat{i_k} = \frac{1.38}{M_{\rm main} r_i}\hat{V}_o + \frac{1.44 M_{\rm main} v_o}{k}\hat{V}_{\rm con} - \frac{1}{r_i}\hat{V}_{\rm main} \quad (32)$$

$$\hat{i}_o = \frac{V_o}{k}\hat{V}_{\rm con} + \frac{0.479}{{M_{\rm main}}^2 r_i}\hat{V}_o. \quad (33)$$

The small-signal model derived from (32) and (33) is shown in Fig. 14. The equation for the output small-signal resistance (r_o) is derived as

$$\mathrm{r_o} = -{M_{\rm main}}^2 r_i. \quad (34)$$

The control-to-$v_{\rm main}$ transfer function can be derived from Fig. 12 as

$$\frac{\hat{V}_{\rm main}}{\hat{V}_{\rm con}} = \frac{1.44 M_{\rm main} V_o}{k}\left[\frac{r_i}{1 + sCr_i}\right]. \quad (35)$$

In two-loop controller configurations, the inner-loop bandwidth is usually designed to be much higher than that of the outer loop in order to accommodate the smooth tracking of the outer-loop reference by the inner-loop control parameter. In this implementation, since PI controllers have steady-state error in tracking the sine reference, an additional grid-voltage feedforward was used to eliminate the steady-state error as shown. The feedback controller bandwidths for the inner loop and outer loop were chosen as 1 kHz and 300 Hz, respectively.

TABLE II
PARAMETERS WITH RESPECTIVE VALUES IN HARDWARE PROTOTYPE

Parameter	Value	Parameter	Value
V_i	120 V	L_m	495 uH
$V_{\rm main}$	225 V	n1:n2:n3	9:3:1
V_{aux1}	75 V	$C_{\rm ch1}$	3 uF
V_{aux2}	25 V	$L_{\rm leak}$	2.773 uH
$V_{\rm ac}$	220 V	$R_{\rm esr}$	0.35 Ω
$f_{\rm ac}$	60 Hz	$C_{\rm ch2}$	5 uF
$F_{\rm sw}$ for S_b	30 kHz	$L_{\rm leak1}$	0.57 uH
L_f and $\rm C_f$	1.8 mH and 2uF	$\rm R_{esr1}$	0.175 Ω
$F_{\rm sw}$ for 27-level inverter			10 kHz

TABLE III
PROTOTYPE COMPONENTS WITH THE PART NUMBERS

Components	Part number
Boost converter switch S_b	SCH2080KE
Aux H-bridge cell switches	IRFP4568
Main H-bridge cell switches	IRFP4868
Diodes	RUR1S1560S

IV. HARDWARE IMPLEMENTATION

The proposed PV PCS using a trinary 27-level inverter was implemented to verify the circuit operation and PWM strategy. The dc/dc converter module prototype was designed for 1-kW rating. The parameters and their respective values used in the prototype are shown in Table II and the components with their part number are shown in Table III. TI DSC TMS320F28335 was used to implement the control scheme in the PCS prototype. First, the design of the charge pump circuit is verified to work under ZCS, resulting in high efficiency. Second, the elimination of regenerative power flow using the proposed jumping strategy is verified. The reduction in the common mode leakage current in the proposed hybrid switching scheme is verified by comparing to other conventional switching schemes. Finally, the inverter grid connection control scheme combined with the MPPT operation for the dc/dc converter is verified. Fig. 15 shows the ZCS turn-OFF operation for didoes D3 and D5 (see Fig. 2) in both charge-pump circuits. The diode currents reach zero during their respective half-resonant periods before the switch turn-OFF, thereby achieving soft switching. The maximum rms current values for $C_{\rm ch1}$ and $C_{\rm ch2}$ in the PV PCS are 5 and 3 A, respectively. Fig. 16 shows the experimental waveforms to verify the modified jumping modulation to remove regeneration when connecting the trinary inverter to a resistive load. It should be noted that the aux2 H-bridge output voltage is positive in the positive half cycle of the inverter, and changes the polarity in the other period to remove regeneration. During the jumping regions, the inductor current is not significantly distorted due to the small magnitude and time of the jumping voltage. This helps

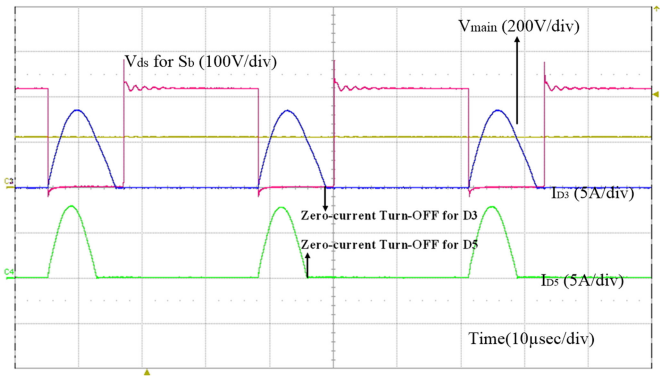


Fig. 15 Experimental waveforms showing ZCS turn-OFF for diodes D3 and D5. From top to bottom: Drain-source voltage for switch S_b, boost converter output voltage, current flowing through diode D3, and diode D5 current.

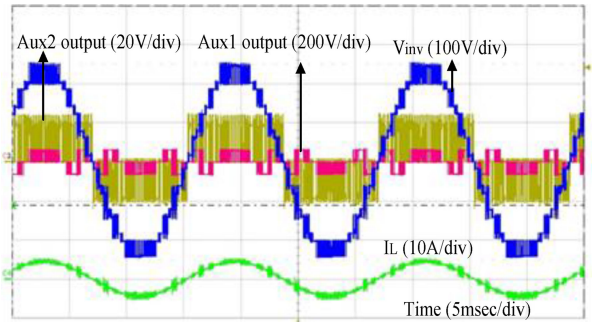


Fig. 16. Experimental waveforms showing the modified jumping-PWM scheme to remove regeneration in the trinary asymmetric inverter. From top to bottom: total inverter output voltage, Aux-2 H-bridge output, Aux-1 H-bridge output, and inductor current.

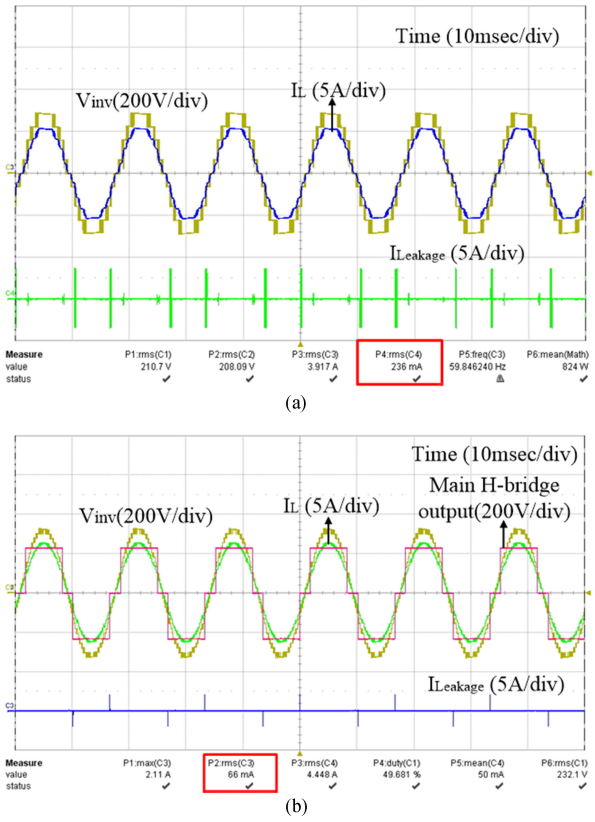


Fig. 17. (a) Experimental result of the leakage current with PWM applied to all H-bridge cells. $I_{\mathrm{Leakage}} = 236\,\mathrm{mA_{rms}}$. From top to bottom: inverter output, voltage output filter inductor current, and leakage current. (b) Experimental result for the leakage current with the proposed hybrid-switching scheme applied to H-bridge cells. $I_{\mathrm{leakage}} = 66\,\mathrm{mA_{rms}}$. From top to bottom: inverter output voltage, output filter inductor current, 60-Hz waveform for Main H-bridge output, and leakage current.

to ensure minimal increase in THDs, which is a major factor for implementing MLIs in PV systems.

Fig. 17(a) shows the leakage current waveform of the trinary asymmetric inverter with conventional PWM applied to all the H-bridge cells with a parasitic capacitance of 100 nF connected to the input in order to emulate the input stray capacitance present in the PV arrays. It should be noted that even though the leakage current is reduced compared to the conventional three-level H-bridge inverter, the leakage current value (236 mA rms) is very marginal to the German standard of 300 mA rms. This is from the high-frequency PWM switching in the main H-bridge and is not advisable to apply to a topology without a transformer. Fig. 17(b) shows the reduction in the leakage current (66 mA rms) of the proposed hybrid-switching scheme for the MLI.

Fig. 18(a) shows the unstable closed-loop operation under a grid-connected operation without the implementation of the zero-error signal in the strategy. It can be seen that the output current becomes seriously distorted during the main H-bridge transition states. Fig. 18(b) shows the current waveform in the grid by the trinary inverter. By adding the external zero-error signal during the main H-bridge transition periods, the control voltage is not saturated during the main H-bridge transition periods and the reference is able to be tracked with minimum distortion. The Fluke 434 power quality analyzer is used to measure the THD values of grid voltage and current. It should be noted that under harsh grid-voltage conditions (3.5% THD), the trinary inverter is still able to deliver the current under unity power factor and 4.3% THD. The jumping in the inverter output voltage indicates that the control scheme was able to successfully regulate the grid current while removing the regeneration in the trinary inverter.

For the MPPT test under grid-connected condition, a dual -module PV simulator (TerraSAS, ELGAR) was used for the PCS hardware prototype. Two PV channels (modules) were connected in parallel to the two individual boost charge-pump converters connected to the dc-bus bars. The physical parameters for the PV panels in channel 1 and channel 2 were chosen as: open circuit voltage (Voc) as 75 and 50 V, short circuit current (Isc) as 5 and 6 A, respectively. The voltage step (ΔV) and the time step (ΔT) for the P&O algorithm were chosen as 3 V and 1 s, respectively. The prototype was tested under a cloudy-day profile, as shown in Fig. 19.

The MPPs vary according to the individual irradiance and temperature profiles, and the MPPT efficiency of the prototype controller was measured by the simulator. The results for the cloudy-day profile test are shown in Fig. 20. Fig. 20(a) and (b) illustrate the MPPT profile result for two modules with different MPP voltage and current values connected to the individual boost charge-pump stages simultaneously. It can be seen that

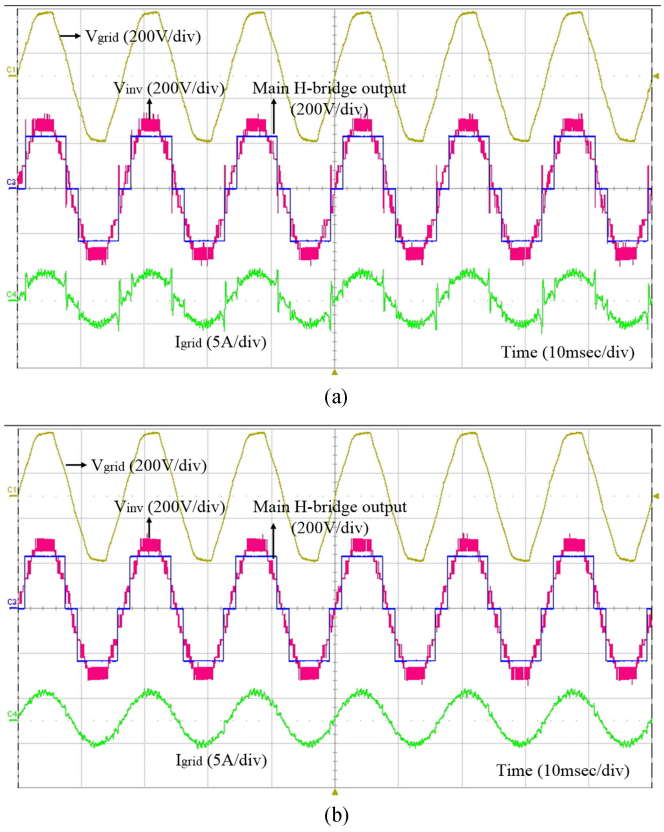


Fig. 18. Experimental waveforms for grid-connected inverter. From top to bottom: grid voltage, total inverter output voltage, main H-bridge output voltage, grid current. (a) Without zero-error signal in control scheme. (b) With the proposed zero-error signal in control scheme.

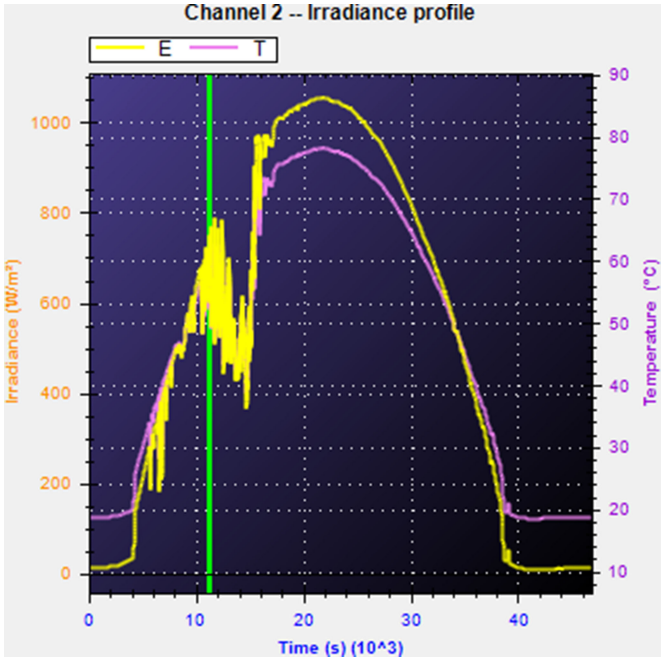


Fig. 19. Cloudy-day profile plot showing the variations in irradiance and temperature during different times of the day.

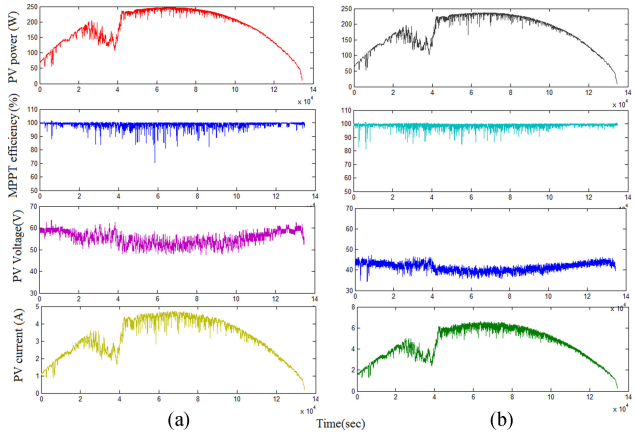


Fig. 20. Experimental results showing PV power, MPPT efficiency, PV voltage, and PV current during the profile test for the two PV channels in parallel connection. (a) Result for module connected to channel 1 and (b) result for module connected to channel 2.

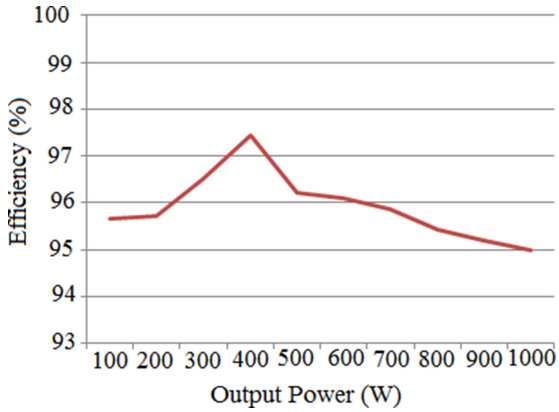


Fig. 21. Efficiency curve for the total PV PCS which includes a multioutput DC–DC converter with the trinary inverter.

during the entire test, even though the power output from the simulator varies continuously, the MPPT efficiency is consistently maintained close to 100% by both multioutput dc–dc converters. It should also be noted that during this test, the boost charge-pump operates under both the DCM and CCM modes. Fig. 21 shows the efficiency curve for the total PCS that includes the multioutput dc–dc converter and trinary inverter. It can be seen that the overall efficiency is above 95% with peak efficiency of 97.44% at 400-W output. European weighted efficiency (Δ_{EU}) for the entire PV PCS is calculated to be 96.03%.

V. Conclusion

In this paper, a centralized 27-level asymmetric CHB inverter with distributed module-integrated converters using a multioutput charge-pump-coupled boost dc–dc converter topology for grid-connected PV power-conditioning applications is presented. A modified hybrid-switching scheme was presented to implement 60-Hz operation for the main H-bridge to enable transformerless operation without leakage current issue as well as to improve the efficiency. Also, a jumping modulation was

used in the auxiliary-2 H-bridge to eliminate the regeneration issue in the trinary inverter. A zero-error signal is introduced in the closed-loop strategy to enable the steady-state operation in grid connection. Multiple charge-pump circuits are coupled with a boost inductor in the circuit to provide isolated dc-link voltage for the auxiliary H-bridge cells. Soft switching is achieved in the charge-pump circuits by designing the capacitor values. For the dc-link balancing, the voltage gain of the charge pump circuit automatically tracks that of the boost converter with the transformer ratio, hence providing a regulated output in a passive manner for the auxiliary dc-link input of the auxiliary H-bridge cells. The proposed PCS maintains the gain in both CCM and DCM conditions. Due to the use of a reduced number of parts, the proposed system is cost effective and reliable. The proposed system is verified using a hardware prototype with a 1-kW output.

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