A Novel Adaptive Quasi-Constant On-Time Current-Mode Buck Converter

Chin-Fu Nien, Dan Chen, Sheng-Fu Hsiao, Le Kong, Ching-Jan Chen, Wei-Hao Chan, and Yen-Liang Lin

***Abstract*—There have been a variety of constant on-time (COT) controllers for dc power converter applications reported in recent years [1]–[5]. In this paper, a novel adaptive quasi-constant on-time current-mode control scheme is proposed and implemented in buck converters. While preserving the advantages of the conventional COT current-mode converters, this scheme allows fast transient response to step-load that is a critical requirement of a computer load with smart management. A small-signal model of the proposed circuit is also developed. Experimental results are also provided. This scheme is well suited for the next-generation dc converters for power management central-processor-unit devices.**

***Index Terms*—Buck converter, constant on-time current-mode (COTCM), describing function (DF), voltage regulators (VRs).**

I. Introduction

In THE past several years, the dc power converters using the constant on-time current-mode (COTCM) control scheme has been adopted for many computer central-processor-unit (CPU) applications. There are three advantages of using this scheme for such an application. First, the current-mode scheme is well suited for the multiphase interleaved converters commonly employed for low-voltage high current applications [6], [7]. Second, it allows easy adjustment of converter output load line for achieving adaptive voltage positioning (AVP) feature commonly required for such an application [8]–[14]. And third, constant on-time scheme allows high conversion efficiency for both the heavy-load and the light-load conditions [15], [16].

However, there is a drawback for a conventional COTCM scheme in general, that is, the converter step-load transient is poor. The output voltage overshoot or undershoot caused by a step load is often exceedingly high. There is usually a stringent requirement placed for an acceptable over/undershoot voltage. To alleviate the problem, a large number of costly and bulky output capacitors are often required that increases the cost and volume of the converter. There is a fundamental reason why this problem exists in using the conventional COTCM scheme, that is, the ON time duration remains fixed during the step-load transient regardless of input/output conditions. For example, when the load is suddenly reduced after the initiation of the on-time, the switch continues "ON" until it expires at the end of a predetermined fixed ON time. As such, energy is continually pumped into the output while the load demand is already reduced that causes unnecessarily high output voltage overshoot. There were papers reported [5], [17], [18] to change the "ON" time to alleviate problems that the fixed on-time may give rise to. In [17], a scheme was proposed to adjust the on-time duration to improve the circuit performances in steady-state operation. Yet it does not help the overshoot problem mentioned earlier, though with the name "adaptive on-time" in current-mode control. In [18], a high-frequency filter circuit is added to sense the output voltage at the load transience and change the on-time duration dynamically with current-mode constant on-time (COT) control. However, the addition of the filter complicates other circuit performance such as the circuit stability. The filter circuit parameters need tuning according to power stage parameters. That is not only troublesome but also impractical due to the fact that the filter cannot be integrated in the controller chip. In [5], the ramp pulse modulation scheme is presented, which focuses on similar issue, also aimed to solve this issue by changing the on-time dynamically. However, since it is the ripple-based COT control, making it hard to do the current-sharing in multiphase converters. Furthermore, no existing model is presented concerning this kind of control scheme. In this paper, a novel adaptive quasi-constant on-time current-mode (AQCOTCM) scheme will be proposed to improve the transient behavior while preserving the advantages of a basic COTCM.

In this paper, a dynamic on-time current mode (DOTCM) scheme will be proposed first. By analyzing the DOTCM scheme, it can be seen that while the step-load transient performance improves, there is a serious drawback of the DOTCM scheme. That is, the converter switching frequency varies widely with load condition even in CCM condition. So, the DOTCM scheme will then be modified to remove the drawback while preserving the fast-transient characteristic. This newly proposed scheme, the main focus of this paper, is the adaptive quasi-on-time current-mode scheme abbreviated as AQCOTCM. A small-signal model will also be developed for this scheme, and can be extended to multiphase structure. Simulations and experimental results will be given to verify the proposed AQCOTCM control scheme.

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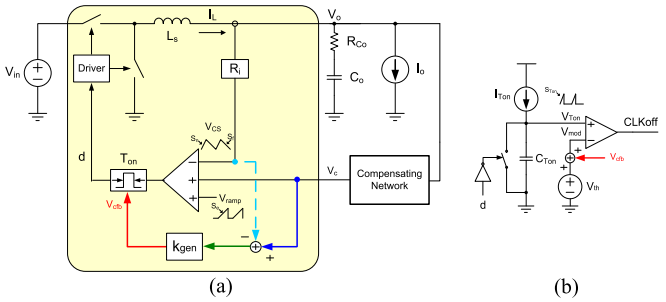

Fig. 1. (a) Circuit diagram of the proposed control schemes, (b) on-time generator, where COTCM: all color lines removed; DOTCM: only the dashed line removed; AQCOTCM: all lines connected.

II. Proposed AQCOTCM Control Scheme for Buck Converters

As mentioned, a description of the DOTCM scheme will be given first, followed by the discussion of the circuit drawback. From the discussion, the proposed AQCOTCM scheme will be given.

A. Description of the DOTCM Circuit

Fig. 1(a) shows the circuit diagram of a buck converter with the proposed DOTCM control scheme when the colored solid lines are connected and dashed line is removed. If all the colored lines are removed, then it is the conventional COTCM circuit. It was mentioned earlier that the on-time $T_{\rm on}$ is fixed regardless of the load change in a conventional COTCM circuit that accounts for the slow output voltage response to step-load change. In the diagram, the colored solid line path provides a path for the control signal V_c to directly affect the initiation and the duration of the ON time. Any change in the output voltage is quickly reflected to V_c, which is amplified through a constant gain $k_{\rm gen}$ to become $V_{\rm cfb}$; then added $V_{\rm th}$, a dc threshold voltage shown in Fig. 1(b), to become $V_{\rm mod}$ signal that directly affects the generation of $T_{\rm on}$. As shown in the diagram, the inductor current is sensed to achieve PWM current-mode operation with the control signal V_c. And $V_{\rm ramp}$ signal is an external ramp signal for increasing noise margin [19], so can be used for stabilizing current loops in multiphase case [20]. Fig. 1(b) shows the circuit diagram of the on-time generator of a DOTCM circuit. The sawtooth waveform $V_{T\rm on}$ is generated when the current source $I_{T\rm on}$ is charging the $C_{T\rm on}$ capacitor during the main switch "ON" time, and is set to zero when the $C_{T\rm on}$ is shorted during the "OFF" time. As a comparison, the on-time generator of a conventional COTCM is shown in Fig. 1(b), with the red line removed. It can be seen that in DOTCM (with the red line connected) the $V_{\rm mod}$ signal, which is directly affected by V_o, is involved in the on-time generation. For example, if V_o suddenly rises due to a step-down load, then $V_{\rm mod}$ would be reduced that immediately leads to a smaller duty cycle during the transience. This would cut down the amount of energy being pumped to the output in accordance with the load demand during the transience, and that would reduce the output voltage overshoot. For the conventional COTCM scheme, that is not the case. Fig. 2(a) shows simulation waveforms of a step-load transient response

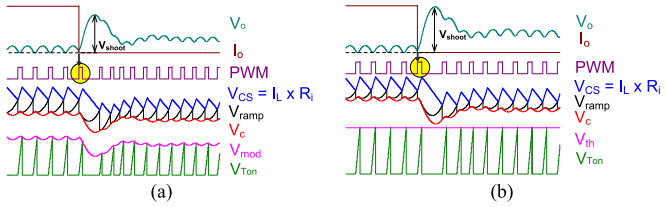

Fig. 2. (a) DOTCM result ($V_{\rm shoot}$ = 387.53 mV), where $k_{\rm gen}$ = 12.5. The encircled ON time is shortened from 2.76 to 2.41 μs when the step-down load occurs. (b) COTCM result ($V_{\rm shoot}$ = 465.57 mV). Notice the encircled ON time remains at 2.76 μs.

TABLE I
Circuit Parameters/Conditions for Simulated Verification

Input voltage $V_{\rm in}$	12 V
Output voltage $V_{\rm o}$	3.3 V
Inductor $L_{\rm s}$	10 μH
DCR of inductor $R_{\rm Ls}$	1 mΩ
Output capacitor $C_{\rm o}$	44 μF
ESR of capacitor $R_{\rm co}$	5 mΩ
On-time generator modulation gain $k_{\rm gen}$	12.5
Current sensing gain $R_{\rm i}$	100 mΩ
Switching frequency at 7 A $f_{s,\rm H}$	100.0 kHz
Current load step $I_{\rm o}$	7 A$\rightarrow$5 A
DC threshold voltage $V_{\rm th}$	5 V

when the DOTCM scheme is used. As can be seen, right after the load-releasing step, the output voltage V_o increases. So, V_c and $V_{\rm mod}$ both decrease. Therefore, the "on-time" pulse is immediately shortened, reducing the amount of energy being delivered to the converter output capacitors. As a comparison, one can see from Fig. 2(b) for the case when a conventional COTCM scheme is used, the reaction of the "on-time" pulse duration stays unchanged, causing a delayed control reaction and longer "off-time" also due to excessive energy delivered to the output capacitors. Table I lists the converter component values and working conditions. In this particular example, a significant improvement of overshoot voltage from 465.57 to 387.53 mV was observed by using the DOTCM scheme. Similar conclusion can be made for undershoot voltage when a step-up load current is encountered. DOTCM scheme does improve the converter dynamic load transient. However, notice in the figure that the steady-state switching frequency of the DOTCM scheme is highly dependent on the load current level, unlike the case of the COTCM scheme. This is a serious drawback for the former because significant switching frequency variation hurts the overall converter efficiency. It can be proved that the switching frequency f_s can be expressed in terms of circuit components and conditions as

$$f_s = \frac{S_{T\rm on}\cdot D + k_{\rm gen}\cdot(S_e + 0.5\cdot S_f)\cdot(1-D)}{k_{\rm gen}\cdot R_i\cdot I_o + V_{\rm th}} \quad \text{(for DOTCM)} \tag{1}$$

where S_e is the slope of the external ramp, S_f is the falling slope of the $V_{\rm CS}$ waveform, and $S_{T\rm on}$ is the rising slope of the $V_{T\rm on}$ waveform. $s_{T\rm on}$ is equal to ($I_{T\rm on}$ / $C_{T\rm on}$). Equation (1) is obtained under the assumption that the converter is operated in CCM, with V_c ripple much smaller than its dc value, and all the slope parameters mentioned are regarded as constant values.

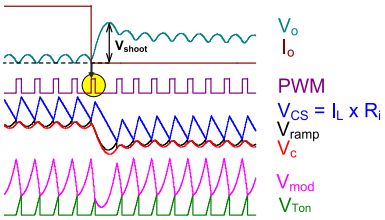

Fig. 3. AQCOTCM waveform during load transient ($V_{\rm shoot} = 337.55$ mV), where $k_{\rm gen} = 12.5$. The encircled on-time is shortened from 2.76 to 2.19 μs when the step-down load occurs, but recovers to 2.76 μs in steady state.

B. Description of the Proposed AQCOTCM Scheme

While the transient response of a DOTCM converter improves dramatically as shown in Fig. 2, the steady-state switching frequency is also altered significantly. From (1), one can see that the steady-state switching frequency f_s is inversely related to the load current I_o when operated even under a continuous conduction mode. This is a significant drawback of the DOTCM scheme because it is difficult to optimize the converter design, in terms of converter size and conversion efficiency, if the switching frequency varies over a large range. In the DOTCM scheme, the $V_{\rm mod}$ signal is used to modulate the on-time. When the load current level is decreased, V_c is reduced that makes $V_{\rm mod}$ smaller also. And, therefore, the on-time $T_{\rm on}$ is decreased from 2.76 to 2.26 μs, as shown in Fig. 2(a). This is the mechanism for a fast load transient response. Under the steady-state condition, same mechanism applies. Therefore, Ton value varies with load current level. Since the duty cycle remains essentially the same under a continuous conduction mode, the switching frequency also varies with load current level under steady-state condition. It is desirable to remove this drawback while preserving the fast transient feature of the DOTCM scheme. This can be accomplished by the proposed $V_{\rm mod}$ signal set by (2) in which $V_{\rm CS}$ is subtracted from V_c. Since V_c tracks the $V_{\rm CS}$ level in steady state by the current loop, the steady-state load current effect on V_c and $V_{\rm CS}$ cancel out each other, and therefore, removes the load-dependent effect of the switching frequency. During the step-load transient, V_c reacts quickly, while $V_{\rm CS}$ cannot change quickly due to the existence of the inductor. So, the $V_{\rm mod}$ signal reacts quickly and causes a quick $T_{\rm on}$ change to speed up the transient response. To implement (2), a proposed circuit diagram is given in Fig. 1, with all the dashed and solid colored lines connected. This is the proposed AQCOTCM scheme. The word "adaptive" is used to describe the fact that the ON time Ton during the transience is adaptive to load change, and the word "quasi" is used to describe the fact that it is still essentially a constant on-time operation during the steady-state condition independent of load level

$$v_{\rm mod}(t) = k_{\rm gen}\left[v_c(t) - v_{\rm CS}(t)\right] + V_{\rm th}. \tag{2}$$

Fig. 3 shows the simulated waveforms for the case of a buck converter using the AQCOTCM scheme. The same parameters listed in Table I were used in the simulations. As can be seen from the waveforms, the steady-state on-times are indistinguishable for different load current level. And the first on-time pulse right after the load change is adaptively shortened from 2.76 to 2.19 μs.

Fig. 4 compares the overshoot and the undershoot for different $k_{\rm gen}$ values, where the component values and working conditions are listed in Table II. The transient behavior of the COTCM scheme is given for comparison purpose. In fact, one can consider COTCM scheme is a special case of AQCOTCM in which $k_{\rm gen}$ is zero.

1) Derivation of the Steady-State Switching Frequency of a Buck Converter Employing the AQCOTCM Scheme: Fig. 5 shows the theoretical waveforms and the mechanism that determine the "ON" time and the "OFF" time of the $T_{\rm on}$ generating circuit. Fig. 5(a) shows the on-time modulation waveforms and Fig. 5(b) shows the off-time modulation waveforms. In Fig. 5(a), point *X* is the point that $V_{\rm Ton}$ touches $V_{\rm mod}$, thus (3) can be obtained. In Fig. 5(b), point *Y* is the point that $V_{\rm CS}$ touches $(V_{\rm ramp} + V_c)$, thus the relation of (4) can be obtained, assuming that V_c ripple magnitude is negligible compared to its average value. By substituting the V_c of (4) into (3), one can obtain (5). From (5), one can see that f_s is independent of I_o, unlike the case for the DOTCM scheme

$$\begin{cases} X: S_{T\rm on}T_{\rm on} = v_{\rm mod}\,(t = T_{\rm on}) \\ \qquad\qquad = k_{\rm gen}\cdot\left[V_c - v_{\rm CS}(t = T_{\rm on})\right] + V_{\rm th} & (3) \\ Y: V_c + S_eT_{\rm off} = v_{\rm CS}(t = T_{\rm on} + T_{\rm off}) \\ \qquad\qquad = v_{\rm CS}(t = T_{\rm on}) - S_nT_{\rm on} & (4) \end{cases}$$

$$f_s = \frac{S_{T\rm on} + k_{\rm gen}S_n\left(1 + \frac{S_e}{S_f}\right)}{V_{\rm th}}\cdot D \quad \text{(for AQCOTCM)}. \tag{5}$$

III. Experimental and Simulation Result

A. Experimental Platform

Fig. 6(a) shows the photo of an experimental chip die of the controller IC with both COTCM and AQCOTCM control functions embedded. Fig. 6(b) shows the experimental setup in which there is a CPU emulator, which can be controlled by the users to interface with the controller IC through I^2C communication link to interchange between the COTCM and the AQCOTCM controllers. It can also be used to change the converter output load current level for a step-load transient test. The circuit parameters/conditions are listed in Table II.

B. Single-Shot Transient Experiment Results

Fig. 7 shows the waveforms associated with single-shot step-load tests for both the AQCOTCM scheme and COTCM scheme. Both the step-up load (from 1 to 11 A) and the step-down load (from 11 to 1 A) were conducted. For a converter, the overshoot or undershoot depends, among other conditions, on the timing of the occurrence of the load step with respect to the on-time pulse. The results obtained in Fig. 7 are the worst scenario, i.e., the load step occurs exactly at the leading edge of the on-time pulse. From the figures, the output voltage overshoot $V_{\rm OS}$ and undershoot $V_{\rm US}$ are in favor of the AQCOTCM case. Notice that in this particular controller, AVP function is embedded. This can

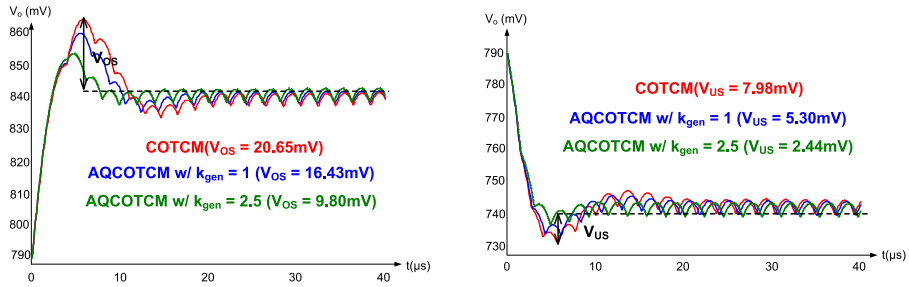

Fig. 4. (a) Overshoot comparison (I_o: 11 A→6 A): COTCM—20.65 mV; AQCOTCM (with $k_{gen} = 1$)—16.43 mV; AQCOTCM (with $k_{gen} = 2.5$)—9.80 mV, (b) undershoot comparison (I_o: 6 A→11 A): COTCM—7.98 mV; AQCOTCM (with $k_{gen} = 1$)—5.30 mV; AQCOTCM (with $k_{gen} = 2.5$)—2.44 mV.

TABLE II
CIRCUIT PARAMETERS/CONDITIONS FOR SIMULATED VERIFICATION

Input voltage V_{in}	19 V
Output voltage V_o	0.9 V
Inductor L_s	470 nH
Output capacitor C_o	220 μF
ESR of capacitor R_{co}	0 mΩ
On-time generator modulation gain k_{gen}	1
Current sensing gain R_i	75.936 mΩ
External ramp slope S_e	111 kV/s
DC threshold voltage V_{th}	1.2 V
On-time generation voltage rising slope S_{Ton}	6.5 MV/s
Switching frequency at 11 A $f_{s,H}$	413 kHz

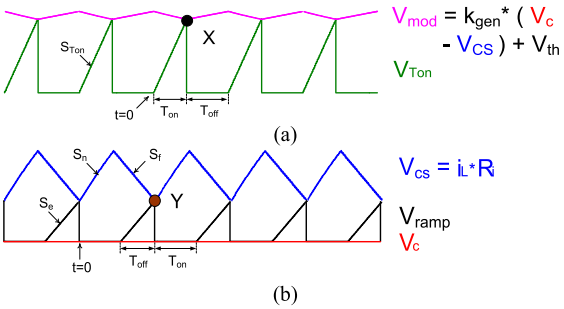

Fig. 5. CCM Waveforms determining (a) on-time and (b) off-time.

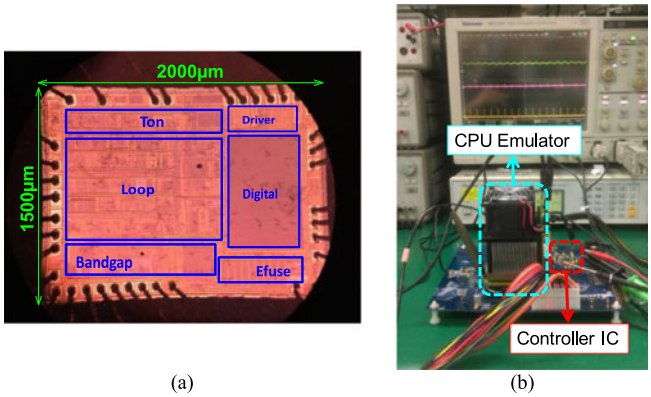

Fig. 6. (a) Die photo of controller IC, (b) experimental platform of the test circuit.

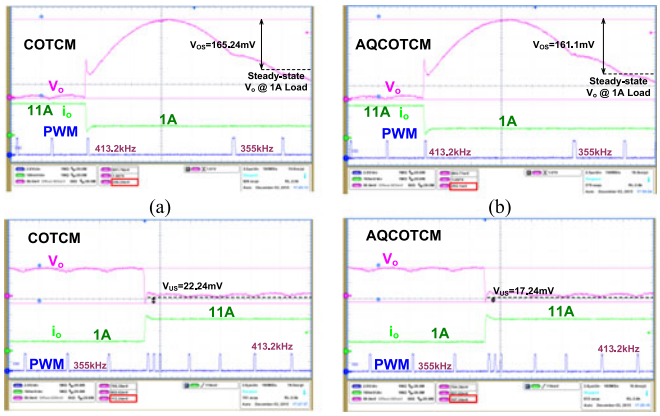

Fig. 7. Single step-load transient tests (a) overshoot (COTCM), (b) overshoot (AQCOTCM), (c) undershoot (COTCM), and (d) undershoot (AQCOTCM).

be seen from the figure that the steady-state V_o level is increased slightly as the load level is decreased. For this reason, the steady-state switching frequency varies slightly, in accordance with (5) due to the change of duty cycle D.

It should be noted that the advantage of the AQCOTCM scheme increases with the steady-state ON time requirement. For the same frequency of operation, the larger the ON time, the larger the duty cycle. In this particular example, a 19–0.9 V conversion, the duty cycle is very low, approximately 5%. The improvement is already apparent. For the cases with higher duty cycle requirement, normally the improvement should be even more pronounced.

C. Dynamic Load Experiment

For CPU V-core applications, there is a stringing requirement imposed by INTEL Corporation on dynamic load test [21]. In the test, the load current excitation waveform is a periodical square wave of varying frequency from 1 kHz to 1 MHz, with the minimum load $I_{o,\min}$ and the maximum $I_{o,\mathrm{Max}}$ excitation specified. As pointed out earlier, the overshoot/undershoot depends on the timing of the step-load occurrence with respect to the on-pulse, and on the load current magnitude and frequency. The worst sum of V_{OS} and V_{US} under this condition must stay within a specified limit. The test results listed in Table III was obtained

TABLE III
DYNAMIC LOAD RESULT COMPARISON OF COTCM AND AQCOTCM CIRCUIT

	COTCM (12 MLCC)	AQCOTCM (12 MLCC)	Improvement in AQCOTCM	Total Improvement in AQCOTCM	AQCOTCM (11 MLCC)
Worst Overshoot $V_{OS,max}$	170.95 mV	163.42 mV	7.53 mV	10.39 mV	168.75 mV
Worst Undershoot $V_{US,max}$	59.05 mV	56.19 mV	2.86 mV		58.09 mV

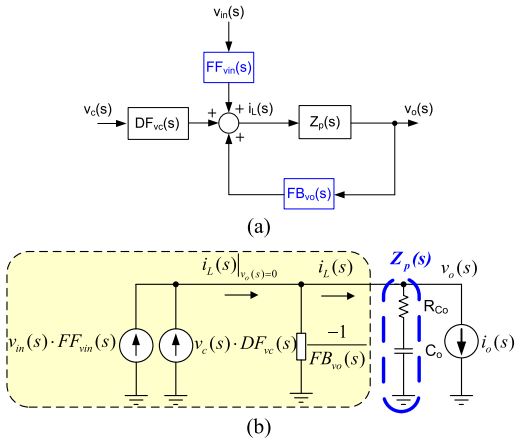

Fig. 8. (a) Complete open-loop model, (b) open-loop equivalent circuit; both are for current-mode control.

under the condition of $I_{o,\min} = 1$ A and $I_{o,\mathrm{Max}} = 11$ A. The worst overshoot/undershoot results were recorded in a storage scope while the exciting frequency varies from 1 kHz to 1 MHz as mandated. In the table, it is indicated in the first two columns that there were 12 Multi-Layer Ceramic Capacitors (MLCC) used. Each MLCC is a 22-μF capacitor. One can see the improvement by using the AQCOTCM scheme, compared to the conventional COTCM. The total improvement of $(V_{\mathrm{OS}} + V_{\mathrm{US}})$ is 10.39 mV. The result indicated in the last column of the table were obtained by removing one output MLCC capacitor.

As it can be seen, by using the AQCOTCM, the total number of the output capacitors can be reduced from 12 to 11, and still perform better than the COTCM in the dynamic load tests. As mentioned in Section III-B, the improvement can be even more pronounced for the cases of lower voltage conversion ratio.

IV. SMALL-SIGNAL MODEL FOR AQCOTCM CONTROLLED BUCK SCHEME

For the design of a buck converter using the proposed AQCOTCM scheme, it is desirable to develop a control model. Fig. 8 shows the general control block diagram of a converter using current-mode control [21]. For a buck converter using the AQCOTCM scheme, the block diagram is applicable except that the transfer function $\mathrm{DF_{vc}}(s)$, $\mathrm{FB_{vo}}(s)$, and $\mathrm{FF}_{vin}(s)$ must be derived according to AQCOTCM scheme. Using the derived $\mathrm{DF_{vc}}(s)$, $\mathrm{FB_{vo}}(s)$, $\mathrm{FF}_{vin}(s)$, and the block diagram, the ultimate goal is to obtain the control (v_c)-to-output voltage (v_o) transfer

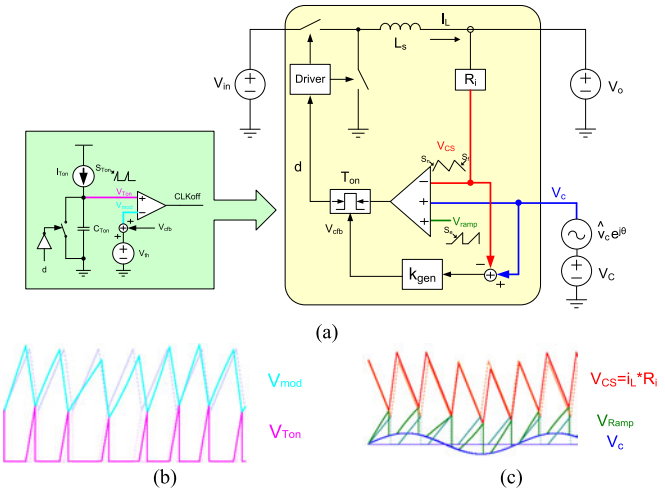

Fig. 9. (a) Adding a perturbing small-signal $\hat{v}_c$ to $\mathrm{V_c}$ for deriving the $\mathrm{DF_{vc}}(s)$. (b) Perturbed waveforms(dotted waveforms) for on-time calculation. (c) Perturbed waveforms(dotted waveforms) for off-time calculation.

function $G_{\mathrm{vc}}(s)$, which serves as the basis for the voltage loop compensator design to ensure stability. In this section, derivations of $\mathrm{DF_{vc}}(s)$, $\mathrm{FB_{vo}}(s)$, $\mathrm{FF}_{vin}(s)$,and $G_{\mathrm{vc}}(s)$ will be given. The complete open-loop model in Fig. 8(a) can be modified as an equivalent circuit model, as shown in Fig. 8(b).

A. Derivation of $DF_{\mathrm{vc}}(\mathrm{s})$ ($\equiv i_L / v_c$, Control-to-Inductor Current Transfer Function)

Transfer functions $\mathrm{DF_{vc}}(s)$ will be derived using the describing function approach [22]–[27]. A standard procedure is given below to obtain the $\mathrm{DF_{vc}}(s)$.

Step 1: Calculating the Perturbed ON-Time and OFF-Time

To derive $DF_{\mathrm{vc}}(s)$, it is required to perturb a signal $\hat{v}_c$ of frequency f_{m} to the control voltage V_c, as depicted by Fig. 9(a). It is much more difficult to derive the $DF_{\mathrm{vc}}(s)$ for the AQCOTCM scheme than that of the COTCM scheme, because the perturbed signal in this case affects both the on-time and the off-time, as shown in Fig. 9(b) and (c). The perturbed on-time difference $\Delta T_{\mathrm{on},i}$ and off-time difference $\Delta T_{\mathrm{off},i}$ in the i_{th} period, are expressed by (6) and (7)

$$\Delta T_{\mathrm{on},i} \approx \frac{k_{\mathrm{gen}}}{S_{T\mathrm{on}} + k_{\mathrm{gen}} S_n} \left\{ 2\,\hat{v}_c \cos\left(2\pi f_m \left[(i-1)T_{\mathrm{sw}} + \frac{T_{\mathrm{on}}}{2} \right] - \theta \right) \sin\left(2\pi f_m \frac{T_{\mathrm{on}}}{2} \right) \right\} - \frac{k_{\mathrm{gen}} S_e}{S_{T\mathrm{on}} + k_{\mathrm{gen}} S_n} \Delta T_{\mathrm{off},i-1} \tag{6}$$

$$\Delta T_{\mathrm{off},i} \approx \frac{S_n}{(S_f + S_e)} \Delta T_{\mathrm{on},i} + \frac{S_e}{S_f + S_e} \Delta T_{\mathrm{off},i-1} - \frac{2}{(S_f + S_e)}\,\hat{v}_c \cos\left[2\pi f_m \left((i-1)T_{\mathrm{sw}} + \frac{T_{\mathrm{sw}}}{2} \right) - \theta \right] \sin\left(2\pi f_m \frac{T_{\mathrm{sw}}}{2} \right). \tag{7}$$

Step 2: Performing Fourier Analysis of the Duty Function

Since both the perturbed on-time and off-time are found in Step 1, the perturbed duty cycle function can also be found. The perturbed duty cycle function can be found with the relationship of the perturbed on-time and off-time given in (6) and (7). The perturbed control signal $v_c(t) = V_c + \hat{v}_c \sin(2\pi f_m t - \theta)$ is hidden in the perturbed duty cycle function $d(t)$. The Fourier coefficient $c_{m(d)}$ of duty cycle function can be expressed as

$$c_{m(d)} \approx \frac{j2\pi f_m}{N\pi} \sum_{i=1}^{M} e^{-j2\pi f_m [(i-1)T_{\rm sw} + T_{\rm on}]} \times \left[\left(\sum_{k=1}^{i} \Delta T_{{\rm on},k} + \sum_{k=1}^{i-1} \Delta T_{{\rm off},k} \right) (1 - e^{-j2\pi f_m T_{\rm off}}) - e^{-j2\pi f_m T_{\rm off}} \Delta T_{{\rm off},i} \right] \quad (8)$$

where N and M shows the commensurability of f_m and f_s, which can be defined as the smallest positive integer-pairs to make $N/M = f_m/f_s$.

Step 3: Obtaining $\mathrm{DF}_{\rm vc}(s)$

The inductor current $i_L(t)$ can be expressed as

$$i_L(t) = \int_0^t \left[\frac{V_{\rm in}}{L_s} d(t) - \frac{V_{\rm out}}{L_s} \right] dt + i_{L0}. \quad (9)$$

Fourier coefficient of the inductor current then can be found by applying Fourier series into (9) as

$$c_m = \frac{1}{j2\pi f_m} \frac{V_{\rm in}}{L_s} c_{m(d)}. \quad (10)$$

Substituting (6) and (7) into (9) and (10), $\mathrm{DF}_{\rm vc}(s)$ can be expressed as (11)

$$D\mathrm{f}_{\rm vc}(s) \equiv \left. \frac{i_L(s)}{v_c(s)} \right|_{\substack{i_o(s)=0 \\ v_{\rm in}(s)=0 \\ v_o(s)=0}} = \frac{c_m}{\hat{v}_c\, e^{-j\theta}} = \frac{V_{\rm in} f_s}{L_s s} \frac{N_F(s)}{1 - e^{-sT_{\rm sw}}} \quad (11)$$

where

$$N_F(s) \equiv \left[\frac{k_{\rm gen} S_e}{S_{\rm TN}} \left(1 - e^{-sT_{\rm off}}\right) e^{-sT_{\rm on}} + \left(1 - e^{-sT_{\rm on}}\right) \right] \cdot M_F(s) + \frac{k_{\rm gen}}{S_{\rm TN}} \cdot \left(1 - e^{-sT_{\rm off}}\right) \left(1 - e^{-sT_{\rm on}}\right)$$

$$M_F(s) \equiv \frac{(1 - e^{-sT_{\rm sw}}) - \frac{k_{\rm gen} S_n}{S_{\rm TN}} (1 - e^{-sT_{\rm on}}) e^{-sT_{\rm off}}}{S_{\rm FE}(s)}$$

$$S_{\rm FE}(s) \equiv (S_f + S_e) - S_e \frac{S_{T\rm on}}{S_{\rm TN}} e^{-sT_{\rm sw}}$$

$$S_{\rm TN} \equiv S_{T\rm on} + k_{\rm gen} S_n.$$

Step 4: Simplifying the Model using Padé Approximation

Equation (11) can be simplified by using Padé approximation, and the result is given as follows:

$$\mathrm{DF}_{\rm vc}(s) = \left. \frac{i_L(s)}{v_c(s)} \right|_{\substack{i_o(s)=0 \\ v_{\rm in}(s)=0 \\ v_o(s)=0}} \approx \frac{V_{\rm in} f_s}{L_s s} \frac{k_{\rm gen}}{S_{\rm TN}} \left\{ \left[S_e \left(\frac{sT_{\rm sw}}{1 + \frac{s}{Q_1 \omega_{\rm sw1}} + \frac{s^2}{{\omega_{\rm sw1}}^2}} - \frac{sT_{\rm on}}{1 + \frac{s}{Q_1 \omega_{\rm on1}} + \frac{s^2}{{\omega_{\rm on1}}^2}} \right) + \frac{S_{\rm TN}}{k_{\rm gen}} \frac{sT_{\rm on}}{1 + \frac{s}{Q_1 \omega_{\rm on1}} + \frac{s^2}{{\omega_{\rm on1}}^2}} \right] M_{F,\rm Pade}(s) + \frac{sT_{\rm off}}{1 + \frac{s}{Q_1 \omega_{\rm off1}} + \frac{s^2}{{\omega_{\rm off1}}^2}} + \frac{sT_{\rm on}}{1 + \frac{s}{Q_1 \omega_{\rm on1}} + \frac{s^2}{{\omega_{\rm on1}}^2}} - \frac{sT_{\rm sw}}{1 + \frac{s}{Q_1 \omega_{\rm sw1}} + \frac{s^2}{{\omega_{\rm sw1}}^2}} \right\} \Bigg/ \left(\frac{sT_{\rm sw}}{1 + \frac{s}{Q_1 \omega_{\rm sw1}} + \frac{s^2}{{\omega_{\rm sw1}}^2}} \right) \quad (12)$$

where

$$Q_1 = \frac{2}{\pi}, \omega_{\rm sw1} = \frac{\pi}{T_{\rm sw}}, \omega_{\rm on1} = \frac{\pi}{T_{\rm on}}, \omega_{\rm off1} = \frac{\pi}{T_{\rm off}}$$

$$M_{F,\rm Pade}(s) \equiv \frac{\frac{S_{T\rm on}}{S_{\rm TN}} \frac{sT_{\rm sw}}{1 + \frac{s}{Q_1 \omega_{\rm sw1}} + \frac{s^2}{{\omega_{\rm sw1}}^2}} + \frac{k_{\rm gen} S_n}{S_{\rm TN}} \frac{sT_{\rm off}}{1 + \frac{s}{Q_1 \omega_{\rm off1}} + \frac{s^2}{{\omega_{\rm off1}}^2}}}{S_f + S_e \frac{k_{\rm gen} S_n}{S_{\rm TN}} + S_e \frac{S_{T\rm on}}{S_{\rm TN}} \frac{sT_{\rm sw}}{1 + \frac{s}{Q_1 \omega_{\rm sw1}} + \frac{s^2}{{\omega_{\rm sw1}}^2}}}.$$

B. *Derivation of* $\mathrm{FF}_{v\rm in}(s)$ *and* $\mathrm{FB}_{\rm vo}(s)$

Not only does control voltage affect inductor current, but also input and output voltage. Feed-forward gain $\mathrm{FF}_{v\rm in}(s)$ is the input voltage-to-inductor current transfer function, while the feedback gain $\mathrm{FB}_{\rm vo}(s)$ is the output voltage-to-inductor current transfer function. Both $\mathrm{FF}_{v\rm in}(s)$ and $\mathrm{FB}_{\rm vo}(s)$ can be derived following the basic approach as described in the derivation of $\mathrm{DF}_{\rm vc}(s)$. The results are shown in (13)–(16)

$$\mathrm{FF}_{v\rm in}(s) \equiv \left. \frac{i_L(s)}{v_{\rm in}(s)} \right|_{\substack{i_o(s)=0 \\ v_o(s)=0 \\ v_c(s)=0}} = \frac{1}{L_s s} \left[D + V_{\rm in} \frac{f_s}{S_F(s)} \frac{1 - e^{-sT_{\rm on}}}{s\frac{L_s}{R_i}} \frac{S_{T\rm on}}{S_{\rm TN}} \left\{ [S_{T\rm on} - k_{\rm gen}(S_f + S_e)] \frac{1 - e^{-sT_{\rm off}}}{1 - e^{-sT_{\rm sw}}} - S_{T\rm on} \right\} \right] \quad (13)$$

$$\approx \frac{T_{\rm on}}{2L_s} \left[\frac{\left(1 + \frac{2S_e}{S_f}\right) S_{T\rm on}}{S_{T\rm on} + k_{\rm gen} S_n + k_{\rm gen} S_e \frac{1-D}{D}} \right] \quad (14)$$

$$\mathrm{FB}_{\rm vo}(s) \equiv \left. \frac{i_L(s)}{v_o(s)} \right|_{\substack{i_o(s)=0 \\ v_{\rm in}(s)=0 \\ v_c(s)=0}} = \frac{1}{L_s s} \times \left[V_{\rm in} \frac{f_s}{sL_s/R_i} \frac{N_F(s)}{1 - e^{-sT_{\rm sw}}} - 1 \right] \quad (15)$$

$$\approx -\frac{T_{\rm on}}{2L_s}\left[\frac{\left(1+\frac{2S_e}{S_f}\frac{1}{D}\right)S_{T\rm on}+k_{\rm gen}S_e\left(\frac{1-D}{D}\right)^2}{S_{T\rm on}+k_{\rm gen}S_n+k_{\rm gen}S_e\frac{1-D}{D}}\right]. \quad (16)$$

C. Derivation of $G_{\rm vc}(s)$

From Fig. 8(b), the control-to-output transfer function $G_{\rm vc}(s)$ can be expressed by

$$G_{\rm vc}(s)=\left.\frac{v_o(s)}{v_c(s)}\right|_{\substack{i_o(s)=0\\ v_{\rm in}(s)=0}}=Df_{\rm vc}(s)\cdot Z_o(s) \quad (17)$$

where

$$Z_o(s)\equiv\left.\frac{v_o(s)}{i_o(s)}\right|_{\substack{v_{\rm in}(s)=0\\ v_c(s)=0}}=Z_F(s)||Z_p(s)$$

$$=\frac{Z_p(s)}{1-Z_p(s)\cdot fB_{\rm vo}(s)}$$

$$Z_F(s)=\frac{-1}{fB_{\rm vo}(s)}$$

and $Z_p(s)$ is the load impedance parallel to the converter, which is serial impedance of the C_o and $R_{\rm co}$. Using (12) and (16), $G_{\rm vc}(s)$ can be obtained. Through this equivalent circuit, a multiplication relationship between $G_{\rm vc}(s)$, $DF_{\rm vc}(s)$, and $Z_o(s)$ can be obtained. This is exactly a picture for all current-mode-controlled circuit, showing that the a current-mode-controlled circuit transforms the inductor into a current source in parallel with a feedback impedance $Z_F(s)$, making current-mode control behave differently from the conventional voltage-mode control.

$G_{\rm vc}(s)$ is a key transfer function based on which the voltage-loop compensator design can be determined. However, it is a complicated transfer function from which important information such as poles and zeros cannot be easily determined for compensation design. A simplified $G_{\rm vc}(s)$ model will be developed in the following sections.

D. Derivation of Simplified $G_{\rm vc}(s)$ Model

Several assumptions are made in the derivation: 1) the duty is less than 0.2; 2) the load is "current load," rather than "resistive load;" and 3) The ESR of the power-stage capacitors is much smaller than $(1/|FB_{\rm vo}|)$. The assumptions are valid for most dc converters for CPU applications.

The result is shown in the following equation, where $G_{\rm vc,sim}(s)$ is the simplified $G_{\rm vc}(s)$ function:

$$G_{\rm vc,sim}(s)\equiv\left.\frac{v_o(s)}{v_c(s)}\right|_{\substack{i_o(s)=0\\ v_{\rm in}(s)=0}}$$

$$\approx K_{\rm AQ}\cdot\frac{1}{1+\frac{s}{\omega_{p,\rm AQ}}}\cdot\frac{1+\frac{s}{Q_{z,\rm AQ}\omega_{z,\rm AQ}}+\frac{s^2}{{\omega_{z,\rm AQ}}^2}}{1+\frac{s}{Q_{e,\rm AQ}\omega_{\rm sw1}}+\frac{s^2}{{\omega_{\rm sw1}}^2}}$$

$$\cdot\frac{1+\frac{s}{\omega_{z,ESR}}}{1+\frac{s}{Q_1\omega_{\rm on1}}+\frac{s^2}{{\omega_{\rm on1}}^2}} \quad (18)$$

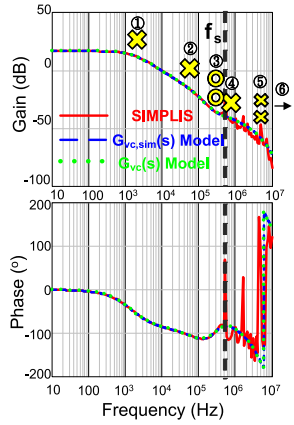

Fig. 10. Bode plots of "AQCOTCM" controlled buck control-to-output using simplified $G_{\rm vc}(s)$ model and its pole-zero-location with comparison to the one using the Padé approximated model.

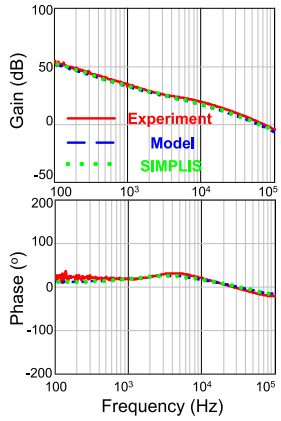

Fig. 11. Plots of loop gain function for verification.

where

$$K_{\rm AQ}=\frac{1}{R_i\cdot|FB_{\rm vo}|},|FB_{\rm vo}|$$

$$=\frac{T_{\rm on}}{2L_s}\left[\frac{\left(1+\frac{2S_e}{S_f}\frac{1}{D}\right)S_{T\rm on}+k_{\rm gen}S_e\left(\frac{1-D}{D}\right)^2}{S_{T\rm on}+k_{\rm gen}S_n+k_{\rm gen}S_e\frac{1-D}{D}}\right],$$

$$\omega_{p,\rm AQ}=\frac{|FB_{\rm vo}|}{C_o},\omega_{z,ESR}=\frac{1}{R_{\rm co}C_o},\omega_{z,\rm AQ}$$

$$=\sqrt{\frac{S_{\rm TN}+\frac{1}{2}k_{\rm gen}S_f+k_{\rm gen}S_e\frac{1-D}{D}}{S_{\rm TN}+k_{\rm gen}S_f+k_{\rm gen}S_e\cdot\left(\frac{k_{\rm gen}S_n}{S_{\rm TN}}+D\right)}}\omega_{\rm sw1},$$

$$Q_{e,\rm AQ}=\frac{Q_1}{1+\frac{2S_e\frac{S_{T\rm on}}{S_{\rm TN}}}{S_f+S_e\frac{k_{\rm gen}S_n}{S_{\rm TN}}}},Q_{z,\rm AQ}$$

$$=\frac{S_{\rm TN}+\frac{1}{2}k_{\rm gen}S_f+k_{\rm gen}S_e\frac{1-D}{D}}{S_{\rm TN}+k_{\rm gen}S_f+k_{\rm gen}S_e}\cdot\frac{\omega_{\rm sw1}}{\omega_{z,\rm AQ}}\cdot Q_1$$

$$S_{\rm TN}=S_{T\rm on}+k_{\rm gen}S_n,Q_1=\frac{2}{\pi},\omega_{\rm sw1}=\frac{\pi}{T_{\rm sw}},\omega_{\rm on1}=\frac{\pi}{T_{\rm on}}.$$

In (18), all the poles and zeros are easily identifiable. Fig. 10 gives plots of the theoretical $G_{\rm vc}(s)$, $G_{\rm vc,sim}(s)$ and simulated

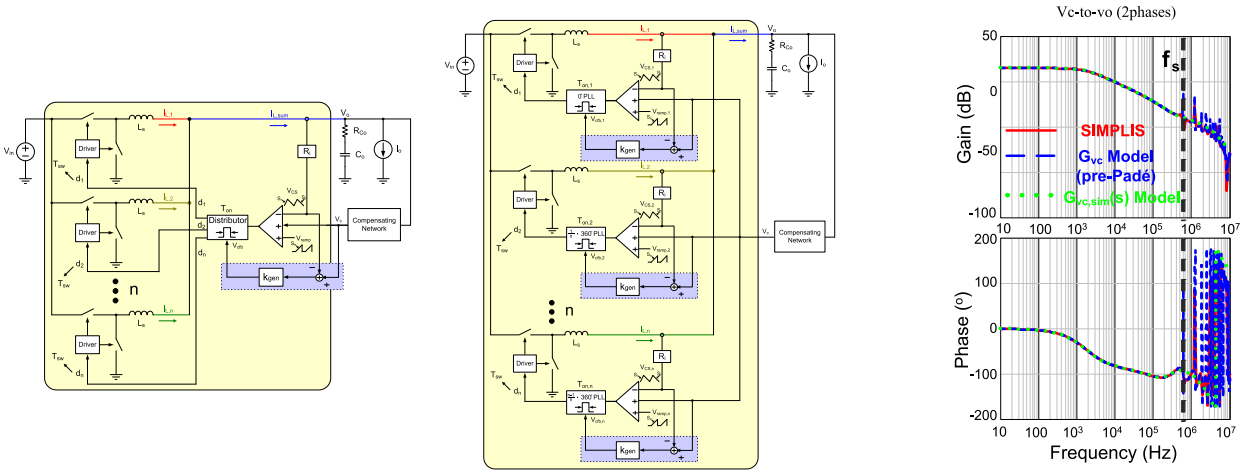

Fig. 12. Circuit diagrams of n-phase AQCOTCM controlled buck based on (a) pulse distribution structure; (b) PLL structure; (c) bode plots of two-phase "AQCOTCM" controlled buck control-to-output $G_{\rm vc}(s)$ based on pulse distribution structure.

result based on parameters listed in Table II. They all agree well with one another up to half switching frequency. From the plot, there are poles and zeros. Starting from the first pole ① from the left, it is the low-frequency pole of $\omega_{p,\rm AQ}$, which would be affected by C_o and $|FB_{\rm vo}|$. Then, the next two poles are ② and ④, which are a pair of poles splitting from half switching frequency $\omega_{\rm sw,1}$, and their splitting extent is affected by their Q factor $Q_{e,\rm AQ}$, which has a lot to do with external ramp slope $S_{\rm e}$. The larger s_e results in smaller $Q_{e,\rm AQ}$, thus further splitting apart. There are still a pair of complex zeros ③ on the location of $\omega_{z,\rm AQ}$ which is around $\omega_{\rm sw,1}$ with Q factor $Q_{z,\rm AQ}$. Finally, a pair of complex poles ⑤ on half on-time frequency $\omega_{\rm on,1}$. There is an ESR zero $\omega_{z,\rm ESR}$ ⑥, that is too high frequency to be marked on this plot. Its dc gain, which can be identified in the low-frequency part of the plot, is $K_{\rm AQ}$, which is the inverse of its $|FB_{\rm vo}|$ and R_i product.

E. Voltage Loop Gain Bode Plot Measurement With AQCOTCM Control

Measurement of $G_{\rm vc}(s)$ cannot be done because the terminal for injecting $\hat{v}_c$ signal is inside the IC and is not accessible. However, the loop gain function, that contains $G_{\rm vc}(s)$ and compensating network, was measured. The circuit parameters/conditions are listed in Table II. The loop gain measurement result, along with the simulation result and the model prediction, is shown in Fig. 11. They all agree well. This proves that the model developed can be used for designing the compensating network.

V. Extension to Multiphase Circuits

In a CPU application, large output current and low output voltage are usually required. Therefore, multiphase interleaving is usually required to achieve such purpose. The concept described in this paper can be extended to the case of multiphase circuit. Fig. 12(a) and (b) shows the diagrams in which the dotted boxes are added to make them function as AQCOTCM.

In Fig. 12(a), which is called the pulse distribution structure, there is only one current sensor, and the "distributor" box is to distribute its output signal to one of these phases [20]. In Fig. 12(b), which is called the phase-locked loop (PLL) structure, each phase current is sensed and fed back to both the comparator and the PLL-embedded on-time generator [28]. The former is simpler and less costly but the performances of the transient response are not as good as the latter. Also, there is an instability issue, but it can be alleviated by using an external ramp [28].

The pulse distribution structure is more popular among commercial products because of its simplicity. The model for the n-phase circuit model can be obtained simply by replacing the L_s, the $T_{\rm sw}$ and the $V_{\rm in}$ in (18), respectively, by (L_s/n), $(T_{\rm sw}/n)$, $(V_{\rm in}/n)$. Fig. 12(c) gives a plots of the $G_{\rm vc}(s)$ result of a two phase (i.e., $n=2$) AQCOTCM controlled buck. It agrees well with simulation result.

VI. Conclusion

A novel AQCOTCM control scheme is proposed and implemented for the buck converters. This scheme was verified by simulations and hardware experiments. A small-signal control model is also developed using a describing function approach. The model can be used for the design of the control circuit. Extension of this concept to multiphase structure is also presented.

The proposed scheme combines the advantages of a current-mode control, a COT operation, and fast step-load transient response, and is particularly suitable for next generation smart-power CPU load.

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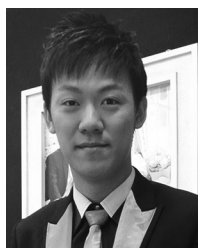

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