Improving the Light-Load Regulation Capability of *LLC* Series Resonant Converter Using Impedance Analysis

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***Abstract*—Generally, an *LLC* series resonant converter (*LLC* SRC) is an attractive topology for applications, which require wide input variation and high conversion efficiency because of its wide gain capability and soft-switching capability. However, there is a regulation problem in which the output voltage increases as the load current decreases. In this paper, Bode plot and impedance asymptote analysis were conducted to obtain an intuitive sense of the regulation characteristic of *LLC* SRC under the light-load condition. Moreover, to improve the regulation capability, a new resonant tank with an additional capacitor is proposed. Its design guidelines were determined by Bode plot and impedance asymptote analysis. Therefore, the proposed *LLC* SRC achieves very light load regulation, while it maintains the advantages of typical *LLC* SRCs.**

***Index Terms*—Bode plot, impedance asymptotes, light-load regulation, *LLC* series resonant converter (*LLC* SRC), no-load regulation, zero-voltage switching (ZVS).**

NOMENCLATURE

V_O	Output voltage.
f_s	Switching frequency of converter.
C_r	Resonant capacitor.
L_r	Resonant inductor.
$L_{\rm lkg}$	Leakage inductance.
L_M	Magnetizing inductor of transformer.
f_o	Resonant frequency of *LLC* SRC.
$V_{\rm RO}$	Reflected V_O to the primary side.
$V_{\rm RO}^F$	Fundamental component of $V_{\rm RO}$.
$V_{\rm IN}$	Input voltage.
$V_{\rm IN}^F$	Fundamental component of $V_{\rm IN}$.
R_O	Output resistor.
$R_{\rm ac}$	Equivalent ac resistance of R_O.
I_O	Load current of output.
$I_{\rm OF}$	Full-load current of output.
k	L_M/L_r.
Q	$1/R_{\rm ac}\sqrt{C_r/L_r}$.
ω_p	$1/\sqrt{L_M C_r}$.
ω_o	$1/\sqrt{L_r C_r}$.
n	Turns ratio of transformer ($N_p : N_s$).
$C_{j,\rm eq}$	Equivalent junction capacitance.
$v_{\rm pri}$	Across voltage of transformer.
i_F	Current flows toward the output stage.
$V_{\rm Cr}$	Initial across voltage of C_r.
$i_{\rm Cj}$	Current of $C_{j,\rm eq}$.
ω_j	$1/\sqrt{2\rm L_r C_{j,eq}}$.
t_1	Quarter of resonant period of ω_j.
$f_{\rm add}$	$1/2\pi\sqrt{L_r C_r}$.
$C_{\rm add}$	Additional capacitor in the proposed *LLC* SRC.
i_p	Primary current.
$i_{C\rm add}$	Current of $C_{\rm add}$.
$i_{\rm Lr}$	Current of L_r.
$C_{\rm oss}$	Output capacitance of switch.
$v_{\rm Cr}$	Across voltage of C_r.
$R_{\rm add}$	Additional register in the proposed *LLC* SRC.

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I. INTRODUCTION

NOWADAYS, a number of electronic devices, such as tablet PCs, smart phones, laptops, and various portable devices, were growing explosively, and their power consumption is continuously increasing. In addition, in order to use the above electronic devices, an appropriate power supply is needed to charge their batteries. Each power supply is continuously improved in terms of output specifications, such as higher power density and higher conversion efficiency [1]–[4]. In this context, resonant converters, which are suitable for high-frequency operation, are regarded as an attractive topology in the portable power supply market. Among resonant converters, an *LLC* series resonant converter (*LLC* SRC), as shown in Fig. 1, could be a great candidate for the portable power supply market. *LLC* SRC regulates the output voltage with pulse–frequency modulation (PFM), and its resonant tank is composed of a resonant capacitor, a resonant inductor, and a magnetizing inductor. Since high-frequency operation makes the magnetic components small, many circuit designers have preferred *LLC* SRC with a high switching frequency to achieve the high power density. Furthermore, because *LLC* SRC achieves zero-voltage

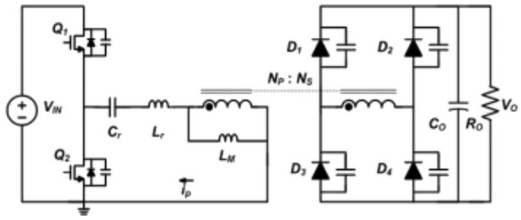


Fig. 1. Circuit diagram of conventional *LLC* SRC.

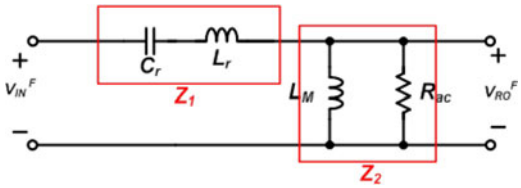


Fig. 2. AC equivalent circuit of ideal LLC SRC.

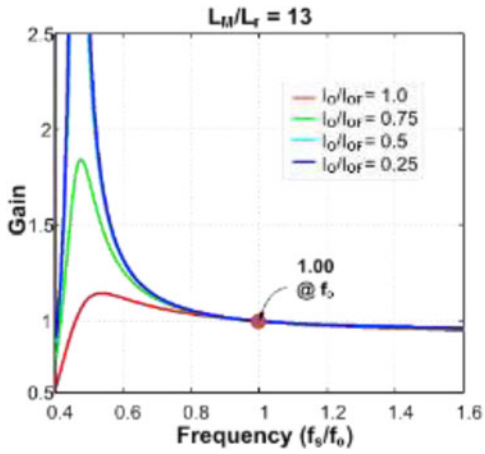


Fig. 3. Gain curve of ideal *LLC* SRC with FHA.

switching (ZVS) under the entire load conditions and has no output inductor, *LLC* SRC can reduce the switching loss and core loss dramatically. Due to these advantages, *LLC* SRCs have been adopted in many applications, such as audio, plasma display panel (PDP) power supply, server power supply, and laptop adapters [1], [5]–[8].

For an ideal *LLC* SRC, fundamental harmonic approximation (FHA) has been widely used to obtain the gain of *LLC* SRC due to its simplicity [9]–[11]. With FHA, since the only fundamental component can be delivered to the output side, the ac equivalent circuit of *LLC* SRC can be configured, as shown in Fig. 2. From the results of FHA, in the case of an ideal *LLC* SRC, the gain is unity at the resonant frequency and the gain decreases continuously as switching frequency increases [9], [10]. As a result, ideally, it is possible to regulate the output voltage under the light-load condition. However, in the case of actual *LLC* SRC, due to the junction capacitor of secondary rectifiers and the parasitic capacitance of the main transformer, the output voltage of *LLC* SRC increases continuously as the switching frequency increases under the very light load condition [11]–[14].

To solve the regulation problem, plasma display panel (PDP) or adapter applications normally use a dummy load to ensure reliable operation under the light-load or no-load condition [11]. Since the dummy load consumes a small constant power, *LLC* SRC can regulate the output voltage under the entire load conditions, preventing *LLC* SRC from operating under the very light load condition. However, the constant power loss becomes the main reason for low conversion efficiency.

Other researchers suggested changing the control method for light-load regulation. In the case of *LLC* SRC with a full-bridge inverter, very light load regulation was achieved by the phase-shift operation of primary switches [15]–[18]. Unfortunately, this phase-shift method cannot be applied to a half-bridge inverter. Moreover, it increases the system complexity due to the additional control elements. Besides, though the burst mode control methods have been also studied for *LLC* SRCs [19]–[23], a voltage and current peaking phenomenon exists and the dynamic response of burst mode control is too slow to return to the nominal state [13], [24]–[26]. Even though additional controls have also been studied to overcome this problem, they also require complicated controls and detecting circuits [26].

Finally, adding an additional output capacitor to the low-side switch was studied in [12]. In this case, since the additional output capacitor increases the commutation period of *LLC* SRC, it reduces the secondary current ripple and decreases the powering current that is delivered to the output. However, *LLC* SRC with additional output capacitor (*LLC*AC) has a narrower ZVS range than the conventional *LLC* SRCs. This result is in contrast with the advantages of *LLC* SRCs in the high-frequency region. Therefore, it is not suitable for various applications, and it also has a limited usage for light-load regulation.

In this paper, the intuitive analysis of the light-load regulation problem in *LLC* SRC is induced by Bode plot and impedance asymptote analysis. In addition, a solution for light-load regulation is proposed. The proposed *LLC* SRC achieves light-load and no-load regulation, while it maintains the advantages of conventional *LLC* SRCs, such as ZVS under the entire load conditions and simple control. The analysis and verification are presented with a 200-W laboratory prototype converter. Because of its simplicity, the proposed *LLC* SRC can be applied to various *LLC* SRC applications.

II. Analysis of Light-Load Regulation Problem

As mentioned before in Section I, *LLC* SRC analysis with FHA is the most common method to obtain the gain. From the FHA and ac equivalent circuit in Fig. 2, the gain of the ideal *LLC* SRC can be obtained as follows [9]:

$$\frac{V_{\mathrm{RO}}^{F}}{V_{\mathrm{IN}}^{F}} = \frac{\frac{\omega^2}{\omega_o^2} \times k}{\left(\frac{\omega^2}{\omega_p^2} - 1\right) + jkQ \times \frac{\omega}{\omega_o}\left(\frac{\omega^2}{\omega_o^2} - 1\right)}. \tag{1}$$

Finally, the gain curve of *LLC* SRC in (1) is shown in Fig. 3. As seen in Fig. 3, in the case of the ideal *LLC* SRC, the gain is unity at f_o, and the gain decreases continuously as f_s increases. However, the actual case is different. In this paper, the analysis of *LLC* SRC with a Bode plot and impedance asymptote is applied for the intuitive and simple solution. In Section II-B, the intuitive analysis for the problem of light-load regulation in *LLC* SRC will be presented. In addition, the operation mode analysis

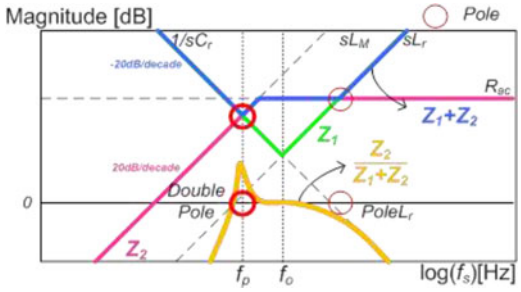


Fig. 4. Bode plot of ideal *LLC* SRC [27].

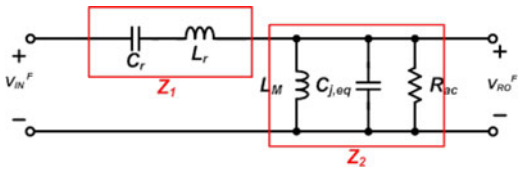


Fig. 5. AC equivalent circuit of *LLC* SRC with $C_{j,\mathrm{eq}}$.

for *LLC* SRC under light-load condition will be presented for accurate analysis in Section II-C.

A. Ideal LLC SRC

In this section, the ideal *LLC* SRC is analyzed with Bode plot and impedance asymptote. Using the ac equivalent circuit of the ideal *LLC* SRC in Fig. 2 and impedance ratio, the gain of *LLC* SRC is defined as $Z_2/(Z_1+Z_2)$ [27]–[31], and it can be displayed in a Bode plot as shown in Fig. 4. Green line indicates the impedance asymptote of Z_1, and pink line indicates the impedance asymptote of Z_2. From these asymptotes, the impedance asymptote of (Z_1+Z_2) is obtained as blue line. Finally, the gain of *LLC* SRC, i.e., $Z_2/(Z_1+Z_2)$ is displayed by yellow line. As seen in Fig. 4, a typical *LLC* SRC should be designed to have a double pole, which is located at the frequency where the impedance magnitudes of L_M and C_r are equal, and its condition is the following [27]:

$$R_{\mathrm{ac}} > \sqrt{L_M/C_r}, \qquad \sqrt{k}Q \le 1. \tag{2}$$

From the results of (2) and Fig. 4, if the magnitude at the double pole was smaller than R_{ac}, the gain of *LLC* SRC could become larger than 1 [27]. In addition, it has unity gain at f_o. Moreover, one more high-frequency pole exists at the frequency where the impedance magnitudes of R_{ac} and L_r are equal (PoleL_{r}). Because of the effect of PoleL_{r}, the gain of ideal *LLC* SRC decreases as f_s increases. Therefore, the ideal *LLC* SRC can regulate the output voltage with PFM control.

B. LLC SRC Including the Junction Capacitors of the Rectifier

The preceding papers suggest that the light-load regulation problem occurs mainly due to the junction capacitors of the secondary-side rectifier [11]–[14]. Fig. 5 shows that these junction capacitors can be represented as $C_{j,\mathrm{eq}}$, whose value is the reflected junction capacitance to the primary side considering n. Table I shows the value of $C_{j,\mathrm{eq}}$ according to the rectifier type [11].

TABLE I
$C_{j,\mathrm{eq}}$ FOR RECTIFIER TYPES

Rectifier type	Equivalent C_j, $C_{j,\mathrm{eq}}$
Center-tapped	$2C_j(N_s/N_p)^2$
Full-bridge	$2C_j(N_s/N_p)^2$
Voltage-doubler	$0.5C_j(N_s/N_p)^2$

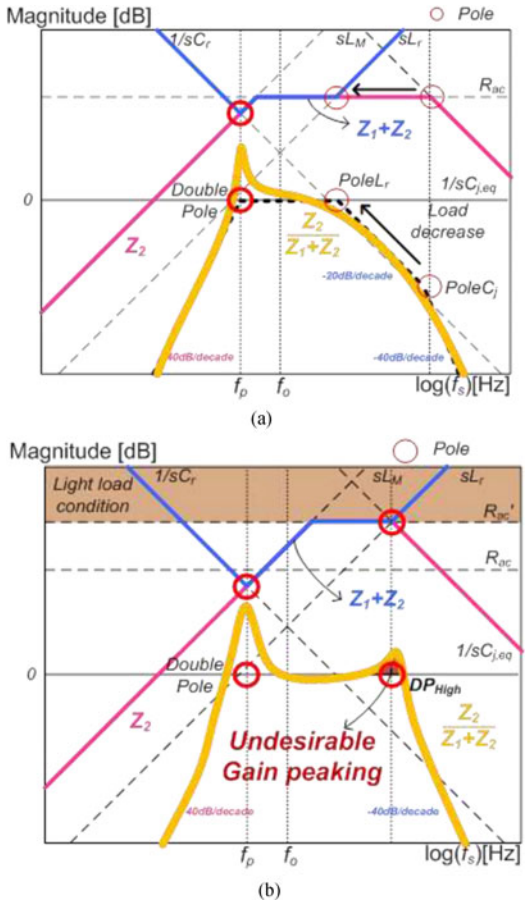


Fig. 6. Bode plot of *LLC* SRC with $C_{j,\mathrm{eq}}$ under (a) heavy load. (b) light load.

A new ac equivalent circuit of *LLC* SRC considering $C_{j,\mathrm{eq}}$ is shown in Fig. 5. In order to obtain the gain of Fig. 5, the asymptote of $C_{j,\mathrm{eq}}$ is added to the Bode plot of the ideal *LLC* SRC, as shown in Fig. 6. Using Fig. 6, the intuitive analysis for the light-load regulation problem can be induced. As seen in Fig. 6, the gain curve of *LLC* SRC considering $C_{j,\mathrm{eq}}$ is changed according to load condition. In the Bode plot, $C_{j,\mathrm{eq}}$ produces a high-frequency pole PoleC_j located at the frequency where the impedance magnitudes of $C_{j,\mathrm{eq}}$ and R_{ac} become equal. The high-frequency pole is located at the higher frequency than f_o and another pole PoleL_r. Under a heavy-load condition, as shown in Fig. 6(a), since PoleC_j is far away from PoleL_r, PoleC_j has a negligible effect to the gain curve, and V_O can be well regulated. However, in the case of light-load condition, as shown in Fig. 6(b), as the load condition decreases, PoleC_j and PoleL_r move closer to each other, because the value of R_{ac} becomes larger under a lighter load condition. When PoleC_j

moves closer to $\mathrm{Pole}L_r$ and meets $\mathrm{Pole}L_r$ under very light load condition, a new double pole DP_{High} is produced. As seen in the Bode plot in Fig. 6(b), the change of slope with second order makes the gain have a peaking point, and this peaking point makes the voltage gain increase as f_s increases. This situation leads to the light-load regulation problem, which increases V_O as the load decreases. The Q value at DP_{High} (Q_{High}) is expressed as

$$Q_{\mathrm{High}} = \frac{1}{R_{\mathrm{ac}}}\sqrt{\frac{L_r}{C_{j,\mathrm{eq}}}}. \tag{3}$$

From (3), it can be noted that as R_{ac} increases or the load condition decreases, Q_{High} becomes smaller, and *LLC* SRC has a larger peak gain at high-frequency region. Therefore, under very light load condition or no-load condition, the undesirable peak gain increases significantly. The rise of the gain curve at high frequency is contrary to the PFM control scheme, which reduces V_O with high frequency. In conclusion, *LLC* SRC with $C_{j,\mathrm{eq}}$ cannot achieve very light load regulation due to $C_{j,\mathrm{eq}}$.

The above analysis is an intuitive analysis for the light-load regulation problem. From the previous papers, since the rectifier diodes do not conduct continuously during the primary switch turned ON, the practical gain curve of *LLC* SRC is higher than impedance analysis [12], [13]. Therefore, in order to achieve the more accurate analysis, the other approach is required.

C. Operation Mode Analysis for LLC SRC With $C_{j,\mathrm{eq}}$

This section includes the analysis for why the actual gain of *LLC* SRC with $C_{j,\mathrm{eq}}$ is higher than impedance analysis under light-load condition. In order to achieve much accurate analysis, the operation of practical *LLC* SRC under light-load condition should be known. From the preceding papers, *LLC* SRC with $C_{j,\mathrm{eq}}$ can be divided into three modes. Fig. 7 shows the key waveforms of actual *LLC* SRC with operation mode analysis [12] and Fig. 8 shows the equivalent circuits of each mode [13]. In order to obtain the gain of *LLC* SRC with $C_{j,\mathrm{eq}}$ simply, the following assumptions are required using the operation mode analysis.

1) The primary switches are ideal. The rectifier diodes are also ideal except C_j. The transformer is ideal except L_M.
2) At mode 1, the time interval of mode 1 is a quarter of resonant period. During this period, v_{pri} is changed from $-V_{\mathrm{RO}}$ to V_{RO}. The initial current of L_r is same with the current of L_M.
3) There is no L_{lkg} of transformer and the average value of i_F is I_O.
4) The value of L_M is much larger than L_r, and the value of C_r is much larger than $C_{j,\mathrm{eq}}$. Therefore, there is no current change of L_M and no voltage change of C_r during mode 1.

Using these assumptions and equivalent circuits, the gain characteristic of *LLC* SRC with $C_{j,\mathrm{eq}}$ under light-load condition can be achieved.

At mode 1 ($t_0 - t_1$), $v_{\mathrm{pri}}(s)$ can be easily obtained using the Laplace equation and the equivalent circuit, as shown in Fig. 8(a), as

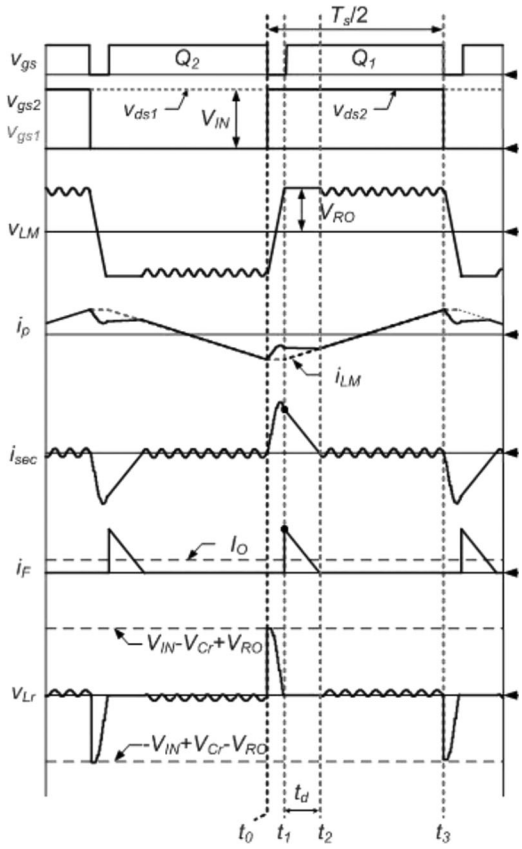


Fig. 7. Key waveforms of actual *LLC* SRC with operation mode analysis.

$$v_{\mathrm{pri}}(s) = -\frac{V_{\mathrm{RO}}}{s} + \frac{\left(sL_M \| \frac{1}{sC_{j,\mathrm{eq}}}\right)}{sL_r + \frac{1}{sC_r} + \left(sL_M \| \frac{1}{sC_{j,\mathrm{eq}}}\right)} \times \left(\frac{V_{\mathrm{in}} - V_{C_r} + V_{\mathrm{RO}}}{s} - \frac{L_r V_{\mathrm{RO}}}{4L_M f_s}\right). \tag{4}$$

Using the assumption 4) and inverse Laplace transform, we can obtain the approximate value of $v_{\mathrm{pri}}(t)$ and $i_{\mathrm{Cj}}(t)$ as follows:

$$v_{\mathrm{pri}}(t) = -V_{\mathrm{RO}} + (V_{\mathrm{in}} - V_{C_r} + V_{\mathrm{RO}})\,\omega_j t \sin(\omega_j t) - \left(\frac{L_r V_{\mathrm{RO}}}{4L_M f_s}\right)\left(\omega_j \sin(\omega_j t) + \omega_j^2 t \cos(\omega_j t)\right) \tag{5}$$

$$i_{C_j}(t) = C_{j,\mathrm{eq}}\left((V_{\mathrm{in}} - V_{C_r} + V_{\mathrm{RO}})\left(\omega_j \sin(\omega_j t) + \omega_j^2 t \cos(\omega_j t)\right) - \left(\frac{L_r V_{\mathrm{RO}}}{4L_M f_s}\right)\left(2\omega_j^2 \cos(\omega_j t) - \omega_j^3 t \sin(\omega_j t)\right)\right). \tag{6}$$

According to (6) and assumption 2), i_{Cj} at t_1 is derived as

$$i_{C_j}(t_1) = C_{j,\mathrm{eq}}\left((V_{\mathrm{in}} - V_{C_r} + V_{\mathrm{RO}})\,\omega_j + \omega_j^2\left(\frac{L_r V_{\mathrm{RO}}\pi}{8L_M f_s}\right)\right). \tag{7}$$

Considering the turns ratio of transformer, the initial current of secondary side, i.e., $i_F(t_1)$, is defined as $n \times i_{C_j}(t_1)$.

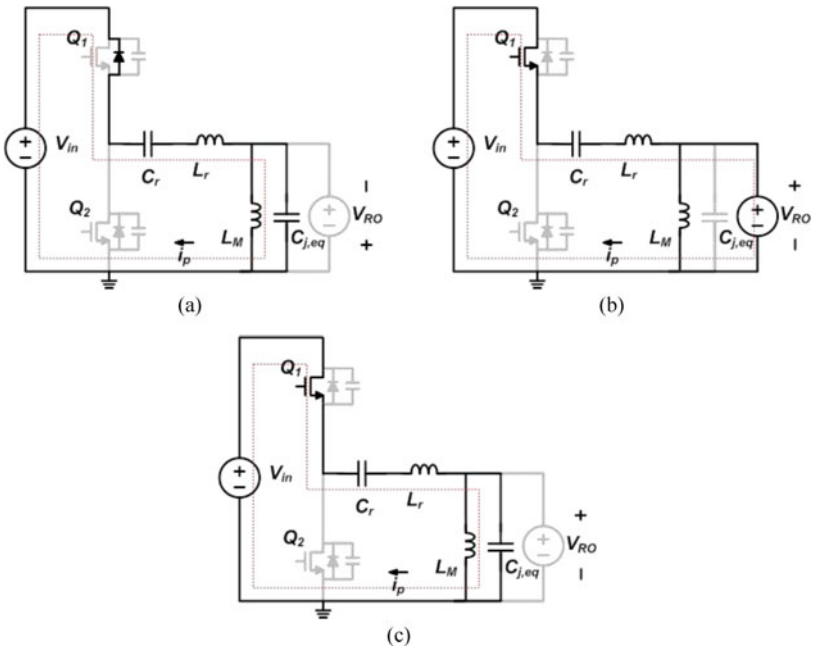


Fig. 8. Equivalent circuits for *LLC* SRC with $C_{j,\mathrm{eq}}$. (a) $t_0 - t_1$. (b) $t_1 - t_2$. (c) $t_2 - t_3$.

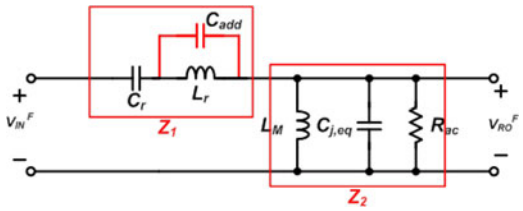


Fig. 9. AC equivalent circuit of proposed *LLC* SRC.

At mode 2 ($t_1 - t_2$), Fig. 8(b) shows the equivalent circuit after v_{pri} is clamped to V_{RO}. At this time, the peak charging current, which is caused by the resonance between L_r and $C_{j,\mathrm{eq}}$, changes the operation mode different with *LLC* SRC under heavy-load condition [12], [13]. In order to achieve simple analysis, the decrease of i_F is determined by the increase of L_M and L_r:

$$i_F(t) = i_F(t_1) - n \times \left(\frac{V_{\mathrm{RO}}}{L_M} + \frac{V_{\mathrm{RO}} - V_{\mathrm{in}} + V_{C_r}}{L_r} \right) t. \quad (8)$$

Using (8), we can easily obtain the value of t_d, i.e., $(t_2 - t_1)$. From the reason that since there is no powering current at mode 1 and mode 3, the average value of $i_F(t)$ at mode 2, which is the same value of I_O, is calculated as

$$I_O = \frac{V_O}{R_O} = 2 f_s \int_{t_1}^{t_2} i_F(t)\, dt = f_s \times i_F(t_1) \times t_d. \quad (9)$$

Finally, combining (7)–(9), we can obtain V_O according to I_O. Because the time of powering mode is smaller than that of half of switching period under the light-load condition, i.e., $t_d < T_s/2$, operation mode analysis is better to achieve the tendency of voltage gain compared with impedance analysis. However, even though the gain of *LLC* SRC with impedance analysis is not perfectly matched under the light-load condition, the increase tendency of the gain curve is similar with operation mode analysis and the main reason for light-load regulation is unchanging. Therefore, the paper proposes the intuitive analysis for the light-load regulation problem of *LLC* SRC and the effective solution using impedance analysis with Bode plot.

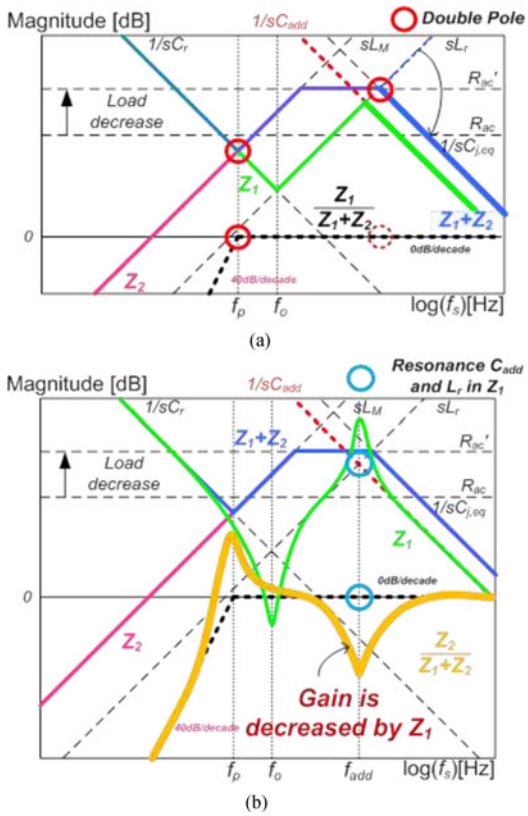


Fig. 10. Bode plot of proposed *LLC* SRC. (a) Z_1 with C_{add}. (b) Actual gain curve.

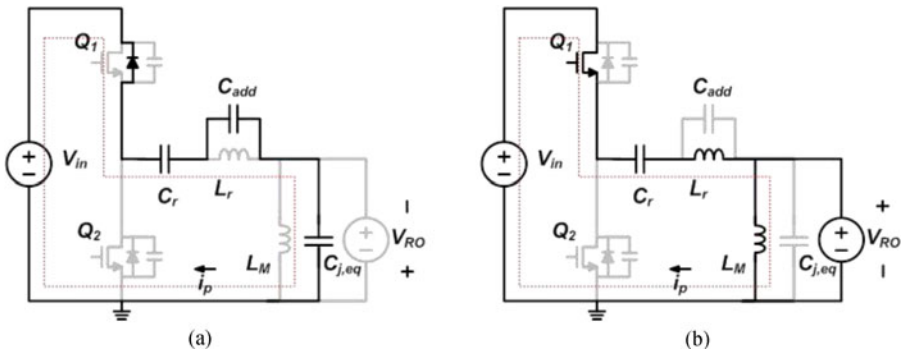


Fig. 11. Equivalent circuits for proposed *LLC* SRC. (a) Transient mode. (b) Powering period.

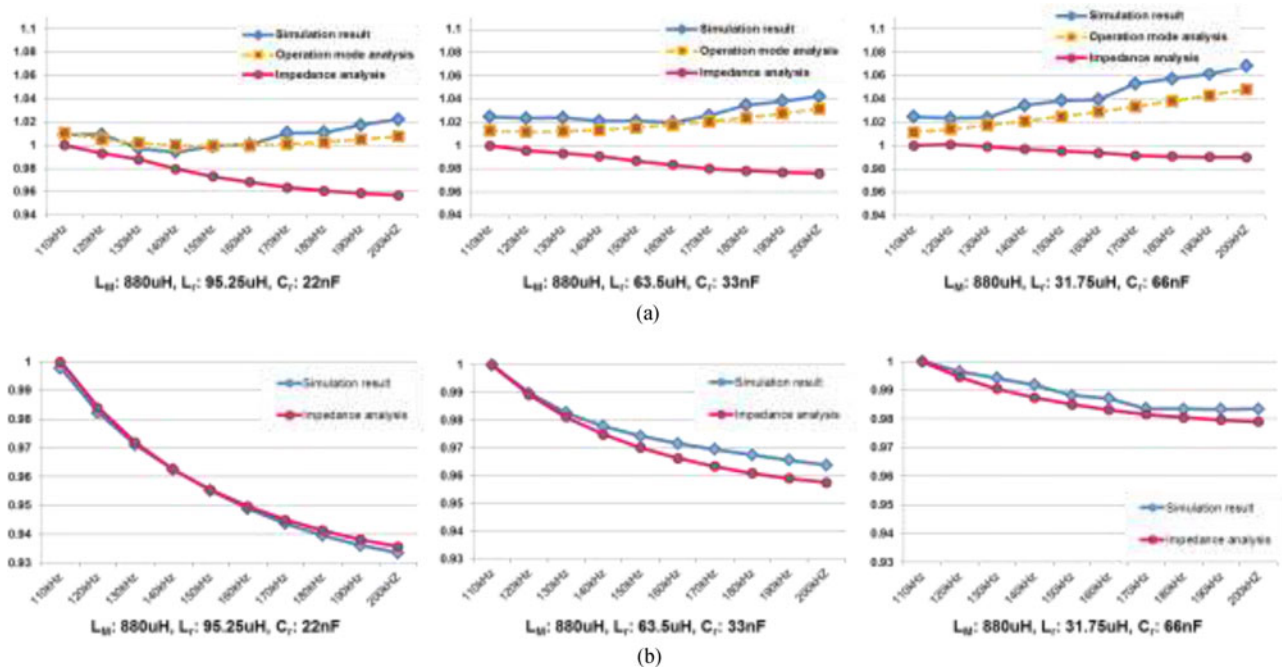


Fig. 12. Gain curve comparison in linear scale under 10% load condition. (a) *LLC* SRC with $C_{j,\mathrm{eq}}$. (b) Proposed *LLC* SRC.

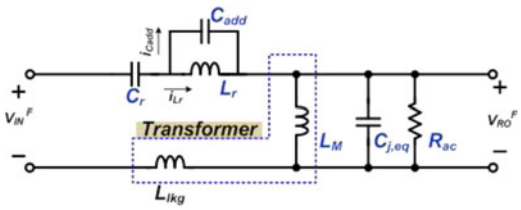


Fig. 13. AC equivalent circuit of proposed *LLC* SRC with L_{lkg}.

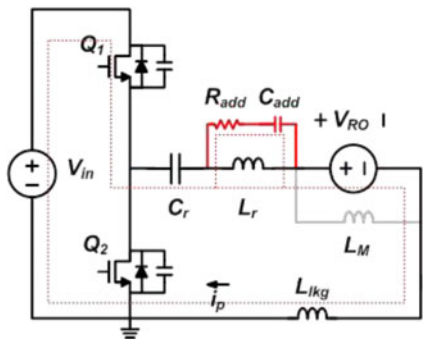


Fig. 14. Equivalent circuit of proposed resonant tank with R_{add}.

III. Proposed Concept for Light-Load Regulation

A. Cancelation of Effects of $C_{j,\mathrm{eq}}$

From the above impedance analysis, the main reason of the light-load regulation problem is $C_{j,\mathrm{eq}}$, which causes DP_{High} in high-frequency region. On the other hands, the peak charging current due to $C_{j,\mathrm{eq}}$ makes the gain of *LLC* SRC high from the operation mode analysis and proceeding papers [12], [13]. In this paper, the effect of $C_{j,\mathrm{eq}}$ can be canceled by the proposed concept with impedance analysis. Therefore, the undesired higher gain does not appear as f_s increases and the proposed *LLC* SRC achieves the light-load regulation.

In order to cancel the effect of $C_{j,\mathrm{eq}}$, a small C_{add} is added to the resonant tank of *LLC* SRC, as shown in Fig. 9. Just by adding C_{add}, Z_1 will be changed and the gain of *LLC* SRC, i.e.,

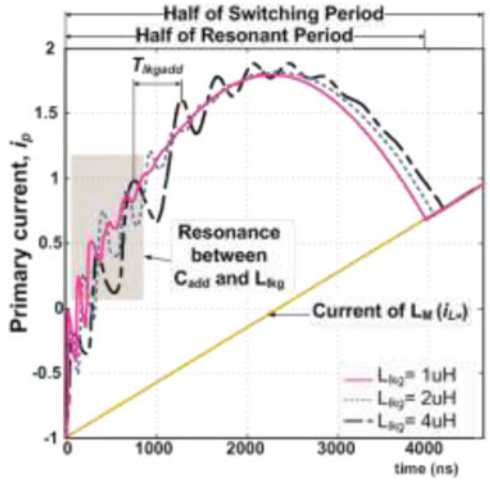


Fig. 15. Waveforms of primary current considering $L_{\rm lkg}$ and $R_{\rm add}$.

$Z_2/(Z_1+Z_2)$, will also be changed. Meanwhile, Z_2 has the same magnitudes with the *LLC* SRC with $C_{j,\rm eq}$.

Fig. 10(a) shows the impedance asymptotes of new resonant tank after adding $C_{\rm add}$. As seen in Fig. 10(a), the dotted black line shows that the effects of $C_{j,\rm eq}$ are eliminated and the asymptote has unity gain after where the impedance magnitudes of $\rm L_M$ and $\rm C_r$ are equal. However, since the actual impedance curve of Z_1 has a large positive peaking due to the resonance between L_r and $C_{\rm add}$, as shown in Fig. 10(b), the gain of proposed *LLC* SRC has a large negative peak point. Therefore, the actual gain curve of the proposed *LLC* SRC will be drawn, as shown in Fig. 10(b). Ideally, the peak magnitude of Z_1 at $f_{\rm add}$ increases infinite, the operation of proposed *LLC* SRC is stable under the light-load condition because of almost zero gain at $f_{\rm add}$. According to this result, the proposed *LLC* SRC with PFM control always regulates the output voltage [30], [32]–[34]. In addition, this reduced gain can help for soft start-up of *LLC* SRCs, and commonly reduces $f_{\rm s}$ under light-load condition [33], [34].

Even though the impedance analysis with light-load condition is not perfectly matched to actual case [12], [13], [35], the proposed concept can be analyzed by impedance analysis due to $C_{\rm add}$. Since $C_{\rm add}$ eliminates the effect of $C_{j,\rm eq}$, which is the unwanted peak charging current, the powering period of proposed *LLC* SRC is almost same with ideal *LLC* SRC, as shown in Fig. 2. Therefore, the proposed *LLC* SRC is well matched with impedance analysis and the proposed method is not only very simple but also powerful that it can be implemented by just adding a small $C_{\rm add}$, without using complex control schemes. The operation mode analysis for the proposed *LLC* SRC is described in detail in the following section.

B. Operation Mode Analysis for the Proposed LLC SRC

In this section, the operation mode analysis for the proposed *LLC* SRC is described. From above analysis, $C_{j,\rm eq}$ makes the unwanted peak charging current, and $C_{\rm add}$ can cancel the effects of $C_{j,\rm eq}$. For the more detail analysis, the equivalent circuits of proposed *LLC* SRC, which are shown in Fig. 11, are also represented such as in Section II-C. The assumptions are almost same with the above analysis except that $C_{\rm add}$ and $C_{\rm add}$ are much smaller than C_r too. In the case of proposed *LLC* SRC, the operation mode is different from above *LLC* SRC with $C_{j,\rm eq}$. In order to charge $C_{j,\rm eq}$ to V_{RO}, a new charging path for $C_{j,\rm eq}$ is made by $C_{\rm add}$ as shown in Fig. 11(a). When Q_1 turns on, the current path only consists of capacitors. Therefore, $v_{\rm pri}$ quickly changes from $-V_{\rm RO}$ to $V_{\rm RO}$. Since the time interval of voltage change is very short, the peak charging current is reduced and there is no additional powering current. The value of $v_{\rm pri}(s)$ in Fig. 11(a) is defined as follows:

$$v_{\rm pri}(s) = (V_{\rm in} - V_{C_r}) \times \frac{C_{\rm add}}{C_{\rm add}+C_{j,\rm eq}}. \tag{10}$$

After $v_{\rm pri}$ reaches $V_{\rm RO}$, the proposed *LLC* SRC operates as the powering mode, which is similar with ideal *LLC* SRC as shown in Fig. 11(b). In the powering period, since L_r, $C_{\rm add}$, and $C_{j,\rm eq}$ are resonate and they make the circulating current within certain period, i.e., $1/\sqrt{2L_r(C_{\rm add}+C_{j,\rm eq})}$, the value of circulating current is too small to effect the conversion efficiency.

From the results of above analyses, the only difference between the operation mode analysis and impedance analysis with proposed *LLC* SRC is that the actual shape of powering current is not perfectly sinusoid, which means the actual value of $R_{\rm ac}$ is little different with ideal *LLC* SRC. Therefore, the gain curve of the proposed *LLC* SRC can also be analyzed with Bode plot and impedance asymptotes under the light-load condition. In other words, since $C_{\rm add}$ makes a new charging path for $C_{j,\rm eq}$ as shown in Fig. 11(a), $C_{j,\rm eq}$ does not affect to the gain curve in proposed *LLC* SRC. In conclusion, the proposed *LLC* SRC with impedance analysis is well matched with experimental results.

C. Design Guideline for $C_{\rm add}$

To maintain the advantages of conventional *LLC* SRC, the effect of $C_{\rm add}$ should be as small as possible. In other words, since C_r is a main factor of the gain curve, the reasonable value of $C_{\rm add}$ should be sufficiently smaller than C_r. In addition, in order to eliminate the effect of $C_{j,\rm eq}$, $C_{\rm add}$ should be larger than $C_{j,\rm eq}$ and the reasonable value is about five to ten times larger than $C_{j,\rm eq}$ considering the junction capacitance variation per diode reverse voltage and (10) as

$$5 \times C_{j,\rm eq} \<lt;\ C_{\rm add} \ll C_r. \tag{11}$$

Since the large value of $C_{\rm add}$ degrade the performance of *LLC* SRC, smaller value of $C_{\rm add}$ is better. However, some applications with high output voltage/high load current can increase $C_{j,\rm eq}$ because of small turns ratio and large current stress. Therefore, the proposed *LLC* SRC should avoid these applications.

Using above analyses, new gain curves of *LLC* SRCs can be obtained such as in Fig. 12. In these graphs, f_o is 110 kHz, *X*-axis is f_s, *Y*-axis is gain, and the condition of I_O is 10%. Fig. 12(a) shows the gain curves of the *LLC* SRC with $C_{j,\rm eq}$ in linear scale. As mentioned in Section II-C, the operation mode analysis is more suitable than impedance analysis in the case of the *LLC* SRC with $C_{j,\rm eq}$. The gain tendency of *LLC* SRC with $C_{j,\rm eq}$ is that the gain increases as f_s increases under the light-load condition. On the other hand, since the effect of

TABLE II
COMPONENTS LIST

Topology	Conventional *LLC*	*LLC*AC [12]	Proposed *LLC* ($C_{\rm add}$, $C_{\rm add}$ with $R_{\rm add}$)	
Additional capacitor	-	470 pF/450 V	680 pF/250 V	680 pF/250 V (10 Ω)
Primary switches			IPW60R280C6	
Rectifier diodes			V60100C	
Transformer (Turns-ratio, $N_p : N_s$)			PQ2620 (39:10)	
Magnetizing inductance, L_M (Leakage inductance, $L_{\rm lkg}$)			878 μH (2.9 μH) 877.8 μH (8.7 μH)	
Resonant tank (L_r, C_r)			61.3 μH, 33 nF	
Dead time			700 ns	
Resonant frequency, f_o (Frequency variation)			110 kHz (82−132 kHz)	

$C_{j,\rm eq}$ is eliminated by $C_{\rm add}$, the gain of the proposed *LLC* SRC decreases as f_s increases, as shown in Fig. 12(b). In addition, the gain of proposed *LLC* SRC is well matched with impedance analysis as mentioned in Section III-B. From these results, the proposed *LLC* SRC has no undesirable gain peaking and no light-load regulation problem.

D. Resonance Between $L_{\rm lkg}$ and $C_{\rm add}$

Typically, the actual transformer has $L_{\rm lkg}$. Since general $L_{\rm lkg}$ has much smaller value than L_r and L_M, it does not affect the gain curve of *LLC* SRC as

$$M = \frac{Z_2}{Z_1 + Z_2 + j\omega L_{L\rm lkg}} \cong \frac{Z_2}{Z_1 + Z_2}. \tag{12}$$

However, the analysis of $L_{\rm lkg}$ is necessary, because it changes the current waveform due to the resonance with $C_{\rm add}$ in powering period. In order to cancel the effect of $C_{j,\rm eq}$, $C_{\rm add}$ should be attached to resonant inductor in parallel, but in practice, $C_{\rm add}$ cannot cover both L_r and $L_{\rm lkg}$ as seen in Fig. 13. From the result, i_p of the proposed *LLC* SRC is the sum of $i_{\rm Lr}$ and $i_{C\rm add}$.

The oscillation of $i_{C\rm add}$ and its period $T_{\rm lkgadd}$ are determined by the resonance between $L_{\rm lkg}$ and $C_{\rm add}$. Even though the resonance between $L_{\rm lkg}$ and $C_{\rm add}$ makes the oscillation, the amplitude of $i_{C\rm add}$ is generally small enough to ignore or is rapidly damped by parasitic components.

Commonly, the transformer should be designed with smaller $L_{\rm lkg}$ as much as possible to avoid the adverse effects of $i_{C\rm add}$. Since the desired value of $L_{\rm lkg}$ cannot be achieved easily in real cases, it is difficult to make the transformer with small $L_{\rm lkg}$ under certain condition. For this reason, the usage of proposed *LLC* SRC can be limited depending on the applications with a large $L_{\rm lkg}$, such as an integrated transformer type [36], [37].

E. Damping With $R_{\rm add}$

If the proposed *LLC* SRC achieves the light-load regulation with large $L_{\rm lkg}$, the ripple current of $i_{C\rm add}$ will not be ignored. In order to reduce the ripple of $i_{C\rm add}$, $R_{\rm add}$, which can accelerate the damping of $i_{C\rm add}$, should be added to $C_{\rm add}$ in series, as shown in Fig. 14. In addition, since $i_{C\rm add}$ is small enough to neglect, the power loss of $R_{\rm add}$ is also small in nominal state and the proposed *LLC* SRC can maintain a high conversion efficiency preserving the light-load regulation. Considering $C_{\rm add}$, $L_{\rm lkg}$, and $R_{\rm add}$, the equation of $i_p(t)$ can be obtained by the equivalent circuit in Fig. 14. Since $i_p(t)$ is same with the current of C_r, $v_{\rm Cr}$ is induced as

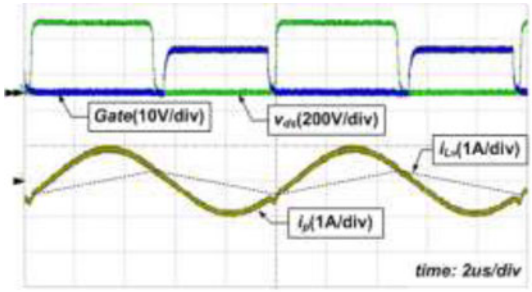
$$v_{C_r}(s) = \left(\frac{V_{C_r}}{s}\right) + \left(\frac{V_{\rm IN} - V_{\rm RO} - V_{C_r}}{s} - \frac{L_{\rm lkg} V_{\rm RO}}{4 L_M f_s}\right) \times \left(\frac{1 + sC_{\rm add}R_{\rm add} + s^2 L_r C_{\rm add}}{s^4(A) + s^3(B) + s^2(C) + sC_{\rm add}R_{\rm add} + 1}\right) \tag{13}$$

where *A* is $L_r L_{\rm lkg} C_{\rm add} C_r$, *B* is $(L_r + L_{\rm lkg}) C_{\rm add} C_r R_{\rm add}$, and *C* is $(L_r C_r + L_r C_{\rm add} + L_{\rm lkg} C_r)$. From (13), the trend of $i_p(t)$ according to $L_{\rm lkg}$ can be presented by inverse Laplace transform and differential equation, as shown in Fig. 15. At this point, the ripple of i_p attenuates rapidly as the value of $L_{\rm lkg}$ decreases. From this result, the reasonable value of $R_{\rm add}$ can be determined by the criterion that $T_{l\rm kgadd}$ should be much larger than time constant of $R_{\rm add}$ and $C_{\rm add}$. In conclusion, in order to reduce the oscillation of i_p, the proposed *LLC* SRC should minimize $L_{\rm lkg}$ or add small $R_{\rm add}$ to accelerate the damping.

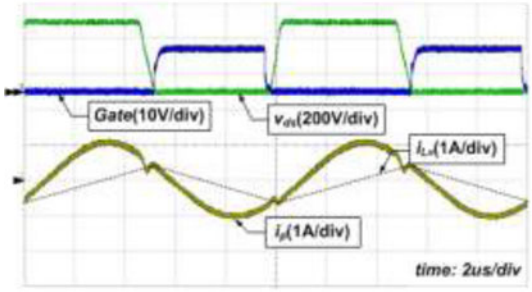
IV. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed *LLC* SRC, the prototype converters have been designed. In order to achieve the light-load regulation without the additional control, *LLC* SRC with additional $C_{\rm oss}$ (*LLC*AC) [12] was selected for comparison. The specifications of prototype converters are as follows: $V_{\rm IN}$: 360−400 V; output power: 200 W (50 V, 4 A); and f_o is 110 kHz. The design parameters utilized in this experiment are presented in Table II. Only the conventional *LLC* SRC has no additional capacitor, and two different transformers are used for $L_{\rm lkg}$ variation. In addition, the proposed *LLC* SRC is divided into two types, i.e., $C_{\rm add}$ and $C_{\rm add}$ with $R_{\rm add}$. In this experiment, the dead time of prototype converters was 700 ns to satisfy the ZVS condition of *LLC*AC at nominal state and f_s variation was from 82 to 132 kHz. Since the higher maximum f_s makes the characteristics of light-load regulation worse, the experiment limited the maximum f_s as 132 kHz [11]. Moreover, in order to reduce the conduction loss of equivalent series resistance, C_r and additional capacitors used the polypropylene capacitors.

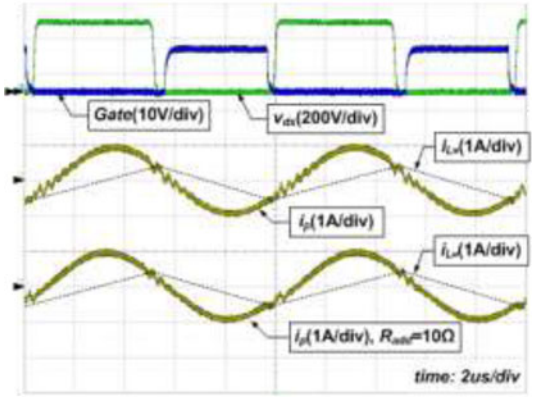
Fig. 16 shows the experimental waveforms of prototype converters that contain gate–source voltage ($v_{\rm gs}$), drain–source voltage ($v_{\rm ds}$), and i_p under the nominal $V_{\rm IN}$ and half-load condition. As shown in Fig. 16, the conventional *LLC* SRC and the proposed *LLC* SRC achieve ZVS operation very well. However, since *LLC*AC has narrow ZVS range due to the additional $C_{\rm oss}$,



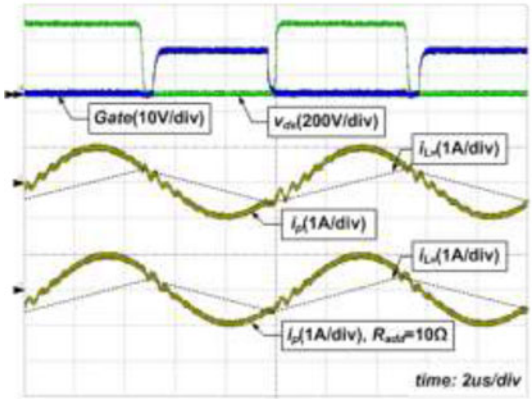
(a)



(b)

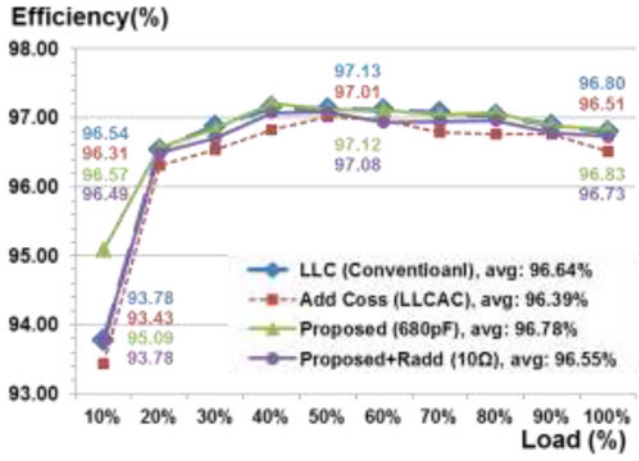


(c)

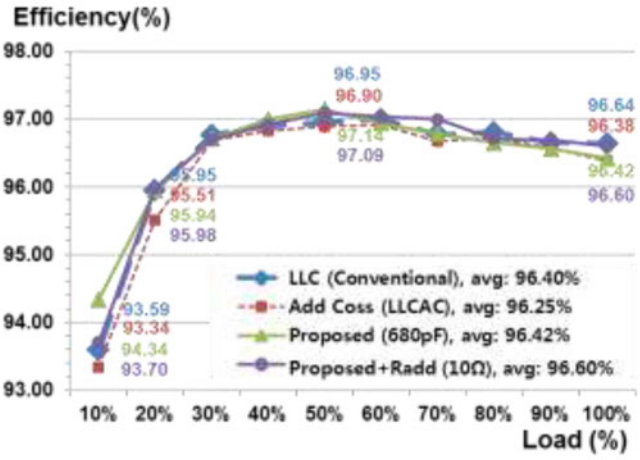


(d)

Fig. 16. Experimental waveforms of *LLC* SRC. (a) Conventional *LLC* SRC ($L_{\rm lkg}$: 2.9 μH). (b) *LLC*AC ($L_{\rm lkg}$: 2.9 μH) [12]. (c) Proposed *LLC* SRC ($L_{\rm lkg}$: 2.9 μH). (d) Proposed *LLC* SRC ($L_{\rm lkg}$: 8.7 μH).



(a)



(b)

Fig. 17. Efficiency comparison with load variation. (a) $L_{\rm lkg}$: 2.9 μH. (b) $L_{\rm lkg}$: 8.7 μH.

ZVS operation of *LLC*AC is barely achieved with large dead time, 700 ns. In the case of proposed *LLC* SRC, as shown in Fig. 16(c) and (d), since the oscillation of i_p is small enough, it does not affect the conversion efficiency. The difference of Fig. 16(c) and (d) is the value of $L_{\rm lkg}$. As shown in Figs. 15 and 16, the damping of the oscillation with large $L_{\rm lkg}$ is slower than with small $L_{\rm lkg}$ because the value of $T_{\rm lkgadd}$ is proportional to settling time. In the case of large $L_{\rm lkg}$ with $R_{\rm add}$, the oscillation is attenuated rapidly by $R_{\rm add}$ as shown in the lower $i_p(t)$ waveforms of Fig. 16(c) and (d).

Fig. 17 shows the efficiency comparisons of four prototype converters depending on the load condition. To obtain the efficiency curves for different $L_{\rm lkg}$, two different transformers are used and $V_{\rm IN}$ condition is 397 V. Fig. 17(a) is the efficiency comparison with small $L_{\rm lkg}$, i.e., 2.9 μH. In the case of heavy-load condition, the proposed *LLC* SRC shows the similar conversion efficiency with the conventional *LLC* SRC. Since the impedance magnitude of $C_{\rm add}$ is much smaller than C_r and L_r, the additional circulating current in the proposed *LLC* SRC is negligible to conversion efficiency in this experiment. Meanwhile, since f_s of the proposed *LLC* SRC is lower than the conventional

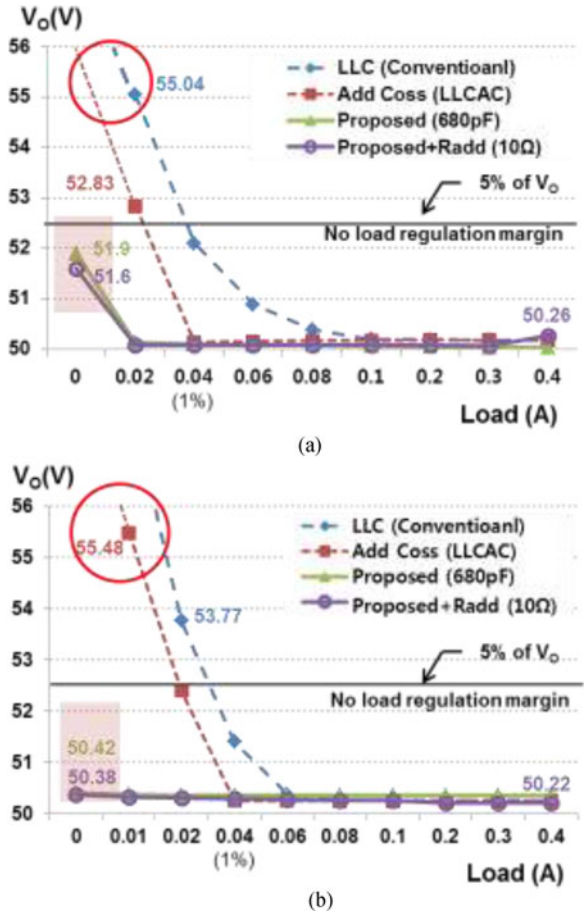


Fig. 18. Characteristics of load regulation. (a) $L_{\rm lkg}$: 2.9 μH. (b) $L_{\rm lkg}$: 8.7 μH.

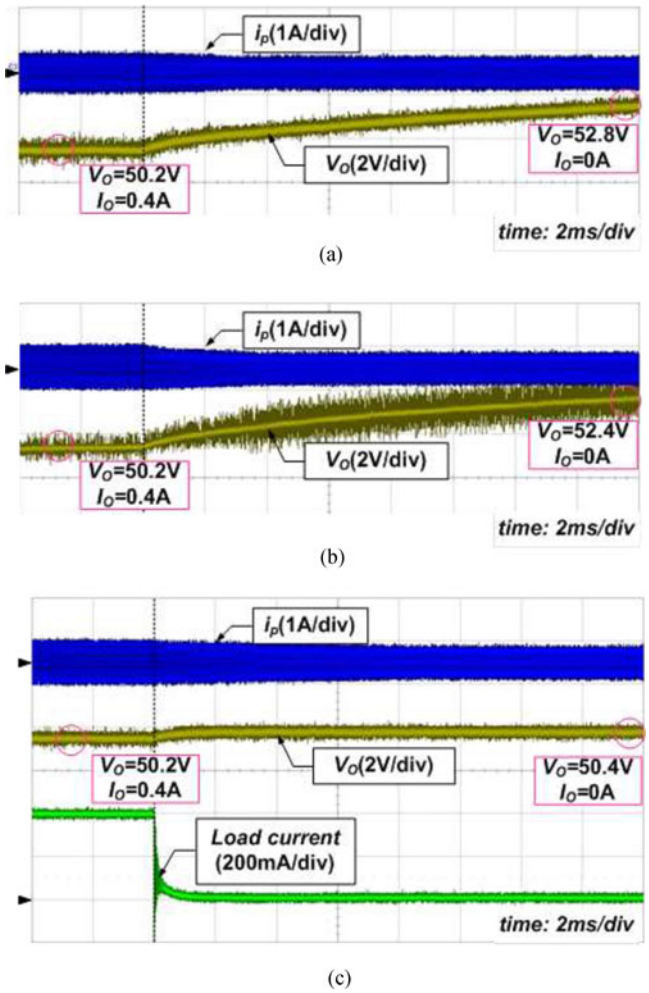


Fig. 19. Waveforms of no-load regulation. (a) Conventional *LLC* SRC. (b) *LLC*AC [12]. (c) Proposed *LLC* SRC ($L_{\rm lkg}$: 8.7 μH).

converters under the light-load condition, the proposed *LLC* SRC improves the light-load efficiency, resulting in reduced switching losses. In the case of proposed *LLC* SRC with $R_{\rm add}$, the efficiency curve with the proposed *LLC* SRC with $R_{\rm add}$ is similar with the proposed *LLC* SRC because the oscillation of i_p is small enough to be neglected. On the other hand, in the case of *LLC*AC, it has a little lower conversion efficiency than the other converters due to the narrow ZVS condition and the circulating current of additional $C_{\rm oss}$.

Fig. 17(b) is the efficiency curve with large $L_{\rm lkg}$, i.e., 8.7 μH. From Fig. 14, the oscillation and large ripple value of $i_{C\rm add}$ can increase the conduction loss of primary switches under heavy-load condition. In other words, if the proposed *LLC* SRC cannot ignore the loss of $i_{C\rm add}$, the proposed *LLC* SRC will add $R_{\rm add}$ in series to reduce the oscillation. On the other hand, since the value of $i_{C\rm add}$ is sufficiently large due to the large $L_{\rm lkg}$, the conversion efficiency of the proposed *LLC* SRC is lower than conventional *LLC* SRC, as shown in Fig. 17(b), under heavy-load condition. However, since the dissipated power of $R_{\rm add}$ is small enough, the propose *LLC* SRC with $R_{\rm add}$ has a similar conversion efficiency with conventional *LLC* SRC under heavy-load condition. Therefore, the proposed *LLC* SRC with $R_{\rm add}$ has more advantages with large L_{lkg}, such as EMI, noise characteristics, and higher conversion efficiency.

Fig. 18 shows the characteristics of load regulation with prototype converters. As shown in Fig. 18, the regulation characteristics of the proposed *LLC* SRCs are very good compared with the conventional *LLC* SRCs. In other words, since the gain of proposed *LLC* SRCs decrease as f_s increases, the proposed *LLC* SRCs achieve the light-load regulation and no-load regulation. In the case of *LLC*AC, even though it has the better light-load regulation characteristic than the conventional *LLC* SRC, *LLC*AC cannot always achieve no-load regulation because *LLC*AC has a narrow ZVS range under very light load and no-load condition.

Fig. 19 also shows the waveforms of no-load regulation. As shown in Fig. 19(a) and (b), when the load turns off from 400 mA to 0 A, V_O of conventional *LLC* SRCs increase continuously. However, as shown in Fig. 19(c), the proposed *LLC* SRC maintains the constant V_O with no-load condition. As shown in Fig. 20(a), *LLC*AC cannot achieve ZVS operation when the load condition is 2% lower than that as mentioned before. On the other hand, as shown in Fig. 20(b), the proposed *LLC* SRC is well operated and achieves ZVS operation under the entire load condition.

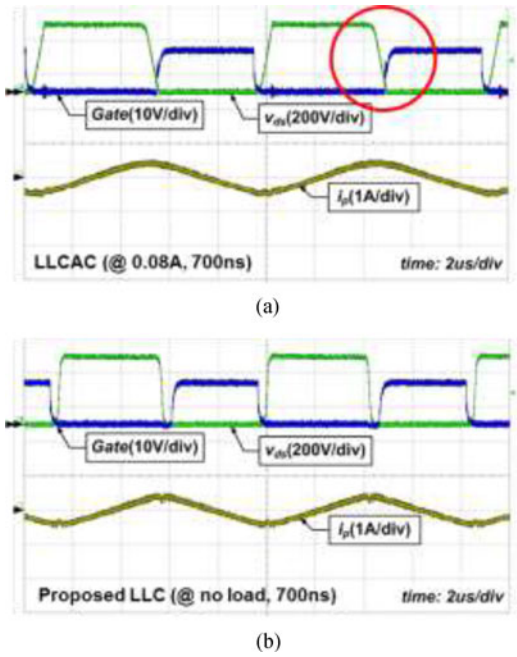


Fig. 20. Experimental waveforms under very light load condition. (a) *LLC*AC [12]. (b) Proposed *LLC* SRC.

In this paper, the characteristics of the proposed *LLC* SRCs are confirmed by the experimental results. The proposed *LLC* SRCs achieve the light-load regulation including the no-load condition without additional control, maintaining the conversion efficiency compared to the conventional *LLC* SRC at nominal state. Furthermore, the proposed *LLC* SRCs improved the light-load efficiency due to reduced switching losses.

V. Conclusion

This paper introduces the intuitive analysis of the light-load regulation problem in *LLC* SRC using Bode plot and impedance asymptote. In addition, in order to eliminate the effects of parasitic capacitors in rectifier diodes, the proposed concept adds $C_{\rm add}$ in parallel with L_r. Through this result, there is a new charging path for $C_{j,\rm eq}$ and the gain curve of *LLC* SRC decreases as f_s increases. Furthermore, the proposed *LLC* SRC achieves no-load regulation within 3% margin. In the case of large $L_{\rm lkg}$, the proposed *LLC* SRC with $R_{\rm add}$ reduces the oscillation without degrading the conversion efficiency. Therefore, the proposed concept is suitable for many *LLC* SRC applications. Moreover, since the proposed concept uses only small additional components without changing control method, it has a better performance compared with the other simple methods [12], [13].

Up to date, even though *LLC* SRCs have many advantages, such as small components and ZVS capability, the usage of *LLC* SRC has been limited due to the light-load regulation problem. However, with the proposed method, *LLC* SRC achieves the no-load regulation without any side effect. Therefore, *LLC* SRC with the proposed technique can be extended more to overall power electronics industry.

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