Fault-Tolerant Control of MMC With Hot Reserved Submodules Based on Carrier Phase Shift Modulation

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***Abstract*—Reliability is one of the most important challenges for the modular multilevel converter (MMC), which is composed of a large number of power electronics submodules (SMs). In order to increase the system reliability, the reserved SMs are often utilized. A novel strategy is proposed in this paper to implement the fault-tolerant control of MMC with the hot reserved SMs based on the carrier phase shift modulation. All the SMs, including the hot reserved SMs, work in the operating mode and the standby mode in turns. A rotating sliding choice box is adopted to select the operating SMs and the corresponding phase-shift angles, which enables the equal burden of each SM. Once the faults are detected and localized, the reserved SMs can simultaneously replace the bypassed failed SMs, which guarantees the fault-tolerant operation with a nearly seamless transition and very short recovery time. Furthermore, the line cycle is set as the rotating period in the control strategy, without increasing much switching loss. The mismatch pulses are greatly reduced as well. This technique can also be easily implemented in a DSP or microcontroller. Simulations in MATLAB/Simulink and experiments based on a downscaled MMC prototype have verified the feasibility and effectiveness of the proposed control strategy.**

***Index Terms*—Carrier phase shift (CPS) modulation, fault-tolerant control, hot reserved submodules (SMs), modular multilevel converter (MMC).**

I. Introduction

TREMENDOUS research work has been conducted on the modular multilevel converter (MMC) since its invention in the early 2000s [1, 2]. Compared with the neutral-point clamped and the flying capacitor multilevel converters, MMC has the advantages of modularity and scalability [3]. By stacking a large number of identical submodules (SMs), the output voltage of MMC can reach arbitrary levels in theory (e.g., hundreds of levels), which enables high-power conversion without large filters or transformers [4]. MMC has been considered as a suitable solution in the high-power applications such as HVdc transmission, STATCOM, and medium-voltage motor drive [5].

Generally, a huge number of components are used in MMC, including very vulnerable semiconductor devices and capacitors [6]. Every component can be regarded as a potential failure point, which threatens the normal operation of the converter. Therefore, the reliability becomes one of the most important challenges for MMC [7]. In order to increase the system reliability, fault diagnosis with quick response and fault-tolerant strategies are necessary for MMC [8], [9]. The diagnosis and the protection of the catastrophic Insulated Gate Bipolar Transistor (IGBT) short-circuit fault are often integrated in the gate drivers, which guarantees that the fault can be detected within 10 μs [10]. Considering the common IGBT open-circuit fault in MMC, several fault diagnosis methods have been proposed based on the state observers, such as the Kalman-filter based observer [8], the sliding-mode observer [11], and the Luenberger observer [12]. Besides, the clustering algorithm based and the calculated capacitance based diagnosis methods are proposed in [13], and the latter is capable of both detecting the failed SMs and pinpointing the fault switches. Once the failed SMs are detected and localized, they must be bypassed immediately. Then subsequent to that, the reserved SMs are often utilized in practice to keep MMC working normally without being interrupted until the next regular maintenance [14], which is the fault-tolerant operation of MMC, namely the major focus of this paper. Several design and control strategies for three-phase MMC with the reserved SMs have been proposed in [15–22], in which four schemes of managing the reserved SMs were mentioned.

Scheme 1: Configure cold reserved SMs [15], [16], which means that the reserved SMs are bypassed in the normal operation, and only activated when the faults occur.

Scheme 2: Configure hot reserved SMs, which means that the redundant SMs operate in the same way as the other SMs. Once the faults occur in one arm, bypass the failed SMs and the same number of normal SMs in the other five arms to achieve the symmetrical operation. This scheme was mentioned in [17].

Scheme 3: Configure hot reserved SMs as *Scheme 2*, and bypass the failed SMs as well as the same number of normal SMs only in the complementary arm [18]. Thus, the three-phase MMC only needs to operate asymmetrically among different phases.

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Scheme 4: Configure hot reserved SMs as *Scheme 2*, and only bypass the failed SMs [19–22]. Thus, the MMC needs to operate asymmetrically among different arms.

Scheme 1 has the drawbacks of long charging time for the cold reserved SMs and the distorted transient waveforms. A seamless transition control strategy was provided in [16] to handle this issue, but the control system is relatively complex. Moreover, the cold reserved SMs are not involved in the normal operation, which is uneconomic with a low semiconductor utilization ratio [19]. Hot reserved SMs are all used in *Schemes 2–4*. Even though they have the drawback of higher conduction loss, the benefits are obvious, such as the better transient performance and a higher semiconductor utilization ratio. Moreover, *Schemes 2* and 3 guarantee the symmetrical operation of MMC, namely same number of SMs in the upper and lower arms, which brings the benefit that the odd order circulating currents [20] and the corresponding issues can be avoided. In contrast, the unsymmetrical operation is allowed in *Scheme 4*, and no extra normal SMs need to be bypassed after the faults occur, which means more economic and more reliable. Thus, *Scheme 4* was adopted in a lot of previous literatures. To deal with the unsymmetrical issue, a simple control strategy was proposed in [17] to adjust the capacitor voltage in the faulty arm, which enables the energy balanced in two complementary arms and thus, the fault ride-through. Another fault-tolerant approach was proposed in [20] through suppressing the fundamental circulating current component caused by the asymmetrical operation. In analogy to the fault-tolerant operation in the cascaded H-bridge converter, a postfault strategy for MMC based on the neutral-shift was provided in [21], which guarantees the desired line-to-line voltage. In fact, most of these fault-tolerant methods are based on the nearest-level modulation only with a little difference from the existing control [22], which can be easily implemented.

Scheme 4 is also adopted in this paper, and a novel fault-tolerant control strategy based on the carrier phase shift (CPS) modulation is proposed, which can make MMC operate symmetrically all the time. CPS modulation is suitable for MMC because it makes the loss evenly distributed among different SMs, consistent with the modularity and scalability of MMC [22]. Compared with the nearest level modulation, CPS modulation is applicable to MMC with fewer SMs [22], [23]. There are two schemes of CPS modulation, namely "$N + 1$" and "$2N + 1$" level modulation. The difference between the two lies in the different phase displacements between the upper and lower carriers, which will influence the interactions between the upper and lower arms, and thus, determines the harmonic features of the output voltage and the circulating current [23]. Both the schemes are effective pulse width modulation (PWM) solutions for MMC and "$N + 1$" level, CPS modulation is adopted in this paper as an example.

After comparing three possible fault-tolerant methods based on the CPS modulation, the one with the best transient performance is selected in the paper. Based on the proposed rotating mechanism, the control structure and implementation flowchart, all the SMs in MMC take turns to work in the operating mode and the standby mode, which achieves the equal burden of each SM on a relatively large time-scale (e.g., dozens of line cycles). Once the failed SMs are detected and localized, they are deleted from the selecting option immediately, which guarantees a nearly seamless transition and very short recovery time.

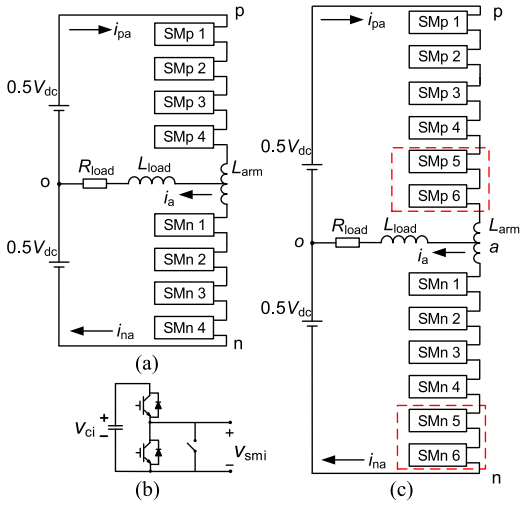

Fig. 1. Single-phase MMC: (a) four SMs per arm, without redundant SMs; (b) half-bridge SM with a bypass circuit breaker; and (c) six SMs per arm, with two hot reserved SMs shown in the dashed box.

This paper is organized as follows. Section II introduces the CPS modulation of MMC with hot reserved SMs. Then, the principle of the proposed fault-tolerant control strategy is presented in Section III. Next, the detailed analysis of the control strategy is provided in Section IV. Simulations in MATLAB/Simulink and the experimental results based on a downscaled MMC prototype in Section V have confirmed the effectiveness of the fault-tolerant control strategy. Finally, Section VI concludes this paper.

II. CPS Modulation of MMC with Hot Reserved SMs

The single-phase MMC with half-bridge SMs in Fig. 1 is adopted to illustrate the proposed fault-tolerant control strategy and the following analysis and conclusions can be extended to three-phase MMC or MMC with full-bridge SMs directly. A center-tapped arm inductor [24] is used here. Fig. 1(a) shows the MMC with four half-bridge SMs per arm (the rated number of SMs $N = 4$), without redundant SMs. Fig. 1(b) displays the half-bridge SM with a bypass circuit breaker. For comparison, Fig. 1(c) shows the case with two hot-reserved SMs per arm (the number of redundant SMs $M = 2$).

A. CPS Modulation of MMC Without Redundant SMs

Based on the CPS modulation, the basic working principle and control strategy of MMC without redundant SMs have been introduced in [24]. In the control algorithm, the voltage references for the upper and lower arms can be given from the system-level closed-loop control. The references are then distributed to the SMs, adjusted slightly for suppressing the circulating current and balancing the capacitor voltages. After that, the references are compared with a series of phase-shifted triangle carriers to generate the PWM signals for the switching devices. For MMC without redundant SMs, in Fig. 1(a), under the "$N + 1$" level CPS modulation, the voltage references and the carriers for the upper and lower SMs, the respective phase-

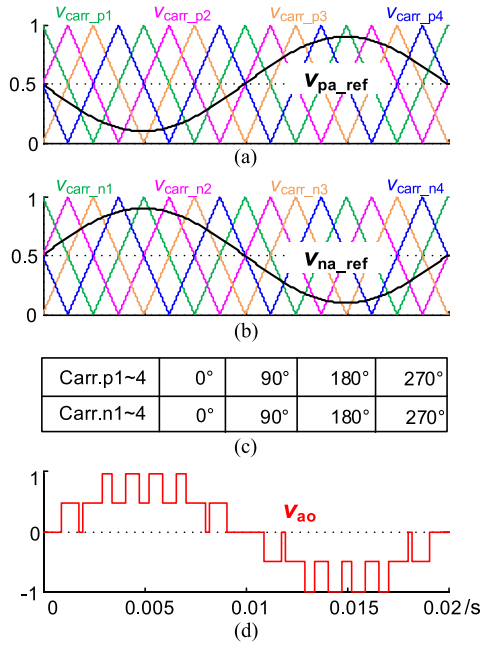

Fig. 2. "$N+1$" level CPS modulation for single-phase MMC without reserved SMs: (a) voltage references and carriers for upper four SMs (p.u.); (b) voltage references and carriers for lower four SMs (p.u.); (c) phase-shift angles for upper and lower carriers; and (d) ideal output voltage (p.u.).

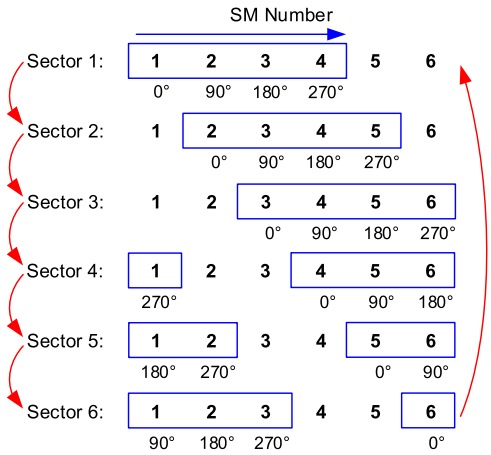

Fig. 3. Sliding choice box to select operating SMs and phase-shift angles.

shift angles of the upper and lower carriers, and the ideal "$N+1$" level output voltage waveform are demonstrated in Fig. 2.

B. Comparison of Three Possible Fault-Tolerant Methods

When the hot reserved SMs are employed, the main task of the redundancy control based on the CPS modulation is to determine the voltage reference and the phase-shift angle for each SM. As introduced in Section I, *Scheme 4* is adopted. There are three possible fault-tolerant control methods, which correspond to different voltage references and carriers.

Method A: All the SMs work in the operating mode at the same time, irrespective of whether they are reserved or not. Therefore, $N+M$ pairs of voltage references and carriers per arm are needed, and the phase-shift angle between two successive carriers is $360°/(N+M)$. Considering that there are some redundant SMs, the switching devices and the capacitors in the SMs operate in the derated condition at first (i.e., the average capacitor voltage $V_c = V_{\rm dc}/(N+M)$). Once F SMs ($F \le M$) are failed and bypassed in one arm, the number of the necessary carriers is reduced to $N+M-F$. In order to maintain less harmonics in the arm voltage, the phase-shift angle should be changed to $360°/(N+M-F)$ [25]. Moreover, the capacitor voltages of the other SMs in the faulty arm should be increased to keep the energy balanced among different arms [17], which results in the transient charging process. The updated average capacitor voltage is

$$V_c' = V_c\sqrt{\frac{N+M}{N+M-F}}\,. \tag{1}$$

Besides, when an unsymmetrical fault occurs in the upper and lower arms, MMC has to work with different number of carriers in the upper and lower arms, which will increase the high-frequency harmonics in the output voltage and the circuiting current.

Method B: All the SMs per arm also work in the operating mode at the same time. Compared with *Method A*, the difference is that through an ingenious overmodulation [22] and the mandatory control measure for the average value of the capacitor voltages (i.e., $V_c = V_{\rm dc}/N$), the devices and the capacitors can operate in the rated condition. The transient charging process can be avoided, but the unbalanced operation with the different number of carriers still exists when the unsymmetrical fault occurs.

Method C: All the SMs per arm work in the operating mode and the standby mode by turns. That is, only N, SMs are involved in the operation simultaneously, and N pairs of references and carriers per arm are needed. The devices and the capacitors work in the rated condition all the time. The seamless transition and the symmetrical operation can be realized after the failed SMs are bypassed. As long as the number of the failed SMs is not larger than the redundant SM number M, MMC can work normally without any performance deterioration.

Due to its obvious merits, *Method C* is adopted in this paper. How to realize the redundancy and the fault-tolerant control strategy is introduced in the following section.

III. Redundancy and Fault-Tolerant Control

In order to realize the fault-tolerant operation in *Method C*, the operating SMs and the phase-shift carriers should be rotated. Inspired by the sector division scheme in the space-vector PWM of two-level inverters [26], a rotating mechanism is proposed to select the operating SMs and the corresponding phase-shift angles.

A. Mechanism to Select Operating SMs and Phase-Shift Angles

For the single-phase MMC in Fig. 1(c), only four SMs per arm are required to keep MMC operate properly. Therefore, there should be two SMs per arm that work in the standby mode. In order to make the burden equally distributed in each SM, all the six SMs should alternately work in the operating mode

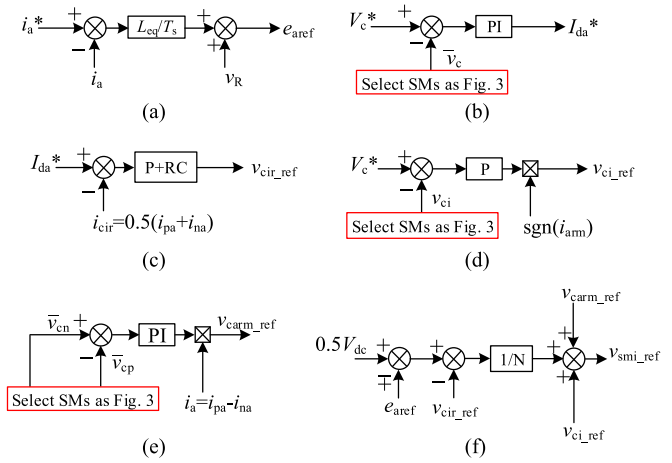

Fig. 4. Redundancy control structure of MMC: (a) output current control; (b) average capacitor voltage control; (c) circulating current suppressing control; (d) individual capacitor voltage balance control; (e) arm capacitor voltage balance control; and (f) voltage command for each SM, in which "$-e_{\mathrm{aref}}$" is for the upper SMs and "$+e_{\mathrm{aref}}$" is for the lower SMs.

and the standby mode. A sliding choice box is used to select the operating SMs and the corresponding phase-shift angles, as shown in Fig. 3. The length of the choice box is $N = 4$, and the SMs outside of the choice box are the hot reserved ones. The relative position of the phase-shift angles is fixed to the sliding choice box. The principle is introduced as follows. First, a sector is defined as a rotating period, and it can be set as one or more switching cycles. When a shorter rotating period is selected, the voltage deviation among different capacitors is smaller. In each sector, four certain SMs are chosen to be the operating SMs, and the selected SMs and their phase-shift angles will not change until the next sector. Second, the arm changes from one sector to another after a rotating period, and the sliding choice box shifts accordingly. There should be $N + M = 6$ sectors in total, and after Sector 6, the arm will return to Sector 1. Third, the chosen operating SMs will work in the PWM mode, and their capacitor voltages need to be sampled and fed back to the control system. In contrast, the unselected SMs will receive bypassing signals.

B. Redundancy Control Structure

Since the operating SMs are rotated, the conventional control strategy of MMC without reserved SMs [24] should be modified to generate the voltage references for the SMs. Fig. 4 shows the control structure for the single-phase MMC, in which the feedback of capacitor voltages are modified because of the rotating mechanism, noted by the red box. The deadbeat control is adopted in the output current control in Fig. 4(a), which is simple and accurate. The average capacitor voltage control in Fig. 4(b) guarantees the energy needed in the converter. The control in Fig. 4(c) with a repetitive controller can significantly suppress the even order harmonics of the circulating current [27], [28]. The individual and arm capacitor voltage balance controls in Fig. 4(d) and (e) make the voltage deviation among different capacitors very small. Fig. 4(f) shows the final voltage commands for the SMs, respectively, which are different for

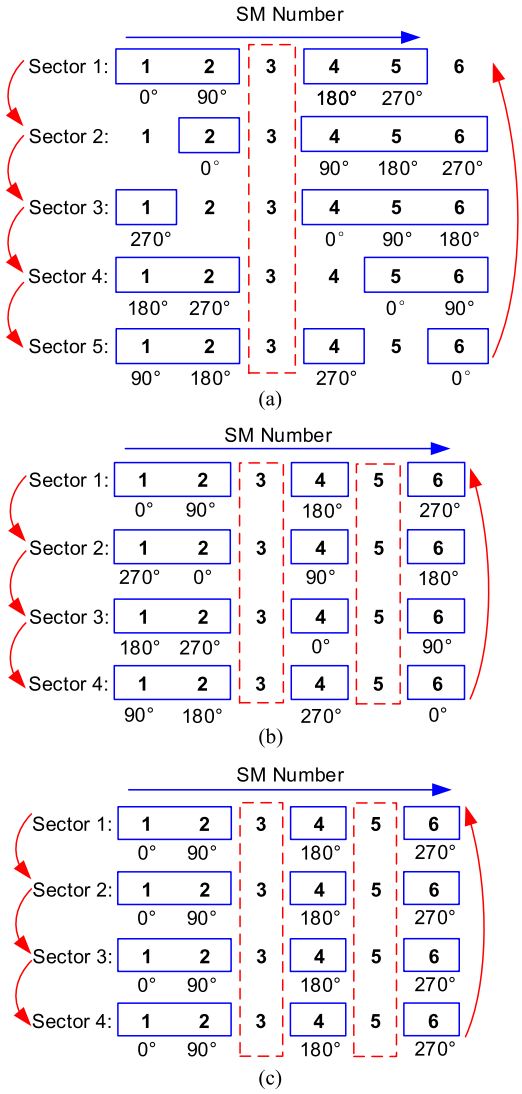

Fig. 5. Sliding choice box when some SMs are failed: (a) only the third SM is failed; (b) third and the fifth SMs both are failed, still with rotating phase-shift angles; and (c) third and fifth SMs are both failed, with constant phase-shift angles.

the upper and lower SMs. Once the voltage command and the carrier phase-shift angle for each selected SM are obtained, the gate signals for each switching device can be generated.

C. Fault-Tolerant Operation

Once one SM is failed in MMC because of the switching devices' short-circuit or open-circuit failures, the fault can be detected out and localized [8–13], and then, the failed SM should be bypassed by the circuit breaker immediately. Fig. 5(a) shows the updated sliding choice box when a fault occurs in the third SM (noted by the red dashed box). The third SM is deleted from the selecting option, and the number of total sectors reduces from six to five, but the rotating phase-shift angles in different sectors are still similar to those in Fig. 3.

Furthermore, when two SMs are failed and bypassed, there is no redundant SM. If the sliding choice box still shifts among different sectors, the phase-shift angle will keep rotating [see

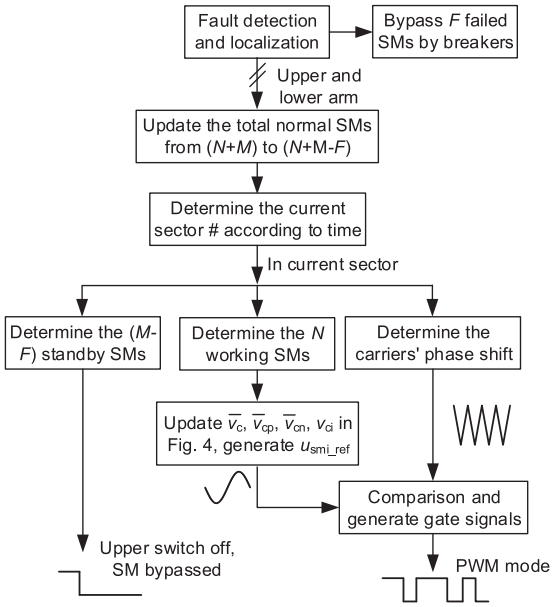

Fig. 6. Flowchart for the implementation of the fault-tolerant control.

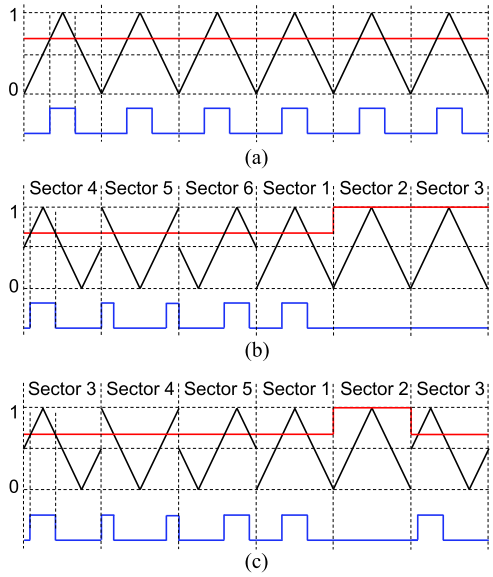

Fig. 7. Voltage reference, rotating carriers, and corresponding control signals for the first SM in the arm: (a) case without redundant SMs or with two failed SMs; (b) six healthy SMs take turns to work in the operating mode or the bypassed mode; and (c) one in the six SMs other than first SM is failed, and the other five healthy SMs take turns to operate.

Fig. 5(b)]. In fact, there is no need for the rotating phase-shift angles when the redundant SMs are used up. Therefore, when no redundant SM exists, constant phase-shift angles can be adopted in the fault-tolerant control strategy, shown in Fig. 5(c). This is just the same as the case of MMC without reserved SMs, shown in Fig. 2.

D. Implementation of Fault-Tolerant Control

The flowchart to implement the fault-tolerant control is shown in Fig. 6. Once *F* failed SMs are detected out and localized, they will be bypassed immediately. At the same time, the failed SMs will be deleted from the selecting option, and thus, the total number of normal SMs will decrease from "$N + M$" to "$N + M - F$". The total number of sectors decreases accordingly. After the fault, a new sector number can be decided, which determines the standby SMs, the operating SMs, and their corresponding carriers' phase-shift angles. Then, based on the redundancy control structure in Fig. 4, the control signals for all the SMs can be generated.

IV. Analysis of Fault-Tolerant Control Strategy

In the rotating mechanism, the length of the rotating period determines the rotating frequency among different sectors because the carriers and the operating SMs are continuously rotated, it turns out that the equivalent switching frequency, the dead time effect to MMC, and the capacitor voltage fluctuation are all influenced by the rotating period selection.

A. Equivalent Switching Frequency

For a start, a switching cycle is selected as the rotating period. The voltage reference, the triangle carriers, and the corresponding control signals for the first SM are demonstrated in Fig. 7 as an example. Since the voltage reference changes only a little in several switching cycles, it is represented by the red straight line. When the voltage reference is smaller than the carriers, a high-level control signal is generated, which means that the SM is inserted. Otherwise, the low-level control signal means that the SM is shorted out.

Fig. 7(a) shows the case of MMC without redundant SMs or with two failed SMs. The carrier of the first SM has constant 0° phase-shift angle, consistent with Figs. 2 and 5(c). On the basis of comparison, all the signal pulses are located in the middle of the sectors, one pulse per switching cycle. The case that all the six healthy SMs take turns to operate is shown in Fig. 7(b), which corresponds to Fig. 3. As the sector rotates, the carrier phase-shift angle changes among 90°, 180°, 270°, and 0°, and the first SM works in the operating mode and the standby mode by turns. It can be seen that two signal pulses are located in Sector 5, distributed in the two sides of the sector, which increases the total number of pulses. Fig. 7(c) demonstrates the case that one SM is failed and the other five healthy SMs take turns to operate, corresponding to Fig. 5(a). Similarly, there are two signal pulses in Sector 4, and the total number of pulses is also increased.

Define the equivalent switching frequency as the total switching counts per second divided by the rated number of SMs in the same arm *N*. With the hot reserved SMs and the rotating mechanism, it is obvious that the total switching counts are increased. Suppose the switching frequency of MMC without redundant SMs in Fig. 7(a) as f_s, and set the rotating period as k switching cycles. The equivalent switching frequency of MMC with hot reserved SMs can be calculated as

$$f_{\mathrm{eq}} = \frac{(N+M-F)\,m}{N \times S \times k} f_s = \frac{m}{N \times k} f_s \tag{2}$$

where "$N + M - F$" is the number of the remaining healthy SMs, "S" is the total sector number $(S = N + M - F)$, and

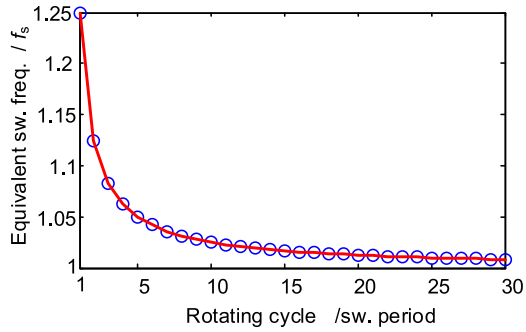

Fig. 8. Equivalent switching frequency versus length of the rotating period.

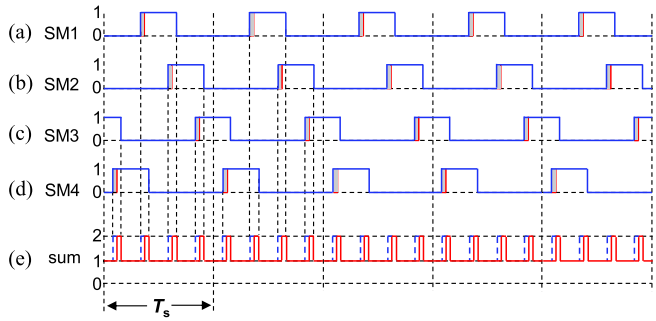

Fig. 9. Control signal pulses of MMC without reserved SMs, considering the dead time effect: (a)–(d) correspond to the control signals of SM1–4, respectively; and (e) sum of the four signal pulses.

"m" is the switching counts of one healthy SM during the S sectors.

For Fig. 7(b) and (c), k equals 1, S equals 6 and 5, respectively, and m equals 5 for both cases. It can be easily derived that $f_{\rm eq}$ equals $1.25f_{\rm s}$. Based on (2), the relationship between the equivalent switching frequency and the length of the rotating period can be depicted in Fig. 8. It can be concluded that a longer rotating period corresponds to the lower equivalent switching frequency and thus, lower total switching loss.

B. Dead Time Effect

The rotating period selection not only affects the equivalent switching frequency of MMC, but also influences the arm voltage through the dead time effect. Since the output voltage of MMC is determined by the difference between the lower and upper arm voltages [29], the rotating period selection has impacts on the output voltage indirectly. For later comparison, the control pulses of MMC without reserved SMs are illustrated in Fig. 9. The dead time setup that the leading edge is delayed a little (noted by the gray shadow) is taken into account in the signal pulses. The sum of the four control signal pulses is also provided, which can represent the arm voltage to some extent.

Take the case with one failed SM in Fig. 5(a) as an example, the influence of dead time is illustrated in Fig. 10, in which the switching cycle is also selected as the rotating period. Fig. 10(a)–(e) correspond to the control signals for the remaining healthy SMs, namely SM1, SM2, SM4, SM5, and SM6. Fig. 10(f) represents the sum of the five signal pulses. It can be

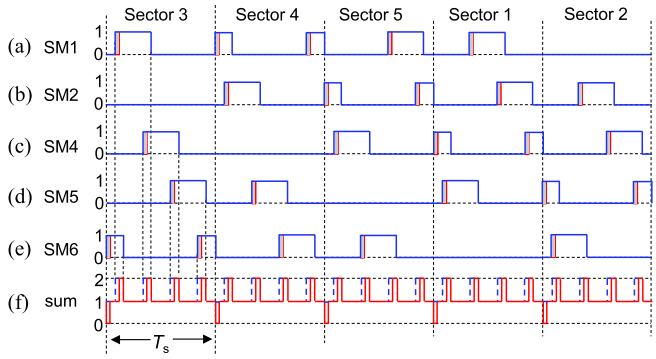

Fig. 10. Control signal pulses for the case in Fig. 5(a) considering the dead time effect: (a)–(e) correspond to the control signal pulses of SM1, SM2, SM4, SM5, and SM6, respectively; and (f) sum of the five signal pulses.

seen that when the sector shifts from Sector 3 to Sector 4, SM1 and SM6 have the simultaneous switching with SM1 inserted and SM6 bypassed at the same time. Thus, due to the dead time effect, a mismatch pulse with a lower level in Fig. 10(f) is generated, compared with Fig. 9(e). This will cause mismatch pulses in the arm voltage, and further influence the output voltage and current. Furthermore, the mismatch pulses will appear in every sector switching moment. Since they are caused by the simultaneous switching, they cannot be eliminated by the conventional dead time compensation methods. Fortunately, the longer rotating period can reduce the occurrence of the mismatch pulses. When a line cycle is selected as the rotating period, the mismatch pulse appears only once every line cycle, and the effect can be neglected.

Considering the requirement to reduce the equivalent switching frequency and to decrease the impact of the mismatch pulses, a longer rotating period is preferred. Moreover, the capacitor voltage has the line frequency ripple in MMC. When an integer multiple of the line cycle is set as the rotating period, the dynamic performance of the capacitor voltage will be better than that with a fractional multiple of the line cycle. From the above statements, setting one or several line cycles as the rotating period is more suitable.

C. Capacitor Voltage Fluctuation

With the proposed fault-tolerant control strategy, the capacitor voltage fluctuation is analyzed as follows. The derivation is also based on the single-phase MMC in Fig. 1(c).

First, the switching cycle is set as the rotating period. The relationship among the two arm currents, the output current, and the circulating current is

$$\begin{cases} i_a = i_{\rm pa} - i_{\rm na} \\ i_{cir} = 0.5\left(i_{\rm pa} + i_{\rm na}\right) \end{cases}. \tag{3}$$

Consider that the active power is balanced between the dc input and the ac output, that is

$$V_{\rm dc} I_{\rm da} = R_{\rm load} {I_a}^2 \tag{4}$$

where $I_{\rm da}$ represents the input dc current and I_a denotes the RMS value of the output ac current.

With the perfect control effect, the actual output current is assumed just the same as the current reference. Once the output current reference is given, the actual output current can be given as i_a*. Thereby, its RMS value can be calculated out. Through (4), the input dc current can be determined as $I_{\rm da}*$. Then, considering that the ac circulating current harmonics can be fully eliminated, the expressions of the actual arm currents can be given as

$$\begin{cases} i_{\rm pa} = I_{\rm da}* + 0.5 i_a* \\ i_{\rm na} = I_{\rm da}* - 0.5 i_a* \end{cases}. \tag{5}$$

Define the average switching functions of the upper and the lower SMs as $d_{\rm pa}$ and $d_{\rm na}$, which are generated by the closed-loop control algorithm and are unknown items. Then, the relationship between the two arm currents and the capacitor voltages is

$$\begin{cases} N d_{\rm pa} i_{\rm pa} = (N + M - F_p)\, C \dfrac{dv_{\rm cpa}}{dt} \\ N d_{\rm na} i_{\rm na} = (N + M - F_n)\, C \dfrac{dv_{\rm cna}}{dt} \end{cases} \tag{6}$$

where F_p and F_n are the number of the bypassed failed SMs per arm. It means that although only *N* SMs are working in the operating mode, but the total charging currents are shared by $N + M - F_p$ or $N + M - F_n$ capacitors. All the capacitor voltages in the same arm are considered the same, represented by $v_{\rm cpa}$ and $v_{\rm cna}$, respectively.

According to the MMC shown in Fig. 1(c), the relationship between the capacitor voltages and the output voltage can be expressed as

$$\begin{cases} N d_{\rm pa} v_{\rm cpa} = \dfrac{1}{2} V_{\rm dc} - v_{\rm ao} - \dfrac{1}{2} L_{\rm arm} \dfrac{di_{\rm cir}}{dt} \\ N d_{\rm na} v_{\rm cna} = \dfrac{1}{2} V_{\rm dc} + v_{\rm ao} - \dfrac{1}{2} L_{\rm arm} \dfrac{di_{\rm cir}}{dt} \end{cases} \tag{7}$$

where $v_{\rm ao}$ represents the actual output voltage. With a given output current reference, the output voltage can be derived as $v_{\rm ao}*$. Besides, the items related to ${\rm d}i_{\rm cir}/{\rm d}t$ can be eliminated because the ac circulating current can be fully suppressed ideally.

Eliminating the unknown items $d_{\rm pa}$ and $d_{\rm na}$ from (6) and (7) and substituting the arm currents in (5), the square of the instantaneous capacitor voltages can be expressed as

$$\begin{cases} {v_{\rm cpa}}^2 = \frac{2}{C(N+M-F_p)} \int_0^t \left(I_{\rm da}* + \frac{1}{2} i_a*\right) \left(\frac{V_{\rm dc}}{2} - v_{\rm ao}*\right) dt \\ \qquad + {V_{\rm cpa0}}^2 \\ {v_{\rm cna}}^2 = \frac{2}{C(N+M-F_n)} \int_0^t \left(I_{\rm da}* - \frac{1}{2} i_a*\right) \left(\frac{V_{\rm dc}}{2} + v_{\rm ao}*\right) dt \\ \qquad + {V_{\rm cna0}}^2 \end{cases} \tag{8}$$

where $V_{\rm cpa0}^2$ and $V_{\rm cna0}^2$ are the integration initial values of $v_{\rm cpa}^2$ and $v_{\rm cna}^2$, undetermined items. Expanding the integral items in the equations, merging the dc items and the ac items, respectively, we can get

$$\begin{cases} {v_{\rm cpa}}^2 = \underline{E_{\rm cp\_dc}} + e_{\rm cp\_ac} + \underline{{V_{\rm cpa0}}^2} \\ {v_{\rm cna}}^2 = \underline{E_{\rm cn\_dc}} + e_{\rm cn\_ac} + \underline{{V_{\rm cna0}}^2} \end{cases} \tag{9}$$

where $E_{\rm cp\_dc}$ and $E_{\rm cn\_dc}$ represent the dc parts of the integral items, and the ac parts noted by $e_{\rm cp\_ac}$ and $e_{\rm cn\_ac}$, respectively. The sum of underlined items in each equation represents the average value of the capacitor voltage square, which is in fact the square of the RMS value of the capacitor voltage. Since the capacitors of MMC are often selected to make the voltage ripple beneath 5% [30], the square value of the capacitor RMS voltage can be approximated by the square of the average capacitor voltage (error $\leq 0.25\%$). Moreover, because only *N* SMs per arm work in the operating mode all the time, the average value of the capacitor voltages is $V_{\rm dc}/N$. Thus, the expressions of the capacitor voltages can be derived as

$$\begin{cases} v_{\rm cpa} \approx \sqrt{\left(\frac{V_{\rm dc}}{N}\right)^2 + e_{\rm cp\_ac}} \\ v_{\rm cna} \approx \sqrt{\left(\frac{V_{\rm dc}}{N}\right)^2 + e_{\rm cn\_ac}} \end{cases}. \tag{10}$$

The above derivation process of the capacitor voltage expression is more reasonable and accurate [31] than that based on a given duty cycle, which is adopted a lot in the literature [14], [32]. From (8), it can be seen that when the switching cycle is selected as the rotating period, with more hot reserved SMs, the capacitor voltage fluctuation will be smaller.

Second, the line cycle is set as the rotating period. Under this condition, the capacitor voltage difference between the operating SMs and the standby SMs is too large to be ignored. In one entire line cycle, the capacitor voltages of the standby SMs are kept constant, and only the other *N* capacitors have energy fluctuations. Thus, the total charging currents in (6) are shared by *N* capacitors. Therefore, the expressions in (8) should be modified as

$$\begin{cases} {v_{\rm cpa}}^2 = \frac{2}{CN} \int_0^t \left(I_{\rm da}* + \frac{1}{2} i_a*\right) \left(\frac{V_{\rm dc}}{2} - v_{\rm ao}*\right) dt + {V_{\rm cpa0}}^2 \\ {v_{\rm cna}}^2 = \frac{2}{CN} \int_0^t \left(I_{\rm da}* - \frac{1}{2} i_a*\right) \left(\frac{V_{\rm dc}}{2} + v_{\rm ao}*\right) dt + {V_{\rm cna0}}^2 \end{cases}. \tag{11}$$

There is no item *M*, F_p or F_n in (11), which means that when the hot reserved SMs are adopted, the capacitor voltage fluctuations of the operating SMs are still the same as those of MMC without any reserved SMs.

Third, a comparison of the capacitor voltage fluctuations with the two rotating periods is provided. When a switching cycle is selected, the peak-to-peak value of the capacitor voltage fluctuation is smaller than that with the line frequency rotating. But when a line cycle is set as the rotating period, the benefit is that all the capacitors operate for *N* line cycles, and then "relax" for $M - F$ line cycles, which means fewer charging and discharging times than those with the switching frequency rotating. It is hard to say which arrangement of the rotating period is better for the capacitors, and the two tie the game from this aspect.

D. Another Rotating Mechanism to Select Phase-Shift Angles

Considering that all the carrier phase-shift angles of the operating SMs should be modified once the sector switches in Figs. 3 and 5, another rotating mechanism is proposed to reduce the total switching counts. The modified version of Fig. 3 is shown in Fig. 11 as an example. The relative position of the phase-shift angles is not fixed to the choice box. It can be seen that the new

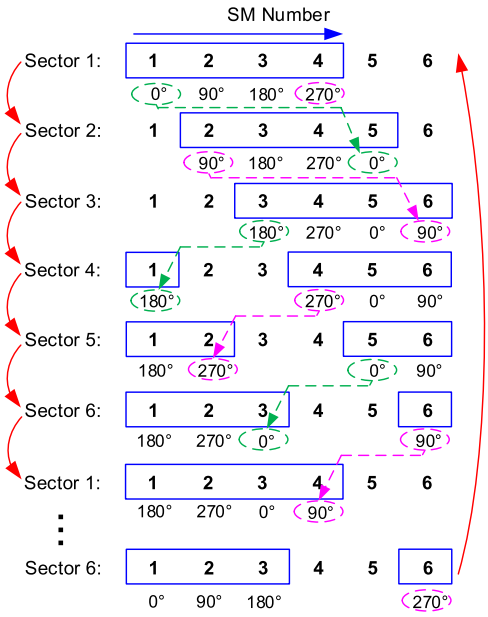

Fig. 11. Another mechanism to select operating SMs and phase-shift angles.

SM which slides into the choice box takes over the phase-shift angle of the SM which slides out of the choice box, and the phase-shift angles of the other operating SMs are kept invariant. For example, when the sector changes from 1 to 2, SM5 is the new SM which slides into the choice box, and it takes over the phase-shift angle of 0°. In contrast, the phase-shift angles of SM2, SM3, and SM4 do not change. Through this new rotating mechanism, the phase-shift angle of a certain SM changes only once every $N = 4$ sectors, so the equivalent switching frequency of MMC is reduced compared with the previous rotating mechanism.

For the same sector (e.g., Sector 1) in Fig. 11, the selected operating SMs are the same, but the corresponding phase-shift angles can be different, especially when some SMs are failed. It means that the relationship between the phase-shift angles and the sector number is not fixed. The implementation of this rotating mechanism involves passing the phase-shift angle from one SM to another, which brings some difficulties in practice. Moreover, when the line cycle is set as the rotating period, the effect of decreasing the equivalent switching frequency and the mismatch pulses is not that obvious. Therefore, this rotating mechanism is not a better choice compared with that mentioned in Section III.

V. Simulation and Experimental Verification

Two simulation cases in MATLAB/ Simulink and the experiments based a downscaled MMC prototype are conducted to verify the proposed redundancy and fault-tolerant control strategy based on the CPS modulation.

A. Simulation Case I

The single-phase MMC with six SMs per arm (see Fig. 1) is chosen for simulation, and the parameters are listed in Table I,

TABLE I
Parameters of the Single-Phase MMC Prototype

Parameters	Values	Parameters	Values
DC-link voltage	$V_{\rm dc} = 300$ V	Device's dead time	DT $= 3.125\,\mu$s
No. of rated SMs per arm	$N = 4$	Rotating period	$T_{\rm RPI} = 1/5000$ s
No. of reserved SMs per arm	$M = 2$		$T_{\rm RPII} = 0.02$ s
SM rated cap. voltage	$V_c = 75$ V	Output ac current control	$k_p\_i_a = 20$
Center-tapped arm inductor	$L_{\rm arm} = 2.5$ mH	Average capacitor voltage control	$k_p\_v_{\rm cave} = 0.1$
SM capacitance	$C = 3280\,\mu F$		$k_i\_v_{\rm cave} = 25$
Load inductance	$L_{\rm Load} = 1$ mH	P + RC circulating current control	$k_p\_i_{\rm cira} = 25/8$
Load resistance	$R_{\rm Load} = 12\,\Omega$		$k_{\rm rc}\_i_{\rm cira} = 1.5$
Output ac current (RMS)	$I_a = 7.2$ A	Individual cap. voltage control	$k_p\_v_{\rm ci} = 0.3$
Carrier frequency	$f_s = 5000$ Hz	Upper/ lower arm voltage balance control	$k_p\_v_{\rm carm} = 0.01$
Line frequency	$f_0 = 50$ Hz		$k_i\_v_{\rm carm} = 1$

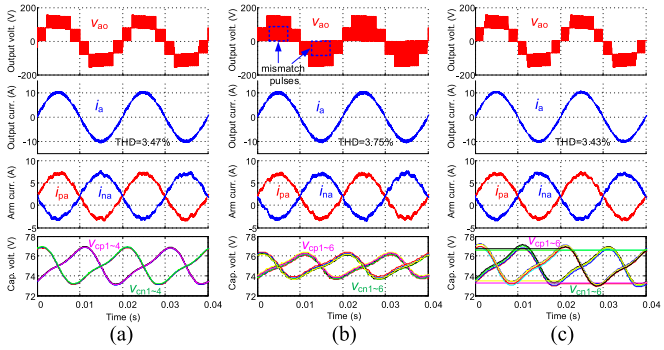

Fig. 12. Steady-state waveforms of the output voltage, the output current, the two arm currents, and the capacitor voltages of MMC: (a) without redundant SMs; (b) with two hot reserved SMs per arm, switching frequency rotating; and (c) with two hot reserved SMs per arm, line frequency rotating.

in which the switching cycle and the line cycle are selected as the rotating periods, respectively.

The steady-state waveforms of MMC with and without reserved SMs are provided in Fig. 12. The $N + 1$ level output voltage, the output current, the arm currents, and the capacitor voltages of MMC without reserved SMs are shown in Fig. 12(a). Since, the ac circulating current is almost fully suppressed, the waveforms of the two arm currents are close to sinusoidal waves. Because of the capacitor voltage balance control, the deviations among different capacitor voltages are very small. For comparison, the waveforms of MMC with two hot reserved SMs are shown in Fig. 12(b) and (c), and the switching cycle and the line cycle are selected as the rotating period, respectively. In Fig. 12(b), some mismatch pulses appear in the output voltage waveform. In fact, the mismatch pulse appears once in every switching cycle, which is caused by the dead time effect. Due to the mismatch pulses, the output current is deteriorated slightly and the Total Harmonic Distribution (THD) is also increased, compared with Fig. 12(a). However, when the line cycle is set as the rotating period, the mismatch pulse appears only once every line cycle, and they

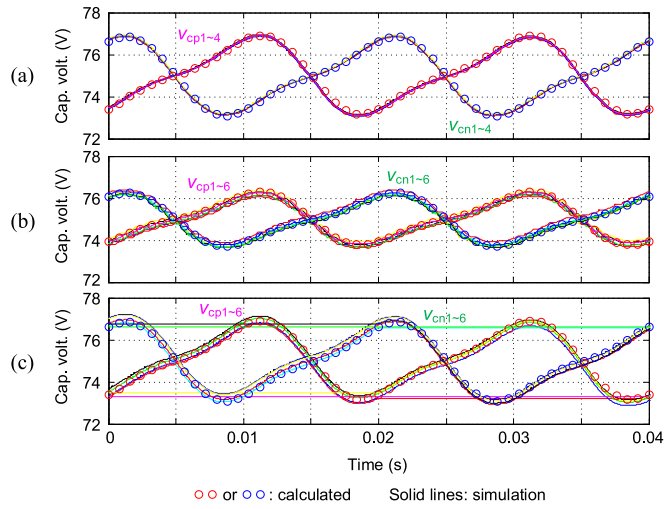

Fig. 13. Comparison of the theoretical analysis and the simulation waveforms of the capacitor voltages of MMC: (a) without redundant SMs; (b) with two hot reserved SMs per arm, switching frequency rotating; and (c) with two hot reserved SMs per arm, line frequency rotating.

are hardly visible in the output voltage waveform in Fig. 12(c). The output current is also improved, compared with that in Fig. 12(b). These conclusions are consistent with the analysis in Section IV-B.

As to the arm currents in Fig. 12, the waveforms are similar for all the three cases, which demonstrates the effectiveness of the suppressing circulating current control in the redundancy control strategy. Then for the capacitor voltage waveforms, the fluctuation is reduced in Fig. 12(b), but the differences among different capacitor voltages are increased, compared with Fig. 12(a). When the line cycle is set as the rotating period, the capacitor voltage fluctuation of the operating SMs in Fig. 12(c) is similar to that in Fig. 12(a), but the capacitor voltage deviations are increased. For MMC with some hot reserved SMs, one SM works in the operating mode for N sectors, then "relaxes" for $M - F$ sectors. Therefore, the larger capacitor voltage deviations are reasonable compared with that of MMC with continuously operating SMs.

On account of the capacitor voltage fluctuation, Section IV-C has provided the expressions for the three cases. A comparison of the theoretical analysis and the simulation waveforms of the capacitor voltages is illustrated in Fig. 13. It can be observed that the calculated waveforms match the simulation waveforms very well, which verifies the correctness of the analysis.

In order to verify the feasibility of the fault-tolerant operation of MMC with hot reserved SMs, a scenario with several successive faults is designed in Fig. 14. At t_1, the third SM in the upper arm is failed; at t_2, the fifth and sixth SMs in the lower arm are failed at the same time; and at t_3, the fifth SM in the upper arm is failed. The catastrophic faults such as the IGBT short-circuit failure are first considered in the simulations, while the nonurgent faults such as the IGBT open-circuit failure will be considered in the later experiments. When some catastrophic faults occur in the SMs, they should be dealt with immediately and the failed SMs need to be bypassed as soon as possible (e.g., within 10 μs). Therefore, the fault-detection time can be

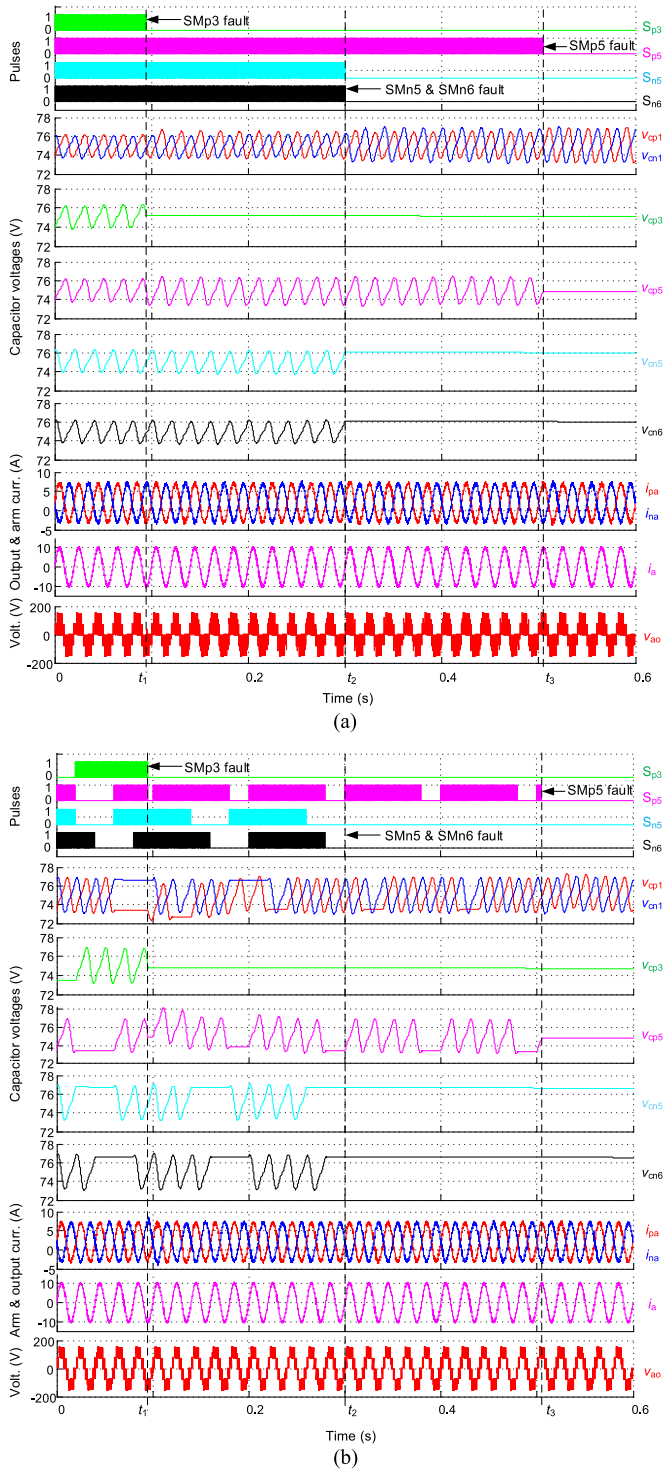

Fig. 14. Scenario of the fault-tolerant operation of MMC when some catastrophic faults occur in the SMs: (a) with the switching frequency rotating; and (b) with the line frequency rotating.

neglected in this condition, which means that the fault occurrence and bypassing the failed SMs occur simultaneously in the simulations.

The fault-tolerant operation waveforms of MMC with the switching frequency rotating and the line frequency rotating are demonstrated in Fig. 14(a) and (b), respectively. The pulses of

the SMs in Fig. 14 refer to the control signals of the upper switches in the half-bridge SMs. Once the pulse of a certain SM is kept at the low level all the time, it means that the SM is bypassed permanently. Fig. 14 shows the capacitor voltage waveforms of the failed SMs, including SMp3, SMp5, SMn5, and SMn6. The capacitor voltages vary little after the faults because once the failed SMs are bypassed, the capacitors will be discharged slowly through the paralleled bleeder resistors. For comparison, the capacitor voltage waveforms of SMp1 and SMn1 are given as well, which represent those of the normal SMs. The scenario in Fig. 14(a) is analyzed first. Before t_1, all the 12 SMs are healthy, and the steady-state waveforms are just the same as those in Fig. 12(b). At t_1, the failed SMp3 is bypassed immediately, and then the capacitor voltage of SMp3 changes little, nearly invariable. The number of the healthy SMs in the upper arm is reduced from six to five, which makes the capacitor voltage fluctuation increased compared with that in the lower arm. At t_2, the failed SMn5 and SMn6 are bypassed at the same time, which brings higher capacitor voltage ripple in the lower arm. At t_3, the failed SMp5 is bypassed, which means all the hot reserved SMs are used up. The capacitor voltage fluctuations of SMp1 and SMn1 are symmetrical again.

Although the line cycle is set as the rotating period in Fig. 14(b), the waveforms of the arm currents and the output current are still similar as Fig. 14(a). From the pulses and the capacitor voltage waveforms in Fig. 14(b), the feature with the line frequency rotating is obvious that the capacitors operate for *N* line cycles and then "relax" for several line cycles. Moreover, the mismatch pulses in the output voltage are greatly reduced, nearly invisible. Comparing Fig. 14(a) and (b) and considering the undesirable mismatch pulses in the output voltage, the line frequency rotating is preferred. It can be pointed out that when the failed SMs are bypassed immediately, whether the switching cycle or the line cycle is set as the rotating period, MMC can work normally even when all the redundant SMs are failed. On account of the transient process of the fault-recovery, the case with the switching frequency rotating seems better, but the line frequency rotating case is still acceptable, with very short recovery time.

Then, based on the waveforms in Fig. 14(b), the benefit and the compromise of the proposed control strategy are analyzed. Since all the SMs, including the hot reserved SMs, take turns to operate and standby, the evenly distributed burden for each SM can be achieved on a relatively large time-scale (e.g., dozens of line cycles), which is the major benefit of the proposed method. Furthermore, the average burden of each SM and thus, the average IGBT junction temperature will be decreased, compared with that of MMC without reserved SMs. On the other hand, from the control pulses in Fig. 14(b), it can be seen that each SM operates for a period and then idles for a while such as a kind of "burst-mode". In this condition, the power loss of each device will not be evenly distributed on the relatively small time-scale. That means although the average IGBT junction temperature is decreased, each device might experience larger IGBT junction temperature ripple. Anyway, the benefit of the proposed fault-tolerant control strategy is truly compromised by the above-mentioned reasons.

TABLE II
PARAMETERS OF THE THREE-PHASE GRID-CONNECTED MMC FOR SIMULATION

Parameters	Values	Parameters	Values
DC-link voltage	$V_{\rm dc} = 40$ kV	Device's dead time	DT $= 5\ \mu$s
No. of working SMs per arm	$N = 20$	Rotating period	$T_{\rm RP} = 0.02$ s
No. of redundant SMs per arm	$M = 4$	Output ac current control	$k_p\_i_a = 60$
SM rated capacitor voltage	$V_c = 2000$ V		$k_i\_i_a = 200$
Center-tapped arm inductor	$L_{\rm arm} = 20$ mH	Average capacitor voltage control	$k_p\_v_{\rm cave} = 0.2$
SM capacitance	$C = 5$ mF		$k_i\_v_{\rm cave} = 20$
Grid line-to-line volt. (RMS)	$V_{s\_ll} = 23$ kV	P + RC circulating current control	$k_p\_i_{\rm cira} = 25$
Output filter inductance	$L_{\rm Load} = 5$ mH		$k_{\rm rc}\_i_{\rm cira} = 5$
Output ac current (RMS)	$I_a = 753$ A	Individual capacitor voltage control	$k_p\_v_{\rm ci} = 0.25$
Carrier frequency	$f_s = 400$ Hz	Upper/ lower arm voltage balance control	$k_p\_v_{\rm carm} = 0.5$
Line frequency	$f_0 = 50$ Hz		$k_i\_v_{\rm carm} = 0.005$

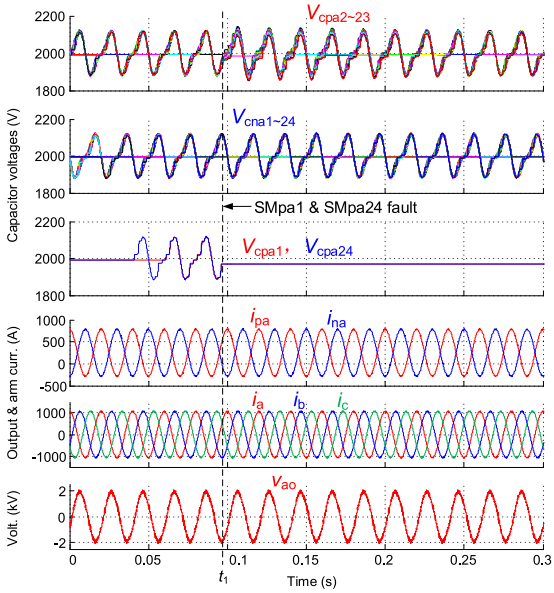

Fig. 15. Fault-tolerant operation waveforms of the three-phase grid-connected MMC.

B. Simulation Case II

In order to test whether the proposed control strategy is applicable in the MMC with a large number of SMs and a very low carrier frequency, the simulations of a realistic case are provided. Take the three-phase grid-connected MMC as an example, and the parameters are listed in Table II. There are total 24 SMs per arm, including four hot reserved SMs. The carrier frequency is selected as 400 Hz, and only the line frequency rotating case is focused on in this simulation.

Fig. 15 demonstrates the simulation waveforms of MMC, including the capacitor voltages, the arm currents of phase *a*, the three-phase output currents, and the output voltage of phase *a*. At first, there is no fault. The waveforms of the arm currents, the output currents, and the output voltage are close to the sinusoidal

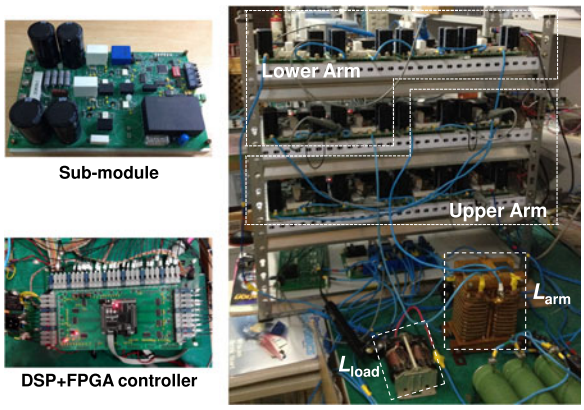

Fig. 16. Picture of the single-phase downscaled MMC prototype.

waves. From the capacitor voltages of v_{cpa1} and v_{cpa24}, it can be seen that the SMs take turns to operate and standby. Since the capacitors discharge only a little during the standby mode, the capacitor voltages are still well balanced. Then, at t_1, the 1st and the 24th SMs in the upper arm of phase *a* are failed and bypassed at the same time. The other capacitor voltages in the upper arm experience a short transient fault-recovery process, and then return to normal. Moreover, the waveforms of the output currents and the output voltage are nearly not affected by the fault-tolerant operation.

From the above waveforms, it can be concluded that the proposed fault-tolerant control strategy is still effective for the realistic case with a large number of SMs and a very low carrier frequency.

C. Experimental Results

To verify the proposed control strategy experimentally, a single-phase MMC prototype is built, with the same circuit parameters tabulated in Table I. The photograph of this prototype is shown in Fig. 16. The TMS320F28335 DSP is used as the system-level controller, which executes the fault-tolerant control algorithms and the generation of PWM signals. An EP4CE15F17C8N Field-Programmable Gate Array (FPGA) is adopted as the interface between the DSP controller and the SMs. The capacitor voltages of all the 12 SMs are collected and transferred to DSP via the FPGA, while the PWM signals generated by the DSP are distributed to the SMs by the FGPA via the optical fibers.

The steady-state waveforms of MMC with two hot reserved SMs per arm are shown in Fig. 17. One switching cycle is set as the rotating period in Fig. 17(a), and a line cycle as the rotating period in Fig. 17(b). The capacitor voltages of three upper SMs (SMp1, SMp3, and SMp5) and three lower SMs (SMn1, SMn5, and SMn6) are shown as the representatives. The upper and lower arm currents, the output current, and output voltage waveforms are also displayed. From Section III-A, it can be concluded that when there is no failed SMs in the arm, the six SMs alternately work in the operating mode for four sectors, and then in the standby mode for two sectors. Thus, when the six SMs rotate with the switching frequency, the capacitor voltages

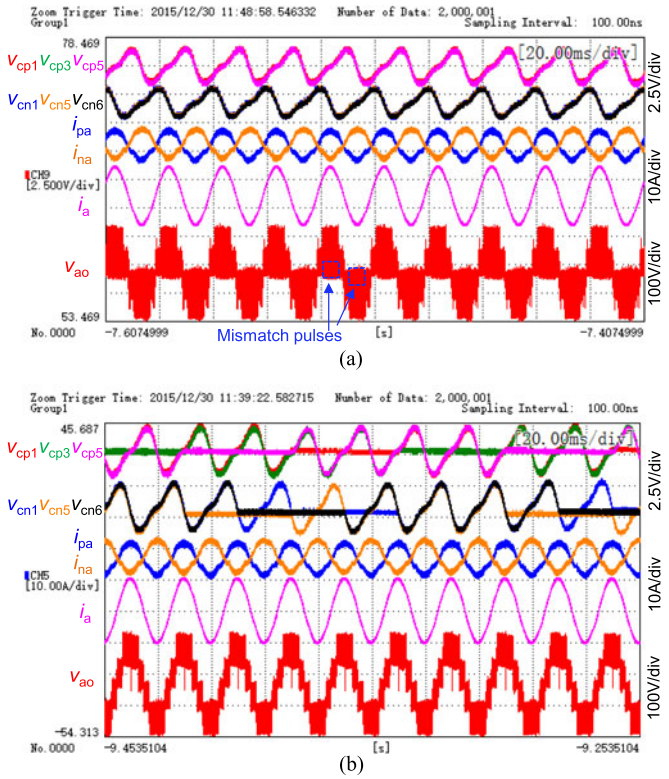

Fig. 17. Steady-state waveforms of the capacitor voltages, the arm currents, the output current, and the output voltage: (a) one switching cycle as the rotating period; and (b) one line cycle as the rotating period.

do not separate dramatically. In other words, they are still well balanced, just as shown in Fig. 17(a). In contrast, when the SMs rotate with the line frequency, the capacitors are being charged or discharged for four line cycles, and then, in the standby mode for two line cycles. Since, the resistance of the paralleled bleeder resistor is very large, the capacitor voltage will decrease very slowly when bypassed. Therefore, the capacitor voltage can almost be seen as constant when working in the standby mode, just as shown in Fig. 17(b). Compared with similar arm currents and output current waveforms, the output voltage waveforms are different in the two cases. With the line frequency rotating, the mismatch pulses in the output voltage waveforms are almost eliminated, just the same as the pervious theoretical analysis and simulation waveforms.

A similar scenario as that in the simulation case I is used to examine the fault-tolerant capability of the proposed control strategy. The upper switch's open-circuit failure, a nonurgent fault [7–13], is chosen as the SM's failure cause, with the fault-detection time about 80 ms [11]. When a series of faults occur in different SMs, the fault-tolerant operation waveforms are demonstrated in Figs. 18 and 19, with the switching frequency rotating and the line frequency rotating, respectively.

First, consider the case with the switching frequency rotating. Fig. 18(a) shows the transient waveforms when the third SM in the upper arm is failed. At t_1, the upper switch in SMp3 has an open-circuit failure. After that, the capacitor voltages will increase [7] until the fault is detected, localized, and bypassed at t_2. Then, SMp3 is deleted from the selecting option [just as Fig.

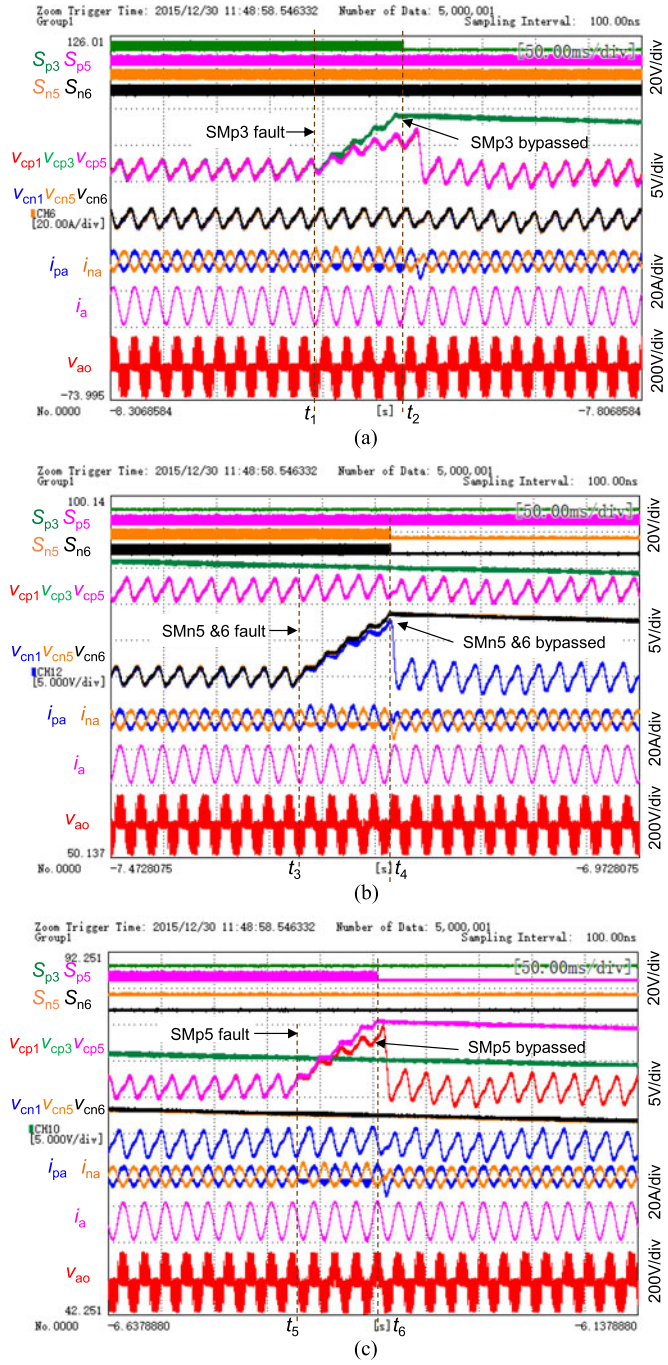

Fig. 18. With switching frequency rotating, fault-tolerant operation waveforms of the control signals, the capacitor voltages, the two arm currents, the output current, and the output voltage: (a) at t_1, SMp3 is failed; at t_2, it is bypassed; (b) at t_3, SMn5 and SMn6 are failed simultaneously; at t_4, they are bypassed; and (c) at t_5, SMp5 is failed; at t_6, it is bypassed.

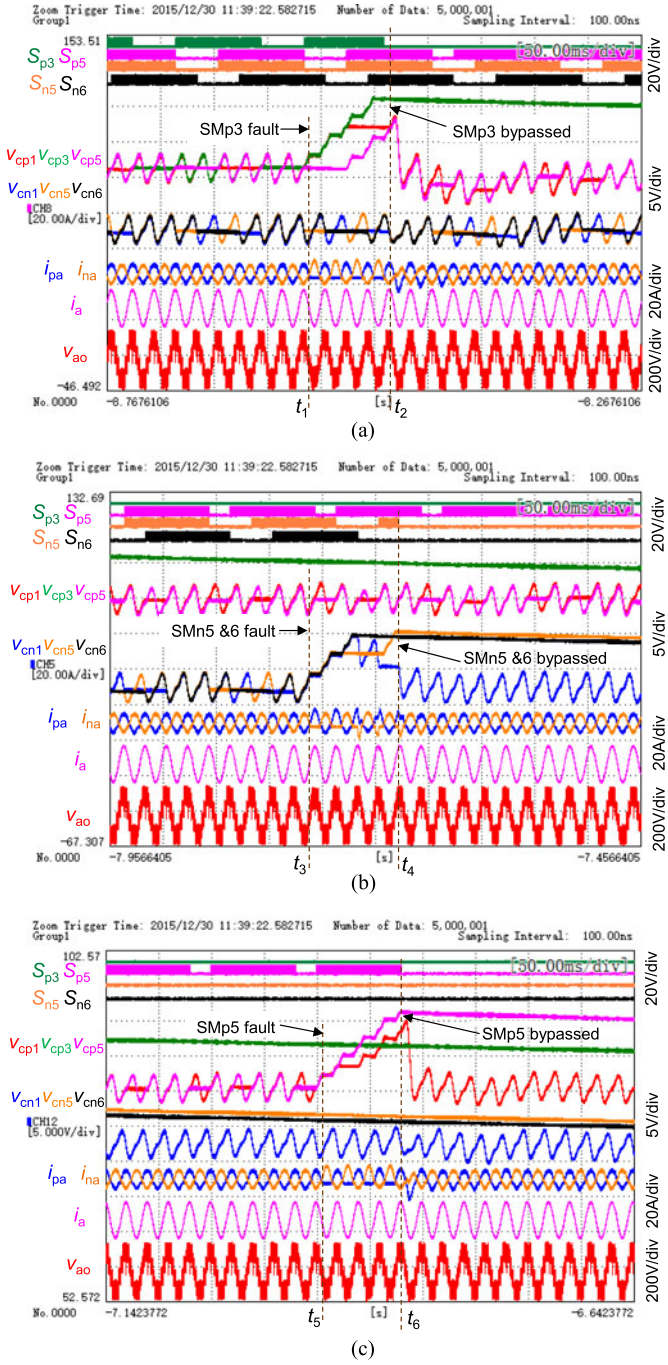

Fig. 19. With line frequency rotating, fault-tolerant operation waveforms of the control signals, the capacitor voltages, the arm currents, the output current, and the output voltage: (a) at t_1, SMp3 fault; at t_2, it is bypassed; (b) at t_3, SMn5 and SMn6 fault simultaneously; at t_4, they are bypassed; and (c) at t_5, SMp5 fault; at t_6, it is bypassed.

5(a)]. The control signal of SMp3 changing to the low level can be seen as a flag of quitting the rotating mechanism. At the same time, the four operating SMs are selected from the remaining five healthy SMs through the rotating mechanism. Then, the capacitor voltages of the healthy SMs (v_{cp1}, v_{cp5}, v_{cn1}, v_{cn5}, and v_{cn6}) in Fig. 18(a) and the arm current waveforms return to normal with very short recovery time, while the bypassed capacitor discharges slowly through the bleeder resistor. The transient waveforms of the output current and the output voltage during the fault are similar as those in the normal condition, which illustrates the fault-detection stage and the fault-recovery stage have only a little impact on them.

Fig. 18(b) illustrates the subsequent waveforms when the open-circuit failures occur in SMn5 and SMn6 simultaneously. This fault can be regarded as the worst case in reality, and it can be ridden through as well in Fig. 18(b). After SMp3, SMn5, and

SMn6 are all failed and bypassed, the waveforms in Fig. 18(c) show the case when the last remaining redundant SM is failed.

With the same fault scenario, the fault-tolerant operation waveforms of MMC with the line frequency rotating are shown in Fig. 19. The feature that the SMs in MMC take turns to work in the operating mode and the standby mode can also be reflected from the control signals and the capacitor voltage waveforms. All the capacitor voltages and the arm currents are similar to those in Fig. 18, deteriorated greatly in the fault-detection stage. In contrast, the output current and the output voltage are only affected slightly. It means that with the line frequency rotating, the nonurgent faults can also be ridden through with very good output waveforms. Furthermore, the distorted waveforms of the two arm currents and the capacitor voltages mainly happen in the fault-detection stage. Once the failed SMs are detected out and the fault-tolerant strategy is activated, the fault-recovery stage is very short and the transition process is relatively smooth, without very long transient time. Compared with Fig. 18, the mismatch pulses in the output voltage waveform are also greatly reduced with the line frequency rotating, as expected.

From Figs. 18 and 19, it can be concluded that with the proposed fault-tolerant control strategy, MMC can realize the fault ride-through even when all the redundant SMs are failed, and the dynamic transition during the fault-recovery stage is short and smooth, only with a very small fluctuation. This confirms the fault-tolerant capability and the seamless transition of MMC after the faults are detected out. Considering the benefits of less switching loss and fewer mismatch pulses, the arrangement with the line frequency rotating is a better choice.

VI. Conclusion

A redundancy and fault-tolerant control strategy for MMC with the hot reserved SMs based on the CPS modulation has been proposed in this paper. Through bypassing the failed SMs and deleting them from the selecting option, the faults of MMC can be ridden through with a nearly seamless transition. The main merits of the proposed strategy include the following:

1) the equal burden of each SM is achieved by setting all the SMs work in the operating mode and the standby mode in turns;
2) the hot reserved SMs can simultaneously replace the bypassed failed SMs, and the transient inrush charging current is avoided;
3) MMC can operate symmetrically even when the unsymmetrical faults occur, the odd order circulating currents, and the corresponding issues can be avoided;
4) the transient process, after the failed SMs are bypassed, have very short recovery time, almost negligible compared with the deterioration in the fault-detection stage;
5) through the proposed mechanism with the line frequency rotating, the switching loss and the mismatch pulses can be kept within an acceptable level, compared with MMC without redundant SMs.

Simulation and experimental results have confirmed the feasibility and effectiveness of the proposed control strategy.

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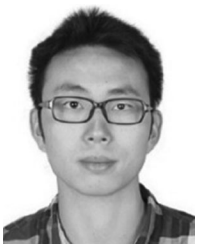

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