An Optimal Digital Pulse-Width-Modulated Dither Technique to Enhance the Resolution of High-Frequency Power Converters

Jingyang Fang, *Student Member, IEEE*, Xu Yang, *Member, IEEE*, Lei Zhang, *Member, IEEE*, and Yi Tang, *Member, IEEE*

***Abstract*—Wide bandgap semiconductor switches have been increasingly utilized to improve the power density and efficiency of power converters, as such devices are able to operate at very high frequencies, e.g., up to 100 MHz, with reduced power losses. However, such a high-frequency operation may impose a challenge to the digital control system, and the system clock frequency should be up to 100 GHz in high-precision applications, which is difficult to realize in low-cost microprocessors. Instead of using extremely high-frequency clocks, preprocessing-based solutions that utilize digital pulse-width-modulated (DPWM) dither techniques can also enhance the DPWM resolution with moderate frequency clocks. Unfortunately, this is usually achieved at the expense of introducing low-frequency harmonics, which may complicate system controller and output filter design. In this paper, an optimal dither technique is proposed to enhance the resolution of DPWM power converters. The concepts of positive dither and negative dither are first proposed in this paper. Furthermore, vector-diagram-based analysis indicates that with proper utilization of positive dithers and negative dithers and carefully selected dither sequences, the lowest order harmonic introduced by the conventional dither technique can be completely eliminated when the dither period is multiples of six switching periods. In other cases, the proposed optimal dither technique can produce minimized lowest order harmonic. Finally, experimental results obtained from a Gallium Nitride (GaN) devices-based synchronous buck converter validate the feasibility of the proposed dither technique.**

***Index Terms*—Digital pulse-width modulation (DPWM), dither, harmonic elimination, high-precision converters, wide bandgap.**

I. Introduction

DIGITAL controllers have been receiving more attentions in switching-mode power converters than their analog counterparts. This is mainly due to their advantages such as easier software modification and update, fewer additional components, more robust to component tolerance and parameter variation, and more flexible implementation of advanced control algorithms at lower costs [1]–[6]. Despite these identified advantages, digital controllers may also encounter several problems in practical applications, especially when a high-precision output is desired. One of the critical issues is the quantization errors introduced by the analog to digital conversion (ADC) and the pulse-width-modulated (PWM) signals generation, which can limit the resolution of power converters [1], [2], [4]. Furthermore, to avoid the well-known limit cycle oscillation (LCO) phenomenon, the resolution of digital PWM (DPWM) should be higher than that of the ADC [1], [2], [5]. Therefore, the prerequisite of the high-precision digital control is the high-resolution DPWM.

For digitally controlled power converters, the DPWM signals are generated periodically based on a counter driven by the system clock. Moreover, the resolution of DPWM is equivalent to the resolution of the duty cycle, which is defined by the ratio of the switching frequency to the counterclock frequency [6]. Recently, wide bandgap semiconductor power switches, e.g., Silicon Carbide (SiC) and Gallium Nitride (GaN) devices, have been increasingly adopted to improve the efficiency and power density of power converters [7]–[9], and the available switching frequency can be boosted up to dozens of megahertz [8], [10] or even 100 MHz [9]. As a result, the system clock frequency of high-precision power converters may approach or even go beyond 100 gigahertz, i.e., the relevant time resolution should be less than 10 ps [11]–[13]. One possibility to achieve such a fine time resolution is to adopt hardware-based methods. Among these methods, ring oscillators composed of oscillation loops formed by multiple cascaded logic gates may offer a simple and reliable solution. However, the time resolution of ring oscillators depends on the delay time of individual logic gate, which can be greatly influenced by component tolerances, voltage references, and ambient temperature [14]. Other hardware-based methods, such as tapped delay lines and hybrid counter/delay-line DPWM, are also sensitive to temperature variations and may require additional strategies to tackle the time mismatch problem between the counterclock and delay line [15]. Although multiple counterclocks can be operated coordinately to enhance the DPWM resolution, this method necessitates high-frequency

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phase-locked loops (PLLs), which can be difficult to realize in practical applications [15]. It should be noted that the DPWM resolution can also be enhanced through interleaved multiphase converters with proper modulation strategies in high-power applications [1], [14]–[16]. With hardware-based methods, the time resolutions of DPWM can be limited to be less than 100 ps, as reported in [17]–[20]. Nonetheless, under higher switching frequency conditions, the DPWM resolution can be hardly further improved due to clock jitters [17], [18]. In addition, for applications of low-power switching-mode converters, e.g., voltage regulation modules (VRMs), using low-resolution DPWM modules with low-frequency clocks and preprocessing-based methods can lead to less silicon area and reduced power losses [1], [4], [21]. Therefore, it is highly desirable that the DPWM resolution can be enhanced through a preprocessing-based solution. It should be highlighted that preprocessing-based solutions can be used together with hardware-based methods to obtain further enhanced DPWM resolutions.

A widely adopted preprocessing-based method of enhancing the DPWM resolution is the dither-based modulation techniques [1], [6], [10], [15], [22]–[26]. The basic idea behind the state-of-the-art DPWM dither techniques is to output one or more pulses with the least achievable width over several switching periods, namely, the dither period, to obtain an averaged output signal with a higher resolution. It should be noted that the dither period can be either fixed or time variable [24], [26], and a longer dither period will give rise to a more accurate output voltage. Among dither-based modulation techniques, the well-known Σ–Δ modulation method produces variable dither periods with different increment Δ. For first-order Σ–Δ modulators, the frequency of the lowest order harmonic can be around or even lower than the cutoff frequency of the output filter when Δ is small, resulting in low-frequency harmonics amplification and difficulties for controller design [10], [27]. In contrast, second-order Σ–Δ modulators can avoid this issue by spreading the spectrum of harmonics based on a statistical principle called noise shaping, and the low-order harmonics can be pushed into a high-frequency range [10]. However, since the dither frequency is still variable and dependent on output, the produced harmonic spectrum is unpredictable, making the output filter design challenging. In [10], only the time-domain waveform is given instead of frequency-domain spectrum. Alternatively, when the dither period is fixed, the introduced low-order harmonics may also limit the maximum dither period that can be achieved and thus the improvement of the DPWM resolution [1], [25]. The reason is that the frequency of the lowest order harmonic is inversely proportional to the dither period, and it should be maintained high enough so that the cutoff frequency of the output filter as well as the control bandwidth can be flexibly designed [27], [28]. Although the lowest order harmonic can be eliminated by evenly distributing the dithers over one dither period, it is not possible to achieve such harmonic elimination under all dither output conditions. Therefore, the lowest order harmonic may still exist in the output when the dither technique is implemented according to [1] and [25]. If such harmonic can be completely suppressed, the DPWM resolution can be further increased by using a larger dither period.

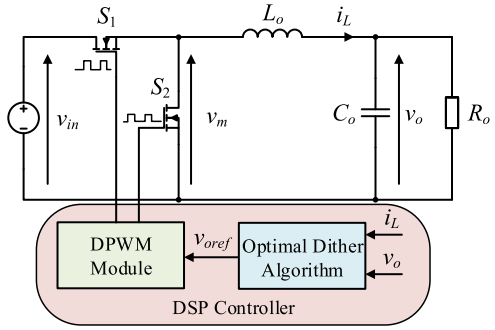

Fig. 1. Schematic diagram of a synchronous buck converter.

In this paper, an optimal DPWM dither technique is proposed to tackle the difficulties mentioned earlier. The proposed dither technique can enhance the resolution of DPWM while eliminating the lowest order harmonic. In Section II, the principle of the conventional dither technique is reviewed in the beginning. Based on the concepts of positive dither and negative dither, the proposed optimal dither technique is then introduced. An analysis of different dither techniques using a vector diagram-based method is presented in Section III. Experimental results obtained from a GaN devices-based synchronous buck converter are shown in Section VI. Finally, Section V concludes the main contribution of the paper.

II. Principles of Conventional and Proposed Dither Techniques

A. System Structure and Principle of Conventional Dither Technique

The schematic diagram of a synchronous buck power converter is shown in Fig. 1. This converter is utilized as an experimental platform to validate dither techniques. In Fig. 1, $v_{\rm in}$ and v_o denote the input voltage and output voltage, respectively. L_o and C_o stand for the filter inductance and the filter capacitance, respectively. S_1 and S_2 represent the semiconductor switches operated complimentarily to regulate the output voltage.

The principle of the conventional DPWM dither technique is shown in Fig. 2. As can be seen, T_s and nT_s denote the switching period and dither period, respectively. T_d and $T_{\rm clk}$ stand for the switching on time without dithering and the least adjustable time step, respectively. $V_{\rm in}$ is the amplitude of $v_{\rm in}$ and v_m is the switching-node voltage. In order to enhance the resolution of DPWM, besides outputting a pulse with a time duration of T_d in each switching period, the conventional dither technique would also output an additional driving pulse with a time duration of $T_{\rm clk}$ in one or more consecutive switching periods over each dither period nT_s. In Fig. 2(a), only one dither is added to the *i*th switching period, and this case is used as an example for simplification of the following analysis.

The resolution of DPWM is equivalent to the resolution of duty cycle, which is defined by the ratio of the converter switching frequency ($f_s = 1/T_s$) to the system counterclock frequency ($f_{\rm clk} = 1/T_{\rm clk}$), represented as [6]

$$\Delta D_o = \frac{f_s}{f_{\rm clk}} = \frac{T_{\rm clk}}{T_s} \tag{1}$$

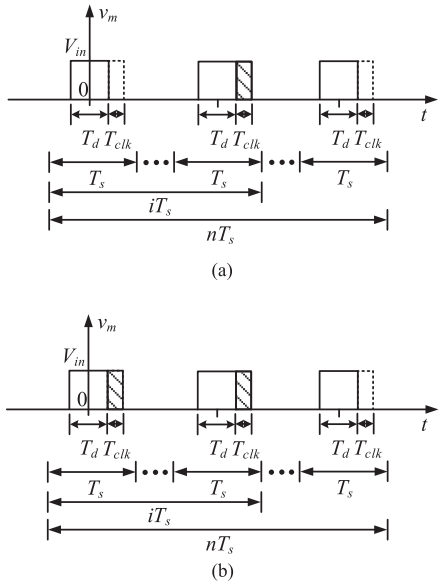

Fig. 2. Principle of conventional DPWM dither. (a) Single dither. (b) Multiple dithers.

where ΔD_o stands for the resolution of duty cycle D_o ($D_o = T_d/T_s$). It is clear from this equation that the value of ΔD_o will be increased if a higher switching frequency is adopted with a fixed counterclock frequency, leading to a decreased DPWM resolution. When $T_{\rm clk} = 0$ s, the undithered waveform of v_m can be expressed based on Fourier transformation as [25]

$$v_{m0} = a_{10} + \sum_{k=1}^{\infty} a_{1k} \cos\left(k\frac{2\pi}{T_s}t\right) \tag{2}$$

where *k* is the order of the harmonics at multiples of the switching frequency. The dc component a_{10} and the amplitudes of harmonics a_{1k} can be, respectively, derived as

$$\begin{aligned} a_{10} &= \frac{1}{T_s}\int_{-\frac{T_d}{2}}^{\frac{T_d}{2}} V_{\rm in}dt = \frac{V_{\rm in}T_d}{T_s} = D_o V_{\rm in} \\ a_{1k} &= \frac{2}{T_s}\int_{-\frac{T_d}{2}}^{\frac{T_d}{2}} V_{\rm in}\cos\left(k\frac{2\pi}{T_s}t\right)dt = \frac{2V_{\rm in}}{k\pi}\sin(\pi k D_o). \end{aligned} \tag{3}$$

From (2) and (3), it can be observed that voltage harmonics only exist at multiples of the switching frequency when the dither technique is not implemented. Considering the voltage increment introduced by the dither in the *i*th switching period, which can be represented as

$$v_{m0} = a_{10} + \sum_{k=1}^{\infty} a_{1k} \cos\left(k\frac{2\pi}{T_s}t\right) \tag{4}$$

where the dc component a_{20i+} and the amplitudes of harmonics a_{2ki+} and b_{2ki+} can be, respectively, derived as

$$\begin{aligned} a_{20i+} &= \frac{1}{nT_s}\int_{(i-1)T_s+\frac{T_d}{2}}^{(i-1)T_s+\frac{T_d}{2}+T_{\rm clk}} V_{\rm in}dt = \frac{V_{\rm in}T_{\rm clk}}{nT_s} \\ &= \frac{V_{\rm in}\Delta D_o}{n} \\ a_{2ki+} &= \frac{2}{nT_s}\int_{(i-1)T_s+\frac{T_d}{2}}^{(i-1)T_s+\frac{T_d}{2}+T_{\rm clk}} V_{\rm in}\cos\left(k\frac{2\pi}{nT_s}t\right)dt \\ &= \frac{2V_{\rm in}}{k\pi}\sin\left(k\frac{\pi T_{\rm clk}}{nT_s}\right)\cos\left\{k\frac{2\pi}{nT_s}\left[(i-1)T_s + \frac{T_d+T_{\rm clk}}{2}\right]\right\} \\ b_{2ki+} &= \frac{2}{nT_s}\int_{(i-1)T_s+\frac{T_d}{2}}^{(i-1)T_s+\frac{T_d}{2}+T_{\rm clk}} V_{\rm in}\sin\left(k\frac{2\pi}{nT_s}t\right)dt \\ &= \frac{2V_{\rm in}}{k\pi}\sin\left(k\frac{\pi T_{\rm clk}}{nT_s}\right)\sin\left\{k\frac{2\pi}{nT_s}\left[(i-1)T_s + \frac{T_d+T_{\rm clk}}{2}\right]\right\}. \end{aligned} \tag{5}$$

From (5), it can be noticed that the resolution of $v_{\rm mi+}$, namely, $a_{20i+}/V_{\rm in}$, is $\Delta D_o/n$ instead of ΔD_o, thereby proving that the resolution of dithered DPWM can be enhanced by *n* times as compared with its undithered counterpart. However, as indicated by the second term of (4), the frequency of harmonics introduced by $v_{\rm mi+}$ is at multiples of f_s/n, and such lower frequency harmonics may restrict the selection of the output filter cutoff frequency as well as the controller bandwidth design, which is particularly serious when a large *n* is considered. The magnitudes of harmonics are determined by their respective magnitudes of sinusoidal components and cosine components, namely, a_{2ki+} and b_{2ki+}, which are dependent on $V_{\rm in}$, $T_{\rm clk}/T_s$, T_d/T_s, *n*, and *i*. The aforementioned analysis is applicable to the single dither case. When multiple dithers are utilized together in one dither period, as shown in Fig. 2(b), the voltage increment can be rewritten as

$$\begin{aligned} v_{\rm misum+} = a_{20{\rm isum}+} + \sum_{k=1}^{\infty}\Bigg[&a_{2k{\rm isum}+}\cos\left(k\frac{2\pi}{nT_S}t\right) \\ &+ b_{2k{\rm isum}+}\sin\left(k\frac{2\pi}{nT_S}t\right)\Bigg] \end{aligned} \tag{6}$$

where the dc component $a_{20{\rm isum}+}$ and the amplitudes of harmonics $a_{2k{\rm isum}+}$ and $b_{2k{\rm isum}+}$ of $v_{m{\rm isum}+}$ can be, respectively, derived as

$$\begin{aligned} a_{20{\rm isum}+} &= \sum_{q=1}^{i} a_{20q+} = \frac{iV_{\rm in}T_{\rm clk}}{nT_s} = \frac{iV_{\rm in}\Delta D_o}{n} \\ a_{2k{\rm isum}+} &= \sum_{q=1}^{i} a_{2kq+} \\ &= \frac{2V_{\rm in}}{k\pi}\sin\left(k\frac{\pi T_{\rm clk}}{nT_s}\right)\sum_{q=1}^{i}\cos\left\{k\frac{2\pi}{nT_s}\left[(q-1)T_s + \frac{T_d+T_{\rm clk}}{2}\right]\right\} \end{aligned}$$

TABLE I
SYSTEM PARAMETERS

Description	Symbol	Value
DC input voltage	V_{in}	48 V
Nominal duty cycle	D_o	0.5
Switching frequency	f_s	1 MHz
Counterclock frequency	f_{clk}	75 MHz
Filter capacitance	C_o	1.0 μF
Filter inductance	L_o	12 μH
Load resistance	R_o	12 Ω
Dither period	n	6
Duty cycle resolution	ΔD_o	0.013

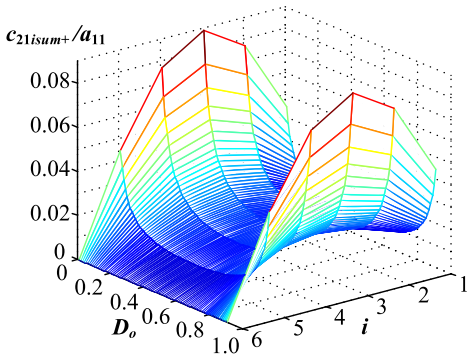

Fig. 3. $c_{21\text{isum}+}/a_{11}$ with variable D_o and i under the condition listed in Table I.

$$b_{2k\text{isum}+} = \sum_{q=1}^{i} b_{2kq+} = \frac{2V_{\text{in}}}{k\pi}\sin\left(k\frac{\pi T_{\text{clk}}}{nT_s}\right)\sum_{q=1}^{i}\sin\left\{k\frac{2\pi}{nT_s}\left[(q-1)T_s + \frac{T_d+T_{\text{clk}}}{2}\right]\right\}. \quad (7)$$

Through adjusting the dither number i in each dither period nT_s, the dc output voltage can be regulated accordingly. The amplitude of the kth harmonic introduced by the conventional dither technique is given by $c_{2k\text{isum}+} = (a_{2k\text{isum}+}^2 + b_{2k\text{isum}+}^2)^{1/2}$, and all the harmonics introduced by the dither technique can be normalized with respect to the first switching harmonic a_{11} denoted in (2). The ratio of $c_{21\text{isum}+}$ and a_{11} with variable duty cycles and dither numbers using the system parameters listed in Table I is illustrated in Fig. 3.

For a given duty cycle D_o, the amplitude of harmonic at the switching frequency a_{11} will be a constant and independent of i according to (2). Under such a condition, the conventional dither technique will produce the highest harmonic magnitude $c_{21\text{isum}+}$ at f_s/n with the dither number i equivalent to $n/2$, as discussed in [1] and [25]. Moreover, $c_{21\text{isum}+}/a_{11}$ will increase when the duty cycle D_o is moved away from 0.5 and toward 0 or 1. Although $c_{21\text{isum}+}$ is relatively small as compared to a_{11}, it should be kept in mind that the frequency of the lowest order harmonic has decreased to f_s/n. For a typical second-order *LC* output filter that has a slew rate of -40 dB/dec after its cutoff frequency, its attenuation ability at f_s/n is only $1/n^2$ of that at f_s. This implies that under the case of $n = 6$, the corresponding output voltage attenuation ratio would be 36 times. Therefore, the lowest order harmonic introduced by the conventional dither technique should not be ignored as suggested in [25].

The switching-node voltage v_m with multiple dithers can be obtained by adding (2) to (6), and the dc component of v_m can be expressed as

$$a_{0+} = a_{10} + a_{20\text{isum}+} = V_{\text{in}}\left(D_o + \frac{i\Delta D_o}{n}\right). \quad (8)$$

The root-mean-square (rms) value of v_m can be derived as

$$V_m = \sqrt{\frac{1}{nT_s}\left[i\int_0^{T_{\text{clk}}+T_d} {V_{\text{in}}}^2 dt + (n-i)\int_0^{T_d} {V_{\text{in}}}^2 dt\right]} = V_{\text{in}}\sqrt{D_o + \frac{i\Delta D_o}{n}}. \quad (9)$$

The rms value of ac components in v_m can be further derived from (8) and (9) as

$$V_{m\text{ac}} = \sqrt{{V_m}^2 - {a_{0+}}^2} = V_{\text{in}}\left[(D_o - {D_o}^2) + \frac{i\Delta D_o}{n}\left(1 - 2D_o - \frac{i\Delta D_o}{n}\right)\right]^{\frac{1}{2}}. \quad (10)$$

The rms value of ac components for undithered v_m can be obtained by setting ΔD_o to 0. As $\Delta D_o/D_o$ is relatively small (the ratio of ΔD_o to D_o is normally less than 0.1), the second term in the bracket of (10) can be neglected as compared to the first one under normal operating conditions. For instance, $V_{m\text{ac}}$ under undithered and dithered cases are found to be 24.000 and 23.997, respectively, using the parameters listed in Table I, with $i = 3$. Therefore, the dither technique would have negligible influence on the ripple factor or total harmonic distortion (THD) of v_m.

B. Principle of Proposed Dither Technique

Since the conventional dither technique analyzed earlier can output driving pulses with longer time durations, it is defined as the positive dither in this paper. In contrast, the principle of the negative dither is illustrated in Fig. 4.

As can be observed from Fig. 4, instead of adding a least achievable time step T_{clk} to T_d, a negative dither refers to the subtraction of T_{clk} from T_d. Again, one negative dither in the ith switching period is illustrated as an example here. The voltage variation under this case can be represented as

$$v_{\text{mi}-} = a_{20i-} + \sum_{k=1}^{\infty}\left[a_{2ki-}\cos\left(k\frac{2\pi}{nT_s}t\right) + b_{2ki-}\sin\left(k\frac{2\pi}{nT_s}t\right)\right] \quad (11)$$

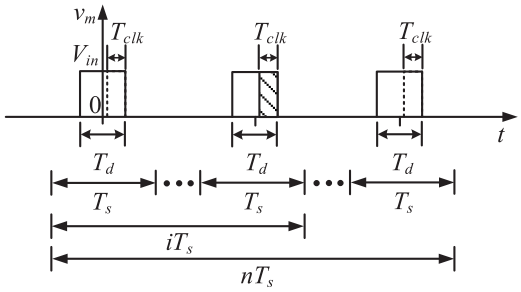

Fig. 4. Principle of negative DPWM dither.

where the dc component a_{20i-} and the amplitudes of harmonics a_{2ki-} and b_{2ki-} can be, respectively, derived as

$$\begin{aligned}
a_{20i-} &= \frac{1}{nT_s}\int_{(i-1)T_s+\frac{T_d}{2}-T_{\rm clk}}^{(i-1)T_s+\frac{T_d}{2}}(-V_{\rm in})dt = -\frac{V_{\rm in}T_{\rm clk}}{nT_s} \\
&= -\frac{V_{\rm in}\Delta D_o}{n} \\
a_{2ki-} &= -\frac{2}{nT_s}\int_{(i-1)T_s+\frac{T_d}{2}-T_{\rm clk}}^{(i-1)T_s+\frac{T_d}{2}} V_{\rm in}\cos\left(k\frac{2\pi}{nT_s}t\right)dt \\
&= -\frac{2V_{\rm in}}{k\pi}\sin\left(k\frac{\pi T_{\rm clk}}{nT_s}\right)\cos\left\{k\frac{2\pi}{nT_s}\left[(i-1)T_s\right.\right. \\
&\quad \left.\left.+\frac{T_d-T_{\rm clk}}{2}\right]\right\} \\
b_{2ki-} &= -\frac{2}{nT_s}\int_{(i-1)T_s+\frac{T_d}{2}-T_{\rm clk}}^{(i-1)T_s+\frac{T_d}{2}} V_{\rm in}\sin\left(k\frac{2\pi}{nT_s}t\right)dt \\
&= -\frac{2V_{\rm in}}{k\pi}\sin\left(k\frac{\pi T_{\rm clk}}{nT_s}\right)\sin\left\{k\frac{2\pi}{nT_s}\left[(i-1)T_s\right.\right. \\
&\quad \left.\left.+\frac{T_d-T_{\rm clk}}{2}\right]\right\}. \qquad (12)
\end{aligned}$$

From (11), the harmonics introduced by the negative dither are located at multiples of f_s/n. Moreover, as indicated by (12), the duty cycle resolution of $v_{\rm mi-}$ is $-\Delta D_o/n$. Comparing a_{2ki-} shown in (12) with a_{2ki+} shown in (5), the only difference besides a minus sign is that $T_d + T_{\rm clk}$ in $a_{2{\rm ki}+}$ is replaced by $T_d - T_{\rm clk}$ in a_{2ki-}, and the same is true for the difference between b_{2ki+} and b_{2ki-}. Under normal operating conditions, $T_{\rm clk} << T_d$, $a_{2ki+} \approx -a_{2ki-}$ and $b_{2ki+} \approx -b_{2ki-}$ can be satisfied. With the parameters listed in Table I, $T_d/T_{\rm clk} = 37.5$, $a_{21i+} = 0.206$, $a_{21i-} = -0.206$, $b_{21i+} = 0.056$, $b_{21i-} = -0.054$ can be derived. Therefore, a_{2ki-} and a_{2ki+} as well as b_{2ki-} and b_{2ki+} can be considered approximately equal in magnitude but opposite in phase. This conclusion will be used in Section III to interpret the mechanism of harmonics cancellation realized by the proposed dither technique. It should be noted that $T_{\rm clk} << T_d$ may not be valid under an extremely low-output-voltage condition.

The principle of the proposed optimal dither technique is to output positive dithers and negative dithers when necessary in a particular sequence in each dither period while maintaining the same dc output voltage as that of the conventional dither technique. The waveforms of v_m for the case of $n = 6$ using the conventional dither technique and optimal dither technique are shown in Fig. 5.

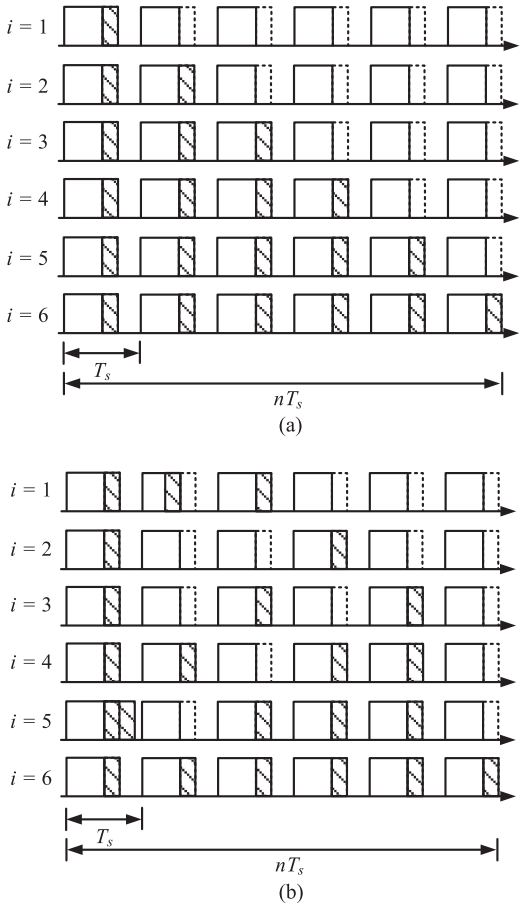

Fig. 5. Waveforms of v_m using conventional dither and optimal dither ($n = 6$). (a) Conventional dither. (b) Optimal dither.

As shown in Fig. 5(b), when only one dither is required, i.e., $i = 1$, the optimal dither technique outputs one positive dither in the first switching period, and then a negative dither in the second switching period followed by a positive dither in the third switching period. In this way, the dc output voltage increment remains to be the same with that of the conventional dither technique, namely, $V_{\rm in}\Delta D_o/n$. If more dithers are required for a higher output voltage, i.e., $i > 1$, the optimal dither technique should output dithers in a special dither sequence. Through the proposed optimal dither technique, the frequency of the lowest order harmonic can be shifted from f_s/n into $2f_s/n$, and the mechanism of frequency shifting will be elaborated in the following section. It should be noted that THD of v_m with the optimal dither is exactly the same with that of the conventional dither, as both the dc component and the rms value of v_m remain unchanged. Therefore, the ac components of v_m with the optimal dither can also be expressed as (10).

III. Vector-Diagram-Based Analysis for Dither Techniques

The vector diagrams of the conventional dither technique and proposed optimal dither technique for the case of $n = 6$

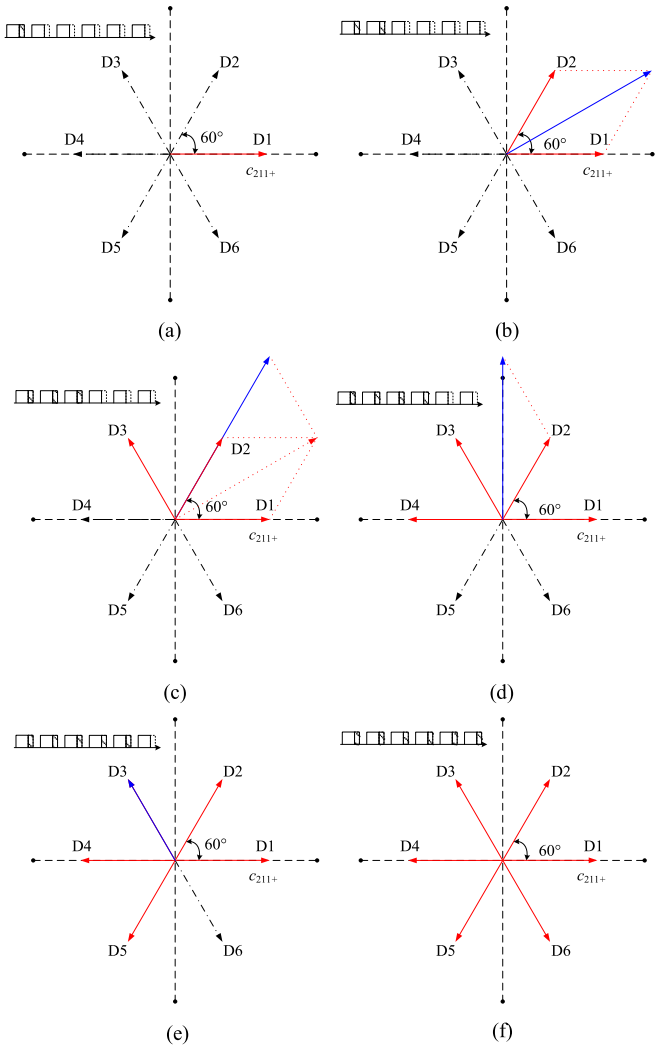

Fig. 6. Vector diagrams of conventional dither ($n = 6$).

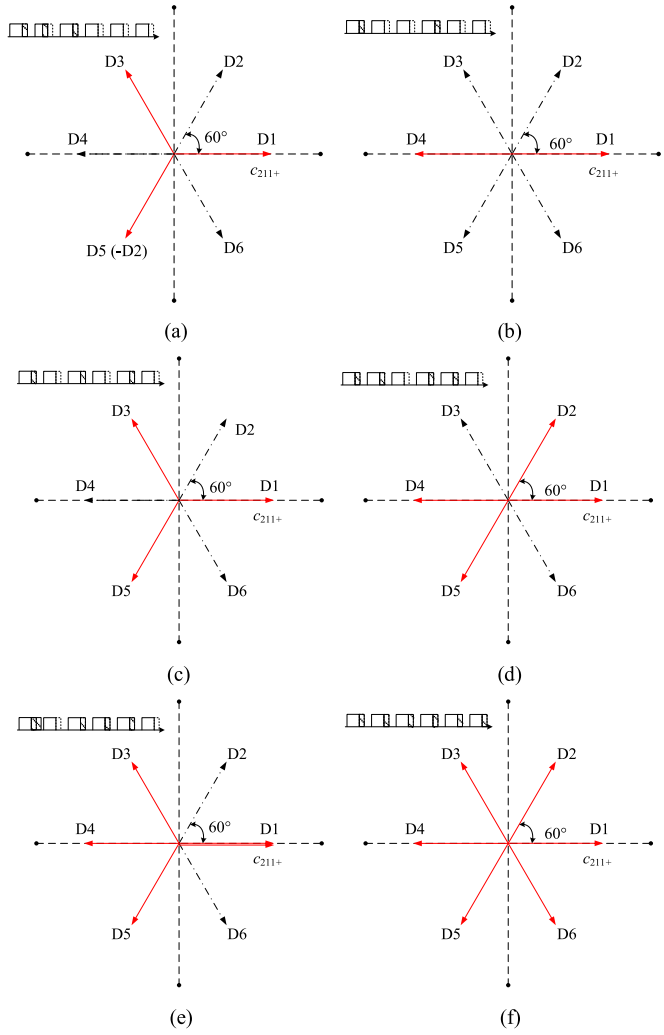

Fig. 7. Vector diagrams of optimal dither ($n = 6$).

are shown in Figs. 6 and 7, respectively. It should be noted that the phase angles of all the vectors plotted in Figs. 6 and 7 are specified to f_s/n. It is clear from these two figures that the magnitude of the lowest order harmonic depends on the vector sum of all the dither vectors. For the conventional dither technique shown in Fig. 6, the lowest order harmonic at f_s/n may always exist under the cases where $i \neq 6$. Its magnitude increases with the increment of i and peaks at $i = 3$ and then gradually decreases to 0 when $i = 6$, which is in agreement with the analysis derived from Fig. 3.

As can be observed from Fig. 7, the idea behind the proposed optimal dither technique is to properly allocate several dither vectors so that they can cancel with each other, resulting in a vector sum of zero while maintaining $N_{di+} - N_{di-} = i$, where N_{di+} and N_{di-} stand for the number of positive dithers and the number of negative dithers, respectively. When $i = 1$ is considered, as shown in Fig. 7(a), a negative dither vector $-$D2 is introduced in the second switching period. For the harmonic component at $f_s/6$, as discussed earlier, this negative dither is essentially equivalent to the positive dither introduced in the fifth switching period D5. Under this condition, the combination of D1, $-$D2, and D3 will produce a zero vector, thereby completely eliminating the harmonic at f_s/n, which is the lowest order harmonic that cannot be removed by the conventional dither technique. The same vector diagram can be readily obtained with the case of $i = 3$. When $i = 5$ is considered, two positive dithers should be introduced in the first switching period, and they can cancel with those in the third, fourth, and fifth switching periods. The harmonic cancellation becomes more straightforward when i is an even number, e.g., 2, 4, 6, as the dither vectors can be distributed in a symmetrical pattern, as shown in Fig. 7(b) (d), and (f). It should be noted that the vector diagrams shown in Figs. 6 and 7 are only applicable to the frequency f_s/n. For other frequencies, e.g., $2f_s/n$, these vector diagrams are no longer valid. In [1] and [25], dithers are evenly distributed based on the understanding that symmetrical waveforms produce fewer low order harmonics. The vector diagram-based analysis proposed in this paper can further visualize the effect of dithers and clearly reveal the elimination mechanism of low order harmonics.

The theoretically calculated spectra of v_m with the conventional (dotted line) and proposed optimal dither (solid-line) techniques ($n = 6$) are shown in Fig. 8. As can be seen from Fig. 8,

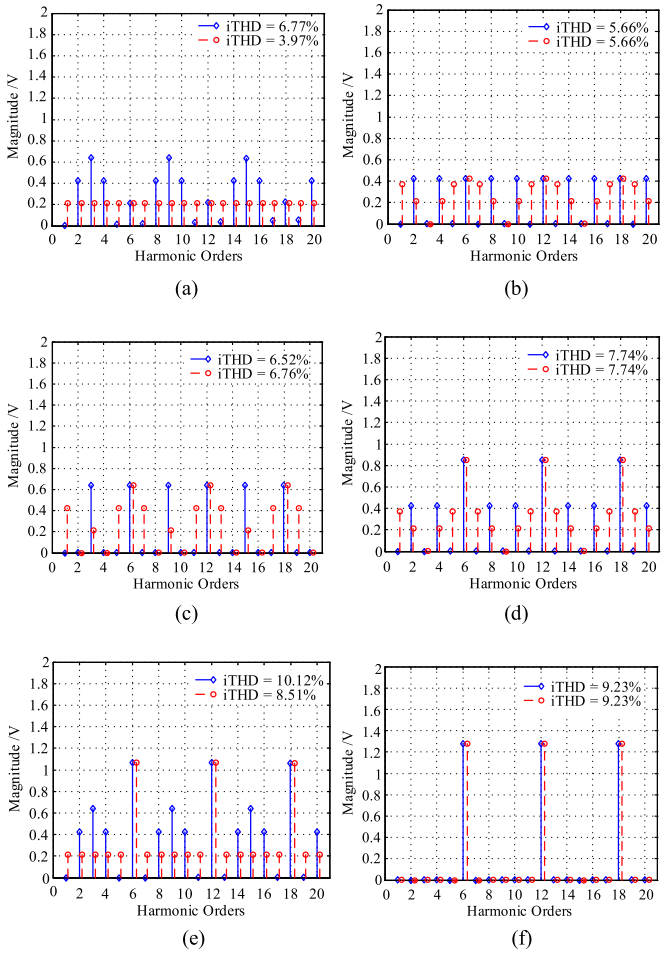

Fig. 8. Spectra of v_m introduced by conventional (dotted-line) and optimal (solid-line) dither ($n = 6$). (a) $i = 1$. (b) $i = 2$. (c) $i = 3$. (d) $i = 4$. (e) $i = 5$. (f) $i = 6$.

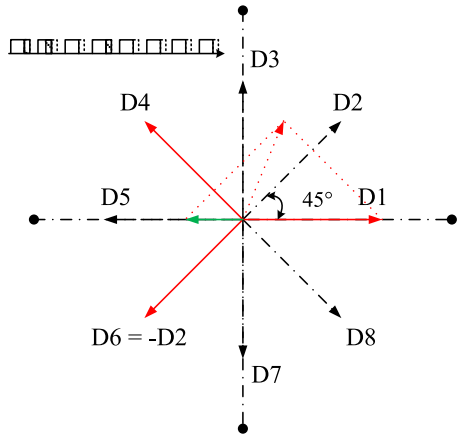

Fig. 9. Vector diagram of optimal dither under the condition of $i = 1$ ($n = 8$).

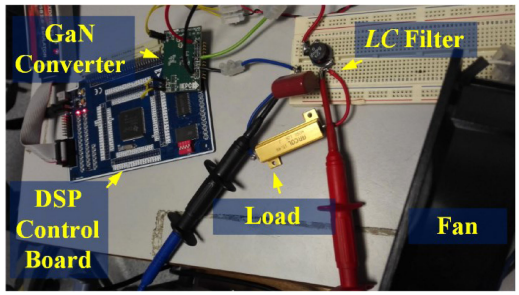

Fig. 10. Experimental platform.

the lowest order harmonic of conventional dither technique can be eliminated under all the cases by the optimal dither technique. As a result, the frequency of the lowest order harmonic has been boosted to $2f_s/n$. Unavoidably, the proposed optimal dither technique would increase the magnitudes of high-frequency harmonics, but generally, these harmonics can be more easily removed by the output low-pass filter, particularly when a second-order *LC* filter with a roll-off rate of -40 dB/dec at high frequencies is used. In most cases, elimination of lowest order harmonic is more of concern, which is also the main focus of this paper. Although the THDs of v_m under all the cases are shown in Fig. 8, it should be noted that Fig. 8 only shows the harmonics of v_m introduced by the dithers, namely, the harmonics calculated from (5) and (12). However, the THD of v_m is mainly caused by the undithered component, namely, those derived from (3). When considering the harmonics at f_s and its multiples derived from (3), the THD of v_m will be the same for the cases of optimal dither and conventional dither. In addition, the harmonics of v_m may not be utilized directly to measure the performances of dither techniques, because the attenuation effect of the *LC* filter has not been taken into consideration when calculating the THDs of v_m. Instead, the spectrum of v_o should be referred to when evaluating the dither techniques. Therefore, the commonly observed phenomenon that the harmonic amplitude decreases with the increase of harmonic order may not be obtained from Fig. 8, and these harmonic amplitudes can be precisely calculated using (5) and (12).

The proposed optimal dither technique can also be generalized to other cases where a large n needs to be adopted to further enhance the DPWM resolution. Under such cases, the lowest order harmonic can be always eliminated as long as n is multiples of 6, i.e., $n = 6m$ ($m \in Z$), using the dither vectors with the same phases as those illustrated in Fig. 7. Considering the case when $n \neq 6m$ and one dither ($i = 1$) is required, the optimal dither vectors are unable to completely cancel with each other. Nonetheless, by selecting the dither vectors whose phases are close to 0°, 120°, and 240°, the magnitude of the lowest order harmonic can still be minimized as shown in Fig. 9 for the case of $n = 8$.

IV. Experimental Results

A GaN devices-based synchronous buck converter was built and tested in the laboratory. Its schematic diagram and platform photo are shown in Figs. 1 and 10, respectively. The dither algorithm was implemented with a DSP controller (TMS320F28335). Its maximum system clock frequency is 150 MHz, and the default frequency of high-speed peripheral clocks for the enhanced PWM module is 75 MHz [29]. The dc

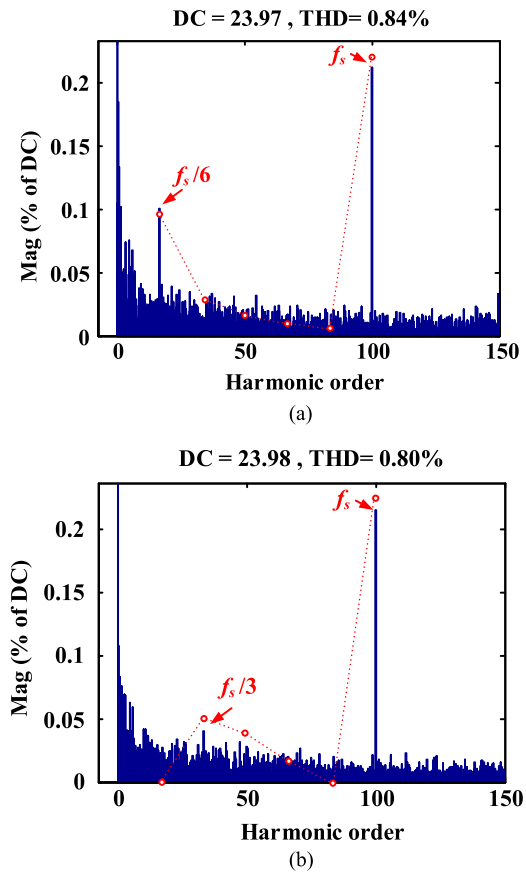

Fig. 11. Spectra of v_o under the condition of $i = 1$ ($n = 6$, dotted line: predicted values). (a) Conventional dither. (b) Optimal dither.

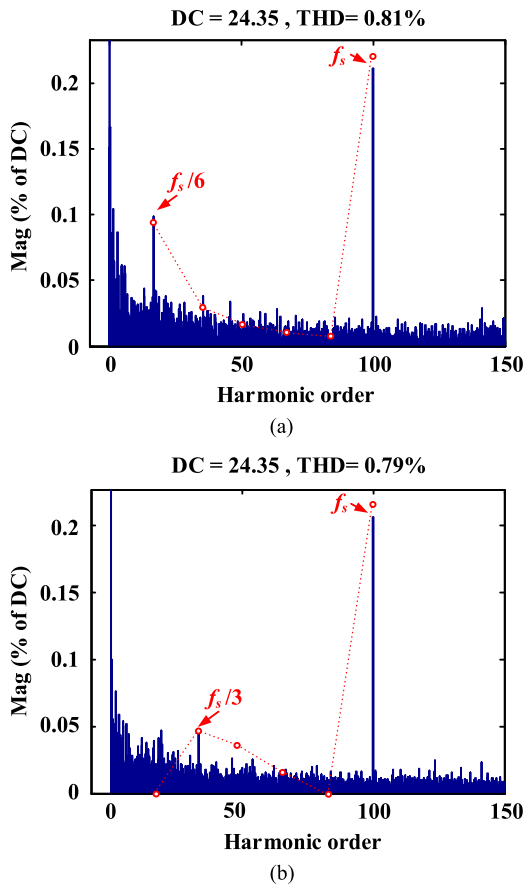

Fig. 12. Spectra of v_o under the condition of $i = 5$ ($n = 6$, dotted line: predicted values). (a) Conventional dither. (b) Optimal dither.

input voltage was obtained from a dc power supply (XKW300-10) and all the waveforms were measured by an oscilloscope (LeCroy 6050) through a voltage probe (ADP30S). A 100V half-bridge GaN devices-based module (EPC9002C) with a gate driver (LM5113) and an output *LC* filter were configured as the synchronous buck converter. The *LC* filter is designed based on the ripple current and ripple voltage requirements [30]. In this paper, a 25% ripple current and a 1.0% ripple voltage are specified, resulting in a cutoff frequency of 45.9 kHz, -53.6 dB attenuation at f_s, and -21.6 dB attenuation at $f_s/6$. The system parameters are listed in Table I.

The software implementation of optimal dither algorithm is based on a lookup table (LUT) [31]. To be more specific, an $n \times n$ LUT is programed offline with n rows representing the dither numbers and n columns standing for the dither sequences. Furthermore, the PWM interruption period is set to be the same as the switching period. In the PWM interruption function, the value of PWM comparison register is revised according to the specific dither sequence. Before the end of each dither period, the next dither sequence should be updated. However, the relatively short interruption period prohibits the LUT reference and data exchange operation. Fortunately, this issue can be resolved by the direct memory access (DMA) module in the DSP controller, which is able to update the dither sequence at around $4n$ system clock periods through the DMA interrupt.

Fig. 11 shows the spectra of v_o under the condition of $i = 1$ ($n = 6$) with the conventional dither and optimal dither techniques. The experimental waveforms of v_o were captured by the oscilloscope and saved as binary files, and then the data were imported into the MATLAB software and the spectra were analyzed through Simulink/FFT. The fundamental frequency is assigned to be 10 kHz. Therefore, the 100th harmonic refers to the switching frequency harmonic. As shown in Fig. 11, the lowest order harmonic of conventional dither locates at $f_s/6$ and that of the optimal dither is shifted to $f_s/3$.

Similar results can be obtained under the condition of $i = 5$ ($n = 6$), as can be observed from Fig. 12. The frequency of the lowest order harmonic under $i = 1$ and $i = 5$ conditions for the conventional dither technique is always located at f_s/n and these cases are known to be the most unfavorable cases. Fortunately, through the optimal dither technique, the frequency of the lowest order harmonic has been boosted up to $2f_s/n$ and the previous lowest order harmonic has been eliminated. The dotted-lines depicted in Figs. 11 and 12 represent the theoretically predicted harmonic amplitudes derived from (3), (5), and (12). The mismatch between the predicted values and measurement values is mainly caused by the variations of inductance, capacitance, and their ESRs under various frequencies. It should be noted that the observable low-frequency harmonics around 50 kHz (fifth) and 100 kHz (tenth) shown in Figs. 11 and 12 are introduced by

TABLE II
HARMONICS OF v_o WITH CONVENTIONAL AND OPTIMAL DITHERS ($n = 6$)

i	Conventional Dither Harmonics (Evenly Distributed Dither Harmonics $i = 1, 5, 6$)					Optimal Dither Harmonics (Evenly Distributed Dither Harmonics $i = 2, 3, 4$)				
	Frequency of Lowest	Magnitude of Lowest/DC	Magnitude of f_s/DC	Magnitude of DC	THD /DC	Frequency of Lowest	Magnitude of Lowest/DC	Magnitude of f_s/DC	Magnitude of DC	THD /DC
1	$f_s/6$	0.10%	0.22%	23.97	0.84%	$f_s/3$	0.04%	0.22%	23.98	0.80%
2	$f_s/6$	0.14%	0.23%	24.05	0.84%	$f_s/3$	0.04%	0.23%	24.06	0.81%
3	$f_s/6$	0.18%	0.23%	24.14	0.85%	$f_s/2$	0.03%	0.23%	24.14	0.81%
4	$f_s/6$	0.14%	0.22%	24.26	0.83%	$f_s/3$	0.04%	0.22%	24.25	0.80%
5	$f_s/6$	0.10%	0.22%	24.35	0.81%	$f_s/3$	0.05%	0.22%	24.35	0.79%
6	f_s	0.21%	0.21%	24.45	0.78%	f_s	0.21%	0.21%	24.45	0.78%

the dc power supply. For other cases, the results are summarized in Table II. It can be clearly observed that the lowest order harmonic of conventional dither has been completely eliminated. Only some harmonics may appear around $2f_s/n$ for the cases of $i = 1$, $i = 2$, $i = 4$, $i = 5$. For $i = 3$ case, the frequency of the lowest order harmonic becomes $3f_s/n$. The harmonics produced by the evenly distributed dither technique are also listed in Table II, the effect of which can be the same as that of the conventional dither technique under the conditions $i = 1, 5, 6$ and as that of the optimal dither pattern under the other conditions $i = 2, 3, 4$. The aforementioned experimental results are in consistence with the theoretical analysis and the vector diagrams presented in Figs. 6 and 7.

The waveforms of v_m under the condition of $i = 1$ ($n = 6$) with the conventional dither and optimal dither techniques are illustrated in Fig. 13. From Fig. 13, the dither patterns and a switching frequency of 1 MHz can be clearly observed. Fig. 14 shows the spectra of v_o under the condition of $i = 1$ ($n = 8$), where the lowest order harmonic may not be fully suppressed by the optimal dither technique. However, as indicated by Fig. 9, the magnitude of the lowest order harmonic has been reduced.

Fig. 15 illustrates the experimental waveforms and spectra of v_o under the condition of $i = 1$ ($n = 6$) with a clock frequency $f_{\rm clk}$ of 25 MHz and a duty cycle $D_{\rm o}$ of 0.2. As discussed in the previous section, a lower clock frequency and a duty cycle approaching zero or unity give rise to a higher ratio of the lowest order harmonic magnitude to the switching frequency harmonic magnitude. As shown in Fig. 15, the magnitude of the lowest order harmonic surpasses that of the switching frequency harmonic using the conventional dither technique. With the help of the optimal dither technique, the former lowest order harmonic has been eliminated and replaced by the second-order one. The disadvantage of proposed optimal dither technique, namely, the amplification of several other low order harmonics, can be observed distinctively from Fig. 15. However, due to the clearance of the lowest order one, the optimal dither technique should be adopted as those evenly distributed dither techniques used in [1], [25], and [31] are subjected to the same shortcoming.

Fig. 16 shows the steady-state waveforms of the output voltage v_o with and without dither techniques. The duty cycle is changed periodically so that the output voltage v_o increases gradually and then suddenly drops. In Fig. 16(a), the output voltage v_o is controlled without activating the dither technique and distinctive voltage steps can be observed. The output voltage resolution is only $\Delta D_o\, V_{\rm in} = 0.64$ V, and this is mainly restricted by the ratio of the switching frequency to the counter-clock frequency.

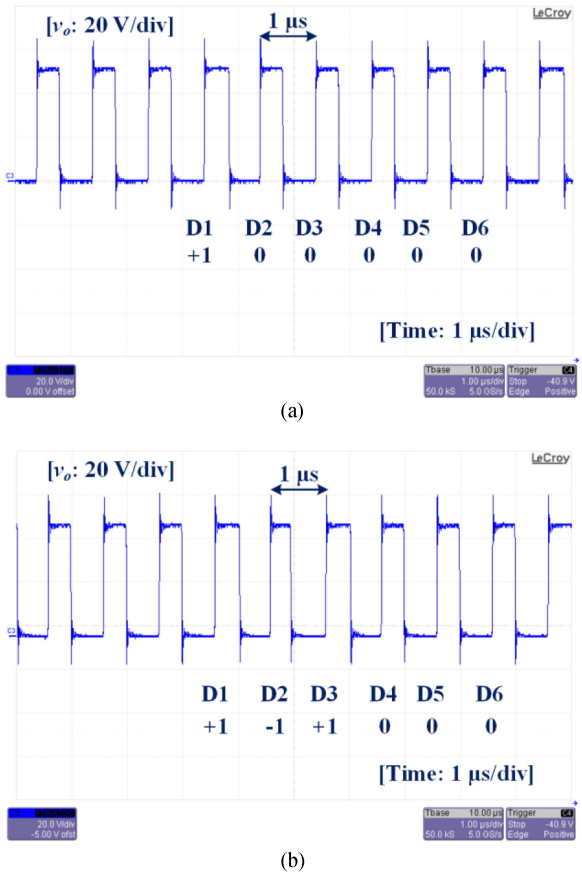

Fig. 13. Waveforms of v_m under the condition of $i = 1$ ($n = 6$). (a) Conventional dither. (b) Optimal dither.

In contrast, when the dither technique (both the conventional dither and optimal dither) is implemented, as shown in Fig. 16(b), the voltage steps disappear and the output voltage v_o can be regulated almost continuously. The reason is that the resolution of v_o can be enhanced to $\Delta D_o\, V_{\rm in}/6 = 0.107$ V, which is improved by six times as compared to that of the undithered case. As a consequence, the proposed dither technique is obviously more preferred than the conventional one as it produces much less harmonics at f_s/n.

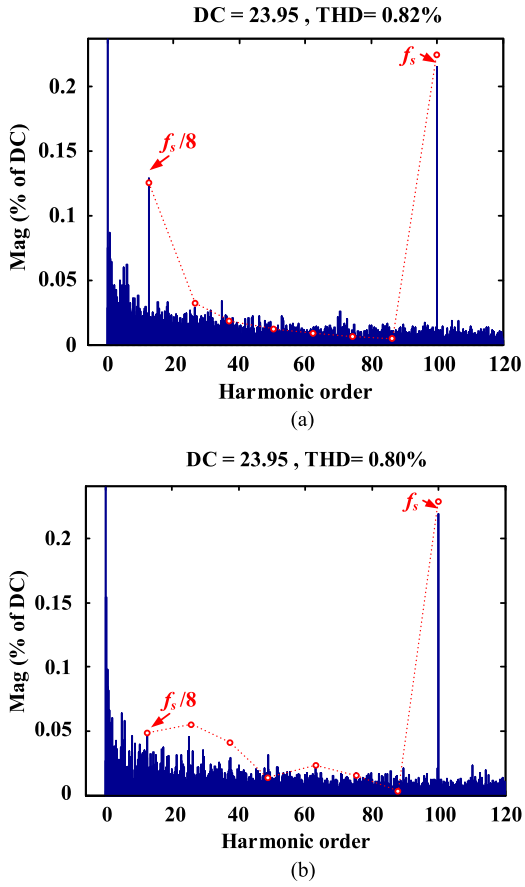

Fig. 14. Spectra of v_o under the condition of $i = 1$ ($n = 8$, dotted line: predicted values). (a) Conventional dither. (b) Optimal dither.

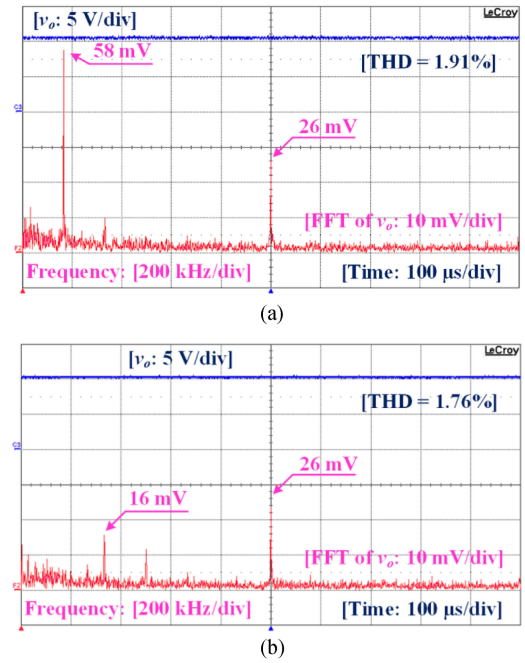

Fig. 15. Waveforms and spectra of v_o under the condition of $i = 1$, $f_{\mathrm{clk}} = 25$ MHz and D_o of 0.2 ($n = 6$). (a) Conventional dither. (b) Optimal dither.

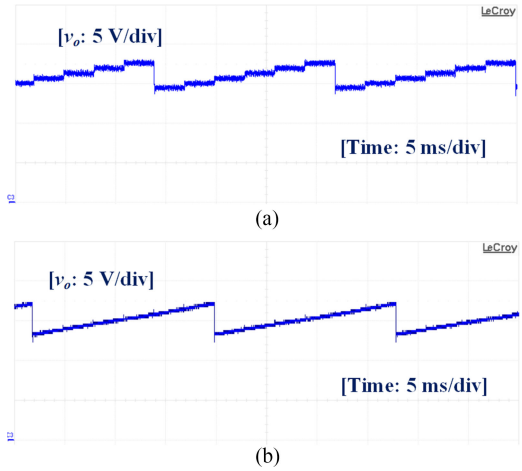

Fig. 16. v_o regulation with and without the dither techniques ($n = 6$). (a) Without dither. (b) With dither.

V. Conclusion

In this paper, an optimal digital PWM dither technique has been proposed to enhance the resolution of wide bandgap device-based high-frequency dc/dc power converters. Instead of using only positive dithers as the conventional dither technique, the proposed optimal dither technique can output both positive dithers and negative dithers in each dither period with an optimized dither sequence, resulting in complete elimination of the lowest order harmonic when the dither period is $6m$ ($m \in Z$) times of the switching period. A vector diagram-based analysis method has been presented to clearly explain the mechanism of harmonic elimination. As the frequency of the lowest order harmonic is doubled, these harmonics can be more easily attenuated by the output filter as compared to those introduced by the conventional dither technique. The controller bandwidth design also becomes more flexible due to the absence of low order harmonics. Finally, experimental results obtained from a buck converter are provided to validate the feasibility of the proposed optimal dither technique.

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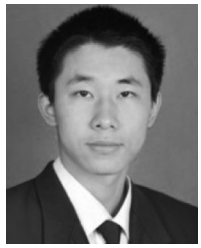

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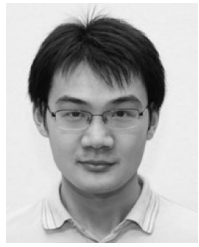

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