A Synchronous Buck DC–DC Converter Using a Novel Dual-Mode Control Scheme to Improve Efficiency

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***Abstract*—A novel dual-mode control scheme is developed here to enable synchronous buck converters (SBC) to operate in a continuous-conduction mode under heavy-load conditions and in a discontinuous-conduction mode under light-load conditions. When an SBC operates in a discontinuous-conduction mode, a quasi-resonant valley switching technique can be employed to turn on a synchronous switch, perform zero-voltage switching at main switches, and improve the light-load efficiency. The proposed scheme does not require the addition of an auxiliary circuit in the SBC, providing it with the advantages of low cost and easily built-in integrated circuits. To verify its feasibility, an SBC equipped with the proposed control scheme is developed, with output voltage and output power of 5 V and 25 W, respectively.**

***Index Terms*—Auxiliary circuit, quasi-resonant valley switching, zero-voltage switching (ZVS).**

I. Introduction

THE market for portable consumer electronic products (e.g., laptop computers and mobile communication devices) has undergone rapid growth in the last few years. In turn, consumers have become increasingly concerned about the usage duration of their electronics devices. Currently, such devices are powered by batteries, and the voltage supply to such products tends to decrease gradually. Therefore, to extend the battery life, synchronous buck converters (SBC) have been widely used in personal and portable devices [see Fig. 1(a)].

Conventional SBCs are controlled using complementary pulse-width modulation (PWM), as shown in Fig. 1(b). Under heavy-load conditions, the low-conduction loss inherent in a switch M_B is used to operate an SBC in a continuous-conduction mode (CCM), thus increasing the conversion efficiency. However, when the mean load current is lower than the inductance current associated with a boundary-conduction mode, the reverse inductance current creates excess loss [1], as shown by the red dotted lines in Fig. 1(b). Specifically, the operation of

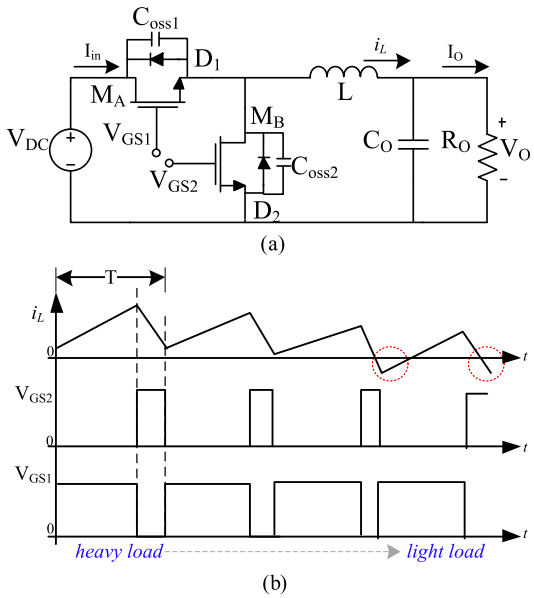

Fig. 1. (a) SBC and (b) key switching waveforms.

SBCs under light-load conditions is inadequate due to the low conversion efficiency.

In order to address the drawbacks of SBC, the hybrid-mode control strategies based on different loading conditions from several different studies have been proposed [2]–[14]. The most popular technique of the dual-mode control is to combine with CCM and discontinuous-conduction mode (DCM). Generally, dual-mode operations can be divided into fixed-frequency mode and variable-frequency mode.

In a variable-frequency control, a pulse frequency modulation (PFM) technique based on the hysteresis of the output voltage determines the timing for the turning on and off of a metal–oxide–semiconductor field-effect transistor (MOSFET) [2]–[5]. In other words, the output power decreases, thereby decreasing the switching frequency. Therefore, the light-load efficiency of the SBC increases. The drawback of this control strategy is a much wider range of switching frequencies, making EMI filter design difficult. In addition, the output ripple voltage for this control strategy is higher than that for the PWM control strategy.

Another variable-frequency technique involves detecting the valley of the inductor current. If the inductor current reaches the valley, the main switch will be triggered on. Thus, the SBC can be operated at the boundary between CCM and DCM. The

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TABLE I
COMPARISON OF SBC CONTROL TECHNIQUES

Operation Mode	Efficiency	Load Range	Output Voltage Ripple	Audio Noise	EMI filter design	Line/load regulation
CCM/DCM (Variable-Frequency) [2]–[9]	Good	Wide	Large	Medium	Hard	Good
CCM/DCM (Fixed-Frequency) [10]–[13]	Medium	Wide	Small	Small	Easy	Good
CCM/DCM (Fixed-Frequency) [14]	Good	Wide	Small	Small	Easy	Good
CCM/DCM (Novel)	Very Good	Wide	Small	Small	Easy	Good

main switch operated in this region has the characteristics of zero-current switching (ZCS) [6]. The quasi-resonant switching technique is similar to the aforementioned control strategy [7]–[9]. This scheme involves resonance generated through the parasitic capacitance and inductance of switches. To improve the efficiency, it turns on the MOSFET when the $v_{\rm ds}$ resonance reaches a valley. The aforementioned control strategies still have problems related to a wider variation range of switching frequencies when the output power drops.

Due to the aforementioned drawbacks of variable-frequency control, some authors have opted for fixed-frequency PWM techniques [10]–[14]. These control methods need to detect the zero point of the inductor current. When the inductor current reaches zero, the synchronous switch is turned off to prevent an inverse inductor current. Another control strategy is to emulate the inductor current with an auxiliary circuit, and the result is the same as for the previous method [13]. In order to improve the efficiency of SBCs under light-load conditions, Wang *et al.* [14] adopted the zero-voltage switching (ZVS) technique. The key point of the control strategy is that the synchronous switch is turned on twice in a complete switching cycle; therefore, the main switch has a ZVS characteristic without considering the $v_{\rm ds}$ of the synchronous switch for the on-state. That is, the synchronous switch generates extra switching losses at the instant that the switch is turned on. In order to overcome this drawback, this paper proposes a novel control strategy.

Previous studies have proposed the use of soft-switching techniques that comprise ZVS and ZCS to improve the efficiency of buck converters. ZVS is commonly applied to computer, communication, and consumer electronics products because it eliminates the need for the switch to be turned on, a process that causes capacitive loss. These techniques generally require external active auxiliary circuits, and main switch (i.e., ZVS) operations are completed using resonance currents generated by *LC* cells. Although these techniques result in good performance, they are associated with increased device volume and circuit complexity, as well as elevated device stress [15]–[22]. Digital control techniques are also feasible solutions [23]–[25]. However, they require complex mathematical algorithms and the adoption of digital signal processors. Furthermore, the overall costs associated with such techniques are considerably high.

This study proposes a novel dual-mode control technique combined with quasi-resonant (QR) valley switching and ZVS. In the DCM region, a limit-frequency QR valley switching technique turns on the main switch to achieve ZVS to increase the efficiency of the SBC. Furthermore, this novel *limit-frequency ZVS controller (LZC) maintains the switching frequency under light-load conditions. The method requires no external auxiliary switches or passive devices containing resistors, inductors, or capacitors (*RLC*) for the SBC main switches to achieve ZVS; only logic circuits and comparators are needed. As a result, the proposed scheme possesses various advantages, such as low cost and easily built-in integrated circuits (IC). SBCs exhibiting a 40-kHz switching frequency, 25 W output power, 12-V input voltage, and 5-V output voltage were employed to verify the advantages of the proposed control technique.

Table I shows a general comparison of the dual-mode control strategies. The SBC with the proposed control strategy exhibits better performance than the other two strategies, especially with regards to the efficiency. In addition, the switching frequency is almost fixed. Therefore, it is a simple process to suppress EMI and audio noise.

The rest of this paper is organized as follows: Section II explains the concepts and operating principles of the proposed control scheme; Section III presents the design of the control circuit; Section IV gives details of the power loss analysis; Section V presents design considerations for relevant devices; Section VI presents experimental results; and Section VII gives the conclusions.

II. PROPOSED DUAL-MODE CONVERTER STRUCTURE AND OPERATING PRINCIPLES

Fig. 2(a) presents the block diagram of the proposed control scheme, including a fixed-frequency PWM controller and an LZC. To achieve ZVS while avoiding reverse inductance currents, an external current transformer and a zero-hysteresis comparator must be used when inductance current levels are less than zero in order to generate v_{Z1_O} signals to turn off the synchronous switch $(\mathrm{M_B})$. In other words, in the proposed control scheme, the SBC operating mode can be divided into a DCM and a CCM. The error signal $v_{\rm EAO}$ is generated by comparing the feedback voltage $v_{\rm FB}$ of the error compensation amplifiers with the reference voltage $V_{\rm ref}$. This signal can be used to determine the duty cycle of the main switch. In addition, $v_{\rm ZCD}$ is mainly supplied by an auxiliary winding for detecting the drain voltage of $\mathrm{M_B}$. Furthermore, the negative edge of v_{Z2_O} triggers LZC to generate $v_{\rm pulse}$ signals, which turn on $\mathrm{M_B}$ and the rest of the PWM controller to implement the valley switching of $\mathrm{M_B}$ and ZVS of the main switch $\mathrm{M_A}$. Here, $V_{\rm ref1}$ is close to $V_{\rm O}/2$.

Fig. 2(b) shows the theoretical waveform of the proposed controller, which involves DCM and CCM operations. The DCM operation is described as follows. When the inductance current drops to zero, the v_{Z1_O} signal changes from a high level to a low level in order to turn off $\mathrm{M_B}$ and prevent the occurrence of a reverse induction current. Subsequently, the LZC begins to detect valley voltages created by inductance and parasitic capacitance $(C_{\rm oss})$ resonance. To prevent the switching frequency from reaching a higher frequency, LZC generates a control signal, $v_{\rm pulse}$, for valley switching of $\mathrm{M_B}$ based on the frequency of

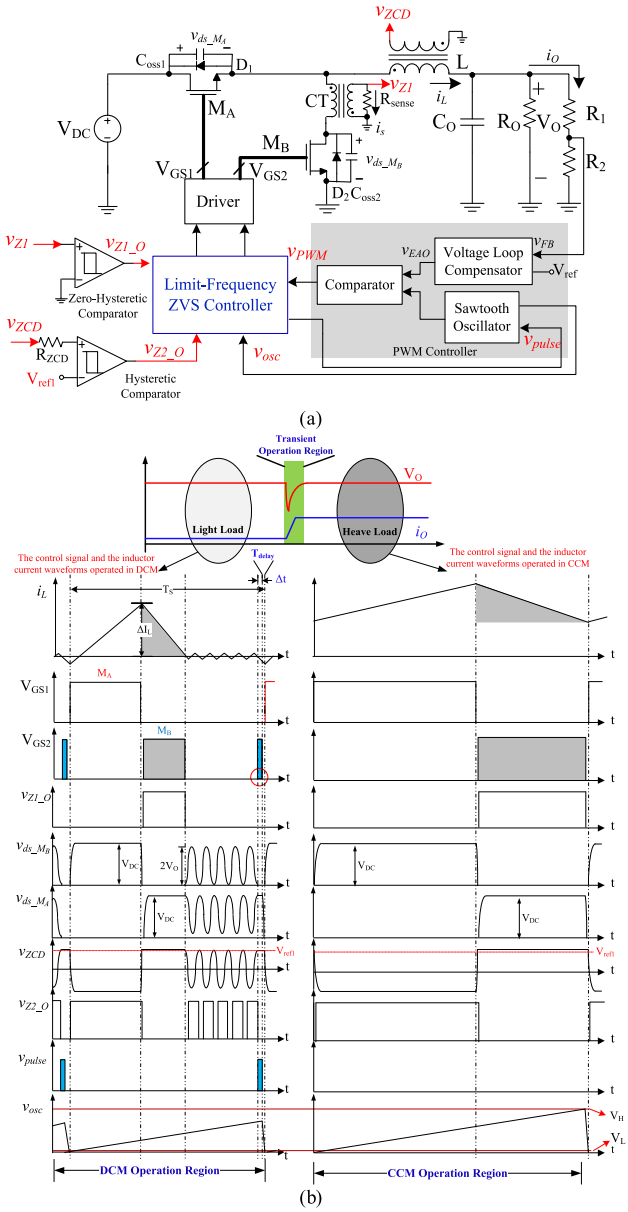

Fig. 2. (a) Proposed dual-mode control scheme and (b) key waveforms of the proposed controller.

v_{osc}. When M_B turns on after Δt, the PWM controller restarts to achieve ZVS of M_A for the next switching cycle.

The CCM operation is described as follows. As the output power increases, the operating mode of the SBCs is changed from DCM to CCM. Concurrently, the synchronous switch and the main switch are turned on complementarily. This will not be influenced by v_{Z1_O}. In conclusion, the controllers in the proposed control scheme can operate SBCs in the DCM under light-load conditions. In addition, the M_A ZVS operation becomes feasible following M_B valley conduction. During CCM operation, the LZC enters a conventional synchronous rectification control mode.

III. Circuit Implementation

QR control strategy usually has a problem about much higher switching frequency. This drawback is typically resolved by

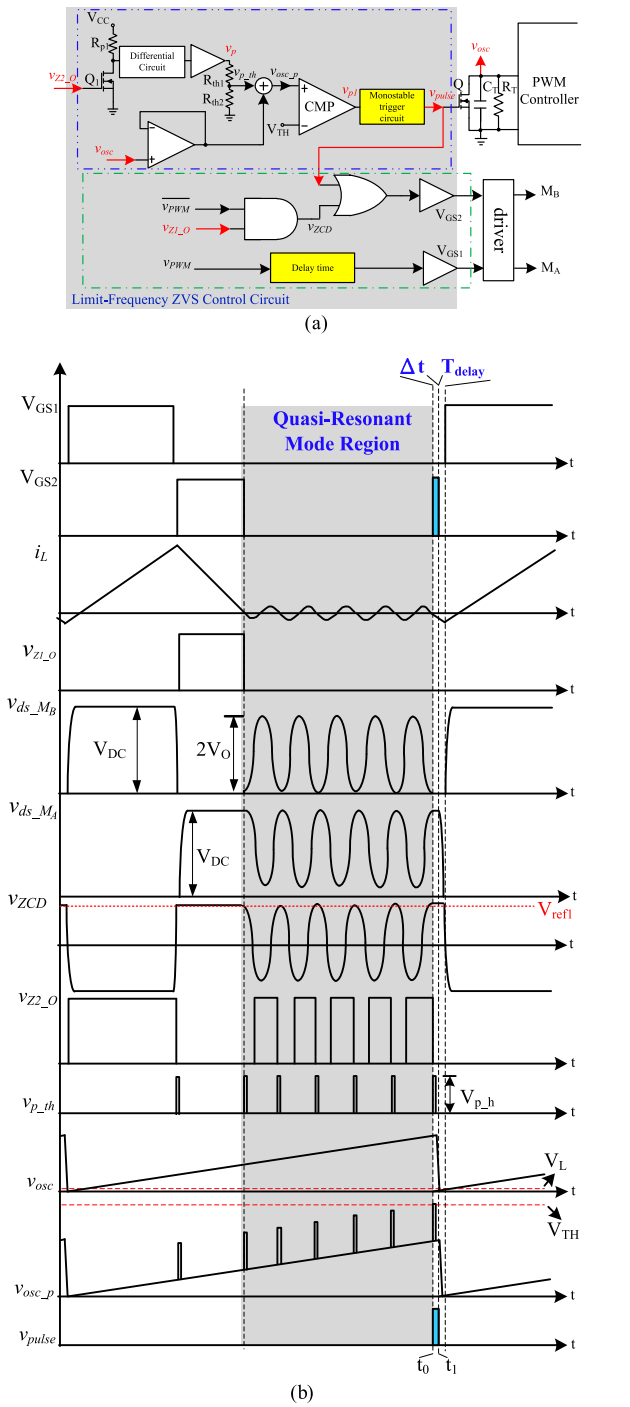

Fig. 3. (a) Proposed LZC logic circuit and (b) theoretical waveforms of the proposed LZC driver under light-load condition.

limiting the highest switching frequency, which can be done by adding a minimum off-time (during which energy is transmitted to an output load) to a switching cycle [26], [27]. Although this technique can prevent an increase in the frequency, it requires the addition of blanking time circuits and time-delay circuits, rendering the overall control circuit design more complex. Instead, this study proposes an LZC that only requires one additional pulse generator circuit to limit the maximum frequency of the QR mode (see Fig. 3). Additionally, M_A has characteristics of ZVS.

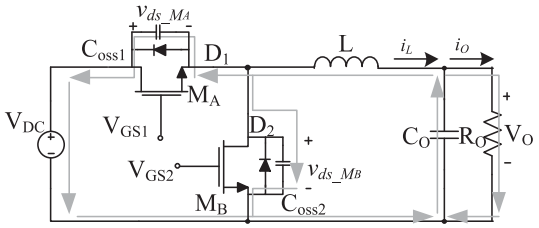

Fig. 4. SBC equivalent circuit in resonance intervals.

When the inductance current i_L drops to zero, the v_{Z1O} signal turns off $\mathrm{M_B}$ through the AND gate. In the QR mode, C_{oss} induces resonance with *L*, as shown in Fig. 3(b). When the $v_{\mathrm{ds\_MB}}$ voltage resonance reaches a valley, the v_{ZO}_2 signal immediately changes from a positive potential to a negative potential, and processing this signal using a differentiator and a resistive divider (R_{th1} and R_{th2}) yields an adjustable pulse signal v_{p_th}. To limit the maximum frequency, the PWM IC oscillator signals v_{osc} and v_{p_th} must be composed for comparison with V_{TH} to determine the valley switching timing [see Fig. 3(a)]. If the v_{soc_p} signal ($v_{\mathrm{soc\_p}} = v_{p\_\mathrm{th}} + v_{\mathrm{soc}\_p}$, where $v_{p\_\mathrm{th}} = V_{p\_h}$) is lower than V_{TH}, then the v_{pulse} signal is maintained at a low potential without influencing the operation of the oscillator. This operating mode is repeated until t_0 is achieved.

At t_0, $v_{\mathrm{ds\_MB}}$ reaches the valley in resonance. At this moment, v_{soc_p} is higher than V_{TH}. Hence, v_{pulse} changes from a low to a high level. During this transient state, $\mathrm{M_B}$ and Q are turned ON simultaneously. This causes the oscillator to discharge rapidly and the inductor starts to store energy. After t_1, $\mathrm{M_B}$ and Q are turned OFF simultaneously. Thus, the PWM controller restarts to change the designed oscillation frequency. As mentioned above, the frequency of the PWM controller increases if v_{p_th} is higher. Conversely, the frequency of the PWM controller will decrease. These results indicate that v_{p_th} can be adjusted according to the maximum switching frequency. Furthermore, the energy stored in the inductor in the previous state causes the parasitical capacitor to discharge, forcing $\mathrm{M_A}$ to achieve ZVS in the subsequent switching cycle. The following circuit design is divided into two parts—the ZVS of $\mathrm{M_A}$ and valley switching of $\mathrm{M_B}$.

A. QR Valley Switching of M_B

Fig. 4 shows an SBC-equivalent circuit in resonance intervals. In this circuit, $i_L(\mathrm{t})$ and $v_{\mathrm{ds\_MB}}(\mathrm{t})$ can be calculated as

$$i_L(\mathrm{t}) = -\frac{V_{\mathrm{O}}}{Z}\sin(\omega \mathrm{t}) \tag{1}$$

$$v_{\mathrm{ds\_MB}}(t) = V_{\mathrm{O}} - V_{\mathrm{O}}\cos(\omega \mathrm{t}) \tag{2}$$

where $\omega = \frac{1}{\sqrt{LC}}$ and $Z = \sqrt{\frac{L}{C}}$, $C = C_{\mathrm{OSS1}} + C_{\mathrm{OSS2}}$.

Fig. 5 depicts the valley switching timing, where T_S and T_r represent the switching cycle and the resonance cycle, respectively. In this study, the conduction time of $\mathrm{M_B}$ was designed to be close to the switching cycle; therefore, the controller reset time was set to t_p. The magnitude of V_{p_h} can be determined as follows:

$$V_{p\_h} = V_{\mathrm{TH}} - \frac{V_{\mathrm{osc\_peak}}}{R_{\mathrm{T}}C_{\mathrm{T}}}(T_S - T_r) \tag{3}$$

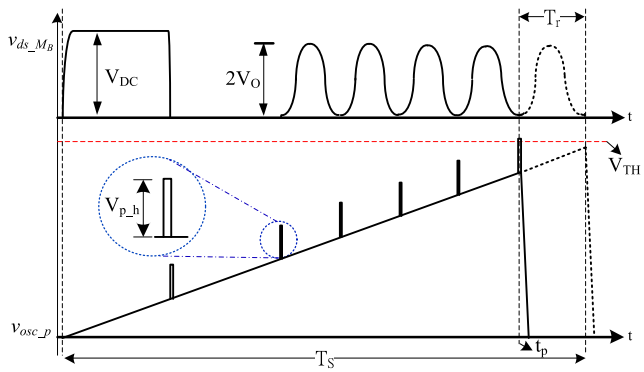

Fig. 5. SBC valley switching timing.

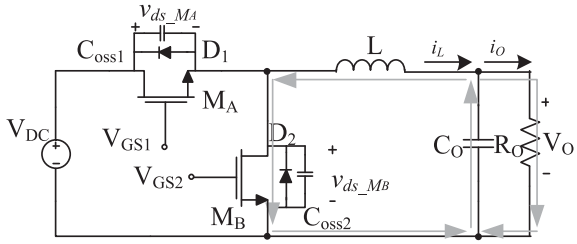

Fig. 6. SBC equivalent circuit in Δt intervals.

where $V_{\mathrm{osc\_peak}}$ is the peak voltage ($V_{\mathrm{osc\_peak}} = 3$ V) of the sawtooth waveform generated from a TL494 oscillator, $T_{\mathrm{S}} = 2\pi\sqrt{LC}$, and $V_{\mathrm{TH}} = 4.8$ V.

B. ZVS of M_A

T_{delay} and Δt of v_{pulse} need to be considered if ZVS of $\mathrm{M_A}$ is achieved. Fig. 6 presents the SBC-equivalent circuit when $\mathrm{M_A}$ is turned OFF and $\mathrm{M_B}$ is turned ON. The voltage across the inductance *L* is $-V_{\mathrm{O}}$. The inductance current i_L is expressed as follows:

$$i_L(t) = \frac{-V_{\mathrm{O}}}{L}(t - t_0). \tag{4}$$

To ensure that the $\mathrm{M_A}$ parasitic capacitance is fully discharged in order to achieve ZVS, the stored inductor energy E_{L} must be greater than the energy stored in parasitic capacitors, $E_{C\mathrm{oss1}}$. The energy storage equation is expressed as follows:

$$(i_{Lp})^2 \times L \geq C_{\mathrm{OSS1}} \times (V_{\mathrm{DC}})^2 \tag{5}$$

where i_{Lp} is the peak value of the inductance current.

Through (2) and (3), the pulse time can be determined as

$$\Delta t_{(\mathrm{min})} \geq \frac{\sqrt{LC_{\mathrm{OSS1}}} \times V_{\mathrm{DC}}}{V_{\mathrm{O}}}. \tag{6}$$

This mode is completed when $\mathrm{M_B}$ is turned OFF.

In this study, the monostable trigger circuit generates a PWM signal v_{pulse}. As shown in Fig. 7, the *RC* circuit determines the width of Δt by using the charging and discharging behavior. Therefore, Δt can be expressed as

$$\Delta t = -\mathrm{RCln}\left(1 - \frac{V_{\mathrm{TH1}}}{V_{\mathrm{CC}}}\right) \tag{7}$$

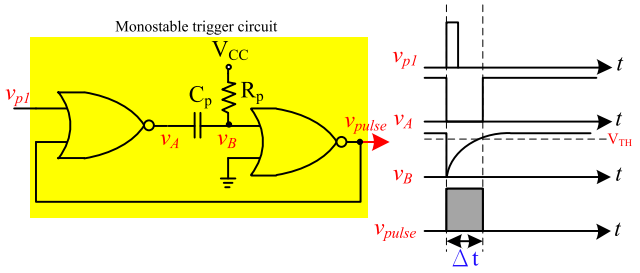

Fig. 7. Structure and control sequence of a monostable trigger circuit.

where V_{TH1} is the high-level input voltage of the NOR gate. The capacitance of C_p can be determined using

$$-R_pC_p\ln\left(1-\frac{V_{\mathrm{TH1}}}{V_{\mathrm{CC}}}\right)\geq\frac{\sqrt{LC_{\mathrm{OSS1}}}\times V_{\mathrm{DC}}}{V_{\mathrm{O}}}. \tag{8}$$

The technique of using a monostable trigger circuit to determine the pulse width of the v_{pulse} signal is thus feasible.

T_{delay} is another key point for $\mathrm{M_A}$ to achieve ZVS. After the PWM controller restarts, the $\mathrm{M_A}$ conduction time is noted because the inductance currents can become positive at any time and charge C_{oss1}, which may result in the failure of the $\mathrm{M_A}$ ZVS. Therefore, the delay time T_{delay} must be approximately one-fourth of the resonance cycle

$$T_{\mathrm{delay}}\cong\frac{2\pi\sqrt{LC_{\mathrm{OSS1}}}}{4}. \tag{9}$$

If $\mathrm{M_A}$ becomes conductive immediately after passing through T_{delay}, the ZVS operation is complete. Subsequently, a new switching cycle restarts.

IV. Power Loss Analysis

Because the aim of this study is to improve the light-load power losses of SBCs that employ conventional control strategies, the device losses are analyzed under light-load conditions. Devices, such as high-side MOSFETs, low-side MOSFETs, and inductors, cause most of the power losses in conventional SBCs. The total power losses in conventional MOSFETs can, thus, be categorized as conduction losses and switching losses. Therefore, $P^{\mathrm{Trad.}}_{\mathrm{Con.\_MA}}$ and $P^{\mathrm{Trad.}}_{\mathrm{Con.\_MB}}$ can be expressed as follows [11], [28]:

$$P^{\mathrm{Trad.}}_{\mathrm{Con.\_MA}}=\left(I^{\mathrm{Trad.}}_{\mathrm{ds,MA(RMS)}}\right)^2\times R_{\mathrm{ds,MA}} \tag{10}$$

$$P^{\mathrm{Trad.}}_{\mathrm{Con.\_MB}}=\left(I^{\mathrm{Trad.}}_{\mathrm{ds,MB(RMS)}}\right)^2\times R_{\mathrm{ds,MB}} \tag{11}$$

where $R_{\mathrm{ds,MA}}$ and $R_{\mathrm{ds,MB}}$ are the static drain–source on-resistances for MOSFET conduction.

Fig. 8 shows the switch and current waveforms for conventional SBC when it is operated in the load range of $0\,\mathrm{A}<I_{\mathrm{O}}<\Delta i_L/2$. The root-mean-square currents passing through $\mathrm{M_A}$ and $\mathrm{M_B}$ can be expressed as

$$I^{\mathrm{Trad.}}_{\mathrm{ds,MA(RMS)}}=\sqrt{\left(\frac{(\Delta i_L/2)^2}{3}+I_{\mathrm{O}}^2\right)\times D}$$

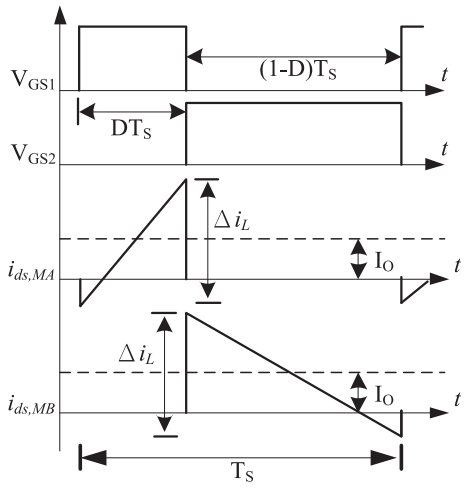

Fig. 8. Key waveform of the conventional SBC operating in CCM under light-load conditions.

and

$$I^{\mathrm{Trad.}}_{\mathrm{ds,MB(RMS)}}=\sqrt{\left(\frac{(\Delta i_L/2)^2}{3}+I_{\mathrm{O}}^2\right)\times(1-D)}$$

where I_{O} is the mean output current.

The parasitic capacitance of the MOSFETs causes V_{ds} and I_{ds} to overlap when the switch is turned on, and this problem causes turn-on switching losses. The loss of $\mathrm{M_A}$ can be expressed as follows [8]:

$$P^{\mathrm{Trad.}}_{\mathrm{Switch\_MA}}=\left(\frac{1}{2}\times V_{\mathrm{ds,MA}}\times I_{\mathrm{O}}\times T_r\times f_s\right)+\left(\frac{1}{2}\times C_{\mathrm{OSS\_MB}}\times V^2_{\mathrm{ds,MA}}\times f_s\right) \tag{12}$$

where T_r is the rise time and f_s is the switching frequency. In addition, the loss of $\mathrm{M_B}$ is similar to that of $\mathrm{M_A}$ [29], and, therefore

$$P^{\mathrm{Trad.}}_{\mathrm{Switch\_MB}}=\left(V_F\times I_{\mathrm{O}}+\left(\frac{V_F+1.1R_{\mathrm{ds,MB}}\times I_{\mathrm{O}}}{2}\right)\times I_{\mathrm{O}}\right)\times\frac{T_r}{2}\times f_s. \tag{13}$$

The proposed scheme facilitates the operation of SBCs in the DCM under light-load conditions, in which $\mathrm{M_A}$ achieves ZVS (see Fig. 9). In this operating mode, the power losses of $\mathrm{M_A}$ are mainly conduction losses [11]

$$P^{\mathrm{Nov.}}_{\mathrm{Con.\_MA}}=\left(I^{\mathrm{Nov.}}_{\mathrm{ds,MA(RMS)}}\right)^2\times R_{\mathrm{ds,MA}}. \tag{14}$$

In the DCM, the root-mean-square current passing through $\mathrm{M_A}$ can be expressed as follows:

$$I^{\mathrm{Nov.}}_{\mathrm{ds,MA(RMS)}}=\sqrt{\left(\frac{(I_{L,\mathrm{peak}})^3\times f_{s1}\times L}{3\times(V_{\mathrm{DC}}-V_{\mathrm{O}})}\right)}$$

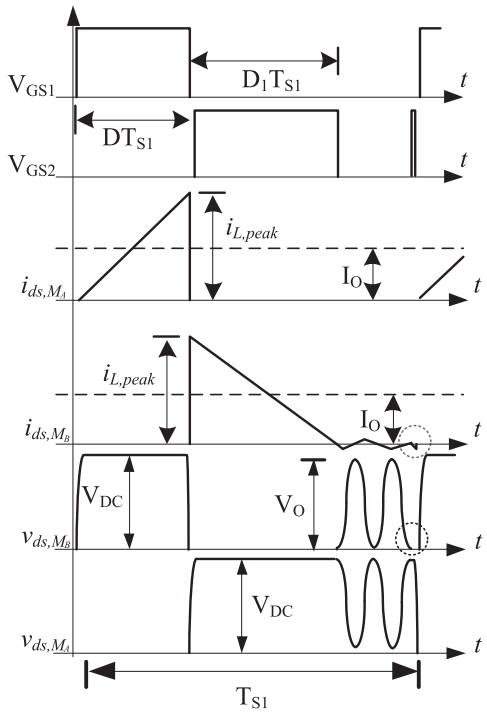

Fig. 9. Key waveform of the proposed SBC operating in DCM under light-load conditions.

where

$$I_{L,\mathrm{peak}} = \sqrt{2\left(\frac{I_{\mathrm{O}} \times V_{\mathrm{O}} \times (V_{\mathrm{DC}} - V_{\mathrm{O}})}{V_{\mathrm{DC}} \times f_{s1} \times L}\right)}.$$

However, the power losses of the low-side MOSFETs are a concern. Although the proposed control strategy enables $\mathrm{M_B}$ conduction to occur twice within a switching cycle (T_1), the second conduction time is transient, indicating that the conduction losses are negligible (given by the red dotted line in Fig. 9). Accordingly, $\mathrm{M_B}$ causes one conduction loss and two switching losses. The conduction losses of $\mathrm{M_B}$ can be expressed as follows [11]:

$$P^{\mathrm{Nov.}}_{\mathrm{Con.\_MB}} = \left(I^{\mathrm{Nov.}}_{\mathrm{ds,MB(RMS)}}\right)^2 \times R_{\mathrm{ds,MB}} \tag{15}$$

where

$$I^{\mathrm{Nov.}}_{\mathrm{ds,MB(RMS)}} = \sqrt{\left(\frac{(I_{L,\mathrm{peak}})^3 \times f_{s1} \times L}{3 \times V_{\mathrm{O}}}\right)}.$$

Next, the switching losses are analyzed. Since $\mathrm{M_B}$ conduction occurs twice in a switching cycle, switching losses can be divided into two categories. The black dotted line in Fig. 9 illustrates the first category, showing that $\mathrm{M_B}$ is controlled in the QR valley switching. Therefore, the turn-on switching loss is derived as follows [8]:

$$P^{\mathrm{Nov.}}_{\mathrm{Switch\_MB\_1}} = \frac{1}{2} \times C_{\mathrm{OSS\_MB}} \times \mathrm{V}^2_{\mathrm{ds,MB}} \times f_{s1}. \tag{16}$$

The second part of the switching loss is similar to (13), with the only difference that the switching frequency changes from f_{s} to f_{s1}. The substituted equation is as follows:

$$P^{\mathrm{Nov.}}_{\mathrm{Switch\_MB\_2}} = \left(V_F \times I_{\mathrm{O}} + \left(\frac{V_F + 1.1R_{\mathrm{ds,MB}}}{2}\right) \times I_{\mathrm{O}}\right) \times T_r \times f_{s1}. \tag{17}$$

Regarding the inductance power losses, the equivalent-series resistance (ESR) of the inductor coils is the main cause of inductance losses. The inductance losses can be approximated as follows, regardless of whether new or conventional control techniques are adopted for the SBCs

$$P_{\mathrm{Inductor}} = P_{\mathrm{winding\_losses}} + P_{\mathrm{core\_losses}}. \tag{18}$$

Here, the $P_{\mathrm{winding\_losses}}$ can be expressed as $I^2_{\mathrm{O}} \times \mathrm{ESR}_L$, and $P_{\mathrm{core\_losses}}$ can be obtained from the datasheet of magnetics vendors.

The total power losses of the SBCs produced using the novel and conventional control schemes can be expressed, respectively, as

$$P^{\mathrm{Trad.}}_{\mathrm{total\_losses}} = P^{\mathrm{Trad.}}_{\mathrm{Con.\_MA}} + P^{\mathrm{Trad.}}_{\mathrm{Con.\_MB}} + P^{\mathrm{Trad.}}_{\mathrm{Switch\_MA}} + P^{\mathrm{Trad.}}_{\mathrm{Switch\_MB}} + P_{\mathrm{Inductor}} \tag{19}$$

and

$$P^{\mathrm{Nov.}}_{\mathrm{total\_losses}} = P^{\mathrm{Nov.}}_{\mathrm{Con.\_MA}} + P^{\mathrm{Nov.}}_{\mathrm{Con.\_MB}} + P^{\mathrm{Nov.}}_{\mathrm{Switch\_MB\_1}} + P^{\mathrm{Nov.}}_{\mathrm{Switch\_MB\_2}} + P_{\mathrm{Inductor}}. \tag{20}$$

Finally, the reduced power losses of the proposed scheme can be estimated by subtracting the total losses of the proposed SBC from the total losses of the conventional SBC

$$\Delta P_{\mathrm{losses}} = P^{\mathrm{Trad.}}_{\mathrm{total\_losses}} - P^{\mathrm{Nov.}}_{\mathrm{total\_losses}}. \tag{21}$$

V. Design Consideration

The SBC design process conforms to the following circuit specifications. The input and output data specifications are as follows: input power $V_{\mathrm{DC}} = 12\,\mathrm{V}$, output power $V_{\mathrm{O}} = 5\,\mathrm{V}$, PWM controller TL494, maximum output power $P_{\mathrm{O(max)}} = 25\,\mathrm{W}$, output voltage ripple $\Delta \mathrm{V_O} = 10\%$, and switching frequency $f_s = 40\,\mathrm{kH_Z}$. General inductor designs should ensure that the inductance current maintains continuity at one-tenth of the rated current [23], [30]. The inductance value can be calculated using (23)

$$I_{\mathrm{o(min)}} = \frac{\Delta I_L}{2} = 0.1\, I_{\mathrm{O}} = 0.5\,\mathrm{A} \tag{22}$$

and

$$L_{(\mathrm{max})} = \frac{(V_{\mathrm{in}} - V_{\mathrm{O}})\, V_{\mathrm{O}} T}{V_{\mathrm{in}} \Delta I_L} = 73\,\mu\mathrm{H}. \tag{23}$$

The output filter inductance L in the prototype circuit is 73 μH. CH172060, which features high flux and is applicable to high-current outputs, is adopted in the iron core of the inductor. The inductor turns are, thus, calculated as follows:

$$N = \sqrt{\frac{L}{Al}} = 48 \tag{24}$$

where $Al = 0.032\,\mu\mathrm{H}$.

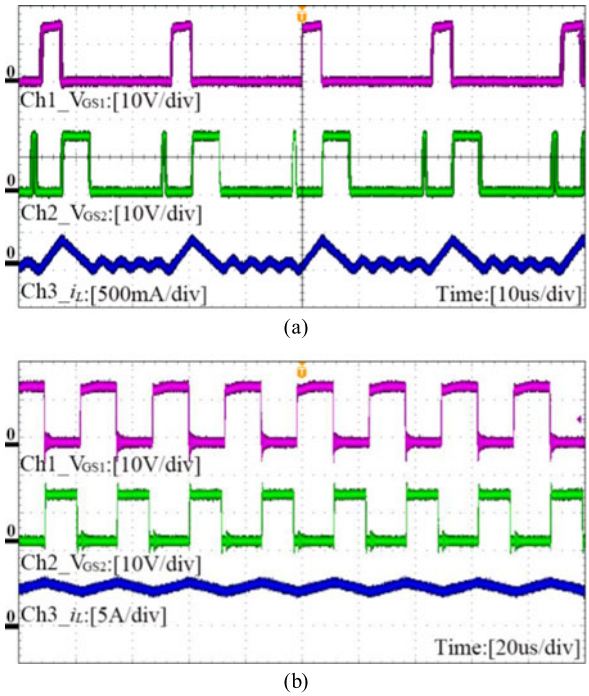

Fig. 10. (a) Light-load control signals and inductance currents and (b) heavy-load control signals and inductance currents.

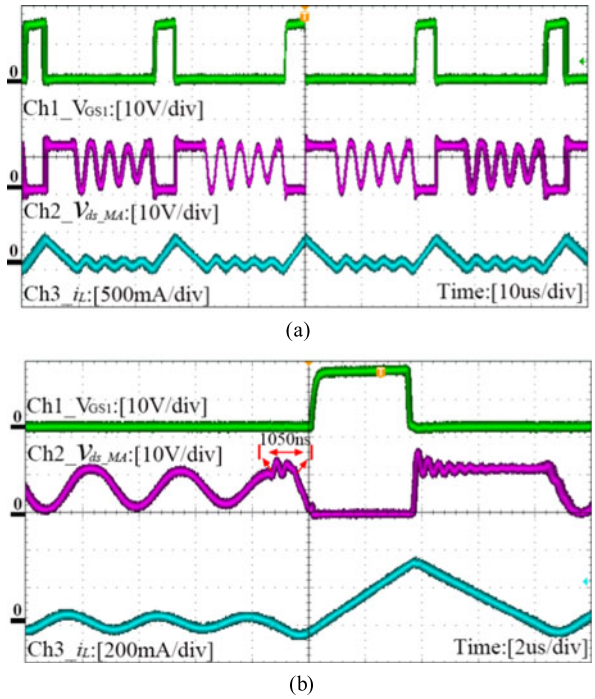

Fig. 11. (a) Key ZVS-related waveforms and (b) enlargement of ZVS-related waveforms.

The selected output capacitance $C_{\rm o}$ must satisfy the output voltage ripple requirement. Under steady-state conditions, the voltage changes caused by 20% load current variation are considered. Given the predetermined data of the output current $(I_{\rm O} = 5\,{\rm A})$ and voltage $(V_{\rm O} = 5\,{\rm V})$, the output current variation $\triangle I_{\rm o} = 1\,{\rm A}$ and output voltage variation $\triangle V_{\rm O} = 100\,{\rm mV}$ can be determined, respectively. On the basis of this result, the maximum ESR of the capacitor is estimated as follows [23], [29]:

$$\mathrm{ESR}_{\max} = \frac{100\ \mathrm{mV}}{1\ \mathrm{A}} = 100\,\mathrm{m}\Omega. \tag{25}$$

According to the aluminum electrolytic capacitor datasheet, ESR $\times$ C can be approximated to a constant number value of 50–80 μF [23], [30]. If ESR $\times\, C = 50\,\mu$F, then $C = 1000\,\mu$F. A value of 1000 μF/16.3 V is selected.

In this study, a CS097060 iron core was used as the current transformer to avoid the defect of conventional resistance (e.g., additional power losses induced by a resistance at high-current applications). Due to the zero-hysteresis comparator requires a check signal of maximum 15 V and the current transformer turn ratio is 1:50, $R_{\rm sense}$ can be determined as follows:

$$R_{\rm sense} = \frac{15}{i_s} = 150\ \Omega \tag{26}$$

where $i_s = \frac{i_O}{N} = 0.1$ A.

Two N channel MOSFET IRFB2907 were used as the SBC main switch and synchronous switch. The parasitic capacitance of the switches was 2100 pF. According to (7), $\Delta t_{(\min)} \geq$ 952 ns can be determined. The pulse-width set in this study was approximately 1050 ns. Finally, known parameters were substituted into (3) to determine the pulse voltage $(V_{p\_h} = 2\,{\rm V})$.

VI. Experimental Results

Fig. 10(a) and (b) illustrates the control signal and inductance current waveforms of the SBCs under light-load (1% load) and heavy-load (100% load) operating conditions, respectively. When the SBCs are operated in the DCM, $\mathrm{M_B}$ is turned OFF when the inductance current drops to zero to prevent the converter from causing additional losses. In addition, within a switching cycle, the second conduction of $\mathrm{M_B}$ leads to inductance charging supplying sufficient energy to complete the $\mathrm{M_A}$ ZVS operation [see Fig. 10(a)]. Fig. 10(b) shows the SBCs operating in the CCM, indicating that $\mathrm{M_A}$ and $\mathrm{M_B}$ are complementary operations identical to those of a conventional synchronous rectification control IC.

The ZVS waveform of $\mathrm{M_A}$ is shown in Fig. 11. The magnification in Fig. 11(b) shows that $\mathrm{M_A}$ conduction is achieved when the voltage $v_{\rm ds\_MA}$ drops to zero, confirming the completion of the ZVS operation. This result demonstrates that the proposed pulse width of approximately 1050 ns is applicable. Fig. 12 shows the waveform measured from the proposed QR mode at $P_{\rm O} = 0.25\,{\rm W}$. Fig. 12(a) illustrates the outcome of the generation of the pulse signal and sawtooth waveform signal $(v_{\rm soc\_p} = v_{p\_\rm th} + v_{\rm soc\_p})$, verifying that the operating frequency of the QR mode is limited at 43.5 kHz when $V_{p\_h} = 2\,{\rm V}$. In Fig. 12(b), the $v_{\rm pulse}$ signal is generated through a comparator that compares the $v_{\rm osc\_p}$ signal and the $V_{\rm TH}$ voltage when the $v_{\rm ds\_MB}$ voltage resonance reaches the valley, thereby triggering the restart of the PWM IC operation. The proposed scheme can, therefore, strongly constrain the operating frequency of the QR mode and prevent an excessively high switching frequency that is observed in conventional control methods during operation under light-load conditions.

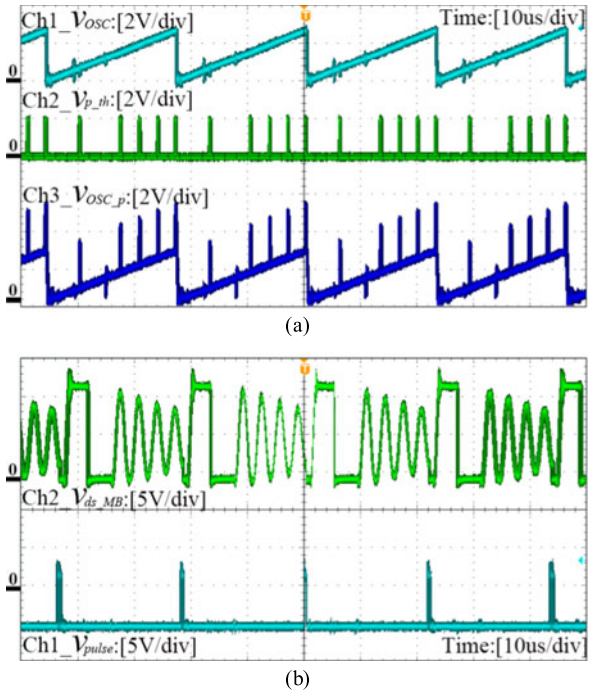

Fig. 12. (a) and (b) Key valley switching-related waveforms.

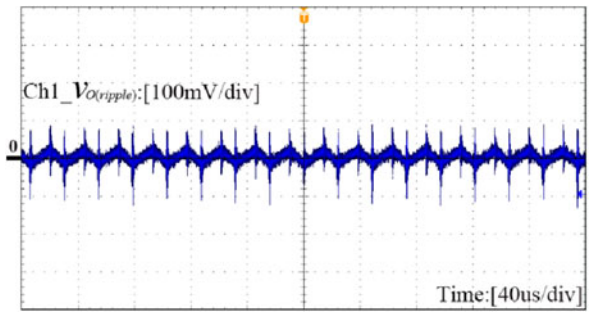

Fig. 13. Output voltage ripple waveform.

Fig. 13 shows the designed SBC output voltage ripple at approximately 100 mV, conforming to the aforementioned design conditions. The transient response of the output voltage is depicted in Fig. 14. According to the measurement results, the variation in the output voltage transient response is lower than 150 mV, regardless of whether the output power is changed from 2.5 to 25 W [see Fig. 14(a)] or from 25 to 2.5 W [see Fig. 14(b)]. In general, the design requirements of line regulation and load regulation are within $\pm 1\%$. Fig. 15 shows the experimental results of the line and load regulations. As seen from the figure, the measurement of SBC with the proposed control method was 37 mV/A when the input voltage was 7.4 V. In addition, the load regulation was still 37 mV/A when the maximum input voltage was 16.8 V. According to the experimental results, the proposed control method can meet the specifications.

It is noticed that Table II shows the SBC power loss data corresponding to (19) and (20). When $P_{\mathrm{O}} = 0.25\,\mathrm{W}$, the SBC utilizing the ZVS control strategy exhibited a loss of approximately 18 mW. In comparison, the SBC utilizing the

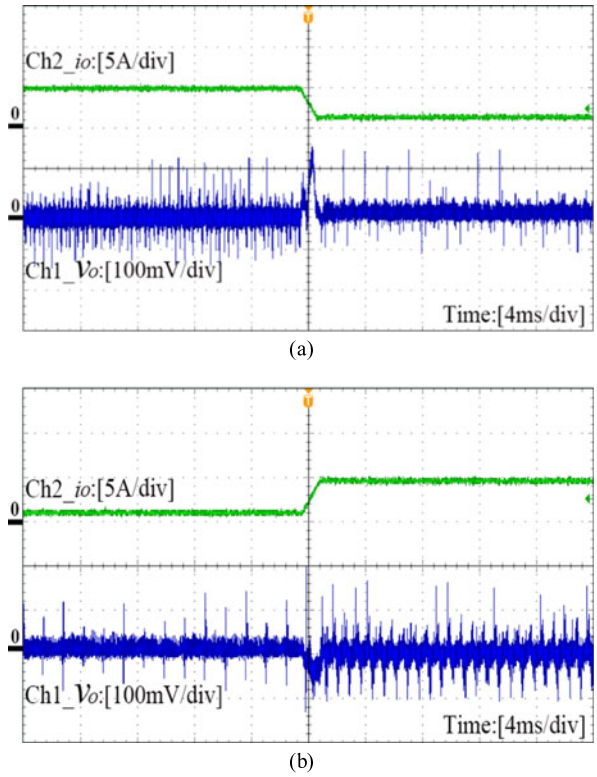

Fig. 14. Output voltage transient response (a) with light-load (10%) changed to heavy-load (100%); (V_{o}: 100 mV/div., V_{pulse}: 10 V/div., and time: 10 ms/div.) and (b) with heavy-load (100%) changed to light-load (10%); (V_{o}: 100 mV/div., V_{pulse}: 10 V/div., and time: 10 ms/div.).

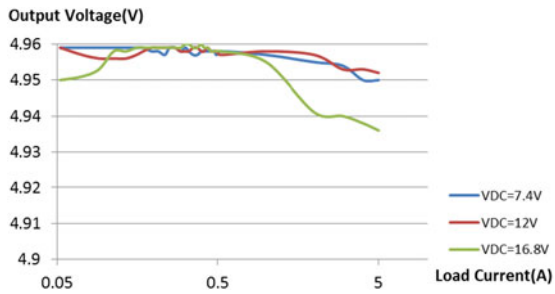

Fig. 15. Line regulation and load regulation of the proposed control scheme.

TABLE II
LOSS ANALYSIS OF THE NOVEL AND CONVENTIONAL SCHEMES

P_{O}	$P^{\mathrm{Trad.}}_{\mathrm{total\_losses}}$	$P^{\mathrm{Nov.}}_{\mathrm{total\_losses}}$	$\Delta P_{\mathrm{losses}}$
0.25 W	45 mW	18 mW	27 mW
0.50 W	60 mW	33 mW	30 mW
0.75 W	66 mW	45 mW	21 mW
1.00 W	82 mW	57 mW	25 mW
1.25 W	98 mW	67 mW	31 mW
1.50 W	112 mW	76 mW	36 mW
1.75 W	126 mW	87 mW	39 mW
2.00 W	136 mW	100 mW	36 mW
2.25 W	150 mW	130 mW	20 mW
2.50 W	172 mW	172 mW	0 W

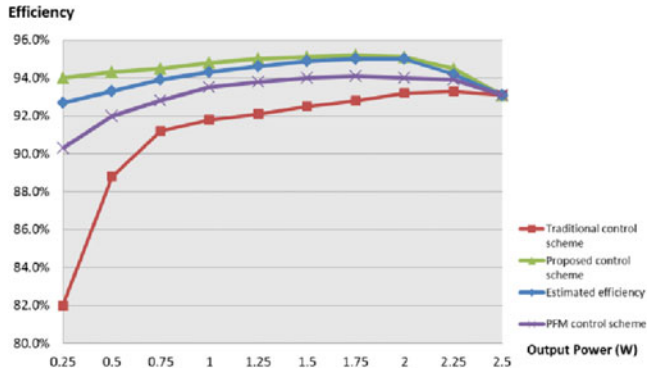

Fig. 16. Efficiency comparison between the novel and conventional scheme.

TABLE III
EFFICIENCY OF THE NOVEL AND CONVENTIONAL SCHEMES

P_O	Efficiency of the traditional SBC	Efficiency of the proposed SBC	Estimated efficiency of proposed SBC
0.25 W	82.0%	94.0%	92.7%
0.50 W	88.8%	94.3%	93.3%
0.75 W	91.2%	94.5%	93.9%
1.00 W	91.8%	94.8%	94.3%
1.25 W	92.1%	95.0%	94.6%
1.50 W	92.5%	95.1%	94.9%
1.75 W	92.8%	95.2%	95.0%
2.00 W	93.2%	95.1%	95.0%
2.25 W	93.3%	94.5%	94.2%
2.50 W	93.1%	93.1%	93.1%

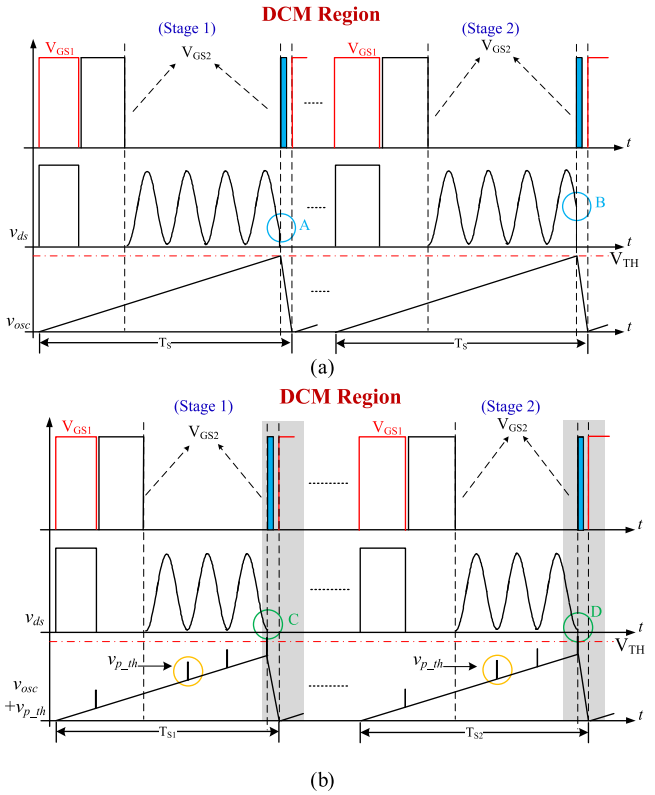

Fig. 17. (a) SBC oscillator signals $v_{\rm osc}$, control signal V_{GS2}, and $v_{\rm ds}$ of the synchronous switch from [14]. (b) SBC key signal $(v_{\rm osc}+v_{p\_th})$, control signal V_{GS2}, and $v_{\rm ds}$ of the synchronous switch with the proposed control strategy.

conventional strategy exhibited a loss of 45 mW. When the output power was approximately 2.5 W, the power losses of the two SBCs were identical.

Fig. 16 compares the efficiencies of the SBCs utilizing the novel and conventional control strategies. The blue and red lines represent the proposed control technique and the conventional control technique (with data detailed in Table III), respectively. The green line is the efficiency estimated according to the data in Table III. The yellow line in the plot shows the efficiency of the SBC with the most popular PFM technique. The experimental results confirm that the proposed control strategy can boost the light-load efficiency of SBCs considerably.

VII. CONCLUSION

In this study, a novel dual-mode control scheme suitable for SBC was developed, and the operating principle of this strategy was explained. It was then analyzed to demonstrate its efficiency. The novel control scheme mainly integrates a CCM and a DCM. In particular, when the SBC was operated in the DCM, the second synchronous switch conduction that occurred before the main switch conduction contributed to the ZVS of the main switch. In addition, composing the pulse and sawtooth waveform signals prompted the synchronous switch to achieve valley switching under limited frequency conditions. This scheme possesses the following advantages. First, it is integrated with a synchronous rectification technique to reduce the conduction losses of the converter and improve the efficiency of the overall circuit. Second, operating an SBC in the DCM can achieve ZVS in the main switch without requiring additional auxiliary switches or passive devices comprising an *RLC*. The simple pulse generators are employed to limit the highest switching frequency of the quasi-resonant mode. Finally, in the Appendix, a comparison between the proposed control method with variable-switching frequency and the control method with constant-switching frequency presented in [14] is provided.

APPENDIX

The purpose of this paper and [14] is to improve the efficiency when the SBC operates under light-load conditions. The analysis of the control strategy is described when the SBC operates under light-load conditions. Fig. 17(a) shows the waveforms of key control signals and $v_{\rm ds}$ of the synchronous switch for the SBC control strategy [14]. This technique utilizes the fixed-frequency control strategy. In state1, in order to achieve ZVS of the SBC main switch, the synchronous switch has to turn on at point A. In the same switching period, when the load condition changes from state1 to state2, the $v_{\rm ds}$ of the synchronous switch changes with the variation of loading as well (from point A to point B). This result causes switching losses in the synchronous switch. The losses can be expressed as [8]

$$P_{\rm Switch\_loss}=\frac{1}{2}\times C_{\rm OSS}\times v_{\rm ds}^2\times f_s \tag{27}$$

TABLE IV
KEY LOSS ANALYSIS OF THE NOVEL AND [14] SCHEMES

V_{DC}	V_O	P_O	$P_{in}^{[14]}$	$P_{in}^{Nov.}$	$v_{ds\_SR\_second}^{[14]}$	$P_{SR\_second\_losses}^{Ref.[14]}$	$v_{ds\_SR\_second}^{Nov.}$	$P_{SR\_second\_losses}^{Nov.}$	$\Delta P_{losses}^{Estimated}$	$\Delta P_{losses}^{measured}$
12 V	5 V	0.35 W	0.382 W	0.375 W	8 V	3.20 mW	1.0 V	0.05 mW	3.15 mW	7.0 mW
12V	5 V	0.70 W	0.737 W	0.731 W	9 V	4.02 mW	1.0 V	0.05 mW	4.00 mW	6.0 mW
24 V	12 V	1.35 W	1.428 W	1.407 W	20 V	20.0 mW	5.0 V	1.30 mW	19.0 mW	21.0 mW
24 V	12 V	2.77 W	2.862 W	2.845 W	21 V	22.1 mW	4.0 V	0.91 mW	21.1 mW	17.0 mW

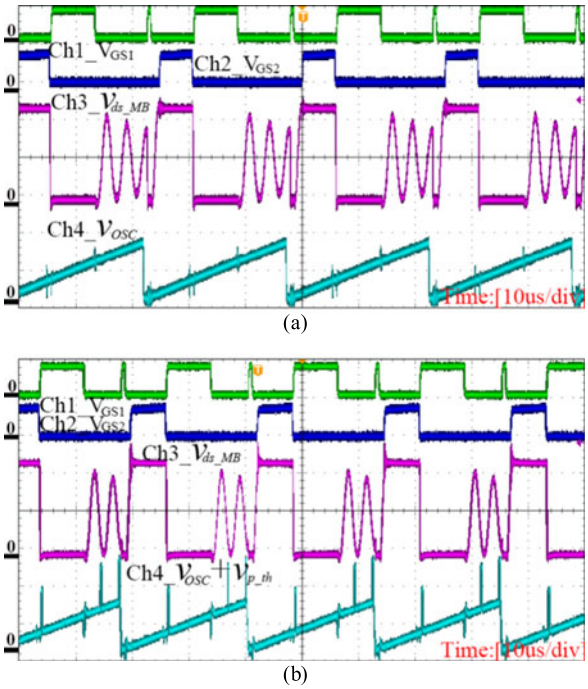

Fig. 18. Waveforms of V_{GS1}, V_{GS2}, v_{ds_MB}, and key oscillator signals for (a) [14] and (b) proposed SBC (Ch1: 20 V/div., Ch2: 20 V/div., Ch3: 5 V/div., and Ch4: 2 V/div.)

where

$v_{ds}(t) = V_O - V_O \cos(\omega t)$ and C_{OSS} is the parasitic capacitance of the synchronous switch.

According to the description above, the control strategy [14] causes extra switching losses. This paper provides a frequency-limited QR control strategy to overcome this disadvantage. Fig. 17(b) shows the waveforms of key control signals and v_{ds} of the synchronous switch for the SBC using the proposed control strategy. The purpose of this technique is to control the synchronous switch to turn on by using v_{p_th} at point C for valley switching (state1). In state2, although the heavier loading makes the v_{ds} valley duration different from the previous state, v_{p_th} can still trigger the synchronous switch at point D. That is, if the synchronous switch's valley is generated in the gray region, the valley turn-on of the synchronous switch can be assured under the frequency-limited condition.

The following experimental results from these two control strategies utilize the designed components in the paper. The only difference was that the switching frequency of the control strategy from [14] was fixed at 40 kHz. The key measured waveforms of the two control strategies for the SBC are shown in Fig. 18 (the output power was 0.7 W). Fig. 18(a) shows that the v_{ds} of the synchronous switch with the control strategy from [14] was 9 V. Based on (27), the switching loss was about 4.05 mW. Fig. 18(b) shows the proposed control strategy. The figure shows that the proposed method can lower the v_{ds} of the synchronous switch ($v_{ds} = 1$ V), and the switching frequency was restricted to about 43.5 kHz. Compared with the previous strategy, the proposed technique can save about 4 mW in switching losses. Table IV provides the measured efficiency of the SBC using a power analyzer PM1000. In this paper, the input and output power under two different voltage specifications are measured. According to the experimental results, the increment of the output voltage causes v_{ds} of the synchronous to increase. If the synchronous switch is not turned on at the valley, the switching losses will be more serious. This result is the disadvantage of [14].

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