A PSR CC/CV Flyback Converter With Accurate CC Control and Optimized CV Regulation Strategy

Zeyu Wang, Xinquan Lai, and Qiang Wu

***Abstract*—This paper presents a primary-side regulation constant current constant voltage (CC-CV) Flyback ac–dc converter characterized by high efficiency and high precision of constant current control. In CC mode, a novel ring detection and demagnetization portion control technique is proposed, with which the ending time of demagnetization can be accurately determined and the portion of demagnetization in switching periods remain precisely the same, which enable the accuracy of constant current output that can reach a level as high as $\pm 0.8\%$. In CV mode, a power stage model based on steady-state analyzing method is established, according to which the expression of static power loss is first obtained. After that total power loss expression including switching loss is derived as well. By MATLAB simulation, power loss mechanism is revealed and analysis is made in detail. According to which, optimized parameters of Flyback converter system and an effective CV regulation strategy are obtained eventually. Simulation as well as experimental results verifies the efficiency of the ac–dc converter system after optimization that can be more than 84.7% at 5 V/1 A application.**

***Index Terms*—Discontinuous conduction mode (DCM), efficiency, model, optimization, ring detection and demagnetization portion control (RD-DPC).**

I. Introduction

In RECENT years, battery charging strategy has been widely researched and explored. With a view to high efficiency, costless, and small in size, primary-side regulation (PSR) Flyback ac–dc converter characterized by constant current constant voltage (CC-CV) is widely used in charger systems as well as adaptors of electronic products. Fig. 1 shows the topology of the proposed PSR CC-CV Flyback ac–dc converter system.

As shown in Fig. 1, when M_1 is ON, the current flows through primary-side inductor and the energy is stored in it. When M_1 is OFF, energy stored in primary-side inductor then transfers to the secondary side with the secondary current starts to decrease from a peak value, the mean value of the secondary current in one switching period is defined as the output current.

Fig. 2 presents the operating processes of the proposed CC/CV converter, as shown in the figure, there are three sequential processes after power-ON. They are start-up state, constant current regulation state, and constant voltage regulation state. In the start-up state, the inner low-voltage power supply as well as bias conditions would be set up. After that, system enters CC mode, during this process, the converter system outputs an accurate large current to quick charge loading equipment. When the output voltage is charged very close to the set value, the constant current regulation mechanism releases the control of the converter system to constant voltage regulation process.

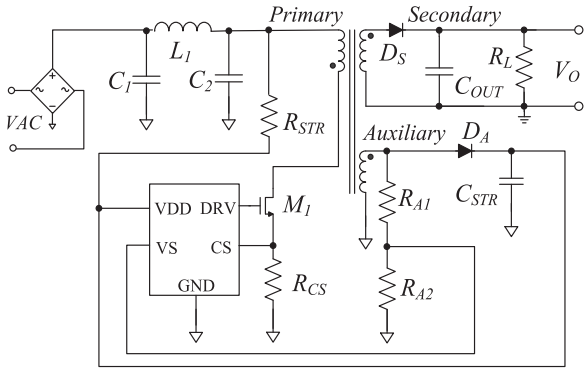

Fig. 1. Topology of the proposed Flyback converter.

Among the operation processes mentioned above, the accuracy of constant output current control in CC mode and the transfer efficiency in CV mode are the two problems that mostly concerned. For the first one, the current flows through R_L should be constant and large enough, so as to quick charge a battery, if not, it will do harm to and shorten the life of the battery. As to the second problem, low transfer efficiency signifies a large energy consumption, quite a number of input power is converted to heat energy and gives rise to an increment of temperature, which is unacceptable and should be inhibited. Hence, to research a high accurate constant current control method as well as an effective CV regulation strategy is of great significance.

In the case of CC control method, several works have been done currently, for one mainstream solution is to control the primary-side current [1], [2]. Referring to Fig. 1, which detects the peak current of the primary side at each switching cycle through a sampling resistor $R_{\rm CS}$, for there is a linearly relationship between the peak primary current and the voltage across resistor $R_{\rm CS}$ named $V_{\rm CS}$. Then, making a comparison of voltage $V_{\rm CS}$ with a reference voltage, when $V_{\rm CS}$ is greater than the reference voltage, M_1 is turned OFF and the current would be constant by this means. This method is easy to realize, while, the value of sampling resistor $R_{\rm CS}$ varies a lot with process, which lead

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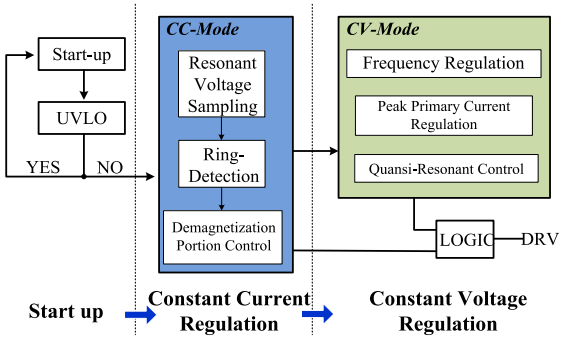


Fig. 2. Operating process of the proposed converter system.

to the control circuit unable to regulate the error immediately cause by process deviation, and the precision of output current is low and hard to control as a result. To solve this problem, another method is proposed [3]–[5]. As the output current of a Flyback converter working at discontinuous conduction mode (DCM) can be expressed as

$$I_{\mathrm{OUT}} = \frac{1}{2} \cdot I_{\mathrm{PP}} \cdot \frac{N_P}{N_S} \cdot \frac{t_{\mathrm{DM}}}{T} \tag{1}$$

where I_{OUT} is output current, I_{PP} signifies the peak primary current, N_P/N_S is the turns ratio of the transformer, T is switching period, and t_{DM} is demagnetization time which is equal to the conduction time of the secondary side. For I_{PP} and N_P/N_S are predetermined, and the beginning time of demagnetization is the moment when M_1 is been turned OFF, therefore, the only problem to realize high precision output current is to determine the ending time of demagnetization so as to make the ratio of t_{DM}/T unchangeable. Referring to Fig. 1, as the auxiliary voltage starts a damped oscillation process when secondary current decreases to zero, the ending time of demagnetization could be defined as the moment when the voltage at VS pin reaches zero, and t_{DM} is obtained in this way. This method is good theoretically, but the resonant period error caused by the output power and the frequency will reduce the accuracy of the secondary-side current averaging measurement [6].

To overcome the drawbacks mentioned above, ring detection and demagnetization portion control (RD-DPC) technique is proposed in this paper. This control strategy is used to precisely detect the ending time of demagnetization based on the resonance of secondary leakage inductor and capacitor. In this way, the influence of process deviation can be eliminated, and there will be no effect on the control accuracy, neither does output power nor switching frequency. For the secondary resonance is a damped oscillation, it is convinced that the ending time of demagnetization is the time when the resonance amplitude is smaller than a given reasonable value. In this way, the time when the secondary current decreases to zero is accurately determined. Consequently, a high precision constant current control is achieved without adopting expensive devices or complicated structures, which is of great importance for low-cost application.

At the end of CC process, system enters CV mode, where efficiency improvement is the most concern. Traditional ways to improve the transfer efficiency are to utilize better devices for they are of less power consumption, or to adopt other circuit structures to improve transfer efficiency [7]–[9], such as taking synchronous rectification technique to reduce energy consumption caused by rectifier diode, or replacing RCD structure with active clamp, so that part of energy stored in leakage inductor is able to be reused in the next switching period. Another familiar approach is to adopt complicate control mechanism [10]–[14]. There is no doubt that all the alike methods contribute to efficiency improvement, however, they result in large resource consumption and lead to various unreliability, which undoubtedly opposes the principle of reliable and cost saving. To overcome the limits of the methods mentioned above, it is important to analyze the effects that different parameters have on the power loss, so as to provide a fundamental solution to improve transfer efficiency. At present, several research works have been lead to illustrate the losses in a Flyback converter system [15], [16]. Nevertheless, the existing models focus their attentions on the single devices or part of the system, as for an analysis from the view of whole system has seldom been made. In the CV part of the paper, a power stage model of Flyback converter system is established according to steady-state analysis. Based on which, losses caused by different parameters are analyzed quantitatively, after that, optimized values of these parameters are determined and an optimized CV regulation strategy is derived.

The paper is organized as follows. The proposed RD-DPC technique is presented in Section II. Power stage modeling, power loss analysis, and optimized CV regulation strategy are presented in Section III. Simulation, experimental results, and discussions are given in Section IV. Finally, conclusions are drawn in Section V.

II. CC Process

Fig. 3 gives the simplified circuits of the states for a Flyback ac–dc converter working in DCM in one switching period.

As to the energy store state, shown in Fig. 3(a), switch S is closed, there is a current flows through primary-side inductor and switch S to ground, with electric energy stored in primary side during this state. At the same time, when D_S and D_A are at the reverse blocking state, there is no current flowing through the secondary side or the auxiliary side. Assuming that the value of primary-side inductor is L_P, input voltage is V_{IN}, switching period is T, the conduction duty cycle of switch S is D_1, then the peak primary current can be derived as

$$I_{\mathrm{PP}} = \frac{V_{\mathrm{IN}}}{L_P} \cdot D_1 \cdot T. \tag{2}$$

When switch S is open, D_S and D_A are forward conductive, as shown in Fig. 3(b), the energy stored in the previous state transfers to both secondary side and auxiliary side. As to the secondary side, C_{OUT} is being charged and V_{OUT} being established with decrease in secondary current starts to decrease from a peak value to zero. For the auxiliary side, C_A is being charged with the voltage V_A slowly decreasing until I_A equals zero. Assume N_P, N_S, and N_A are the turns number of primary side, secondary side, and auxiliary side respectively, then we have

$$I_{\mathrm{PP}} \cdot N_P = I_{\mathrm{SP}} \cdot N_S + I_{\mathrm{AP}} \cdot N_A \tag{3}$$

$$V_A = \frac{N_A}{N_S} \cdot V_S \tag{4}$$

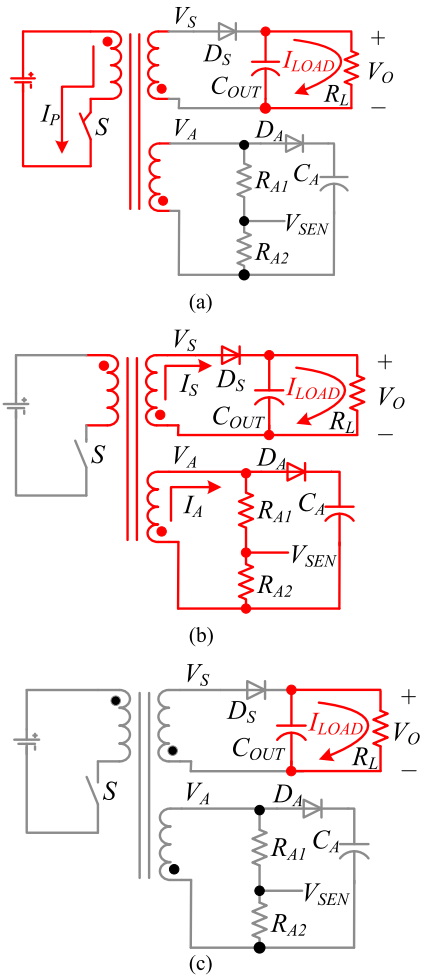


Fig. 3. Operation states in DCM in one switching period. (a) Energy store state. (b) Energy transfer state. (c) Resonant state.

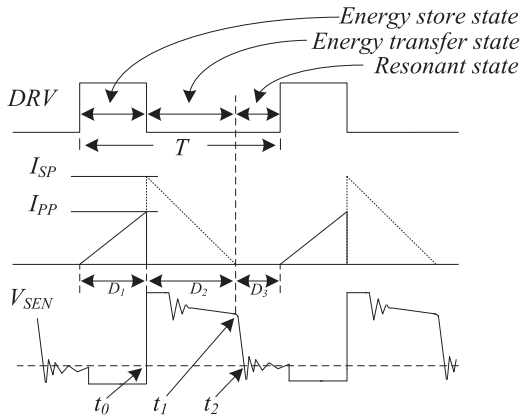


Fig. 4. Main waveforms of the three states.

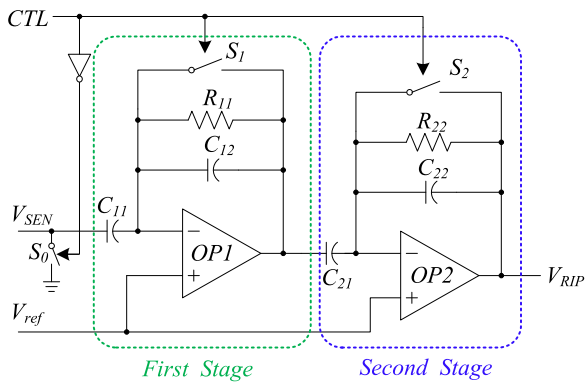


Fig. 5. Ring amplification of RD.

where $I_{\rm SP}$ is the peak secondary current, $I_{\rm AP}$ is the peak auxiliary current, V_S is the secondary voltage, and V_A is the auxiliary voltage.

At the end of the energy transfer state as shown in Fig. 3(c), currents I_S and I_A decrease to zero, then system enters damped resonant state. In this state, the magnetizing inductor oscillates with the parasitic capacitors. Fig. 4 gives the main waveforms of the three states.

In Fig. 4, D_2 is the conduction duty cycle of secondary side, D_3 is the duty cycle of resonant state, time t_0 is the moment when switch S is turned OFF, t_1 is the moment when secondary current reaches zero, namely, the ending time of energy transfer state, so that, the duration time of demagnetization process is

$$t_{\rm DM} = t_1 - t_0. \tag{5}$$

As has expressed in (1), to make a constant ratio of $t_{\rm DM}/T$ is the key to realize high precision of constant current output. In order to achieve this purpose, two steps named RD and DPC are indispensable.

A. RD Process

RD process composes two sequential steps, ring amplification and ring discrimination. Fig. 5 shows the design scheme of the ring amplification, which is a two-stage switched-capacitor amplifier. The first stage acts as a ripple amplifier, the second stage acts as a buffer, and $V_{\rm ref}$ is a bias voltage, making its value close to the central point of input common mode range of *OP1* when designing the amplifier. CTL is a control signal, the frequency of which is gradually increasing in CC mode when operation. Bias condition of the detector is established when CTL is high, with switches $\rm S_1$, $\rm S_2$ are closed and $\rm S_0$ is open. On the contrary, when CTL turns low, switches $\rm S_1$ and $\rm S_2$ are open and $\rm S_0$ is closed, the detector then amplifies the ring part of signal $V_{\rm SEN}$.

The transfer function of the detector can be expressed as

$$H(s) = \begin{cases} 1, & \text{CTL} = 1 \\ -\dfrac{R_{11} \cdot C_{11} \cdot s}{R_{11} \cdot C_{12} \cdot s + 1}, & \text{CTL} = 0 \end{cases} \tag{6}$$

where C_{11} acts as a stopping capacitor, making only high-frequency part of signal $V_{\rm SEN}$ goes through and be amplified, R_{11} is dc feedback component of the amplifier, and C_{12} forms the alternating current path when switch S_1 is open.

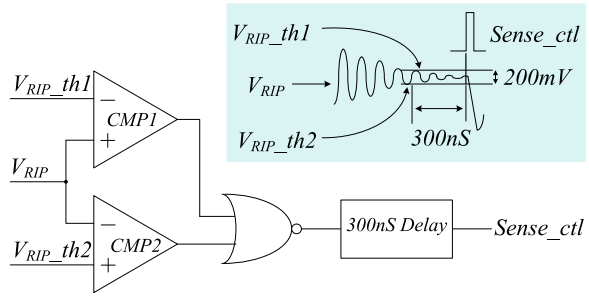


Fig. 6. Ring discrimination.

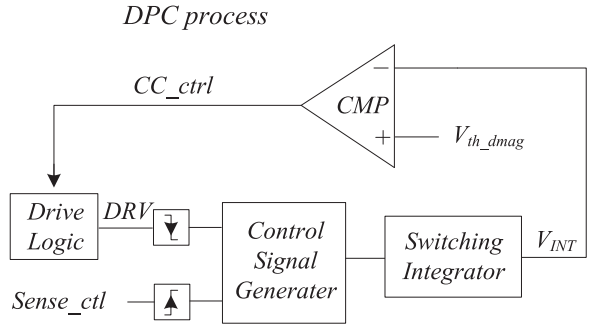


Fig. 7. Control strategy of DPC.

According to (6), setting the values of C_{11} and C_{12} to obtain a proper gain, say *M*, of the detector, then the ring part of $V_{\rm SEN}$ is amplified by *M* times and output voltage $V_{\rm RIP}$.

Fig. 6 shows the design scheme of ring discrimination. The voltage $V_{\rm RIP}$ got previously is then compared with two threshold voltages of 200 mV differ in amplitude. If $V_{\rm RIP}$ lies between the two threshold voltages for a relatively long time, it is convinced that the secondary current has decreased to a very small value close to zero, and this moment is considered to be the most accurate ending time of demagnetization, namely, the ending time of the secondary-side conduction.

In Fig. 6, $V_{\rm RIP}$_th1 and $V_{\rm RIP}$_th2 are two threshold voltages, $V_{\rm RIP}$_th1 is equal to $V_{\rm ref}$ + 100 Mv and $V_{\rm RIP}$_th2 equals $V_{\rm ref}$ − 100 mV. The rising pulse named *Sense_ctl* is generated 300 ns after $V_{\rm RIP}$ lies between the two threshold voltages, indicating the secondary current is about to decreasing to zero. So that, the duration of demagnetization process in a switching period is determined by the falling edge of signal DRV and the rising edge of signal *Sense_ctl*.

B. DPC Process

Fig. 7 shows the control strategy of DPC, where $V_{\rm th\_demag}$ is a threshold voltage, and the relationship between output current and V_{th_demag} is

$$I_O = \frac{V_{\rm IN}\cdot T}{2}\cdot\sqrt{\frac{1}{L_P\cdot R_L}} \cdot\left[\frac{N\cdot V_{\rm OUT}\cdot(V_{\rm th\_demag}-V_L)}{V_{\rm IN}\cdot(V_{\rm th\_demag}-V_L)+N\cdot V_{\rm OUT}\cdot(V_H-V_L)}\right]^2. \tag{7}$$

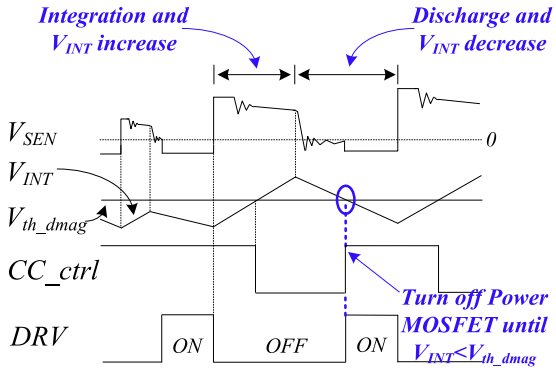


Fig. 8. Schematic diagram of DPC control.

Making DRV and *Sense_ctl* as the control signals of an integrator, which starts to integrate on the falling edge of signal DRV and stops on the rising edge of signal *Sense_ctl* every switching period, so that the integration time equals the demagnetization time.

The integration function is given by

$$V_{\rm INT} = k\cdot\int_{t_{\rm DM}} V_{\rm CONST}\cdot dt = k\cdot V_{\rm CONST}\cdot t_{\rm DM} \tag{8}$$

where *k* is an integration constant and $V_{\rm CONST}$ is the voltage for integration. From (8), the integrator output voltage $V_{\rm INT}$ has a linear relationship with the demagnetization time of a switching period. Fig. 8 presents the waveforms of the DPC control technique.

From Figs. 7 and 8, the integrator output voltage $V_{\rm INT}$ is compared with a threshold voltage $V_{\rm th\_dmag}$. If the portion of demagnetization is smaller than the target value, $V_{\rm INT}$ is smaller than $V_{\rm th\_dmag}$, the comparator outputs high, with the drive logic block starts to generate a DRV pulse to start a new switching period, otherwise, DRV pulses generated by drive logic are blocked and the primary-side switching power MOSFET remains closed until $V_{\rm INT}$ is discharged below the voltage of $V_{\rm th\_dmag}$. By this means, the demagnetization portion of a switching period can be remains constant, and constant output current is achieved eventually.

III. CV Process

At the end of constant current mode, the output voltage reaches the set value, system then enters constant voltage regulation mode automatically.

A. Steady-State Power Stage Modeling

As have been analyzed previously, there are three states when operating in DCM mode. Fig. 9 shows their equivalent circuits. Particularly, as shown in Fig. 19(b), the model of rectifier diode in secondary side can be built according to [17] and [18], where V_F is the forward voltage drop of the rectifier diode.

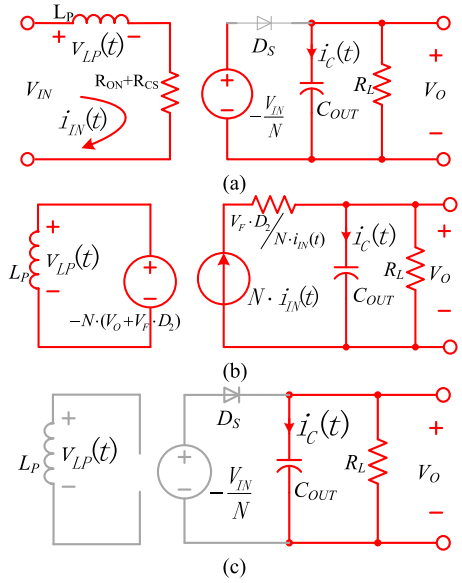


Fig. 9. Equivalent circuits of three states in DCM mode. (a) Energy store state. (b) Energy transfer state. (c) Resonant state.

As shown in Fig. 9, assuming the voltage across L_P is $v_{\mathrm{LP}}(t)$, the current flow through C_{OUT} is $i_C(t)$, as to Fig. 9(a), there is

$$\begin{cases} v_{\mathrm{LP}}(t) = V_{\mathrm{IN}} - i_{\mathrm{IN}}(t) \cdot (R_{\mathrm{ON}} + R_{\mathrm{CS}}) \\ i_C(t) = -\frac{V_O}{R_L} \end{cases} \tag{9}$$

as for Fig. 9(b), we have

$$\begin{cases} v_{\mathrm{LP}}(t) = -N \cdot (V_O + V_F \cdot D_2) \\ i_C(t) = N \cdot i_{\mathrm{IN}}(t) - \frac{V_O}{R_L} \end{cases} \tag{10}$$

for Fig. 9(c),

$$\begin{cases} v_{\mathrm{LP}}(t) = 0 \\ i_C(t) = -\frac{V_O}{R_L}. \end{cases} \tag{11}$$

Ignoring the ripples of $v_{\mathrm{LP}}(t)$ and $i_C(t)$ compared with their dc components V_{LP} and I_C, and basing on the voltage-second balance principle, there is

$$\begin{aligned} v_{\mathrm{LP}}(t) = {} & D_1 \cdot V_{\mathrm{IN}} - D_1 \cdot (R_{\mathrm{ON}} + R_{\mathrm{CS}}) \cdot I_{\mathrm{IN}} \\ & - N \cdot V_F \cdot {D_2}^2 \cdot -N \cdot D_2 \cdot V_O = 0. \end{aligned} \tag{12}$$

As to (12), it is obtained by using Kirchhoff voltage law to find the primary-side inductor voltage during each state in one switching period. The result is averaged and set to zero, which also states that the sum of three terms having the dimensions of voltage are equal to $v_{\mathrm{LP}}(t)$ or zero. Hence, (12) is of the same form as a loop equation. In particular, it describes the dc components of the voltage around a loop containing the primary-side inductor, with loop current equal to the input dc inductor current I_{IN}. Therefore, a mesh circuit corresponding to (12) is able to be constructed as shown in Fig. 10(a). Both the first and third terms in (12) are dc input voltages, so voltage sources of value $D_1 \cdot V_{\mathrm{IN}}$ and $N \cdot {D_2}^2 \cdot V_F$ are introduced, respectively. For the second term, resistance of value $D_1 \cdot (R_{\mathrm{ON}} + R_{\mathrm{CS}})$ is able to well match the voltage drop of the corresponding term.

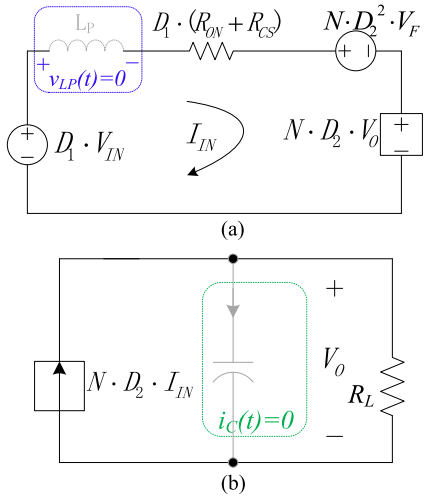


Fig. 10. Equivalent mesh circuits. (a) Mesh circuit corresponding to (12). (b) Mesh circuit corresponding to (13).

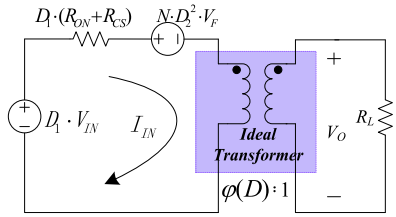


Fig. 11. Equivalent model of Flyback converter.

With regard to the forth term, it depends on the output voltage, thus, a dependent voltage source is appropriate.

In the same way, according to the principle of charge conservation, there is

$$\left(-\frac{V_O}{R_L}\right) \cdot D_1 + \left(N \cdot I_{\mathrm{IN}} - \frac{V_O}{R_L}\right) \cdot D_2 + \left(-\frac{V_O}{R_L}\right) \cdot D_3 = 0 \tag{13}$$

by using Kirchoff current law, the corresponding circuit of (13) can be conducted as in Fig. 10(b).

By combining the circuits of Fig. 10(a) and (b) into a single circuit, an equivalent but more physically meaningful model is derived in Fig. 11.

In Fig. 11, $\phi(D)$ is the equivalent conversion ratio, which expression is given as

$$\phi(D) = N \cdot D_2 \tag{14}$$

As shown in Fig. 11, the steady-state model of Flyback ac–dc converter operating in DCM is constructed with consideration of the power consumption caused by sampling resistance, the conduction loss of power switching MOSFET, and the rectifier diode. Compared with models mentioned in [19] and [20], the model constructed avoids complicated calculation of small signals and keep a relatively high accuracy when dealing with static power loss.

B. Loss Analysis

Based on the model derived, it is able to analysis the loss mechanism when operation. By converting secondary side to primary side, $I_{\rm IN}$ can be written as

$$I_{\rm IN} = \frac{D_1 \cdot V_{\rm IN} - N \cdot {D_2}^2 \cdot V_F}{D_1 \cdot (R_{\rm ON} + R_{\rm CS}) + \varphi^2(D) \cdot R_L} \tag{15}$$

hence, the static power loss is

$$P_{\rm LOSS\_static} = {I_{\rm IN}}^2 \cdot D_1 \cdot (R_{\rm ON} + R_{\rm CS}) + I_{\rm IN} \cdot N \cdot {D_2}^2 \cdot V_F \tag{16}$$

where according to the principle of conservation of energy, D_1 and D_2 have the following relationship:

$$D_2 = D_1 \cdot \sqrt{\frac{V_{\rm IN}}{N \cdot V_O}} \tag{17}$$

besides, according to the analysis in [21] and [22], an equivalent expression of switching loss can be written as

$$P_{\rm LOSS\_switching} = \frac{1}{6} \cdot V_{\rm DS\_max} \cdot {t_r}^2 \cdot \frac{V_{\rm IN}}{L_P} \cdot (t_r + t_f) \cdot f_{\rm SW} + \frac{1}{2} C_{\rm OSS} \cdot {V^2}_{\rm DS\_max} \cdot f_{\rm SW} \tag{18}$$

where $V_{\rm DS_{max}}$ is the transient maximum drain voltages when the power MOSFET is turned OFF, to simplify the calculation, and $V_{\rm DS_{max}}$ is approximately equals to $(V_{\rm IN} + N * V_{\rm OUT} + N * V_F)$. t_r and t_f are the rising and falling time of the drive signal, respectively, and $C_{\rm OSS}$ is the output capacitance of power MOSFET.

So that the total power loss can be written as

$$P_{\rm LOSS} = P_{\rm LOSS\_static} + P_{\rm LOSS\_switching}. \tag{19}$$

Fig. 12 provides the MATLAB simulation results of $P_{\rm LOSS}$.

Fig. 12(a) shows the relationship between $P_{\rm LOSS}$ and D_1 at different values of N with a given $f_{\rm SW}$, which could be used to describe the static power loss in one switching period. From which, it can be found that larger D_1 results in more power loss. Fig. 12(b) provides the curves of $P_{\rm LOSS}$ versus $f_{\rm SW}$ at different N with a given D_1, which is given to illustrate the switching power loss. In Fig. 12(b), it is able to observe that the switching loss becomes larger with an increasing switching frequency, therefore $f_{\rm SW}$ should be decrease when load turns light. Besides, it also can be derived by combining Fig. 12(a) with (b) that the smaller N, the larger the power loss, that is to say the turns ratio is the larger the better when practical design. Fig. 12(c) provides the comprehensive relationship of $P_{\rm LOSS}$ with D_1 and $f_{\rm SW}$, which demonstrates that, compared with switching frequency, duty cycle has a greater impact on the total power loss. In other words, for a peak current mode converter system, the peak primary current should be decreased when load turns light to improve the transfer efficiency.

According to the analysis made above, to realize high transfer efficiency, the duty cycle is the smaller the better when DCM mode. As the switching frequency does not make a significant difference on the power loss compared with duty cycle, it can be set by complying the principle that high frequency at heavy load and vice versa. As to N, for an overlarge duty cycle will make the converter system enters continuous conduction mode and lead to stability problems, hence, the value of which should be set at a moderate value according to Fig. 12.

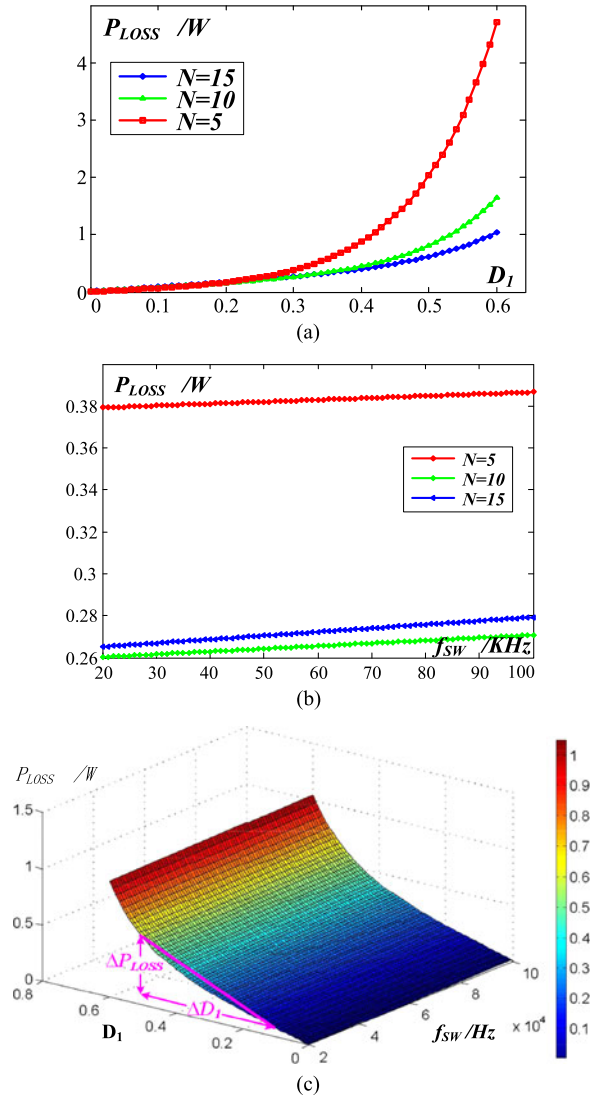


Fig. 12. Curves of $P_{\rm LOSS}$. (a) $P_{\rm LOSS}$ versus D_1 at different N. (b) $P_{\rm LOSS}$ versus $f_{\rm SW}$ at different D_1. (c) $P_{\rm LOSS}$ varies with D_1 and $f_{\rm SW}$.

C. Optimized CV Regulation Strategy

Based on the previous analysis, the turns ratio is set at 13.5 in this paper, and the maximum duty cycle is set at 0.45 as a compromise. For the expression of input power is,

$$P_{\rm IN} = \frac{1}{2} \cdot L_P \cdot {I_{\rm PP}}^2 \cdot f_{\rm SW} \tag{20}$$

hence, the input power should be reduced correspondingly in light load condition. Due to the transfer efficiency requirement for ac-dc 5 W(5 V/1 A) application according to DoE.6 standard is not less than 77.72%, which is the average efficiency of full load, 75% full load, 50% full load, and 25% full load, so that $I_{\rm PP}$ as well as $f_{\rm SW}$ should be carefully considered. Particularly, when system enters light load mode, the switching

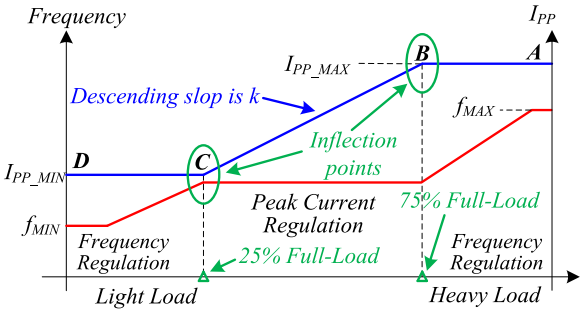
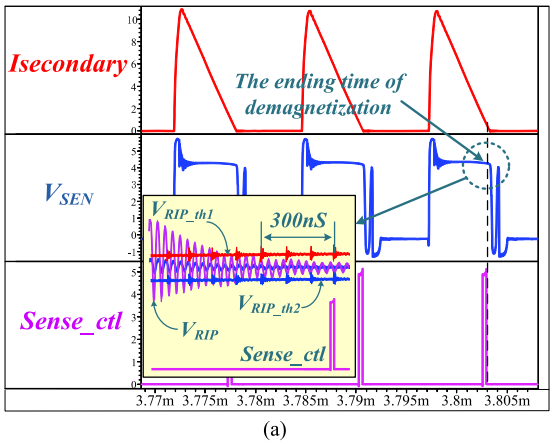
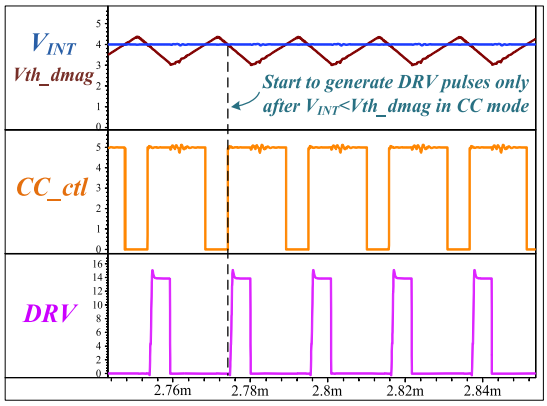


Fig. 13. Curve of optimized CV regulation.



(a)



(b)

Fig. 14. RD-DPC control technique. (a) RD process. (b) DPC process.

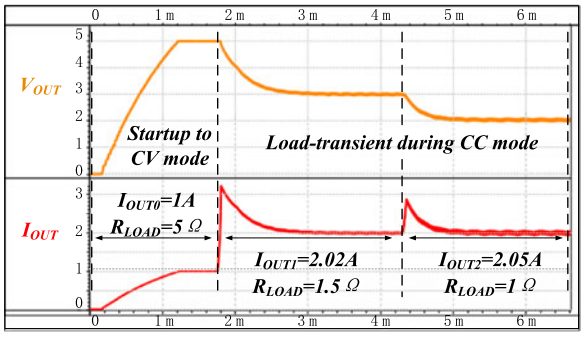
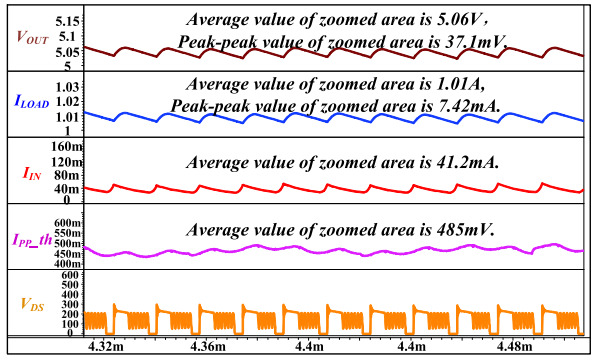
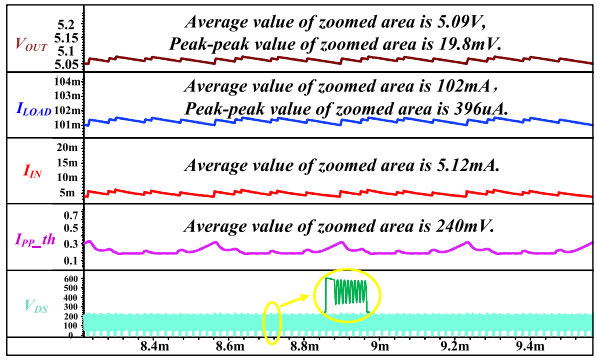


Fig. 15. Constant current in different load conditions.



(a)



(b)

Fig. 16. Constant voltage regulation. (a) Output voltage is 5 V, R_{LOAD} is 5 Ω. (b) Output voltage is 5 V, R_{LOAD} is 50 Ω.

loss of outside power MOSFET and the losses caused by snubber circuit as well the transformer account for the main portion of whole power loss, in addition, these losses are proportional to I_{PP} and f_{SW}, so that the values of the two parameters should be decreased when load turns light and vice versa.

For I_{PP}, as a larger value leads to a larger duty cycle, which contributes to static power loss, therefore, setting a bigger I_{PP} when heavy load to satisfy loading capability and a smaller one when light load to reduce power loss is appropriate. The variation tendency is given in Fig. 13, where interval *AB* corresponds to heavy load condition, interval *CD* represents light load condition, and *BC* is adaptive adjustment interval when load gradually turns light. Besides, the descending slop of I_{PP} in BC interval is determined by referring to the curve of P_{LOSS} shown in Fig. 12(c), and its expression is

$$k = \frac{\Delta P_{\mathrm{LOSS}}}{\Delta D_1} \tag{21}$$

where $\triangle D_1$ is the operating range of D_1, $\triangle P_{\mathrm{LOSS}}$ is the variation range corresponding to $\triangle D_1$.

Moreover, in order to achieve better dynamic response, switching frequency should also be autoregulated. According to [23] and [24], to reduce switching frequency when load turns light helps us to improve the phase margin, so that the variation tendency of switching frequency is designed as follows, when heavy load condition, f_{SW} maintains at a high value to ensure a good loading capability. When load turns light, the switching frequency gradually decreases to achieve faster loop

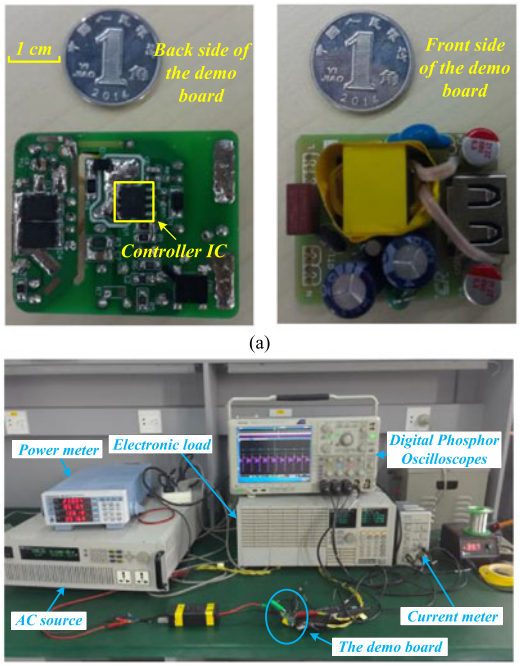


Fig. 17. Photograph of experimental Flyback CC/CV converter and testing environment.

response and small output ripple. To achieve this purpose, some thresholds should be set to predict load conditions, as shown in Fig. 13, two inflection points of 75% full load and 25% full load are set, respectively, dividing the whole range of load into three intervals to achieve an optimal regulation.

Besides, it can be found in Fig. 13 that the variation tendency of switching frequency is similar to that of I_{PP}, while only one of the two critical variables changes in each load interval, which ensures f_{SW} and I_{PP} are always in an optimal combination state, and it is of great importance for the transfer efficiency improvement as well as the stability of the converter system in any load conditions. In addition, a frequency jitter circuit is integrated to improve the electromagnetic compatibility character of the system.

IV. Simulation and Experimental Results

To further validate these proposed strategies, simulation as well as experimental tests is carried out. The design specifications and circuit parameters of this proposed Flyback ac–dc converter shown in Fig. 1 are given as follows: $L_{\mathrm{P}} = 907\ \mu$H, N_{P}:N_{S}:$N_{\mathrm{A}} = 13.5$:1:3.5, M_1: DMG4N65CT, $R_{\mathrm{CS}} = 0.75\ \Omega$, D_{S}:BAS21-TP, D_{A}: SPR10U45SP5, $C_{\mathrm{STR}} = 10\ \mu$F, $C_{\mathrm{OUT}} = 200\ \mu$F, $R_{\mathrm{S1}} = 120\ \mathrm{k}\Omega$, and $R_{\mathrm{S2}} = 30\ \mathrm{k}\Omega$. These control strategies work well at universal input voltage, to given as an example, simulation as well as experimental results at 145 V input voltage are given as follows.

First, Fig. 14 presents the simulation results of the RD-DPC control technique.

From Fig. 14(a), it is obvious to see that the *Sense_ctl* pulses happen when the secondary current decreases almost to zero, so

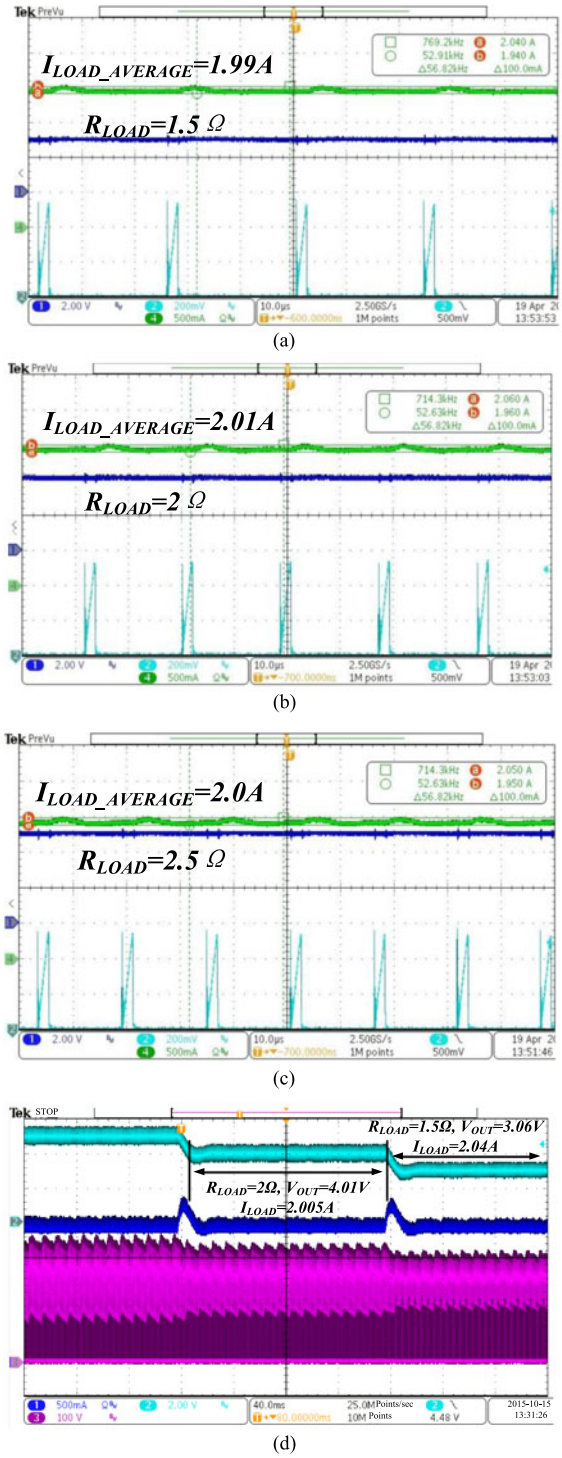


Fig. 18. CC experimental result under different load conditions. (a) V_{OUT} is 3 V, average I_{LOAD} is 1.99 A. (b) V_{OUT} is 4 V, average I_{LOAD} is 2.01 A. (c) V_{OUT} is 5 V, average I_{LOAD} is 2 A. (d) Load transient in CC mode.

TABLE I
CC Accuracy Comparison With Other Work

	[1]	[2]	[3]	[6]	This paper
CC Accuracy	±7%	±2%	±2%	±1%	±0.8%

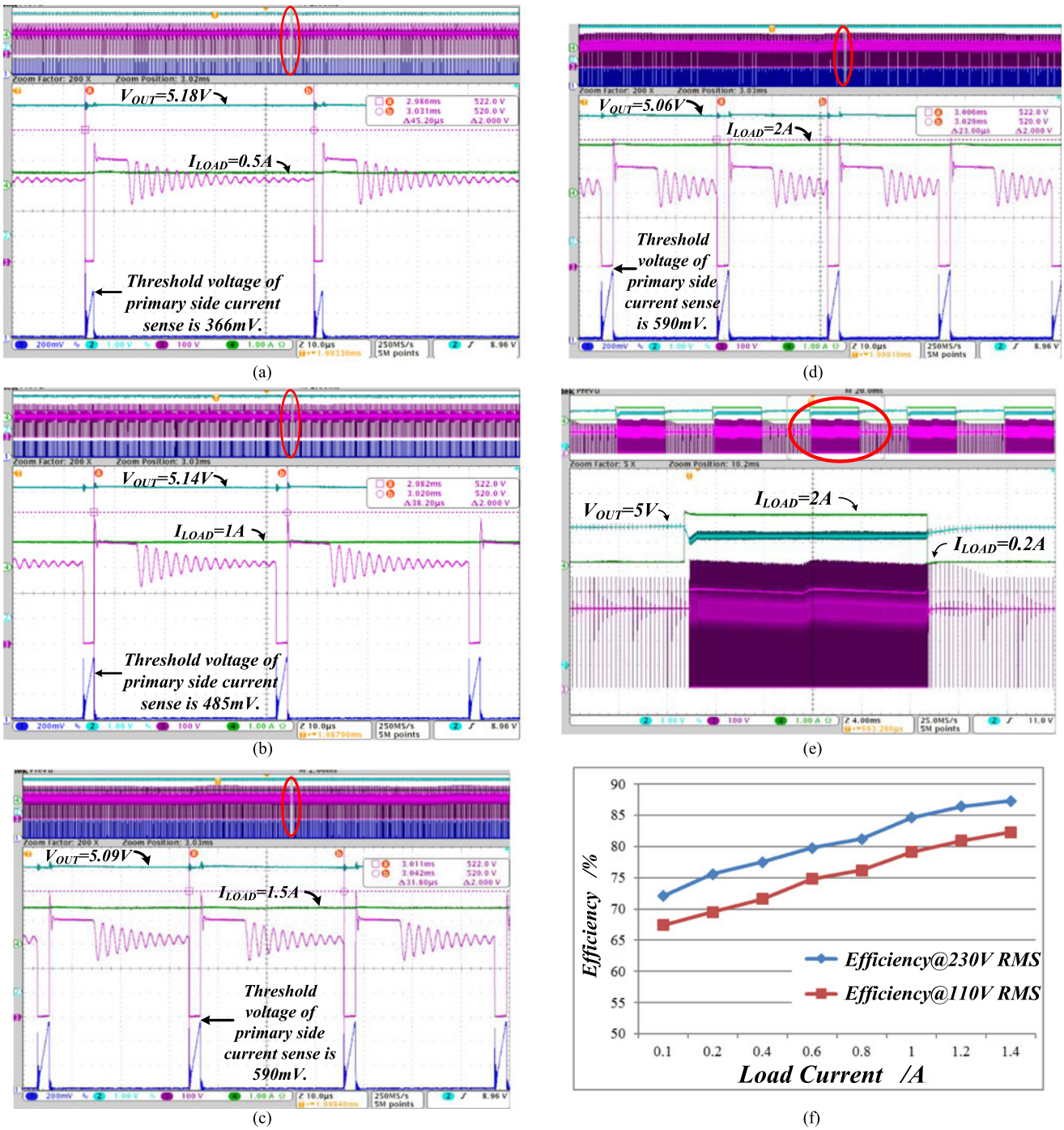


Fig. 19. CV experimental results. (a) V_{OUT} is 5 V, I_{LOAD} is 25% full load. (b) V_{OUT} is 5 V, I_{LOAD} is 50% full load. (c) V_{OUT} is 5 V, I_{LOAD} is 75% full load. (d) V_{OUT} is 5 V, I_{LOAD} is 100% full load. (e) Load transient from 0.2 to 2 A. (f) Measured transfer efficiency.

that the ending time of demagnetization is precisely obtained. After that, an integration is made during the demagnetization process with a triangular waveform is obtained as Fig. 14(b) shows, the waveform is then compared with a threshold voltage to generate a width-variable pulse train, which determines the generation of driving signal and makes the portion of demagnetization in each switching period precisely stay the same consequently.

Fig. 15 provides the constant current character of the proposed ac–dc converter system by adopting RD-DPC control strategy in different load conditions.

In this proposed converter system, the target constant current value is set to 2 A. As shown in Fig. 15, when load resistance is 1.5 Ω, the output current is 2.02 A, when it turns to 1 Ω, the output current is 2.05 A. Namely, the output current regulation accuracy reaches a level as high as ±0.8%.

TABLE II
EFFICIENCY COMPARISON WITH OTHER WORK

	Transfer efficiency (Condition: 5 W output of 5 V/1 A)
[25]	78%
[26]	81.7%
[TI] UCC28910	77%
[Fairchild] FAN6100	81%
This work	84.7%

The simulation result of constant voltage regulation is given in Fig. 16.

In Fig. 16(a), the output voltage is 5 V, the load current is 1 A, the average threshold of peak primary current sense is 485 mV with the average input current is 41.2 mA. So that the transfer efficiency in this load condition is 85.5%. In Fig. 16(b), the load current is 0.1 A, and the efficiency is 69.8%.

The prototype of the proposed Flyback ac–dc converter system integrated with the proposed control strategies is shown in Fig. 17(a) with the controller IC is on the back side of the demo board, the test environment is given in Fig. 17(b).

The experimental results of CC character of the proposed converter system under different load conditions are presented in Fig. 18, the CC accuracy comparison with existing methods are given in Table I.

As shown in Fig. 18(d), when R_{LOAD} is 2 Ω, the output current is 2.005 A, when R_{LOAD} is 1.5 Ω, the output current is 2.04 A, so that, the accuracy of constant output current in CC mode is ±0.8%.

The experimental results of CV character of the proposed converter system are shown in Fig. 19.

Fig. 19(a)–(d) provides the CV performance at 25%, 50%, 75%, and 100% of full load, respectively. From which, it is able to observe that the threshold voltage of primary-side current sense remains at its maximum value of 590 mV when load ranges from 100% full load to 75% full load, when load turns to 50% full load, the threshold changes into 485 mV, when load condition is 25% full load, the threshold voltage is 366 mV, which coincide with the variation tendency of the optimized CV regulation curve given previously. Fig. 19(e) shows the performance of transient response. It can be found that the proposed converter system still able to stabilize the output in a short time even load jumps from almost no-load to full load. Fig. 19(f) provides the measured efficiency of the optimized converter system. Obviously, the transfer efficiency can reach a level as high as 84.7% when 5 V/1 A output, which is also consistent with the theoretically analysis and the simulation results.

Table II lists the comparison result of transfer efficiency of this proposed converter system with other work.

V. CONCLUSION

This paper presents a high transfer efficiency PSR CC/CV Flyback ac–dc converter for low-cost application characterized by accurate constant current control and optimized CV regulation strategy.

In CC mode, an RD-DPC control strategy is proposed for low-cost application, by directly detecting the voltage across the auxiliary side inductor inside the controller when power MOSFET is turned OFF, the ending time of demagnetization can be accurately determined without any other external devices. Besides, by making the demagnetization portion to maintains the same in each switching period, high precision output current is able to be realized as a result. When Flyback converter operating in CV mode, a power stage model is built to find out the expression of power loss. Based on the model, static power loss is first derived, after that the expression of total power loss is obtained with switching power loss is included. By analyzing the power loss, effects of different factors have on the power loss are revealed and be quantified. According to MATLAB simulation results, optimized values of these factors are determined and an optimal control strategy when CV process is proposed. With such strategy, transfer efficiency of Flyback ac–dc converter system is greatly improved with better transient performance.

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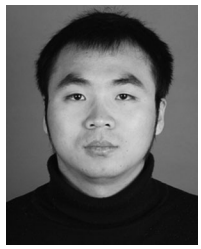

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