# A Design of a 92.4% Efficiency Triple Mode Control DC–DC Buck Converter With Low Power Retention Mode and Adaptive Zero Current Detector for IoT/Wearable Applications

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***Abstract*—This paper presents a retention/ pulse frequency modulation (PFM)/ pulse width modulation (PWM) mode dc–dc buck converter with adaptive zero current detector (AZCD) and spread spectrum clock generation (SSCG) for IoT/Wearable systems. The proposed dc–dc buck converter is capable of handling loads from 10 $\mu$A to 20 mA with high efficiency by applying triple mode (retention mode, PFM mode, and PWM mode), gate split technique, and AZCD. Retention mode is proposed to extend wide load range at ultralight load. Gate split technique adjusts the conduction loss and switching loss. AZCD reduces the operation duty of the high-speed comparator and avoid reverse current below light load. In IoT applications, each node communicates with other nodes through a Bluetooth low energy transceiver, which consumes very low current and is highly sensitive to supply noise. Therefore, the proposed dc–dc buck converter adopts the SSCG technique to reduce electromagnetic interference by up to 18 dB. This chip is implemented using 0.13 $\mu$m CMOS technology with an active area of 820 $\times$ 800 $\mu$m$^2$. The maximum power efficiency of the proposed dc–dc buck converter is 92.4% at a switching frequency of 2.5 MHz when the load current range is 10 to 20 mA. The input voltage range and the regulated output voltage are 2.2–3.3 and 1.7 V, respectively. In addition, the proposed dc–dc buck converter achieves over 74.2% efficiency in retention mode when the load current range is from 10 to 500 $\mu$A.**

***Index Terms*—DC–DC buck converter, frequency hopping, pulse frequency modulation (PFM), pulse width modulation (PWM), retention, triple mode, ultralight load, zero current detector (ZCD).**

## I. Introduction

RECENTLY, there has been rapid growth in the need for Internet of Things (IoT) systems or Bluetooth low energy (BLE). Because low power and energy-harvesting devices are not installed under normal conditions and their batteries cannot be easily exchanged, many portable applications demand a long battery lifetime according to the load conditions. They require low power consumption, small chips, small external components, such as inductors and capacitors, and high efficiency. Therefore, low power and high efficiency power management integrated circuit (PMIC) is important to extend battery life and sustain the system without charging. To reduce the power loss factors [Printed Circuit Board (PCB) loss, line loss, parasitic element loss, etc.], a recent trend is to integrate a buck converter with an IoT/Wearable or RF Transceiver system [1].

Fig. 1 shows the role of PMIC in an IoT/Wearable device. The range of the input voltage (VBAT) is 2.2–3.3 V. The target output voltage, $V_{BUCK\_OUT}$ is 1.7 V for supplying voltage to each low drop out (LDO) regulator, such as analog LDO, digital LDO, and retention LDO in Fig. 1. Retention LDO is designed for the sleep mode of the IoT/Wearable device. If the retention LDO is turned OFF, modem cannot wake up and control the digital signal. Therefore, the retention LDO is always turned ON before operating in active and standby modes. The dc–dc buck converter is also operated in the retention mode to reduce power consumption and extend efficiency.

In IoT/Wearable device systems, dc–dc buck converter must sustain high power conversion efficiency even at ultralight load current as $\mu$A. Implementation of pulse width modulation (PWM) and pulse frequency modulation (PFM) modes for high efficiency under various load conditions have been investigated in [2] and [3]. These modes must be automatically changed according to load conditions since they have different advantages and disadvantages reported in [4]. Therefore, it should be selected by load condition properly.

The ultralow power transceivers which are newly released in [5]–[7] require small active area and wide input voltage range. Typically, Li-Ion battery supplies the voltage range of 2.2–4.2 V. Therefore, the proposed dc–dc buck converter uses 5-V transistors to prevent the melting down of Power MOSFETs. If it uses 3.3-V transistors, the reliability of dc–dc buck converter would be seriously degraded, even though the efficiency of dc–dc buck converter which uses 3.3-V transistors is higher than

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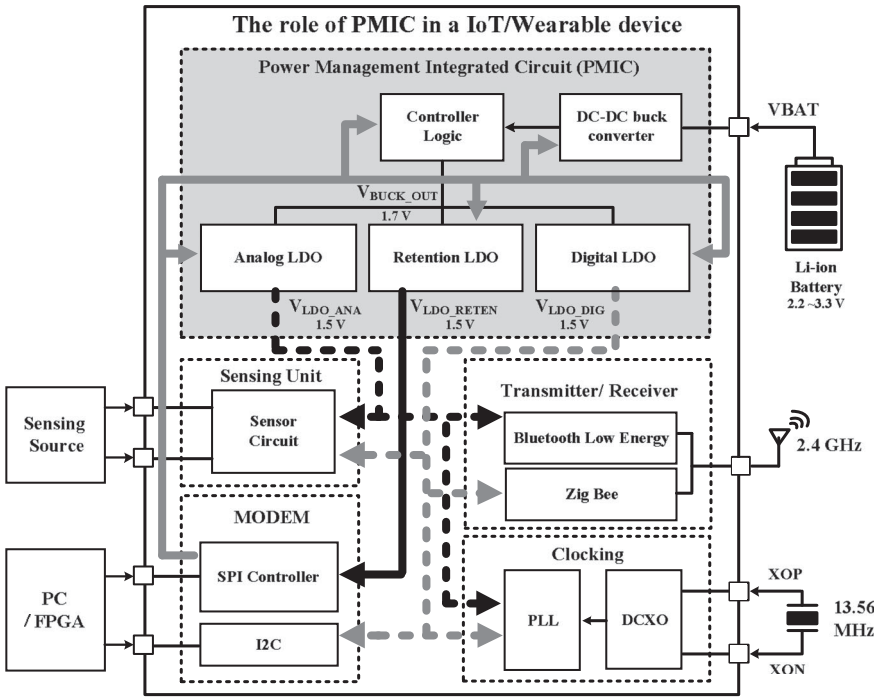



Fig. 1. Role of a PMIC in a low-power IoT/Wearable device.

5 V transistors. Therefore, we adopt 5-V transistors to satisfy the reliability and propose various techniques, such as triple mode (retention mode, PFM mode, and PWM mode) that changes the modulation mode depending on load conditions, Gate split which changes the size of power MOSFET to optimize conduction loss and switching loss, and adaptive zero current detector (AZCD) that blocks the reverse current and minimize the operation time of the high speed comparator. These techniques increase the efficiency and achieve the wide load range.

In addition to the ultralow power requirement of the transceiver in the active mode, power consumptions in the waiting modes (stand-by or sleep mode and so on) are very critical to minimize the battery changing times or stain the long operation time since it operates in those modes over 95% of full operating time [5]–[7]. Generally, there is a tradeoff between the high regulation characteristics and low power consumption in the dc–dc buck converter. In the waiting modes (stand-by mode or sleep mode), the internal blocks of system-on-a-chip (SoC) are almost turned OFF up to 90% and do not require the high-regulation performance. Therefore, the proposed retention mode is implemented to more improve the power efficiency.

Under light load conditions, the dc–dc buck converter achieves the maximum power efficiency by blocking the reverse current in the discontinuous conduction mode (DCM) rather than continuous conduction mode (CCM) [5], [6]. To operate in the DCM mode, a zero current detector (ZCD) changes the on duty of low side power MOSFET to block the reverse current [7]. It generally requires a high-speed comparator to cutoff the reverse current as fast as possible, while the power consumption of internal circuits is very large. Under light load conditions, the current consumption of the building blocks of dc–dc buck converter decreases the efficiency drastically, where the current consumption of the ZCD is dominant. So, limiting the activation time of the high-speed comparator by only sensing the zero current region is the one of the effective solution to optimize the current consumption depending on the load current. Therefore, AZCD is proposed to minimize the current consumption and improve the power efficiency in DCM.

To optimize the power efficiency, triple mode (PWM, PFM, and retention mode) is implemented in a single chip, depending on the load condition [4], [11]. In addition, the large portion of the efficiency of dc–dc buck converter is dominated by conduction and switching loss. On resistances and parasitic capacitances are changed by the sizes of power MOSFETs. Thus, Gate split is adopted to optimize and maximize the efficiency depending on load conditions.

Recently, the mobile devices are developed including transceiver and power management unit in a single chip. IoT/Wearable devices need to be designed with low process and small active area. These requirements generate the undesired spurious noises affecting to the performance of other blocks. These problems in IoT/Wearable devices become the main issue degrading the performance of transmitter and receiver. The phase noise of PLL and sensitivity of receiver are affected by the output noise of the power management unit. Because the output noises of crystal oscillator and dc–dc buck converter are modulated and generate another harmonics, they dramatically change the performance of the transmitter and receiver.

To solve these problems, the spread spectrum clock generator (SSCG) is proposed to spread the output noise. When the switching frequency is constant, the spurious noise and harmonies are very high. Thus, the variable switching frequency is adopted. However, IoT/Wearable devices cannot consumes a lot of current and essentially require the small active area. To satisfy these requirements, this paper uses a frequency hopping technique that can automatically change the switching frequency. It

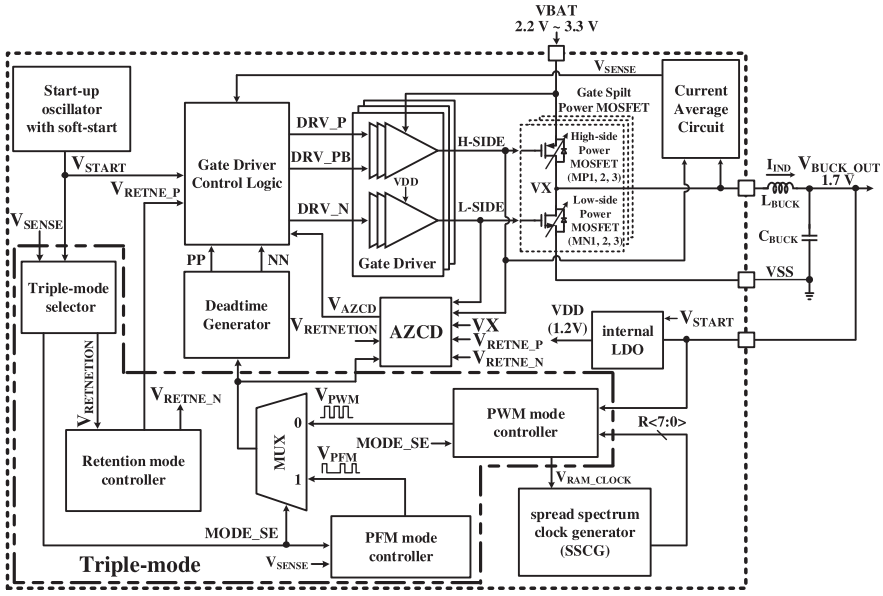



Fig. 2. Block diagram of the proposed dc–dc buck converter.

TABLE I
CHARACTERISTICS OF THE PROPOSED DC–DC BUCK CONVERTER AT PWM/PFM/RETENTION MODES

| Functions | PWM mode | PFM mode | Retention mode |
|---|---|---|---|
| Output Regulation | Excellent | Good | Bad |
| Load Condition | 10 mA ~ | 500 uA ~ 10 mA | ~500 uA |
| Switching frequency | 2 MHz | Variable frequency | 32 KHz |
| Output ripple voltage | Small | Medium | Large |
| Current consumption | Large (270 $\mu$A) | Small (110 $\mu$A) | Extremely small (500 nA) |
| Switching loss | Fixed | Depends on frequency | Extremely small |

reduces the output noise effect to the transmitter and receiver. In addition, internal control blocks inside the proposed dc–dc buck converter use 1.2 V generated by internal LDO to maximize power conversion efficiency by reducing the self-current consumption.

This paper is organized as follows. The system architecture and power-on sequence are introduced in Section II. The details of Triple-Mode, AZCD, Gate Split technique, and SSCG of the proposed dc–dc buck converter design are shown in Section III. The experimental results are detailed in Section IV. Finally, the paper is concluded in Section V.

## II. ARCHITECTURE OF THE RETENTION/PFM/PWM TRIPLE-MODE DC–DC BUCK CONVERTER

Fig. 2 shows a block diagram of the proposed dc–dc buck converter. The power efficiency of the dc–dc buck converter is determined by the conduction loss, switching loss, and internal control circuit loss [11], [12]. The load condition also affects the efficiency of the dc–dc buck converter.

The proposed dc–dc buck converter is designed for IoT/Wearable applications, which consume less power than portable devices. Therefore, in order to maximize the efficiency, the power consumption of building blocks and loss factors needs to be reduced. Thus, the triple mode, AZCD, and Gate split technique are proposed to improve the efficiency in this paper.

First, triple mode is implemented by the PWM, PFM, and retention mode controller in Fig. 2. Table I shows the characteristics of each mode. In the PWM mode, the fixed switching frequency generates an excellent output regulation characteristic and has a constant switching loss. It is the highest frequency comparing with other modes [13]. PWM mode controller receives feedback from the output of the dc–dc buck converter. In the PWM mode, the power consumption is 270 $\mu$A and blocks related to PFM and retention modes are turned OFF.

In the PFM mode, the switching frequency is adjusted based on the load conditions. Thus, the output regulation characteristic at the PFM mode is degraded due to the variable switching frequency [14]. The switching frequency of PFM mode is lower than that of PWM mode. In the PFM mode, dc–dc buck converter consumes 110 $\mu$A, turning OFF the blocks related to PWM and retention mode controller. DC–DC buck converter in the retention mode uses the lowest clock frequency to minimize the switching loss, turning OFF most circuits to extend the high efficiency at ultralight load. It consumes only 500 nA, while the regulation and output ripple characteristics are worst among them.

As a result, triple mode has different characteristics and the current consumption depending on the load conditions as shown in Table I.

Second, in the DCM operation, the ZCD circuit limits the conversion efficiency due to the large current consumption of the internal comparators explained in [11]. Therefore, AZCD is proposed to minimize the current consumption of the comparator through decreasing the operation time of the comparator.

Third, Gate split technique that power MOSFETs are divided into MP1, 2, 3, and MN1, 2, 3, based on operation modes is proposed to optimize the efficiency of the dc–dc buck converter. Dominant loss factors are different according to operation modes. Therefore, power MOSFETs with variable sizes are necessary to adjust the conduction loss and switching loss.

Fig. 3 shows the timing diagram of the power-on sequence of the proposed dc–dc buck converter. Start-up oscillator with

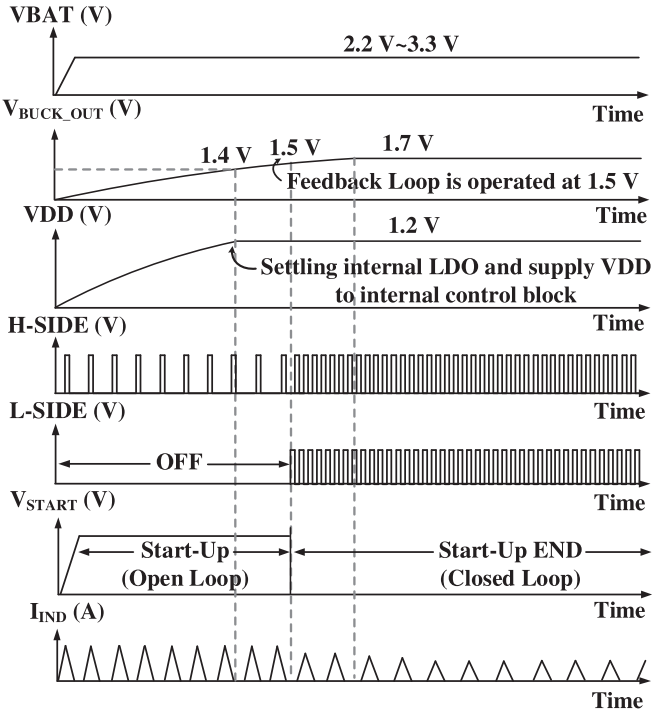



Fig. 3. Waveform of the power-on sequence using a Start-up oscillator with soft-start.

the soft-start in Fig. 2 is used to turn ON the internal blocks in the initial operation. When VBAT is supplied from a Li-ion battery, it generates the switching frequency of 400 kHz to settle the $V_{BUCK\_OUT}$ slowly to 1.7 V, reducing the inrush current. It increases the settling time up to 150 $\mu$s. If the switching frequency is too fast, the $V_{BUCK\_OUT}$ is suddenly increased that generates high inrush current and destroy power MOSFETs [15]. Until the output voltage reaches 1.5 V, the proposed dc–dc buck converter operates in the open-loop state.

In this state, low-side power MOSFET is always turned OFF and high-side power MOSFET only receives a constant duty from the start-up oscillator with soft-start. When the output voltage is over 1.4 V, internal LDO starts to generate an internal supply voltage of 1.2 V, VDD, to supply the internal control circuit. After $V_{BUCK\_OUT}$ reaches to 1.5 V, the power enable signal of the start-up oscillator with the soft-start switches to low and is turned OFF. The feedback loop operates normally using the internal supply voltage. This power-on sequence eventually can reduce power consumption of the internal circuit. [16], [17].

## III. Building Blocks

### *A. Triple-Mode, Current Average Circuit, and Triple-Mode Selector*

Conventional dc–dc buck converters cannot achieve the highest efficiency over the wide load range [2]–[4], [12]. Therefore, the current average circuit and triple mode selector are proposed in the dc–dc buck converter to automatically satisfy the high efficiency and minimize the loss factors depending on the load conditions, as shown in Fig. 2. The PWM and PFM are enabled under the load current of over 10 mA and between 500 $\mu$A and 10 mA, respectively, while the retention mode is enabled when the load current is less than 500 $\mu$A. In the PWM mode, PFM and retention mode controller are turned OFF for minimizing the current consumption of internal circuits. Similarly, in the PFM mode, PWM and retention mode controller are totally turned OFF. In Table I, the current consumption of building blocks related to PWM and retention mode are 270 $\mu$A and 500 nA, respectively. Therefore, the power consumption of 892.65 $\mu$W can be saved in PFM mode when the VBAT is 3.3 V. The current consumption is automatically changed by the signal of triple mode selector.

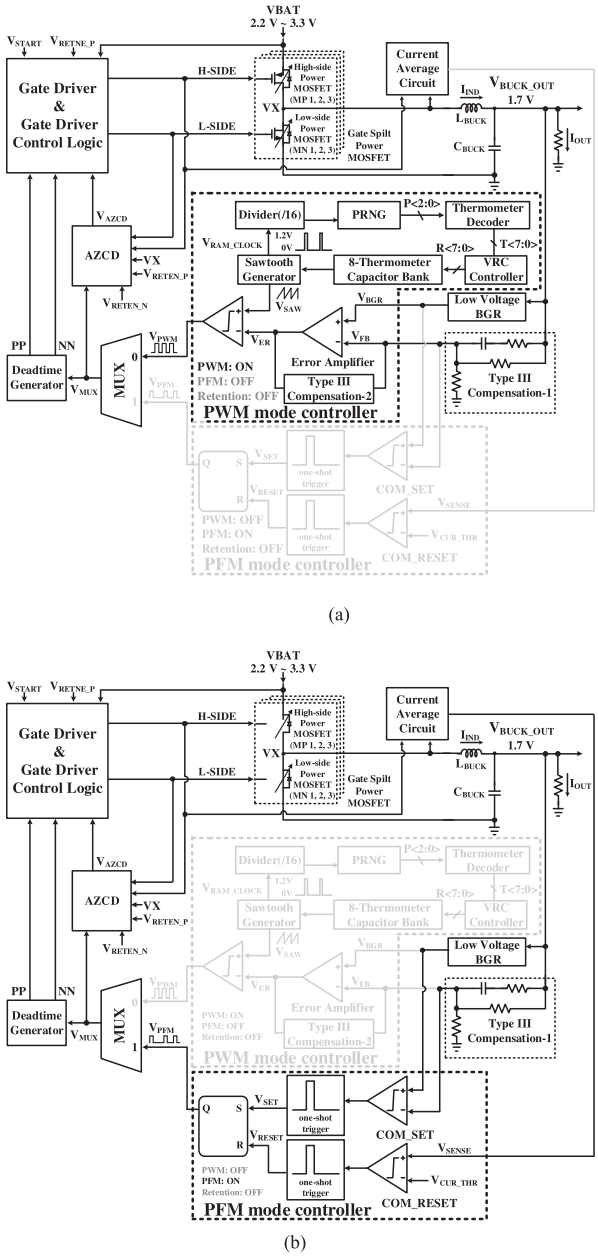



Fig. 4. Internal circuits activated for PWM and PFM mode controllers. (a) When PWM mode controller is turned ON. (b) When PFM mode controller is turned ON.

Fig. 4(a) and (b) shows the internal circuits activated for PWM and PFM mode controllers, respectively. Fig. 4(a) shows

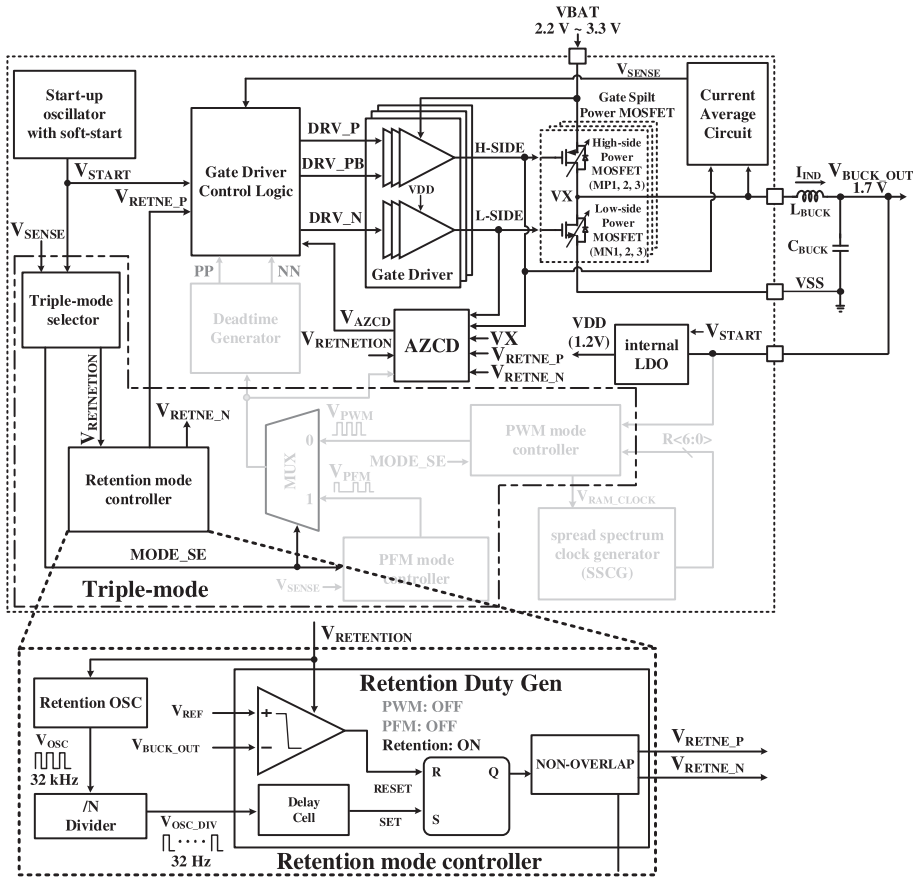



Fig. 5. Block diagram of the proposed retention mode controller when PWM and PFM mode controller are turned OFF.

that the PWM mode controller consists of low-voltage band gap reference (BGR), Type III Compensation-1 and 2, Sawtooth Generator, Divider (/16), PseudoRandom Number Generator (PRNG), Thermometer Decoder, VRC Controller, and 8-Thermometer Capacitor Bank. Among them, the Divider (/16), PRNG, Thermometer Decoder, VRC Controller, and 8-Thermometer Capacitor Bank are activated only in the SSCG operation.

The output voltage $V_{\mathrm{BUCK\_OUT}}$ is sensed through Type-III Compensation-1 to make $V_{\mathrm{FB}}$ and it is compared with $V_{\mathrm{BGR}}$ (860 mV) generated by low-voltage BGR. The error between $V_{\mathrm{FB}}$ and $\mathrm{V_{BGR}}$ is amplified by error amplifier. The output of the error amplifier $V_{\mathrm{ER}}$ is compared with $V_{\mathrm{SAW}}$ signal to generate the $V_{\mathrm{PWM}}$ signal. $V_{\mathrm{SAW}}$ is generated by the Sawtooth Generator to determine the switching frequency of the dc–dc buck converter. The duty of $V_{\mathrm{PWM}}$ is determined by comparing $V_{\mathrm{SAW}}$ with $V_{\mathrm{ER}}$. As $V_{\mathrm{FB}}$ is increased, the duty ratio of $V_{\mathrm{PWM}}$ is decreased. On the other hand, as $V_{\mathrm{FB}}$ is decreased, the duty ratio of $V_{\mathrm{PWM}}$ is increased to adjust the output voltage [18], [19].

The PFM mode controller consists of two comparators (COM_SET and COM_RESET), one-shot trigger and SR-Latch, as shown in Fig. 4(b). PFM mode controller is used to increase the efficiency under light loads by slowing down the switching frequency. When the $V_{\mathrm{FB}}$ is lower than $V_{\mathrm{BGR}}$, a COM_SET makes $V_{\mathrm{SET}}$ from low to high to set the SR latch through the one-shot trigger. The supply voltage begins to store energy to the $L_{\mathrm{BUCK}}$ until the $V_{\mathrm{SENSE}}$ sensing the output peak current reaches $V_{\mathrm{CUR\_THR}}$. A COM_RESET generates $V_{\mathrm{RESET}}$ from low to high to reset the SR latch to release the energy stored in the inductor, as $V_{\mathrm{SENSE}}$ is higher than $V_{\mathrm{CUR\_THR}}$. Therefore, PFM mode is enabled only for the load current range between 500 $\mu$A and 10 mA, which increases the efficiency of the proposed dc–dc buck converter to 80% under light load condition [2], [13].

Retention mode controller is illustrated in Fig. 5. It consists of retention OSC, /N Divider, and Retention Duty Gen. The operation frequency of the retention mode controller is lower than that of PFM mode controller in the asynchronous mode, which degrades the regulation characteristics very much. Therefore, the synchronous type retention mode controller is proposed in this paper. If PFM mode controller is activated under ultralight load, the current consumption of PFM mode controller occupies the large portion of the internal circuits and deteriorates the efficiency of the dc–dc buck converter.

The proposed retention mode has some different operation comparing with the burst mode controller and gated oscillator [20–21]. Output voltage sensing blocks are periodically activated by the constant duty based on $V_{\mathrm{OSC\_DIV}}$ to compare $V_{\mathrm{BUCK\_OUT}}$ with $V_{\mathrm{REF}}$. If the $V_{\mathrm{BUCK\_OUT}}$ is below the $V_{\mathrm{REF}}$, the power MOSFET is turned ON for a short period of time. In the retention mode, Retention OSC, /N Divider, and Retention Duty Gen are operated in subthreshold region to achieve

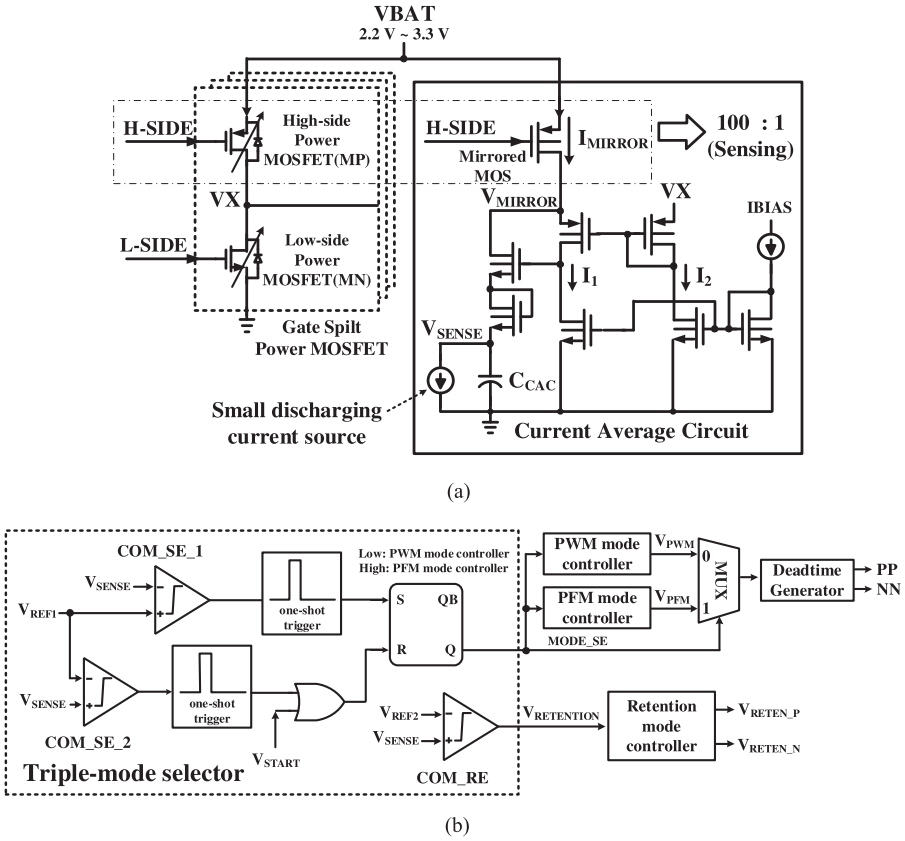



Fig. 6. Block diagram of (a) current average circuit and (b) triple-mode selector.

the low power consumption. In addition to reducing the current consumption, the internal circuits are turned OFF, disabling retention mode controller and AZCD. Also, it generates the clock $V_{\mathrm{OSC\_DIV}}$ with the extremely low clock frequency of 32 Hz, which is much lower than the switching frequency of PFM mode controller to overcome the current consumption by Retention OSC and /N Divider under the ultralight loads.

Retention Duty Gen generates $V_{\mathrm{RETEN\_P}}$ and $V_{\mathrm{RETEN\_N}}$ used for the Gate Driver and AZCD, respectively. The low-side power MOSFET (MN3) is controlled by the AZCD with $V_{\mathrm{RETEN\_N}}$ signal, while the Retention Duty Gen controls the high-side power MOSFET, MP3, through the $V_{\mathrm{RETEN\_P}}$ signal. When $V_{\mathrm{RETENTION}}$ signal is high, only the retention mode controller, AZCD, and current average circuit are active, which enhances the efficiency of the dc–dc buck converter and extends the load current range to ultralight load.

The total current consumption of retention mode controller and AZCD are designed to be less than 500 nA, and the load condition can be extended down to 10 $\mu$A. Even though the output voltage ripple and regulation characteristics are worse than those in PFM and PWM modes, the regulation characteristics are not so important factor under the ultralight load, because the most of the blocks supplied by the dc–dc buck converter are turned OFF.

A conventional current-sensing circuit senses the load current using external resistors to take the average output load current information by converting the output load current to voltage level [22]. However, it needs the external resistors, which is not preferable for IoT/Wearable devices because of the demands for the small external devices. Therefore, current average circuit shown in Fig. 6(a), is proposed to sense the input current using the current mirror with the current ratio of 100:1 without the external devices. An averaging capacitor $C_{\mathrm{CAC}}$ is charged and discharged by the mirrored current. $I_1$ and $I_2$ pull the same current from $V_{\mathrm{MIRROR}}$ node based on $I_{\mathrm{BIAS}}$. The small discharging current source is designed to be smaller than the mirrored current ($I_{\mathrm{MIRROR}}$). Therefore, $V_{\mathrm{SENSE}}$ reflects the average current from the load current with the ratio of 100:1 by the current average circuit.

Fig. 6(b) shows the control logic of the triple mode selector that determines the PWM, PFM, and retention mode through $V_{\mathrm{SENSE}}$ and $V_{\mathrm{START}}$ signals. Three comparators, COM_SE_1, COM_SE_2, and COM_RE, compare $V_{\mathrm{SENSE}}$ signal with reference voltages $V_{\mathrm{REF1}}$ and $V_{\mathrm{REF2}}$ to generate the MODE_SE and $V_{\mathrm{RENTION}}$ signals. These signals control the MUX located in front of PWM and PFM mode controllers illustrated in Fig. 2 to select the PWM or PFM modes and turn ON and OFF the retention mode controller [8], [12]. Also, the malfunction of dc–dc buck converter can be occurred when the switching back and forth at each mode boundary. Therefore, the COM_SE_1, COM_SE_2, and COM_RE in proposed triple mode selector are used hysteresis comparator to prevent the problems.

Fig. 7 shows the waveform of the proposed dc–dc buck converter with triple mode selector. PWM mode is active when the MODE_SE and $V_{\mathrm{RETENTION}}$ are low under the load current of over 10 mA.

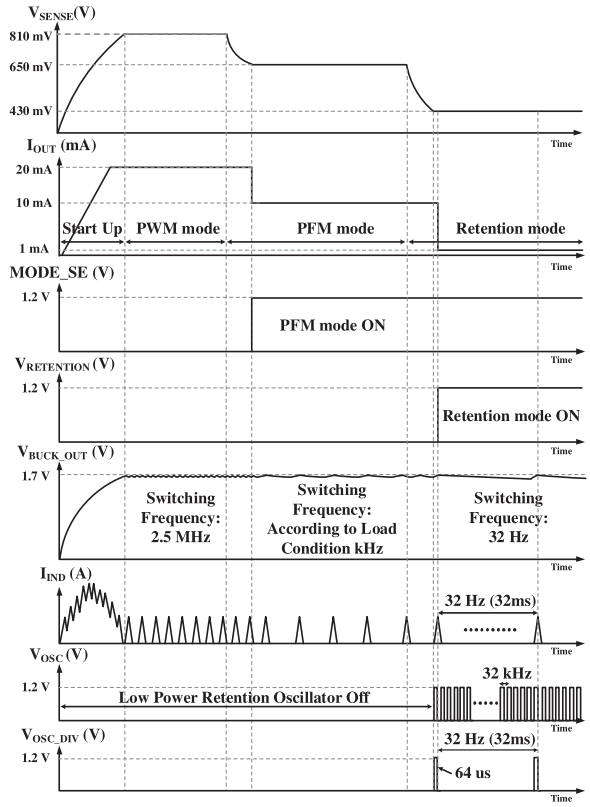



Fig. 7. Waveform of the proposed dc–dc buck converter with triple mode selector.

The switching frequency at PWM mode is 2.5 MHz and has a constant output voltage ripple. In the PFM mode, MODE_SE signal is changed from low to high when $V_{\mathrm{SENSE}}$ is between 650 to 430 mV.

The switching frequency of PFM mode relates to the output load current $I_{\mathrm{OUT}}$, because it changes a discharging time of inductor current, $I_{\mathrm{IND}}$. Therefore, the output voltage ripple and inductor current are dynamically changed depending on the $I_{\mathrm{OUT}}$.

The retention mode is active when $V_{\mathrm{SENSE}}$ is below 400 mV. When $V_{\mathrm{RETENTION}}$ and MODE_SE are high, the Retention OSC begins to generate the clock frequency of 32 kHz. This clock is divided by the /N Divider to generate $V_{\mathrm{OSC\_DIV}}$, 32 Hz. It turns ON the high-side power MOSFET for 64 $\mu$s within the period of 32 ms. Therefore, it dramatically reduces the total current consumption and increases the efficiency of the dc–dc buck converter under ultralight load.

### *B. Automatic Gate Split Technique*

The efficiency of switching type regulator is affected by the size of power MOSFET. In particular, the dominant factors for the efficiency are changed depending on load conditions. In the heavy load, the dominant loss factor to the efficiency is the conduction loss, while the switching and internal losses are more dominant than conduction loss in the light load [23], [24]. Generally, power MOSFET with the fixed size is used so that the optimized efficiency can be reached at the fixed load current. However, the efficiency at other load current is decreased due to the on-resistance, leakage current, and so on. Therefore, the segmented power MOSFET can achieve the higher efficiency than the fixed size of power MOSFET.

Table II shows the efficiencies with respect to different sizes of the segmented power MOSFET. When the size of power MOSFET is 20 mm/10 mm under the load current of 20 mA (PWM mode), the efficiency is maximum. In the PFM mode under the load current of 10 mA, 8 mm/4 mm shows the maximum efficiency. Also, below 500 $\mu$A, retention mode shows the maximum efficiency at the size of 2 mm/1 mm. Therefore, the size ratio of power MOSFETs is determined to be 6:3:1 for PWM, PFM, and retention modes, respectively. In order to minimize the die area and cost, power MOFSETs in the retention mode is reused for PWM and PFM modes, while those in the PFM mode is reused for those in the PWM mode. When the power MOSFET is segmented depending on the load condition, the Gate drivers of power MOSFET are also divided based on the sizes of power MOSFET for minimizing the current consumption.

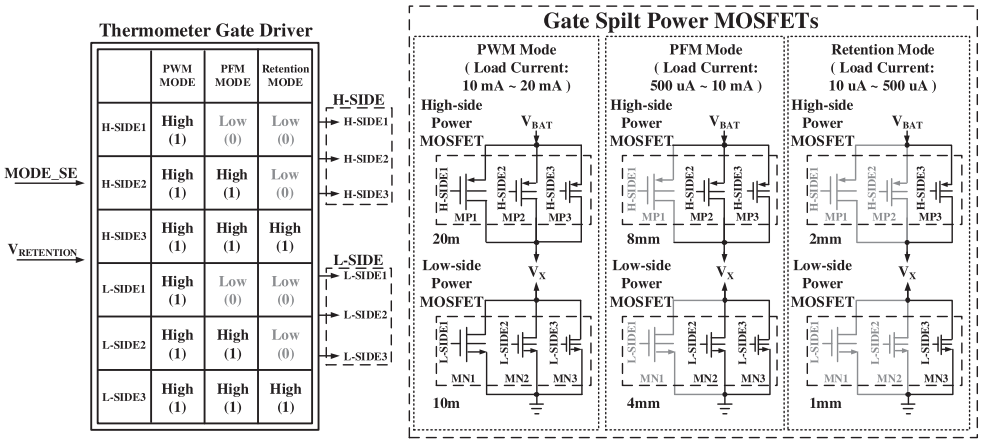
As a result, high-side and low-side power MOSFETs are segmented into MP1, 2, 3 and MN1, 2, 3, respectively. The relative ratios between MP1 (MN1), MP2 (MN2), and MP3 (MN3) are determined to be 6:3:1.

Also, the current sensing block also requires the minimum current consumption to control Gate split depending on the load condition since IoT/Wearable device is designed to consume the low current. If analog–digital converter (ADC) consuming a lot of current senses the load current, the resolution can be higher than the conventional current sensing method [25]. However, the current consumption of internal control block degrades the efficiency at the light load. Therefore, the proposed Gate split uses average current sensing block with the minimum current consumption.

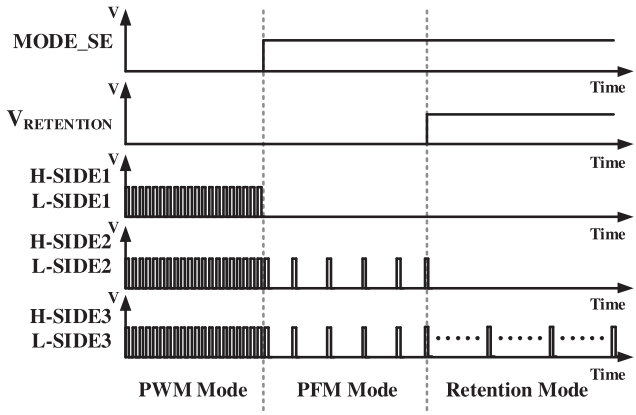
Fig. 8(a) and (b) shows the block diagram and timing diagram of the Gate split technique for triple mode operation, respectively. The Gate split technique and segmented Gate driver use MODE_SE and $\mathrm{V_{RETENTION}}$ signals to change the operating mode. Gate split power MOSFETs are controlled by the H-SIDE1, 2, 3 and L-SIDE1, 2, 3 signals that are generated from the Thermometer Gate Driver. When the sizes of the power MOSFETs are increased, their related parasitic capacitances and resistances are increased and decreased, which are related to the switching losses and conduction losses, respectively. In the PWM mode, the conduction loss is a dominant factor in the efficiency due to the large current consumption. Thus, the Gate split power MOSFETs need to be configured to reduce the conduction loss. Thermometer Gate Driver set H-side1, 2, 3 and L-side1, 2, 3 to all high. In the PFM mode, Thermometer Gate Driver turns OFF H-side1 and L-side1 to reduce the parasitic capacitances and switching loss since the switching loss is more dominant loss factor under the light load. On the other hand, in the retention mode, Thermometer Gate Driver turns ON only H-side3 and L-side3 since retention mode operates at the lowest frequency under the ultralight load condition. Retention mode uses only about a tenth part of power MOSFETs to minimize the parasitic capacitance and switching loss.

TABLE II
EFFICIENCY OF THE DC–DC BUCK CONVERTER WITH RESPECT TO THE WIDTH OF THE POWER MOSFET

| Load current | High / Low side Power MOSFET width size (DC–DC buck converter efficiency) | | | | |
|---|---|---|---|---|---|
| | 30 mm/15 mm | 28 mm/14 mm | 20 mm/10 mm | 8 mm/4 mm | 2 mm/1 mm |
| 20 mA (2.5 MHz) | 92.6% | 93.1% | 93.2% | 92.5% | 89.8% |
| 10 mA (1 MHz) | 90.1% | 90.8% | 91.9% | 92% | 91.2% |
| Under 500 $\mu$A (32 Hz) | – | – | – | 76.1% | 83.7% |




(a)




(b)

Fig. 8. (a) Block diagram. (b) Timing diagram of gate split technique for triple mode operation.

### *C. Adaptive Zero Current Detector (AZCD)*

In the light load condition, the conventional ZCD is used when CCM is changed to DCM, which requires a high-speed comparator, because the reverse current must be blocked as fast as possible [26]–[28]. If the high-speed comparator is not implemented, the efficiency of dc–dc buck converter is extremely reduced due to the high-side and low-side diode conduction loss. Thus, it is essentially required to use the high-speed comparator in DCM [28]. Thus, in order to increase efficiency much more at light load, the internal current consumption has to be reduced through reducing the current consumption of ZCD. Because the high speed comparator occupies the large portion of current consumption at the PFM mode, AZCD is proposed to optimize the current of the high-speed comparator through changing the power enable signal of the high-speed comparator automatically.

IoT/Wearable devices whose load currents are lower than those of the high-power devices are more affected by the internal current consumption. The efficiency and current consumption have a very close relationship [29]. Therefore, the proposed AZCD enables the high-speed comparator only when the zero current is sensed. It efficiently reduces the current consumption of internal circuits and improves the power efficiency in DCM mode more and more as the load current is decreased.

Fig. 9 shows the block diagram of the proposed AZCD. It consists of Rising trigger, Falling trigger, comparator

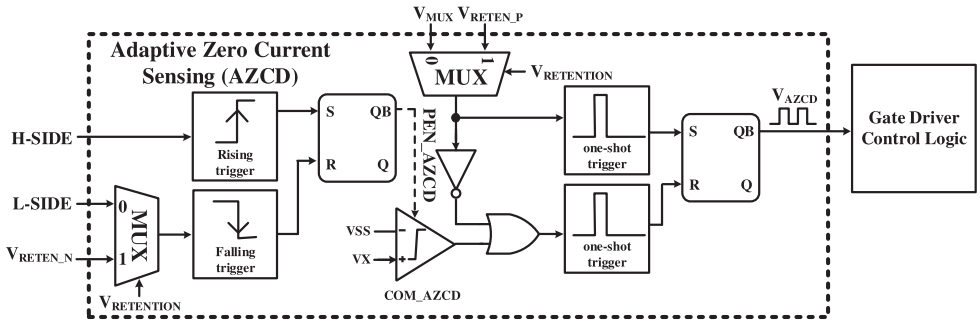



Fig. 9. Block diagram of the proposed AZCD.

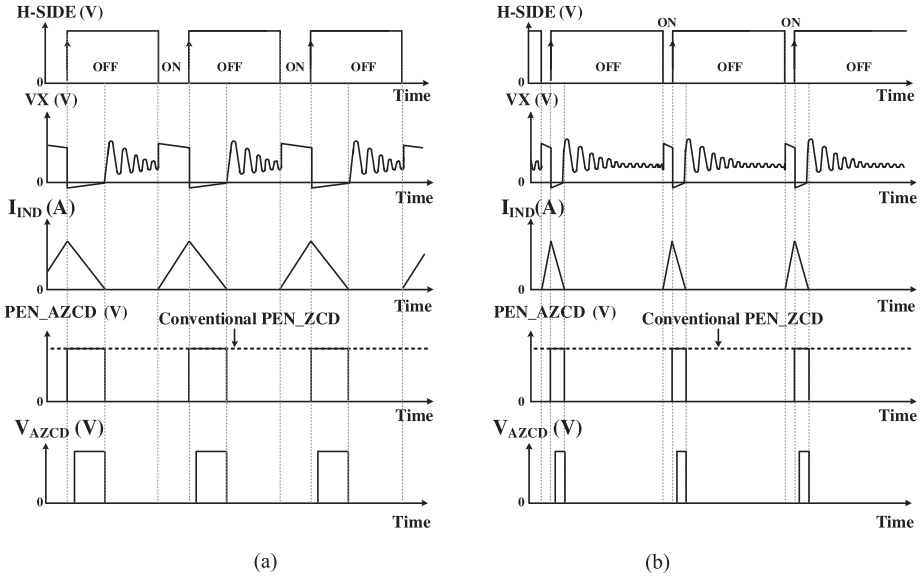



Fig. 10. Waveforms of AZCD at (a) PWM mode and (b) PFM mode.

(COM_AZCD), one-shot trigger, and D-FF. The proposed AZCD senses H-SIDE and VX nodes and operates only when the VX node is changed from negative voltage to positive voltage.

Fig. 10(a) and (b) shows the waveforms of AZCD at PWM mode and PFM mode, respectively. As can be seen from Fig. 10(a) and (b), in case of the conventional ZCD, the enable signal (PEN_ZCD) always maintain high so that the high-speed comparator is always enabled [27].

However, in the proposed AZCD, PEN_AZCD signal becomes high to enable COM_AZCD only when the VX node is negative voltage. When AZCD senses zero current, the inductor current $(I_{\mathrm{IND}})$ becomes zero and PEN_AZCD signal goes to low. It eventually turns OFF low-side power MOSFET.

Fig. 10(b) shows that the duty is also changed in PFM mode when the operation frequency is changed by the load current.

As a result, the circuit can operate with the low-power consumption compared to PWM mode under the light load condition, since the turn-on duration of high-speed comparator becomes shorter. Moreover, in the retention mode, $V_{\mathrm{RETENTION}}$ signal is high and $V_{\mathrm{RETEN\_N}}$ is asserted to reduce the duty signal of the low-side power MOSFET so that current consumption can be much reduced than PFM mode.

### *D. Spread Spectrum Clock Generator (SSCG)*

The proposed dc–dc buck converter has three modes corresponding to the system operating modes of active, stand-by, and sleep modes, respectively. In the active mode, the noises at the switching frequency of dc–dc buck converter can degrade the performance, such as the phase noise of the PLL or the sensitivity of the receiver. To solve these problems, SSCG is designed to spread the noise spectrum around the switching frequency of dc–dc buck converter. On the other hand, the transceiver or PLL is not activated at the stand-by mode or sleep mode, where only the essential blocks such as retention memory are active. Thus, the SSCG is not designed in the stand-by and sleep modes.

Fig. 11 shows the block diagram of a Sawtooth Generator with SSCG. Conventionally, SSCG can be implemented in two ways: hard switching [30], [31] and soft switching [32]. In this paper, the hard-switching technique is adopted. SSCG has three spreading methods; up spread, down spread, and center spread. In the up spread, the switching loss is continually increased, reducing the efficiency at PWM mode since the switching frequency is increased. On the other hand, in the down spread, while the switching loss is decreased, the output ripple $\triangle V_{\mathrm{OUT}}$ would be increased, degrading the regulation characteristics.

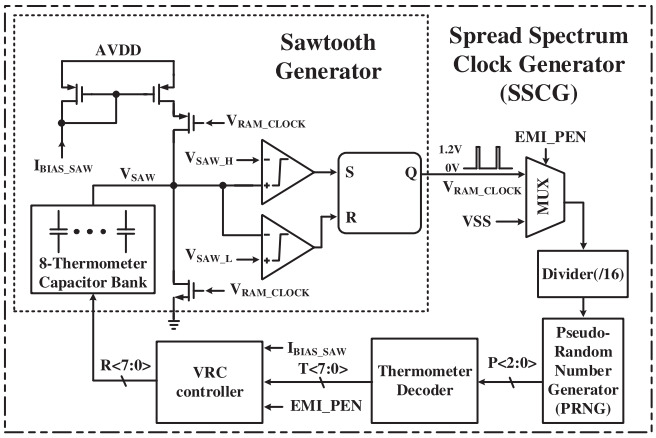



Fig. 11. Block diagram of the SSCG.

Equation (1) shows which factors affect the output ripple of the dc–dc buck converter

$$\Delta V_{\mathrm{OUT}} = \frac{\Delta Q}{C} = \frac{\Delta I_L}{8C} \times T_S = \frac{(V_{\mathrm{IN}} - V_{\mathrm{OUT}}) \times D}{8 \times L \times C} \times {T_S}^2. \tag{1}$$

To optimize the switching loss and output ripple, the proposed SSCG adopts center spread. The center spread has smaller switching loss than the up spread and smaller output ripple than the down spread. As a result, the center spread prevents the degradation of efficiency and deteriorating regulation characteristics.

Many techniques based on the frequency hopping are already reported in [30] and [32]–[34] to solve the spurious noise problems. The proposed frequency hopping reduces the spurious noise at IoT/Wearable applications by minimizing the current consumption. In order to achieve it, Sawtooth Generator fixes the minimum bias current and only control the Capacitor Bank. The frequency modulation clock is generated by the dividing of Sawtooth Generator clock. To achieve the low-power consumption and high power efficiency, simple PRNG-based frequency hopping is implemented rather than the high-performance and high-power Sigma-Delta Modulator. The frequency of the $V_{\mathrm{SAW}}$ signal is adjusted continuously based on random numbers from the PRNG block, whose profile is determined by the period of $V_{\mathrm{RAMP\_CLOCK}}$. It is divided by the Divider (/16) and applied to PRNG for synchronization.

A 3-bit binary signal $(\mathrm{P} < 2 : 0 >)$ from the PRNG is converted into the 8-bit thermometer signal $(\mathrm{T} < 7 : 0 >)$ through the Thermometer Decoder. The fundamental switching frequency of the dc–dc buck converter is 2.5 MHz, and it is modulated by the VRC Controller and 8-Thermomter Capacitor Bank from 2 to 3 MHz. If the code transition step is too large in the conventional 3–8 code or gray code, the output ripple of the dc–dc buck converter can be very large [35]. Therefore, Thermometer Decoder is designed in this paper to change the frequency control bits only one bit a time, which can minimize the output ripple of the dc–dc buck converter.

The spurious tones at the output of the dc–dc buck converter can be reduced by the SSCG. Theoretically, output noise reduction can be written as

$$A_{\mathrm{MOD}} = \frac{(f_{\mathrm{MAX}} - f_{\mathrm{MIN}})}{f_C} \times 100\% \tag{2}$$

$$f_{\mathrm{MOD}} = (f_C/\mathrm{DEV})/TC \tag{3}$$

$$\text{Power Attenuation} = 10 \log \left[ \frac{f_C \times A_{\mathrm{MOD}}}{f_{\mathrm{MOD}}} \right] \tag{4}$$

where, $f_{\mathrm{MAX}}$, $f_{\mathrm{MIN}}$, $f_C$, DEV, TC, $A_{\mathrm{MOD}}$, and $f_{\mathrm{MOD}}$ are a maximum switching frequency, a minimum switching frequency, a center switching frequency, deviation value, thermometer code value, a modulation depth, and frequency modulation, respectively.

Furthermore, the second and third harmonic spurious tones can be lowered to below the basic noise floor. The spurious tones are attenuated by the SSCG to minimize the effect of the dc–dc buck converter noise on the noise figure of the RF receiver.

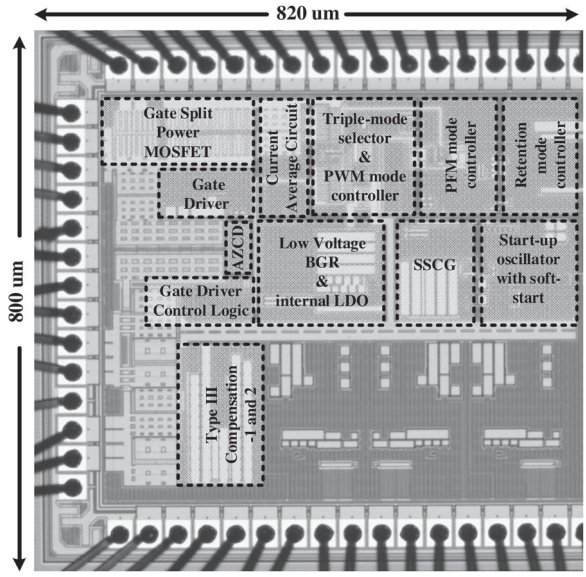



Fig. 12. Microphotograph of the proposed dc–dc buck converter.

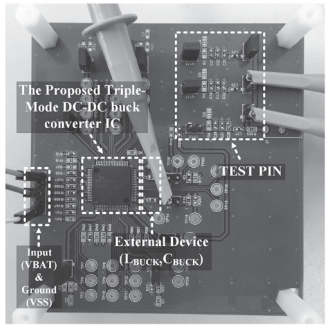



Fig. 13. Measurement board of the proposed triple-mode dc–dc buck converter.

## IV. Experimental Results

The chip was fabricated using the 0.13 $\mu$m CMOS process with a single poly layer, four layers of metal, MIM capacitors,

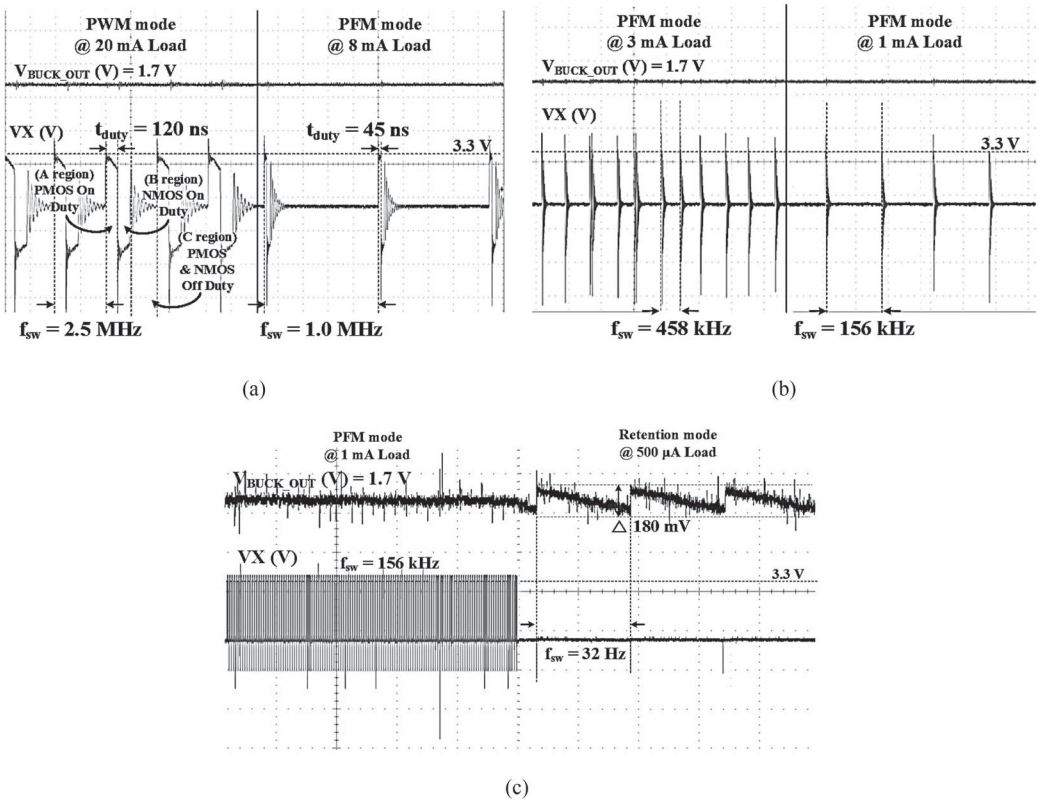



Fig. 14. Measured waveform of the triple mode buck converter at (a) PWM (@20 mA) to PFM (@8 mA), (b) PFM (@3 mA) to PFM (@1 mA), and (c) PFM (@1 mA) to Retention (@500 $\mu$A).

and high sheet resistance poly resistors. Fig. 12 shows a microphotograph of the chip. The active area is $820 \times 800\ \mu\text{m}^2$.

Fig. 13 shows the measurement board. The proposed dc–dc buck converter is located at the center of the PCB. An external inductor and capacitor are placed next to the integrated circuit chip. Internal signals, such as VX, H-side, L-side, and so on, are measured through the TEST PIN. An oscilloscope, a power supply, and an electric load generator are used to change the load condition and input voltage. The input voltage range of the converter is 2.2–3.3 V.

Fig. 14(a)–(c) shows the measured waveforms of the mode changes. Fig. 14(a) shows that the mode is changed from PWM mode to PFM mode. When the load current is suddenly changed from 20 to 8 mA, the switching frequency observed at VX node is also changed from 2.5 to 1 MHz. Fig. 14(a) shows three different operating regions (A region, B region, and C region). At the first duration (A region), $L_{\text{BUCK}}$ is charged by the current and H-side is turned ON while L-side is turned OFF. At the second duration (B region), the inductor is discharged and H-side is turned OFF while L-side is turned ON. In the last duration (C region), H-side and L-side are both turned OFF to block the reverse current.

Fig. 14(b) shows that the switching frequency in the PFM mode is changed from 458 to 156 kHz when the load current is changed from 3 to 1 mA. Fig. 14(c) shows the measurement result when the PFM mode is changed to retention mode. Retention mode has the lowest switching frequency (32 Hz), so the output ripple of $V_{\text{BUCK\_OUT}}$ is higher than PFM mode.

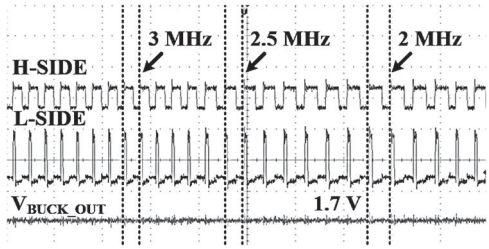



Fig. 15. Measured waveforms regarding switching frequencies of H-side and L-side.

Fig. 15 shows the measured waveform of the dc–dc buck converter with the SSCG operation when the input voltage, output voltage, and load current are 3.3 V, 1.7 V, and 20 mA, respectively. The duty is continually changed by the switching frequency of SSCG operation. The regulated output voltage ($V_{\text{BUCK\_OUT}}$) is almost constant. The output spectrum is measured using a real time spectrum analyzer.

Fig. 16 shows the measured output spectrum of the dc–dc buck converter when the SSCG is OFF. The maximum spurious power at the switching frequency is –38.85 dBm and there are many large harmonics, which degrade the noise performance of the RF transceiver.

Fig. 17 shows the output spectrum of the dc–dc buck converter when the SSCG is ON. The spurious tones at the switching frequency are reduced by about 18 dB and all harmonics are removed. As a result, the SSCG operation dramatically reduces output spurious noise and minimizes the effect of harmonics.

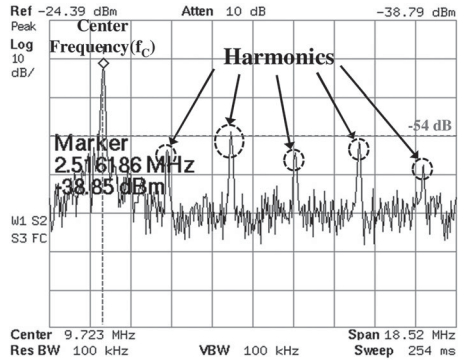



Fig. 16. Measured output spectrum of the dc–dc buck converter when the SSCG is OFF.

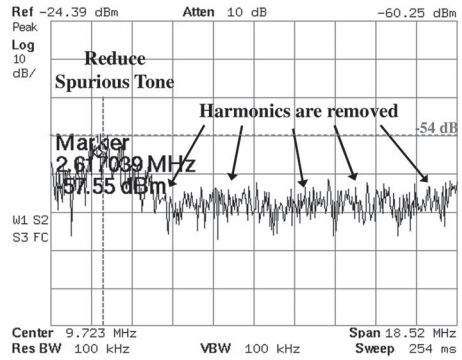



Fig. 17. Measured output spectrum of the dc–dc buck converter when the SSCG is ON.

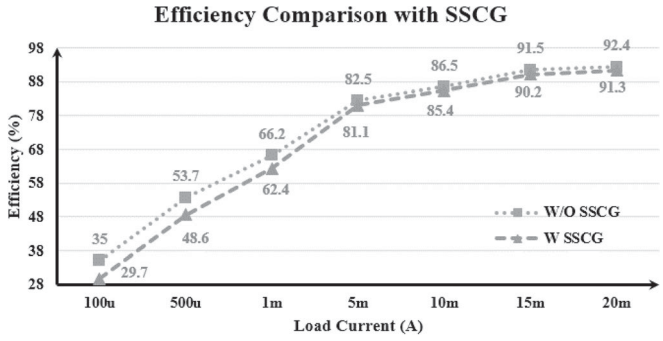



Fig. 18. Efficiency of dc–dc buck converter when SSCG is OFF and ON.

Fig. 18 shows the efficiency of the dc–dc buck converter when SSCG is OFF and ON. Changing the switching frequency increases the output voltage ripple, and decreases the total efficiency of the proposed dc–dc buck converter by about 1%. Thus, SSCG is not used in PFM or retention mode since the power consumption of the oscillator is large.

Fig. 19 shows the measured waveform at VX node. AZCD reduces internal control loss by sensing the VX node. It shows that there are no diode conductions of high side and low side. Therefore, AZCD blocks the reverses current on time, reduces diode conduction loss and optimizes the current of the high-speed comparator.

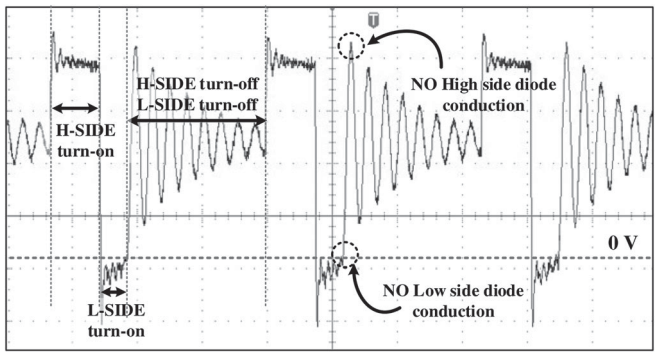



Fig. 19. Measured waveform at VX node with AZCD.

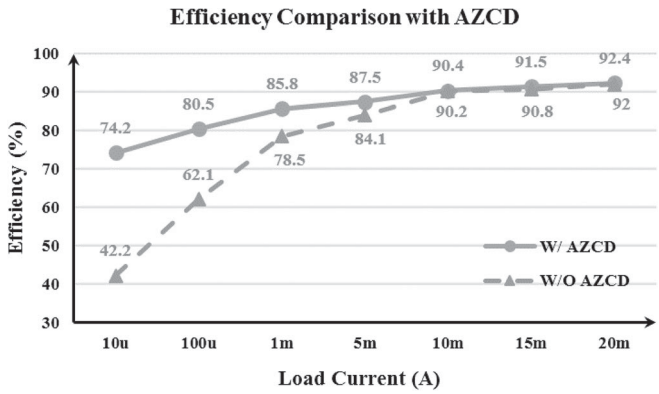



Fig. 20. Efficiency comparison of dc–dc buck converter with and without AZCD.

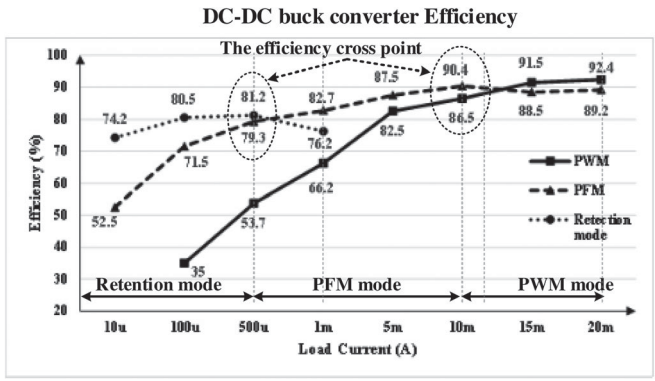



Fig. 21. Measured efficiency of the dc–dc buck converter at triple modes.

Fig. 20 shows the efficiency comparison of the proposed dc–dc buck converter with AZCD and without AZCD. AZCD increases the efficiency drastically under light and ultralight loads. Also, the efficiency of the proposed dc–dc buck converter in the DCM is also increased at the PWM mode.

Fig. 21 shows the efficiency of the proposed dc–dc buck converter at triple modes. We measured the proposed dc–dc buck converter by changing mode through external mode control to analyze the efficiency which is already verified through

TABLE III
PERFORMANCE COMPARISON OF THE TRIPLE MODE BUCK CONVERTER WITH PRIOR WORKS

| Reference | [2] TPE 08 | [4] TICAS 11 | [8] JSSC 14 | [11] JSSC16 | This Work |
|---|---|---|---|---|---|
| Technology | 0.35 $\mu$m CMOS | 0.25 $\mu$m CMOS | 45 nm CMOS | 0.18 $\mu$m CMOS | 0.13 $\mu$m CMOS |
| Overall Efficiency (%) | PFM: 95 PWM: 94 | Dual Modulation: over 85 | PWM: 94 | PFM: over 70 PWM: 92 | Retention: 81.2 PFM: 90.2 PWM: 92.4 |
| Operation Frequency (MHz) | 0.1 – 0.6 | 5 | 0.1 | 1.65 | 2.5 |
| Input Voltage Range (V) | 2.7–5 | 3–4.5 | 0.6–1.1 | 0.55–1 | 2.2–3.3 |
| Load Current (mA) | 3–460 | 1–600 | 0.050–10 | 0.0001–20 | 0.01–20 |
| Output Voltage (V) | 1 | 1.8 | 0.3–0.55 | 0.35–0.5 | 1.7 |
| Mode | PWM / PFM | Dual-Mode | PWM | PWM /PFM/AM | Triple-Mode (PWM/PFM/ Retention) |
| EMI & Spur compensation | N/A | N/A | N/A | N/A | Compensated (SSCG) |
| Die Area($\mathrm{mm}^2$) | $1.89 \times 1.89$ | $1.15 \times 1.2$ | $1.05 \times 0.45$ | $1.2 \times 1.2$ | $0.82 \times 0.8$ |
| Inductor/Capacitor | 10 $\mu$H / 10 $\mu$F | 1 $\mu$H / 4.7 $\mu$F | 220 $\mu$H / – | 4.7 $\mu$H / 4.7 uF | 3 $\mu$H / 3 $\mu$F |

simulation. We measured in each mode (PWM, PFM, and retention modes) by changing load current from 10 $\mu$A to 20 mA.

When the load current is from 10 to 20 mA, proposed dc–dc buck converter operates in the PWM mode, where the efficiency of PWM mode is higher than that of PFM mode under the load current condition ranging from 15 to 20 mA. Also, efficiency of PFM mode is higher than that of retention mode under the load current condition ranging from 500 $\mu$A to 10 mA. It shows that the current average circuit in the proposed triple mode dc–dc buck converter changes the mode automatically. The proposed triple mode operates in PWM mode under the load current condition of above 10 mA, and PFM mode under that load current of above 500 $\mu$A. Moreover, under that load current of below 500 $\mu$A, the proposed dc–dc buck converter operates in the retention mode, so it can be operated with maximized efficiency through all load current condition.

In Fig. 21, when dc–dc buck converter operates in the normal mode, PWM mode is selected under the load current from 10 to 20 mA and has a maximum efficiency of over 90%; this has the best regulation characteristics. The operating mode is changed from PWM mode to PFM mode when the load current is less than 10 mA, because the efficiency at the PFM mode is higher than that of PWM mode at 10 mA. The efficiency at the PFM mode is over 80%. Finally, retention mode can be enabled when the load current is below 500 $\mu$A. Retention mode decreases the internal current consumption by up to 500 nA, and keep the acceptable efficiency under the ultralight load down to 10 $\mu$A. Thus, triple mode can maximize the overall efficiency by decreasing the current consumption, switching, and conduction loss under various load conditions.

Table III shows a performance comparison with prior works. The overall efficiency of this paper is highest except [2] and [8]. However, the load current range is wider than that in [4], and the operation frequency is higher than that in [2].

In addition, the inductor value and die area are smallest compared with [2], [8], and [11]. The efficiency of the proposed dc–dc buck converter is higher than [2], [4], and [8] at light load. In addition, the triple mode (PWM/PFM/retention) is proposed to achieve more wide the load range than [2], [4], and [8]. It increases and extends the efficiency at the ultralight load. The SSCG technique is not designed in [2], [4], [8], and [11]. This paper proposes the SSCG technique to reduce the spurious noise effect and minimize the current consumption and active area for IoT/Wearable devices.

## V. CONCLUSION

Many IoT/Wearable and portable devices require a longer battery life in normal state and standby mode. This paper presents a high-efficiency dc–dc buck converter. The proposed dc–dc buck converter concentrates on achieving high efficiency under a light load. It is suitable for several types of low-power system. Triple mode and AZCD reduce the internal current consumption by turning OFF unnecessary blocks based on the load conditions, and operate in a wide load current range. The Gate split technique enables optimization of conduction loss and switching loss. The proposed SSCG reduces noises and spurious tones for the RF transceiver. The proposed chip is implemented using a 0.13 $\mu$m CMOS process and the active area is 820 $\times$ 800 $\mu$m$^2$. The input voltage range is 2.2–3.3 V and the peak efficiency is 92.4% at a switching frequency of 2.5 MHz. The inductor size is 3 $\mu$H, which is appropriate for IoT/Wearable devices.

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