A Current-Fed Isolated Bidirectional DC–DC Converter

Xiaofeng Sun, *Member, IEEE*, Xiaoying Wu, Yanfeng Shen, *Student Member, IEEE*, Xin Li, and Zhigang Lu

***Abstract*—This paper proposes a current-fed isolated bidirectional dc–dc converter (CF-IBDC) that has the advantages of wide input voltage range, low input current ripple, low conduction losses, and soft switching over the full operating range. Compared with conventional CF-IBDCs, the voltage spikes of the low-voltage (LV) side switches in the proposed converter can be eliminated without additional clamp circuits. The converter adopts the pulse width modulation plus hybrid phase-shift control scheme such that the bus voltage can match the output voltage by means of the transformer. Thus, the current stresses and conduction losses of the converter become lower. In addition, the practical zero voltage switching (ZVS) of the secondary-side switches can be realized by adjusting the phase-shift angle within the secondary side when in light load or no load condition. The operating principles and characteristics including the power transfer, root-mean-square (RMS) current, and soft switching are investigated in detail. Then the design guidelines of inductors are also given. Finally an experimental prototype with 30–60 V input and 400 V/2.5 An output is built to verify the correctness of theoretical analyses.**

***Index Terms*—Current-fed bidirectional isolated dc–dc converter, pulse width modulation (PWM) plus hybrid phase-shift control, practical ZVS, wide input voltage range.**

I. Introduction

FUEL cell is an important technology for power generation systems [1] and hybrid electric vehicles [2]–[4]. The fuel cell stack has a wide output voltage range and demands low input current ripple for the sake of long lifetime [5]. Therefore, the isolated bidirectional dc–dc converters (IBDCs) applied in the fuel cell system should meet the demands mentioned above.

IBDCs can be divided into two classes, i.e., voltage-fed IBDC (VF-IBDC) [6], [7] and current-fed IBDC (CF-IBDC) [8]–[18]. Normally, VF-IBDCs have high current ripples, whereas CF-IBDCs can decrease the input current ripple effectively [8], [9] and prolong the service lifetime of fuel cells [10]. In addition, the low-voltage (LV) side of CF-IBDC can be equivalent to a boost circuit, which makes the CF-IBDCs have the advantages of high-voltage gain [11] and wide input voltage range. However, the soft-switching ranges of CF-IBDCs are limited and there are very high voltage spikes in LV side switches caused by the transformer leakage inductor [12]. All of these problems restrict the applications of CF-IBDCs in the fuel cell systems.

Many CF-IBDCs are proposed in order to decrease the voltage spikes of switches [13]–[18]. The L-L type CF-IBDC with an active clamp circuit proposed in [13] has low input current ripple with two input inductors and eliminates the high-voltage spikes with the help of the active clamp circuit. The boost full-bridge CF-IBDCs with different snubber circuits are proposed in [14]–[17]. The high-voltage spike is eliminated by the RCD snubber circuits, however, the energy absorbed in the buffer capacitor is dissipated on the resistor, resulting in low efficiency [14]. Reference [15] introduces a boost full-bridge CF-IBDC with a simple active clamp circuit, in which the auxiliary switches cannot achieve soft switching and reduce the efficiency. The flyback snubber circuits proposed in [16] and [17] clamp the voltage across the LV side switch to the desired value just slightly higher than the voltage across the low-side transformer. However, the implementations of the snubber circuits and the control scheme are complex in these publications.

The CF-IBDCs mentioned above have low input current ripple and the high-voltage spike is reduced by using the clamp circuit, which however increases the power losses and circuit complexity. In addition, these converters and their control schemes cannot ensure that all switches achieve zero voltage switching (ZVS) over the full operating range. However, all switches in the boost half-bridge CF-IBDC proposed in [18] can realize ZVS over the full operating range by the pulse width modulation (PWM) plus phase-shift control, and the high-voltage spike across the LV side switches is inexistent without additional snubber circuits.

On the other hand, most of the control schemes presented in the above literatures only consider the theoretical ZVS constraint, i.e., the inductor current at the switching instant should have the right polarity. However, taking the parasitic output capacitors of MOSFETs into account, the minimum inductor current to charge or discharge the parasitic output capacitors of MOSFETs during the dead time interval must be considered. If the amplitude of inductor current to realize practical ZVS is larger than that of the required minimum inductor current at heavy load, the conduction losses would increase [19].

Manuscript received July 9, 2016; revised September 11, 2016; accepted October 19, 2016. Date of publication October 31, 2016; date of current version April 24, 2017. This work was supported in part by the National Natural Science Foundation of China under Grant 51677162 and in part by the Natural key research and development project of China under Grant 2016YFB0900300, by Natural Science Foundation of Hebei Province E2015203407 and E2017203337, and by the Lite-On Technology Corporation. Recommended for publication by Associate Editor M. Ferdowsi.

X. Sun, X. Wu, X. Li, and Z. Lu are with the Key Laboratory of Power Electronics for Energy Conservation and Motor Drive of Hebei Province, Department of Electrical Engineering, Yanshan University, Qinhuangdao 066004, China (e-mail: sxf@ysu.edu.cn; wxy2630@qq.com; yddylixin@ysu.edu.cn; zhglu@ysu.edu.cn).

Y. Shen is with theDepartment of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: yaf@et.aau.dk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2623306

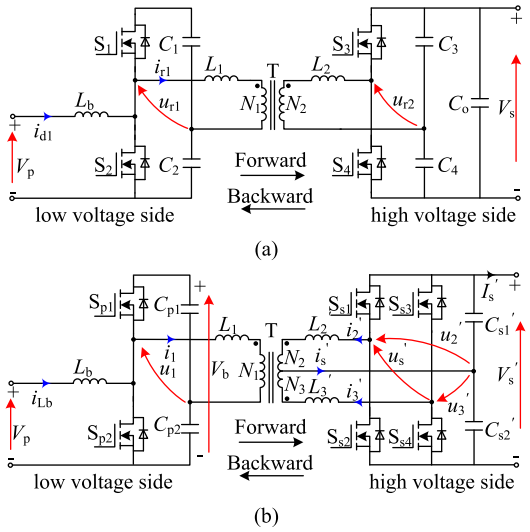


Fig. 1. (a) Boost half-bridge CF-IBDC shown in [18]. (b) Proposed CF-IBDC.

A novel CF-IBDC that has the common features of aforementioned CF-IBDCs, such as wide input voltage range and low input current ripple, is proposed in this paper. Because the voltage spikes across the primary-side switches in the proposed converter are eliminated without extra active clamping or snubber circuits, the converter structure is simpler when compared with topologies in [13]–[17]. In addition, the proposed converter can achieve practical ZVS for all power switches over the full operating range by adopting the PWM plus hybrid phase-shift (HPS) control, which decreases the switching losses, improves the efficiency of the converter, and reduces the electromagnetic interference emission [20]. Moreover, the bus voltage matches the output voltage for the PWM control. Thus, the RMS current and conduction losses are also decreased.

This paper is organized in six sections. The descriptions of the proposed CF-IBDC topology and modulation are discussed in Section II. The operating principle, power transfer, and RMS current are investigated in Section III. Section IV explores the soft-switching characteristic and inductor design of the converter, and the control strategy is also presented in this Section. Experimental results are presented in Section V, and conclusions are finally drawn in Section VI.

II. Topology and Modulation Descriptions

A. Topology Description

The proposed converter has a high-voltage gain because of the same primary-side structure with that of the boost half-bridge CF-IBDC. And by adding an identical secondary-side configuration shown in Fig. 1(a) and combining the two capacitor legs into one (C'_{s1} and C'_{s2}), a new CF-IBDC is proposed, as shown in Fig. 1(b).

The LV side input inductor L_b and the switch leg (S_{p1}, S_{p2}) constitute a bidirectional buck/boost converter. The phase-shift inductances L_1, L'_2, and L'_3, which are the sum of leakage inductances and series inductances, are utilized as the main energy transfer element. The divided capacitors (C_{p1}, C_{p2}, C'_{s1}, and C'_{s2}) are assumed to be large enough, and therefore, the voltages across these capacitors are regarded as

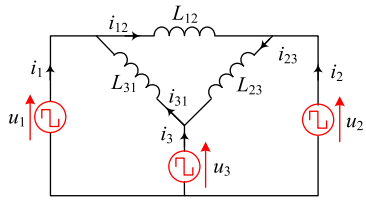


Fig. 2. Δ-type primary-referred ac equivalent circuit.

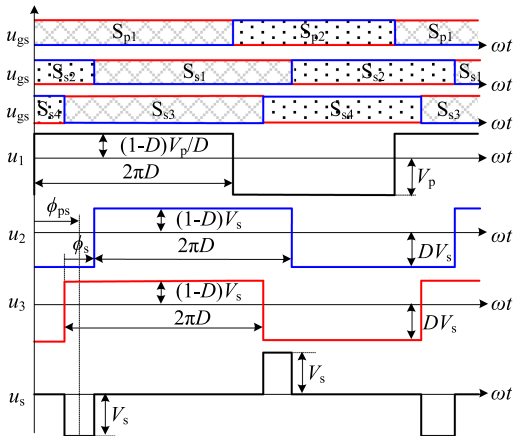


Fig. 3. Driving sequence and definition of phase-shift angles.

constants. The transformer electrically isolates the two ports and matches the voltage on both sides. And the transformer has a turns ratio of $n = N_1 : N_2 = N_1 : N_3$. All secondary-side electrical parameters are indicated with the superscript " '."

In order to facilitate the following analysis, the Δ-type primary-referred equivalent circuit of the proposed converter is derived by ignoring the magnetic inductor L_m whose inductance is much larger than the phase-shift inductance, as shown in Fig. 2.

The ac terminal currents i_1, i_2, and i_3 can be expressed with the inductor currents i_{12}, i_{23}, and i_{31} in the Δ-type equivalent circuit, i.e.,

$$\begin{cases} i_1 = i_{12} - i_{31} \\ i_2 = -i_{12} + i_{23} \\ i_3 = -i_{23} + i_{31} \end{cases}. \tag{1}$$

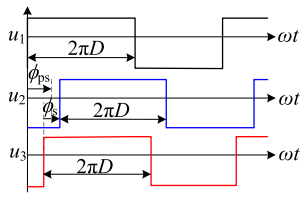
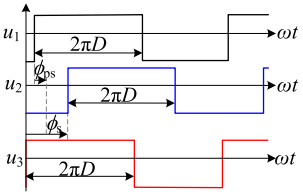
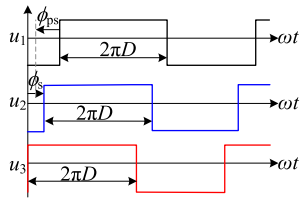
B. Modulation

The duty cycle D of the buck/boost half bridge can be regulated to stabilize the bus voltage V_b when the input voltage changes in a wide range. And on this basis, it is possible to match the bus voltage with the output voltage by choosing an appropriate number of turns for transformer windings, i.e.,

$$V_p/D = nV_s' = V_\mathrm{b}. \tag{2}$$

In order to minimize the RMS current, the duty cycles of the three half bridges are the same. The positive amplitudes of three primary-referred ac voltages are equal to each other and so are the negative amplitudes. Neglecting the dead time, the ac voltages applied to the transformer and the sequence of the driving signal are shown in Fig. 3, where $u_s = u_2 - u_3$. The phase-shift angle between the primary and secondary switching

TABLE I
OPERATING WAVEFORMS AND CONDITIONS FOR THREE MODES

Modes	Operating Waveforms	Conditions
I		$\phi_{ps} > \phi_s/2$ $\phi_{ps} < \phi_{smax} - \phi_s/2$
II		$\phi_{ps} > -\phi_s/2$ $\phi_{ps} < \phi_s/2$
III		$\phi_{ps} < -\phi_s/2$ $\phi_{ps} > -\phi_{smax} + \phi_s/2$

units is defined as $\phi_{\rm ps}$. When the power flows forward, $\phi_{\rm ps}$ is positive, as shown in Fig. 3. The phase-shift angle within the secondary side is ϕ_s and it is positive when u_2 lags u_3.

If ϕ_s remains zero and only phase-shift angle $\phi_{\rm ps}$ and duty cycle D are modulated, u_2 and u_3 are always synchronous and this modulation method is named as the PWM plus single phase-shift (SPS) modulation. If the phase-shift angle ϕ_s is not zero, the PWM plus dual phase-shift (DPS) modulation is applied to the converter. Obviously, the PWM plus SPS modulation is a particular case of the PWM plus DPS modulation. And the analyses below are based on the PWM plus DPS modulation.

III. PWM PLUS DPS MODULATION

A. Operating Modes

For the sake of simplifying the control and analysis, we assume phase-shift angle ϕ_s is greater than or equal to zero and the three inductors in the Δ-type primary-referred equivalent circuit are equal to each other, i.e., $L_{12} = L_{23} = L_{31} = L$.

Depending on the relationship between the rising edges of three ac voltages, three different operating modes can be identified, as shown in Table I. Due to the asymmetrical voltage applied to the transformer windings, there is a limit on the phase-shift angles, which is found to be

$$\begin{cases} \phi_{\rm ps} \pm \phi_s/2 \le \min\{D\pi, (1-D)\pi\} \\ \phi_s < \phi_{\rm smax} \\ \phi_{\rm smax} = \min\{D\pi, (1-D)\pi\} \end{cases}. \tag{3}$$

In order to reduce the proportion of reactive power, the phase-shift angle is usually limited to less than $\pi/4$, and the duty cycle D is constrained within a relatively narrow range near 0.5, e.g., from 0.3 to 0.7 in this paper. Therefore, the restricted condition imposed by (3) will not be a problem for a practical application.

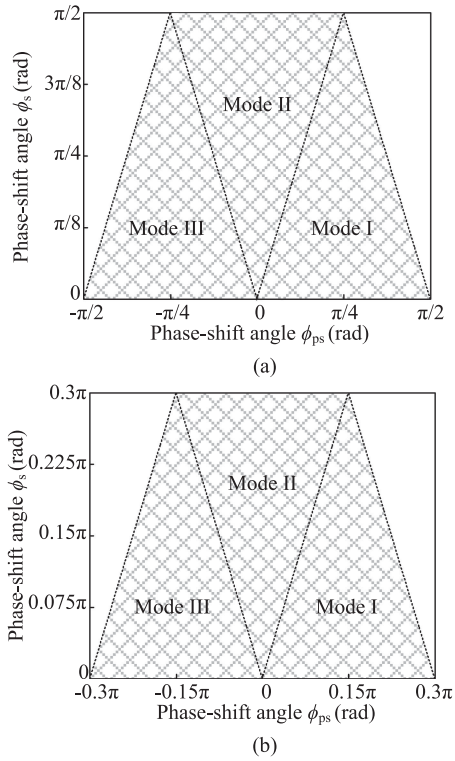


Fig. 4. Three operating areas with different $\phi_{\rm ps}$ and ϕ_s for a constant duty cycle: (a) $D = 0.5$; (b) $D = 0.3$ or $D = 0.7$.

B. Operating Principles

The operating areas with respect to the phase-shift angles $\phi_{\rm ps}$ and ϕ_s with different D are depicted in Fig. 4. Forward power flow occurs in modes I and II, and reverse power flow exists in modes II and III.

Ignoring the dead time, the idealized voltage and inductor current waveforms are shown in Fig. 5. Mode I is taken as an example to explain the operation of the converter under the PWM plus DPS control. As we can see from Fig. 5(a), one switching cycle can be divided into six stages. Due to symmetry, only three stages over a part of switching cycle [0, $2\pi D$] are detailed below.

Stage 1 [0, γ] (cf. Fig. 5*(a) and* Fig. 6*(a)):* The three switches S_{p2}, S_{s2}, and S_{s4} have been conducting before this stage. At the onset of this interval, S_{p1} is turned ON and S_{p2} is turned OFF accordingly. If $i_1(0) < i_{\rm Lbmax}$ at this moment, the antiparallel diode of S_{p1} conducts before the transistor does. Namely, S_{p1} is turned ON with ZVS. When S_{s4} is turned OFF, this interval is over. To simplify the analysis, normalized variables are used in the equations and expressions throughout the paper. The defined power and current bases are defined as

$$\begin{cases} P_{\rm base} = \dfrac{{V_s}^2}{\omega L} \\ I_{\rm base} = \dfrac{V_s}{\omega L} \end{cases} \tag{4}$$

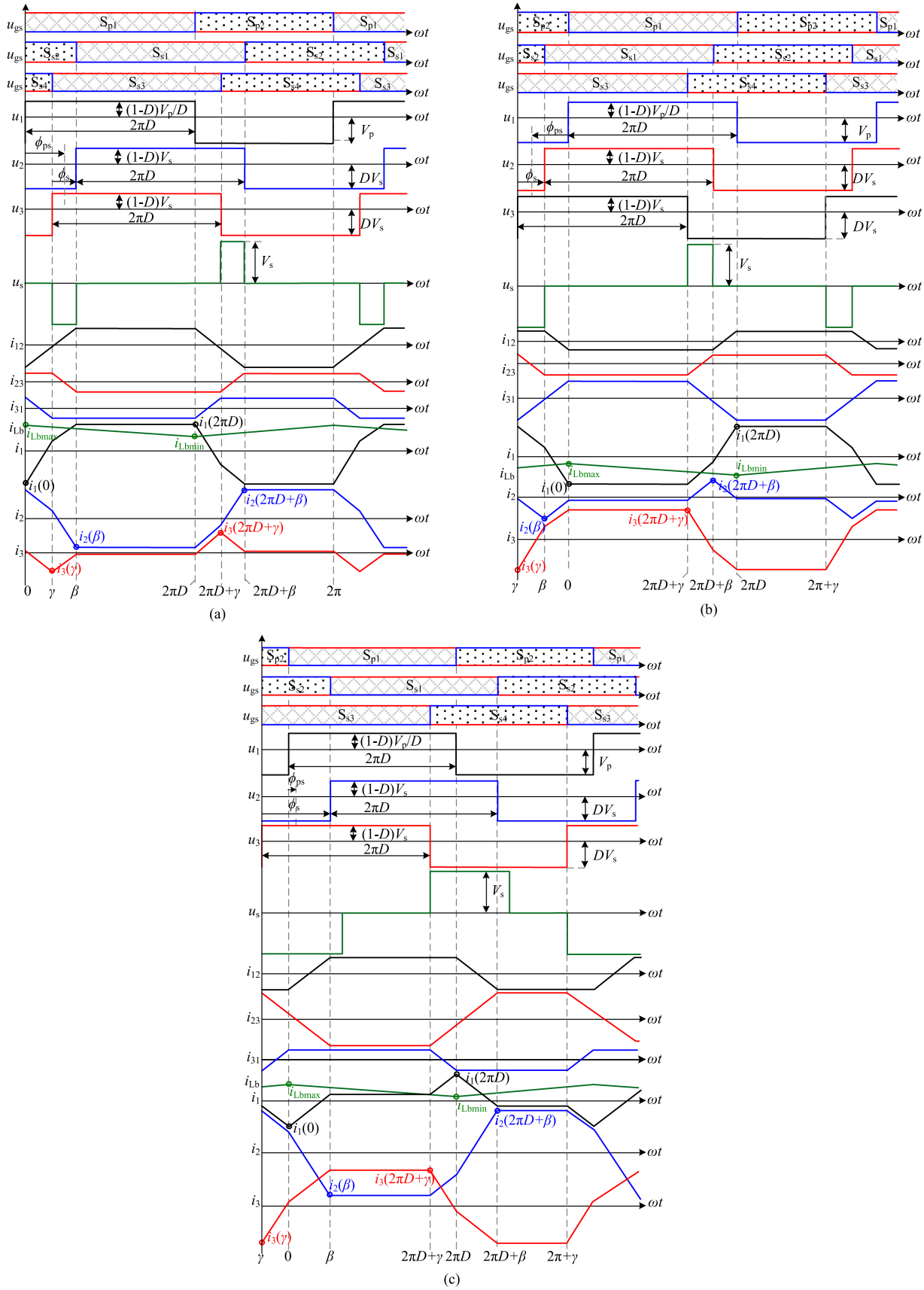


Fig. 5. PWM plus DPS modulation scheme and idealized operating waveforms in (a) mode I; (b) mode III; (c) mode II.

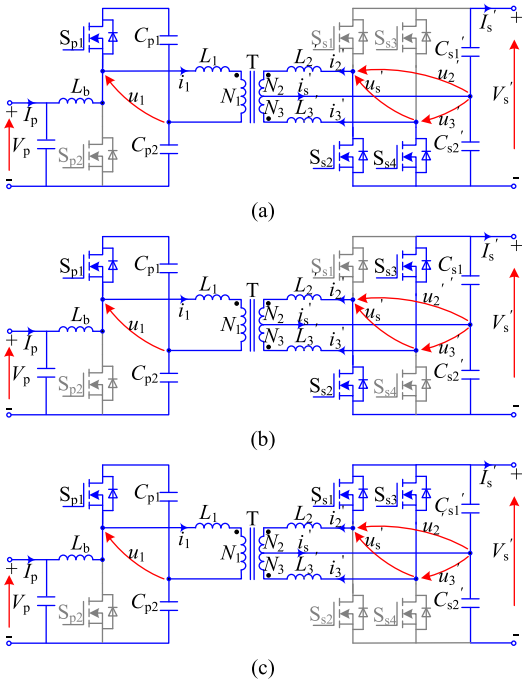


Fig. 6. Equivalent circuits of the proposed converter with the PWM plus DPS control in mode I: (a) stage 1 [0, γ]; (b) stage 2 [γ, β]; (c) stage 3 [β, $2\pi D$].

where $\omega = 2\pi f_s$, f_s is the switching frequency.

Stage 2 [γ, β] (cf. Fig. 5*(a) and* Fig. 6*(b)):* S_{p1}, S_{s2}, and S_{s4} have been conducting before this stage. At the onset of this interval, S_{s3} is turned ON and S_{s4} is turned OFF accordingly. If $i_3(\gamma) < 0$ at this moment, S_{s3} is turned ON with ZVS. When S_{s2} is turned OFF, this interval is over.

Stage 3 [β, $2\pi D$] (cf. Fig. 5*(a) and* Fig. 6*(c)):* S_{p1}, S_{s2}, and S_{s3} have been conducting before this stage. At the onset of this interval, S_{s1} is turned ON and S_{s2} is turned OFF accordingly. If $i_2(\beta) < 0$ at this moment, S_{s1} is turned ON with ZVS. S_{p1} is turned OFF at the end of this stage.

C. Power Characteristics

The normalized power $P_o{}^*$ of the proposed converter with the PWM plus DPS control can be derived as

$$P_o{}^* = \frac{1}{P_{base}} \cdot \frac{1}{2\pi} \int_0^{2\pi} u_1 \ i_1 \mathrm{d}\theta$$

$$= \frac{1}{4\pi} \begin{cases} -8\left(-1+D\right) D\pi\phi_{ps} - 2{\phi_{ps}}^2 - \frac{1}{2}{\phi_s}^2 & \text{ModeI} \\ -8\left(-1+D\right) D\pi\phi_{ps} - 2\phi_{ps}\phi_s & \text{ModeII} \\ -8\left(-1+D\right) D\pi\phi_{ps} + 2{\phi_{ps}}^2 + \frac{1}{2}{\phi_s}^2 & \text{ModeIII} \end{cases} \quad (5)$$

where the phase-shift angle ϕ_{ps} and ϕ_s are in radians.

The normalized power $P_o{}^*$ with respect to the two phase-shift angles ϕ_{ps} and ϕ_s for different duty cycles can be plotted, as shown in Fig. 7. As can be seen from Fig. 7(b), the direction of power flow is fully controlled by the phase-shift angle ϕ_{ps}, instead of ϕ_s. And $P_o{}^*$ increases with the phase-shift angle ϕ_{ps} over the entire phase-shift range. Therefore, the phase-shift

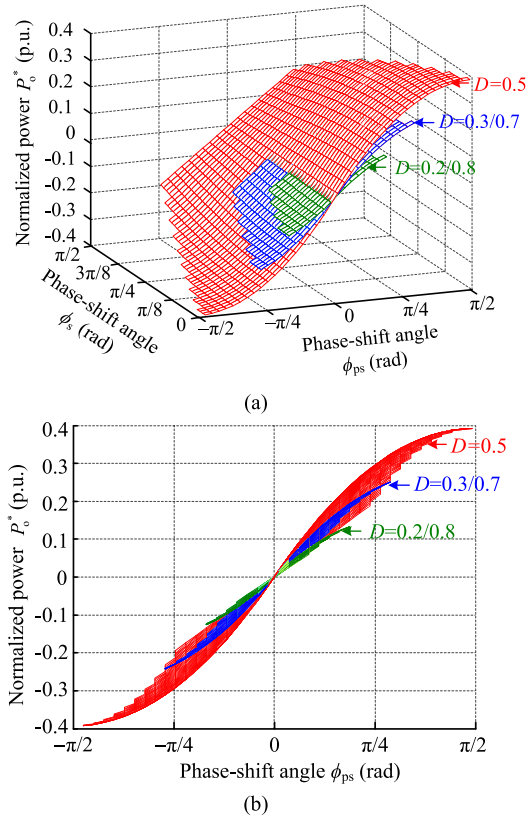


Fig. 7. (a) Normalized power $P_o{}^*$ with respect to two phase-shift angles ϕ_{ps} and ϕ_s for different duty cycles. (b) Projection of (a) in the ϕ_{ps} -$P_o{}^*$ plane.

angle ϕ_{ps} is chosen as the dominant control variable of the normalized power $P_o{}^*$. The duty cycle D is decided by the input and output voltages. And it clearly shows that as the duty cycle D becomes either larger or smaller than 0.5, the maximum phase shift is constrained to a smaller value and the power flow also becomes less.

D. RMS Current

On the LV side, the current flowing through the switch leg S_{p1}, S_{p2} is the difference between the input current i_{Lb} and the primary-side phase-shift inductor current i_1. On the HV side, currents i_2 and i_3 flow through the switch leg S_{s1}, S_{s2} and switch leg S_{s3}, S_{s4}, respectively. Therefore, the primary-referred total LV-side and HV-side normalized square RMS currents are defined as (6) and (7), respectively.

Fig. 8 shows the 3-D graphs of the total LV- and HV-side normalized square RMS currents with respect to ϕ_{ps} and ϕ_s for different duty cycles. As can be seen, the normalized square RMS current gets larger with the increase of the phase-shift angle ϕ_s for the constant ϕ_{ps} and D. Consequently, the phase-shift angle ϕ_s should be kept as small as possible to minimize the conduction losses when ϕ_{ps} is small. However, when ϕ_{ps} is greater than $0.5D\pi$, the LV-side normalized square RMS current decreases with the increase of ϕ_s, and the decrease is fairly small. Therefore, it is appropriate to keep ϕ_s as small as possible Eqn(6)–(7) are shown at the bottom of the next page.

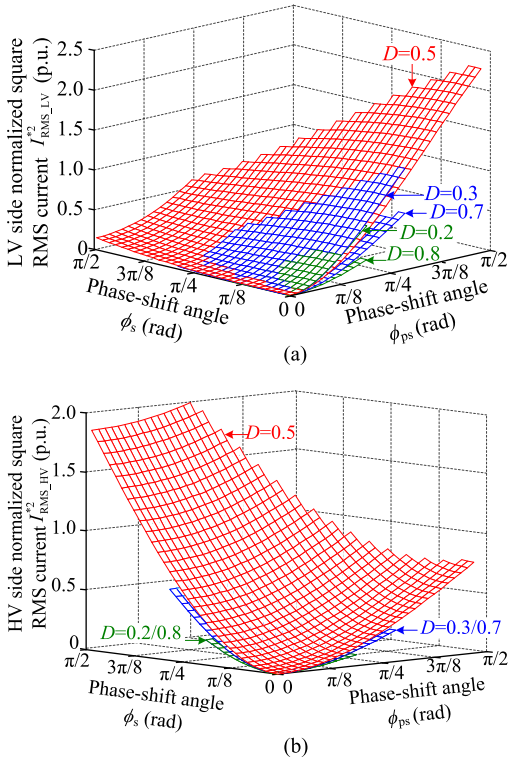


Fig. 8. Primary-referred total normalized square RMS current with respect to two phase-shift angles ϕ_{ps} and ϕ_s for different duty cycles. (a) LV side; (b) HV side.

E. Advantages of Modulation

If the converter only adopts the phase-shift control, the duty cycle D is kept as 0.5 and the bus voltage would be changed with the alteration of the input voltage V_p. Thus, the bus voltage cannot match the output voltage V_s when $V_p \neq 0.5\,V_s$. If the converter adopts the PWM plus phase-shift control, the bus voltage is constant and matches the output voltage always. The

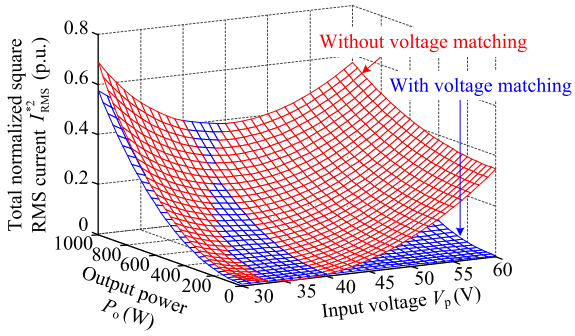


Fig. 9. Total normalized square RMS current with respect to the input voltage V_p and the output power P_o.

total normalized square RMS currents of the proposed converter with and without voltage matching are shown in Fig. 9. The total normalized square RMS current is defined as

$$I^{*2}_{\mathrm{RMS}} = I^{*2}_{\mathrm{RMS\_LV}} + I^{*2}_{\mathrm{RMS\_HV}}/n^2. \tag{8}$$

As can be seen from Fig. 9, the total normalized square RMS current without voltage matching is less than that with voltage matching when the input voltage is between 35 to 40 V. It is because the bus voltage is twice over the input voltage without voltage matching, which influences the magnitudes of the output power and the inductor current. However, the total normalized square RMS current is greatly decreased with voltage matching in other cases. Therefore, the PWM control helps the proposed converter to decrease the conduction losses and improve the efficiency.

Ignoring the dead time, the ideal voltage and inductor current waveforms with the PWM plus SPS control and the PWM plus DPS control are shown in Fig. 10. As we can see from Fig. 10, the amplitudes of $i_2(\beta)$, $i_2(2\pi D+\beta)$, $i_3(\gamma)$, and $i_3(2\pi D+\gamma)$ become larger under the PWM plus DPS control,

$$\begin{aligned} I^{*2}_{\mathrm{RMS\_LV}} &= \frac{1}{2\pi}\int_0^{2\pi}\left(\left(i^*_1(\theta)-i^*_{\mathrm{Lb}}(\theta)\right)^2\right)\mathrm{d}\theta \\ &= \frac{1}{192D^2L_{\mathrm{b}}^2\pi^2}\begin{cases} -24L_{\mathrm{b}}\phi_s^2(4D^3\pi^2(-1+D)L+2D\pi\,|\phi_{\mathrm{ps}}|\,(DL+2L_{\mathrm{b}})-L_{\mathrm{b}}\phi_{\mathrm{ps}}^2) \\ \quad +16(4D^4L^2\pi^4(-1+D)^2-24D^2\pi^2\phi_{\mathrm{ps}}^2L_{\mathrm{b}}(-1+D)(DL+2L_{\mathrm{b}}) \\ \quad -4DL_{\mathrm{b}}\pi|\phi_{\mathrm{ps}}|^3(DL+6L_{\mathrm{b}}-4DL_{\mathrm{b}})+3L_{\mathrm{b}}^2\phi_{\mathrm{ps}}^4)+32D^2L_{\mathrm{b}}^2\pi\phi_s^3+3L_{\mathrm{b}}^2\phi_s^4 & \text{Mode I \& III} \\ 8(D^2L_{\mathrm{b}}\pi\phi_s^3(-L+2L_{\mathrm{b}})-12D\pi L_{\mathrm{b}}\phi_s\phi_{\mathrm{ps}}^2(DL-2DL_{\mathrm{b}}+4L_{\mathrm{b}}) \\ \quad +6L_{\mathrm{b}}\phi_s^2(-2D^3\mathrm{L}\pi^2(-1+D)+L_{\mathrm{b}}\phi_{\mathrm{ps}}^2) \\ \quad +8D^2\pi^2(-1+D)(D^2L^2\pi^2(-1+D)-6L_{\mathrm{b}}\phi_{\mathrm{ps}}^2(DL+2L_{\mathrm{b}}))) & \text{Mode II} \end{cases} \end{aligned} \tag{6}$$

$$\begin{aligned} I^{*2}_{\mathrm{RMS\_HV}} &= \frac{1}{2\pi}\int_0^{2\pi}\left(i_2^{*2}(\theta)+i_3^{*2}(\theta)\right)\mathrm{d}\theta \\ &= \frac{1}{24\pi^2}\begin{cases} -(16\phi_s^3+8\phi_{\mathrm{ps}}^2(6(-1+D)D\pi+|\phi_{\mathrm{ps}}|)+6\phi_s^2(18(-1+D)D\pi+|\phi_{\mathrm{ps}}|)) & \text{Mode I \& III} \\ -(\phi_s^3+12\phi_{\mathrm{ps}}^2\phi_s+48\phi_{\mathrm{ps}}^2(-1+D)D\pi+108\phi_s^2(-1+D)D\pi) & \text{Mode II} \end{cases}. \end{aligned} \tag{7}$$

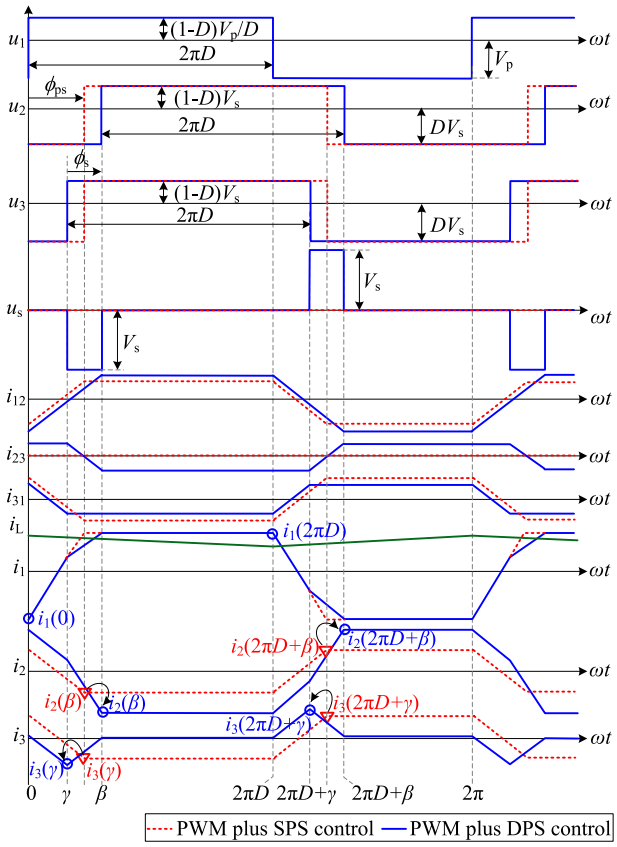


Fig. 10. Differences between the PWM plus SPS control and the PWM plus DPS control.

which is beneficial to the practical ZVS realization of the secondary-side switches. However, the large current amplitude at the switching instant results in the large conduction losses and low efficiency. Hence, the PWM plus DPS modulation can be adopted to realize practical ZVS at light load and the PWM plus SPS modulation can be used to decrease the circuiting power effectively at heavy load.

IV. Soft-Switching Analysis and Control Scheme

A. ZVS of Primary-Side Switches

The currents to realize theoretical ZVS for primary-side switches are determined by the input current i_{Lb} and the primary-side phase-shift inductor current i_1. Thus, the theoretical ZVS conditions for the primary-side switches are derived as

$$\begin{cases} i_1(0) - (I_{\mathrm{Lb}} + \triangle I_{\mathrm{Lb}}/2) < 0 \\ i_1(2\pi D) - (I_{\mathrm{Lb}} - \triangle I_{\mathrm{Lb}}/2) > 0 \end{cases} \tag{9}$$

where I_{Lb} is the average input current, ΔI_{Lb} is the amplitude of the ripple current in i_{Lb}, given by

$$\triangle I_{\mathrm{Lb}} = (1-D)V_p/(L_{\mathrm{b}} f_s). \tag{10}$$

The primary current i_1 at the switching instant can be found

$$\begin{cases} i_1^*(0) = -2D\phi_{\mathrm{ps}} \\ i_1^*(2\pi D) = -2(-1+D)\phi_{\mathrm{ps}} \end{cases}. \tag{11}$$

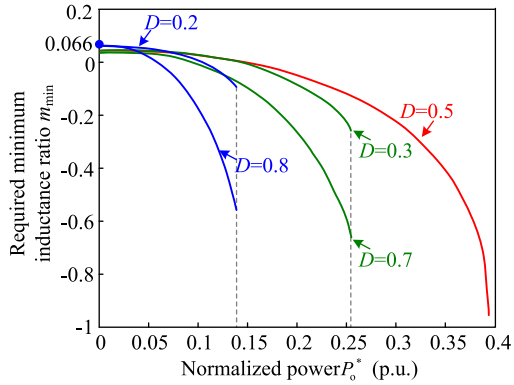


Fig. 11. Required minimum inductance ratio $m_{\min}$ with respect to the normalized power P_{o}^*.

As can be seen from Fig. 5(a), when power flows forward, S_{p1} can realize theoretical ZVS more easily than S_{p2} for the larger current flowing through S_{p1} at switching instant. Thus, only the theoretical ZVS constraint of S_{p2} is considered:

$$\phi_s^2 > -4\phi_{\mathrm{ps}}^2 - 8D^2\pi^2(1-D)m \tag{12}$$

where $m = L/L_b$ is the inductance ratio.

The phase-shift angle ϕ_{ps} is greater than or equal to 0, and thus the expression on the right-hand side of (12) is always less than 0. As a result, S_{p1} and S_{p2} can always realize theoretical ZVS.

The parasitic output capacitance of transistors leads to incomplete commutation in practice, and a minimum reverse current I_{ZVS} is needed by transistors at each switching instant. According to (9) and replacing 0 with $-I_{\mathrm{ZVS}}$, the restricted condition of the inductance ratio m for primary-side switches to realize practical ZVS can be calculated as

$$m > m_{\min},\ m_{\min} = \frac{-8DI_{\mathrm{ZVS}}^*\pi + 4\phi_{\mathrm{ps}}^2 + \phi_s^2}{8(-1+D)D^2\pi^2}. \tag{13}$$

Based on (5) and (13), the required minimum inductance ratio $m_{\min}$ with respect to the normalized power $P_{\mathrm{o}}{}^*$ is shown in Fig. 11. The required minimum inductance ratio $m_{\min}$ increases with the decrease of the normalized power $P_{\mathrm{o}}{}^*$. Therefore, the inductance ratio m must be larger than the maximum in Fig. 11 such that S_{p1} and S_{p2} can realize practical ZVS over the full operating range.

B. Design Guidelines

To allow for a desired maximum power flow $P_{\mathrm{o}}{}^*$, the maximum inductance is determined by the maximum/minimum operating duty cycle as shown in Fig. 12 (choose the smaller inductance value), where the inductance is expressed in p.u. with the base defined as $L_{\mathrm{base}} = V_s^2/\omega P_{\mathrm{o}}$.

In addition, a small phase-shift inductance means the low current stress, circulating current and small size. However, a small phase-shift inductance will increase the sensitivity of the power flow to the phase shift and thus require a higher accuracy of the control circuit. And the bigger phase-shift inductance means the larger inductance ratio m, which is beneficial to realizing practical ZVS for the primary-side switches. All in all, the inductance

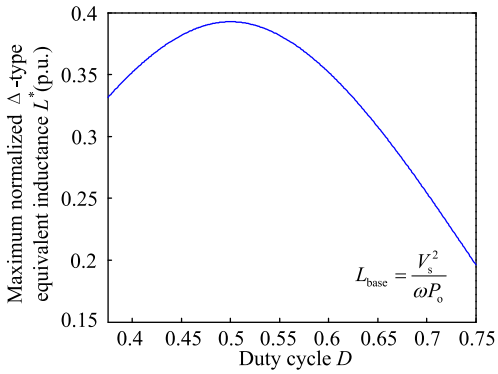


Fig. 12. Maximum allowed Δ-type equivalent inductance L with respect to the duty cycle D.

L is a tradeoff among the losses of the converter, the ability of the control circuit and the realization of practical ZVS, and must be smaller than the maximum in Fig. 12.

According to the requirement of the input current ripple, the input inductor L_b is designed as

$$L_{\rm b} = (1-D)V_p/(\triangle\, I_{\rm Lb} f_s). \tag{14}$$

C. ZVS of Secondary-Side Switches

The current to realize theoretical ZVS for secondary-side switches is only determined by the secondary-side currents of the transformer at the switching instant. The theoretical ZVS conditions for the switches $\rm S_{s1}$–$\rm S_{s4}$ are

$$\begin{cases} i_2^*(\beta) = (-1+D)\,(3\phi_s + 2\phi_{\rm ps})/2 < 0 \\ i_2^*(2\pi D+\beta) = D\,(3\phi_s + 2\phi_{\rm ps})/2 > 0 \end{cases} \tag{15}$$

$$\begin{cases} i_3^*(\gamma) = (1-3D)\,\phi_s/2 + (-1+D)\,\phi_{\rm ps} < 0 \\ i_3^*(2\pi D+\gamma) = (2-3D)\phi_s/2 + D\phi_{\rm ps} > 0 \end{cases}. \tag{16}$$

Thus, the restricted condition to realize theoretical ZVS can be derived for the switches $\rm S_{s1}$ and $\rm S_{s2}$

$$\phi_s > -2\phi_{\rm ps}/3. \tag{17}$$

Similarly, the theoretical ZVS condition for switches $\rm S_{s3}$ and $\rm S_{s4}$ can also be presented as

$$\begin{cases} \phi_s < \dfrac{-2(-1+D)}{1-3D}\phi_{\rm ps} \cap \phi_s > \dfrac{-2D}{2-3D}\phi_{\rm ps}, 0 < D < \dfrac{1}{3} \\ \phi_s > \dfrac{-2(-1+D)}{1-3D}\phi_{\rm ps} \cap \phi_s > \dfrac{-2D}{2-3D}\phi_{\rm ps}, \dfrac{1}{3} < D < \dfrac{2}{3} \\ \phi_s > \dfrac{-2(-1+D)}{1-3D}\phi_{\rm ps} \cap \phi_s < \dfrac{-2D}{2-3D}\phi_{\rm ps}, \dfrac{2}{3} < D < 1 \end{cases}. \tag{18}$$

In mode I, the phase-shift angles $\phi_{\rm ps}$ and ϕ_s are positive. Hence, (17) is met always, and thus, switches S_{s1} and S_{s2} can operate with theoretical ZVS. By substituting the conditions of two phase-shift angles in mode I (cf. Table I) into (18), we can find that switches S_{s3} and S_{s4} can also realize theoretical ZVS. Therefore, all secondary-side switches can operate with theoretical ZVS in mode I.

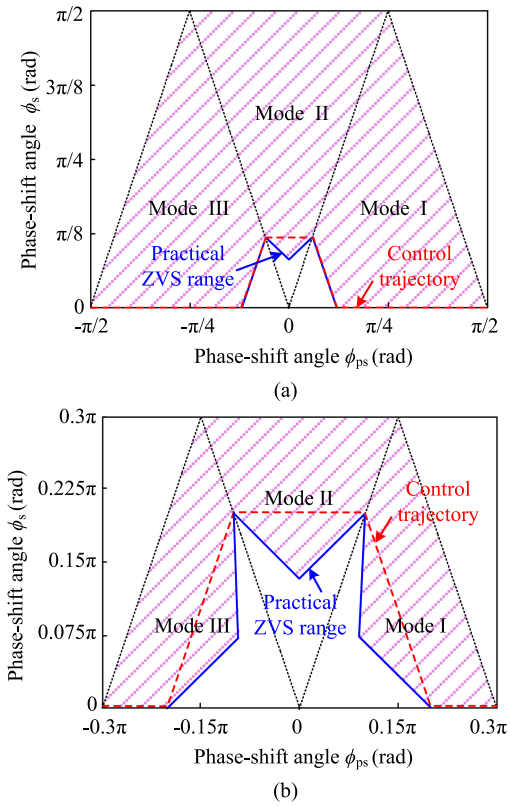


Fig. 13. Practical ZVS range of the secondary-side switches (solid lines) and the simplified control trajectory (dashed lines) with different duty cycles. (a) $D = 0.5$; (b) $D = 0.3$ or $D = 0.7$.

By replacing 0 with $-I_{\rm ZVS}^*$ in (15) and (16), the practical ZVS conditions of secondary-side switches can be derived and plotted in Fig. 13 (solid lines). It clearly shows that as the duty cycle D becomes either larger or smaller than 0.5, the practical ZVS region is reduced. According to RMS current characteristic, ϕ_s should be kept as small as possible to minimize conduction losses at light load. Therefore, in order to realize the practical ZVS for secondary-side switches and minimize conduction losses, ϕ_s shall be controlled in accordance with the boundary of the practical ZVS region.

The boost half-bridge CF-IBDC shown in Fig. 1(a) can realize theoretical ZVS over the full power range [18]. The practical ZVS range of secondary-side switches in the boost half-bridge CF-IBDC is shown in Fig. 14. As can be seen, the secondary-side switches in the boost half-bridge CF-IBDC cannot achieve practical ZVS at light load. Therefore, the proposed CF-IBDC has obvious advantages at light load.

D. Control Scheme

The practical ZVS boundary in Fig. 13 is a piecewise function and becomes complicated when duty cycle D is unequal to 0.5. A simplified control trajectory is obtained at the expense of degrading system efficiency, as shown by the dashed lines in Fig. 13.

The required phase-shift angle ϕ_s for achieving practical ZVS of secondary-side switches can be derived, as listed in Table II.

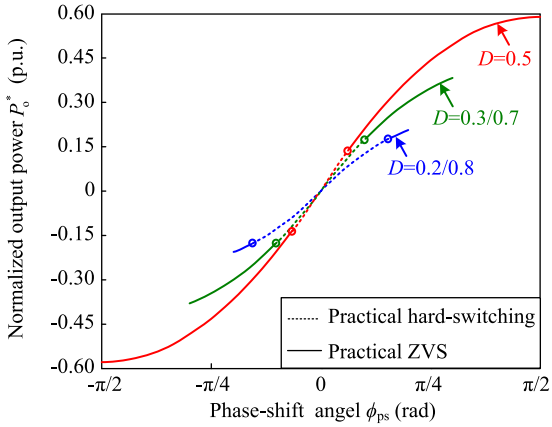


Fig. 14. Practical ZVS range of secondary-side switches in the boost half-bridge CF-IBDC.

TABLE II
REQUIRED SECONDARY-SIDE PHASE-SHIFT ANGLE ϕ_s IN DIFFERENT CONDITIONS FOR ACHIEVING PRACTICAL ZVS OF SECONDARY-SIDE SWITCHES

Modes & conditions		Required phase-shift angle ϕ_s	Modulation
II		I^*_{ZVS}/M	PWM + DPS
I and III	$\lvert\phi_{ps}\rvert \le I^*_{ZVS}/M$	$-2\lvert\phi_{ps}\rvert + 2I^*_{ZVS}/M$	PWM + DPS
	$\lvert\phi_{ps}\rvert > I^*_{ZVS}/M$	0	PWM + SPS

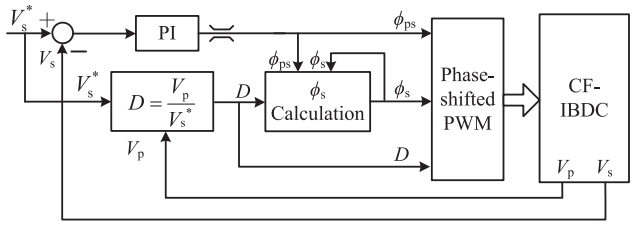


Fig. 15. PWM plus HPS control scheme applied to the proposed converter.

If the proposed converter operates in mode II, the phase-shift angle ϕ_s is equal to I^*_{ZVS}/M, where $M = \min\{D, 1-D\}$. However, when it enters modes I and III, the phase-shift angle ϕ_s begins to linearly decline with respect to the phase-shift angle ϕ_{ps} if $|\phi_{ps}| \le I^*_{ZVS}/M$. And ϕ_s is kept to be 0 to minimize the conduction losses when $|\phi_{ps}| > I^*_{ZVS}/M$.

As shown in Fig. 15, the proposed control scheme employs one PI controller that devotes to regulate V_s. The duty cycle D is aimed at matching the output voltage and bus voltage to minimize the RMS current, and the phase-shift angle ϕ_s is utilized for the practical ZVS of secondary-side switches. Specifically, D is controlled based on (2), and ϕ_s is calculated in terms of Table II. The control scheme is fully digitalized and implemented with a digital signal processor (DSP).

V. EXPERIMENTAL RESULTS

To verify the correctness of the aforementioned analyses, a 1-kW laboratory prototype has been built based on the TMS320F28334 DSP. The detailed parameters are presented in Table III, and the photo of the experimental prototype is shown in Fig. 16. The LV side bridge capacitor is composed of seven 4.7 uF polypropylene film capacitors connected in parallel with an electrolytic capacitor to solve the high current.

TABLE III
PARAMETERS OF THE CONVERTER PROTOTYPE

Description	Symbol	Parameter
Primary-side voltage range	V_p	30–60 V
Secondary-side voltage	V_s'	400 V
Duty cycle	D	0.375–0.75
Rated power transfer	P	1 kW
Rated output current	I_s'	2.5 A
Switching frequency	f_s	100 kHz
Transformer turns ratio	$N_1 : N_2 : N_3$	2: 10: 10
Input inductor	L_b	10.54 μH
Phase-shift inductors	L_1	0.74 μH
	L_2'	18.56 μH
	L_3'	18.41 μH
Primary-side capacitors	C_{p1}, C_{p2}	33 μF
Secondary-side capacitors	C_{s1}', C_{s2}'	6.6 μF
Power switches	S_{p1}–S_{p2}	IPP041N12N3($R_{ds,on}$ = 0.0038 Ω)
	S_{s1}–S_{s4}	IRFP450($R_{ds,on}$ = 0.4 Ω)

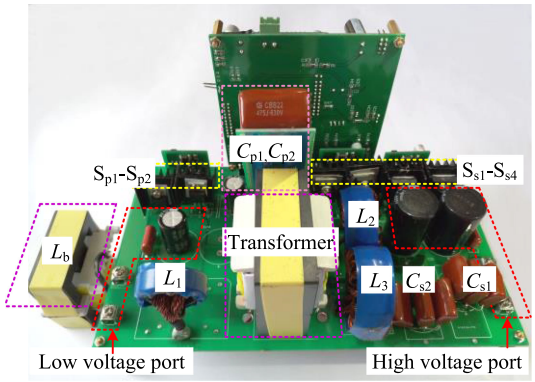


Fig. 16. Experimental prototype of the proposed converter.

For high voltage MOSFET transistors, the reverse current that is greater than 2 A is supposed to be sufficient to recharge the parasitic output capacitance within a 200 ns dead-time interval, leading to the realization of the practical ZVS [22]. Therefore, $I_{ZVS} = 2$ A is adopted in this paper.

Fig. 17 shows the steady-state operating waveforms of the converter under the PWM plus HPS modulation in three modes. As one can see, the proposed CF-IBDC operates pretty well in all modes, with the waveforms matching with the analysis in Section III. For a range of primary-side voltage $V_p \in [30\,\text{V}, 60\,\text{V}]$, the duty cycle D varies from 0.375 to 0.75, which is determined by the voltage matching condition (2). When the converter operates in mode II, the phase-shift angle ϕ_s is kept as 0.022π, as indicated in Fig. 17(b). When the operation enters modes I or III, ϕ_s begins to decrease with the increase of the power, as indicated in Fig. 17(a)–(d). When the power is large enough, ϕ_s is kept as 0 to minimize the conduction losses, as shown in Fig. 17(d) and (f).

Fig. 18 illustrates the ZVS behavior of the proposed CF-IBDC. As can be seen, the voltage spikes of the primary-side switches are negligible and all switches in the converter achieve practical ZVS. Even at light load (0.15 kW), shown in Fig. 18(a),

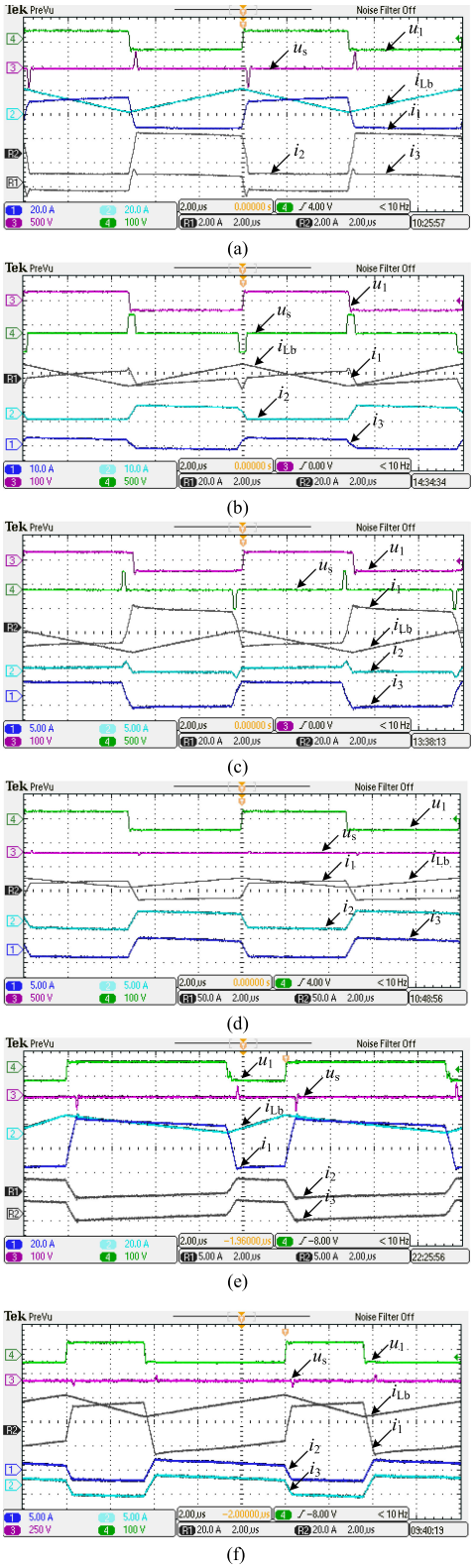


Fig. 17. Steady-state operating waveforms of the proposed converter in different modes. (a) Mode I: $\phi_s \neq 0, V_p = 40\,\text{V}, D = 0.5, \phi_{\text{ps}} = 0.017\pi, P_{\text{o}} = 0.15\,\text{kW}$; (b) Mode II: $\phi_s \neq 0, V_p = 40\,\text{V}, D = 0.5, \phi_{\text{ps}} = 0.01\pi, P_{\text{o}} = 0.1\,\text{kW}$; (c) Mode III: $\phi_s \neq 0$, $V_p = 40\,\text{V}$, $D = 0.5$, $\phi_{\text{ps}} = -0.02\pi$, $P_{\text{o}} =$ - 0.16 kW; (d) Mode I: $\phi_s = 0, V_p = 40\,\text{V}, D = 0.5, \phi_{\text{ps}} = 0.11\pi$, $P_{\text{o}} = 0.83\,\text{kW}$; (e) Mode I: $\phi_s = 0, V_p = 60\,\text{V}, D = 0.75, \phi_{\text{ps}} = 0.11\pi$, $P_{\text{o}} = 0.52\,\text{kW}$; (f) Mode I: $\phi_s = 0$, $V_p = 30\,\text{V}$, $D = 0.375$, $\phi_{\text{ps}} = 0.11\pi, P_{\text{o}} = 0.66\,\text{kW}$.

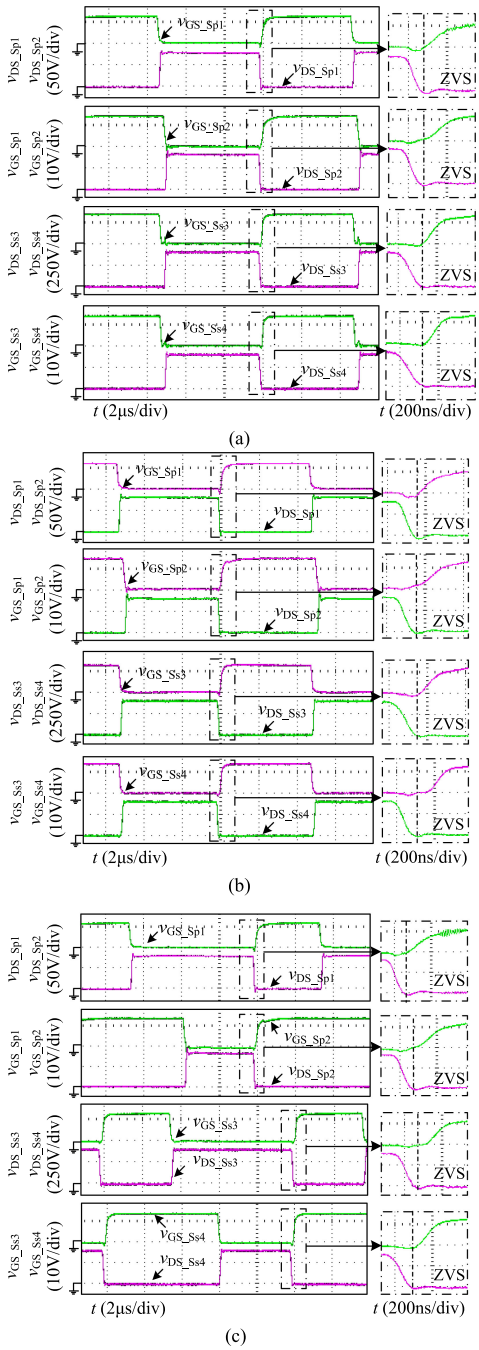


Fig. 18. Experimental soft-switching waveforms of the proposed CF-IBDC under the PWM plus HPS control. (a) Mode I: $\phi_s \neq 0, V_p = 40\,\text{V}, D = 0.5, \phi_{\text{ps}} = 0.017\pi, P_{\text{o}} = 0.15\,\text{kW}$. (b) Mode I: $\phi_s = 0, V_p = 40\,\text{V}, D = 0.5, \phi_{\text{ps}} = 0.11\pi, P_{\text{o}} = 0.83\,\text{kW}$; (c) Mode I: $\phi_s = 0, V_p = 30\,\text{V}, D = 0.375, \phi_{\text{ps}} = 0.11\pi, P_{\text{o}} = 0.66\,\text{kW}$.

the practical ZVS is also attained with an appropriate ϕ_s ($\phi_s = 0.01\pi$). However, the secondary-side switches in the boost half-bridge CF-IBDC, shown in Fig. 1(a), cannot achieve practical ZVS at light load (0.2 kW), as shown in Fig. 19. Therefore, the proposed CF-IBDC has a better practical ZVS characteristic than that of the boost half-bridge CF-IBDC at light load.

The efficiency of the proposed converter is equal to the output power divided by the input power. The output power is

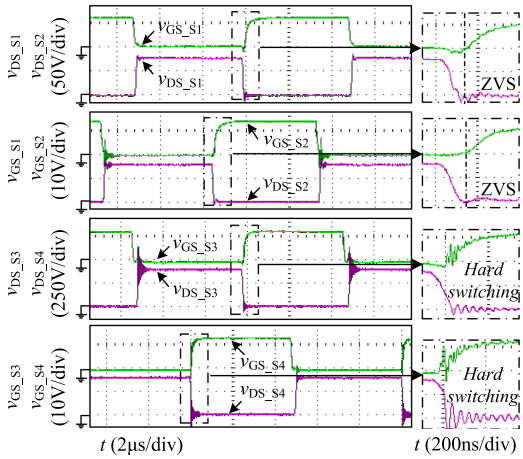


Fig. 19. Experimental soft-switching waveforms of the boost half-bridge CF-IBDC: $V_p = 40$ V, $V_s = 400$ V, $D = 0.5$, $\phi_{ps} = 0.026\pi$, $P_o = 0.2$ kW.

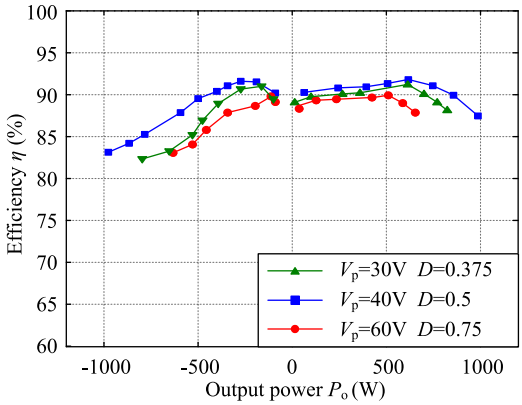


Fig. 20. Efficiency curves with respect to the output power P_o with different input voltages.

measured by the single phase power analyzer PM100 made by Voltech. The input power is equal to the input voltage times the input current. And the input voltage and current are obtained by the digital multimeters made by FLUKE. Fig. 20 shows the efficiencies of the converter with the PWM plus HPS control when input voltages are 30, 40, and 60 V. As the duty cycle D becomes either larger or smaller than 0.5, the maximum output power P_o decreases and the efficiency becomes lower. The maximum efficiency is 91.79% in Fig. 20, and the efficiency of the converter can still reach up to 88.7% with forward power flow at light load. In addition, for a range of primary-side voltage $V_p \in [30\,\text{V}, 60\,\text{V}]$, the efficiency with respect to V_p is plotted in Fig. 21 and the maximum efficiency occurs when $D = 0.5$, i.e., $V_p = 40\,\text{V}$.

Fig. 22 plots the efficiencies of the proposed CF-IBDC and the boost half-bridge CF-IBDC. On account of ZVS, the efficiency of the proposed CF-IBDC is higher than that of the boost half-bridge CF-IBDC when the output power is below approximate 300 W. With the increase of output power, the efficiency of the proposed CF-IBDC is lower than that of the boost half-bridge CF-IBDC for the losses occurred on the secondary side of the proposed CF-IBDC. However, at heavy load, the

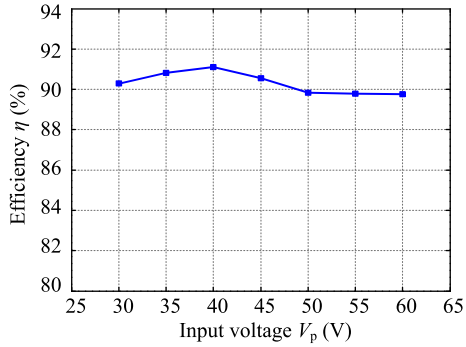


Fig. 21. Efficiency curve with respect to the input voltage with the same output power $P_o = 430$ W.

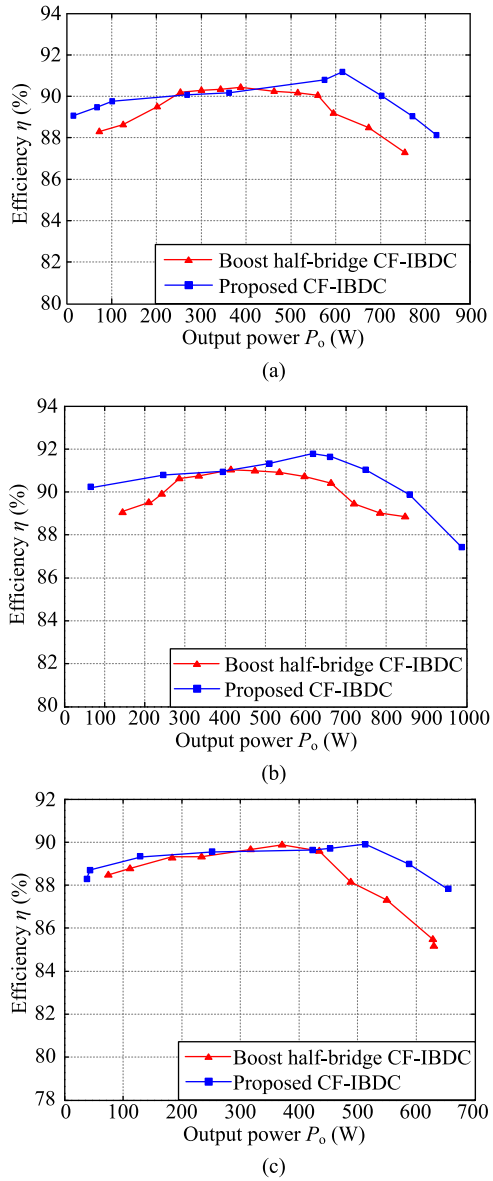


Fig. 22. Efficiency curves of the different CF-IBDCs for different input voltage: (a)$V_p = 30$ V; (b)$V_p = 40$ V; (c)$V_p = 60$ V.

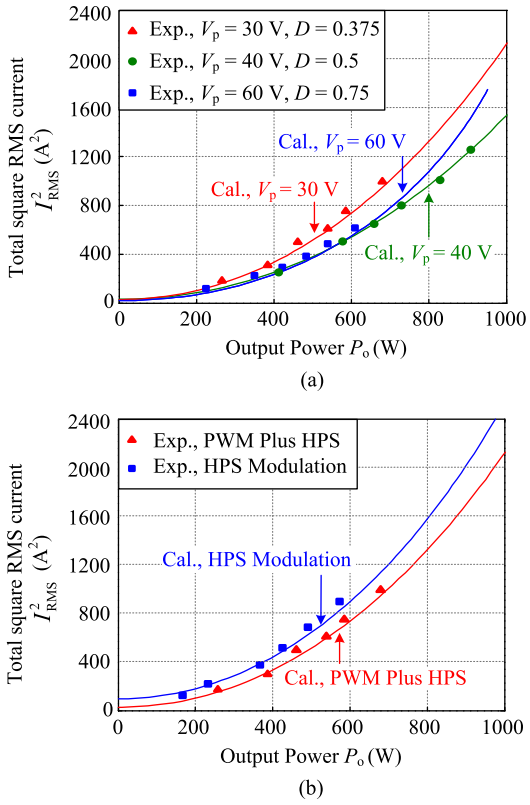


Fig. 23. (a) Total square RMS current versus output power for different primary-side voltages. (b) Total square RMS current versus output power when $V_p = 30$ V for different control strategies.

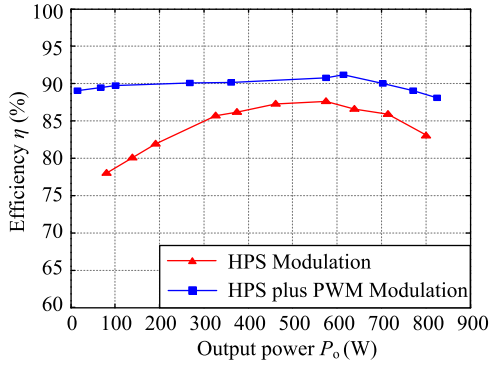


Fig. 24. Efficiency curves of the converter at $V_p = 30$ V with different modulations.

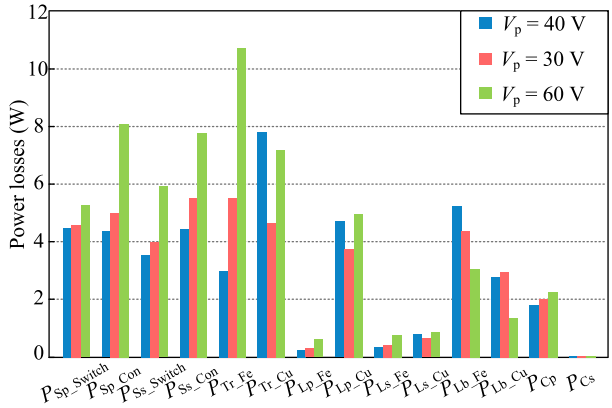


Fig. 25. Power loss breakdown of the proposed CF-IBDC at half load with the PWM plus HPS control.

secondary-side phase-shift inductor current of the proposed CF-IBDC is shared by two half bridges such that the conduction losses on the secondary side is reduced by half. Hence, the efficiency of the proposed CF-IBDC is higher than that of the boost half-bridge CF-IBDC at heavy load.

The calculated and measured total square RMS currents for different input voltages are shown in Fig. 23(a). With the same output power, the square RMS current is the minimum when $V_p = 40$ V. Taking $V_p = 30$ V as an example, the calculated and measured total square RMS currents for different control strategies are presented in Fig. 23(b). The experimental results coincide with the theoretical calculations and only small error remains. In comparison with only HPS control, the PWM plus HPS modulation can match the bus voltage with the output voltage, and thus the RMS current and the conduction losses are reduced. Therefore, the efficiency is improved by 5%–10% with the PWM plus HPS control, as shown in Fig. 24.

Fig. 25 presents the calculated half-load power loss breakdown that includes the switches losses, transformer losses, inductor losses, and capacitor losses for three input voltage cases. The switches losses are calculated by an estimation of the switching time and information about the current and voltage around the switching event [23]. The transformer and inductor losses consist of copper losses and core losses. The copper losses are related to the ac and dc resistances of the conductors [24], [25]. The core loss per unit volume of cores can be obtained from the typical core loss curve recommended in the datasheet. And the power losses in capacitors are generally caused by two phenomena: dielectric losses and thermal losses [26].

As can be seen, the losses of MOSFETs and the transformer account for the largest proportion of total power losses. And on account of the large current on the primary side, the losses on the primary-side phase-shift inductor are bigger than that on the secondary-side phase-shift inductors. The input inductor L_b is realized with EE55 ferrite core wound 12 turns by copper foil. The loss of the input inductor L_b can be reduced by 6.6 W if the inductance increases to 50uH, and an efficiency improvement of 1.32% can be achieved. In addition, employing advanced power switches with lower on-state resistances can significantly improve the efficiency performance.

VI. Conclusion

A novel CF-IBDC with a wide input range has been proposed in this paper. The primary side of the proposed converter is a bidirectional buck/boost half bridge that owns the advantages of small input current ripples, wide input voltage range, and LV stress on primary-side switches. In addition, the voltage spikes of primary-side switches in the proposed converter are eliminated without any clamping circuits, and thus the topological structure is simplified.

The primary-referred Δ-type equivalent circuit is used to simplify the analysis procedure. The operating principles and

characteristics including the soft-switching, power transfer, and RMS current are detailed with the PWM plus DPS modulation. In the proposed converter, all switches can realize practical ZVS turn ON over the full operating range. The ZVS for primary-side switches is affected by the inductance ratio *m* and the secondary-side switches can realize practical ZVS by adjusting the phase-shift angle ϕ_s. Furthermore, the guide lines for the design of input inductor and three phase-shift inductors are also explained.

A PWM plus HPS modulation is proposed in this paper to enable the proposed converter to operate efficiently within wide input voltage range. The power is mainly determined by the phase-shift angle $\phi_{\rm ps}$. A nonzero phase-shift angle ϕ_s is needed for the practical ZVS of secondary-side switches at light loads and ϕ_s is kept as zero at heavy load to ensure the maximum power. In addition, the bus voltage and the output voltage can be matched by the PWM control, which can reduce the RMS current and the current stress of all switches effectively and improve efficiency.

All theoretical analyses are verified with experimental results from a 1-kW converter prototype with 30–60 V input and 400 V output.

REFERENCES

[1] J. Kim, I. Jeong, and K. Nam, "Asymmetric duty control of the dual-active-bridge DC/DC converter for single-phase distributed generators," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 75–82.

[2] J. I. Metri, C. T. Saadeh, and H. Y. Kanaan, "Design, control and simulation of a fuel-cell-fed power conversion system for electric vehicles," in *Proc. Int. Conf. Renewable Energies Developing Countries*, Nov. 2014, pp. 199–204.

[3] X. W. Pan and A. K. Rathore, "Novel bidirectional snubberless soft-switching naturally clamped zero current commutated current-fed dual active bridge (CFDAB) converter for fuel cell vehicles," in *Proc. Energy Convers. Congr. Expo.*, Sep. 2013, pp. 1894–1901.

[4] U. R. Prasanna, X. W. Pan, A. K. Rathore, and K. Rajashekara, "Propulsion system architecture and power conditioning topologies for fuel cell vehicles," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 640–650, Jan./Feb. 2015.

[5] X. Yu, M. R. Starke, L. M. Tolbert, and B. Ozpineci, "Fuel cell power conditioning for electric power applications: A summary," *Electr. Power Appl. IET*, vol. 1, no. 5, pp. 643–656, 2007.

[6] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.

[7] J. Kan, S. J. Xie, Y. Tang, and Y. Y. Wu, "Voltage-fed dual active bridge bidirectional DC/DC converter with an immittance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3582–3590, Jul. 2014.

[8] S. Chakraborty and S. Chattopadhyay, "Analysis and comparison of voltage-source and current-source asymmetric dual-active half-bridge converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 2072–2079.

[9] Y. X. Shi, R. Li, Y. S. Xue, and H. Li, "Optimized operation of current-fed dual active bridge DC–DC converter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, Nov. 2015.

[10] X. H. Liu, Z. Wang, and H. Li, "A new fuel cell power conditioning system with extended life time and minimized DC-bus capacitor," in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 1926–1930.

[11] D. K. Jeong, M. H. Ryu, H. G. Kim, and H. J. Kim, "An optimized design of bi-directional dual active bridge converter for low voltage battery charger," in *Proc. 16th Int. Power Electron. Motion Control Conf. Expo.*, Sep. 2014, pp. 177–183.

[12] Y. S. Noh, S. C. Choi, E. J. Ha, B. J. Kim, and C. Y. Won, "Current-fed two-inductor bi-directional DC/DC converter with wide output voltage range," in *Proc. Int. Conf. Elect. Mach. Syst.*, Oct. 2015, pp. 2099–2103.

[13] H. Xiao and S. Xie, "A ZVS bidirectional DC–DC converter with phase-shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 812–823, Mar. 2008.

[14] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC–DC converter for bidirectional high power applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006.

[15] K. Wang, F. C. Lee, and J. Lai, "Operation principles of bi-directional full-bridge DC/DC converter with unified soft-switching scheme and soft-starting capability," in *Proc. IEEE 15th Annu. Appl. Power Electron. Conf. Expo.*, 2000, pp. 111–118.

[16] T. F. Wu, Y. C. Chen, J. G. Yang, and C. L. Kuo, "Isolated bidirectional full-bridge DC–DC converter with a flyback snubber," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1915–1922, Jul. 2010.

[17] T. F. Wu, J. G. Yang, C. L. Kuo, and Y. C. Wu, "Soft-switching bidirectional isolated full-bridge converter with active and passive snubbers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1368–1376, Mar. 2014.

[18] F. Z. Peng, H. Li, G. J. Su, and J. S. Lawler, "A new ZVS bidirectional DC–DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[19] J. Fedison, M. Fornage, M. Harrison, and D. Zimmanck, "Coss related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. IEEE 29th Annu. Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 150–156.

[20] H. Chung, S. Y. R. Hui, and K. K. Tse, "Reduction of power converter EMI emission using soft-switching technique," *IEEE Trans. Electromagn. Compat.*, vol. 40, no. 3, pp. 282–287, Aug. 1998.

[21] A. Ganz, "A simple, exact equivalent circuit for the three-winding transformer," *IRE Trans. Component Parts*, vol. 9, no. 4, pp. 212–213, Dec. 1962.

[22] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.

[23] L. E. A. Lirio, M. D. Bellar, J. A. M Neto, M. S. dos Reis, and M. Aredes, "Switching losses analysis in sic power mosfet," in *Proc. IEEE 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf.*, Nov. 2015, pp. 1–6.

[24] P. L. Dowell, "Effects of eddy currents in transformer windings," *Proc. Institution Elect. Eng.*, vol. 113, no. 8, pp. 1387–1394, Aug. 1966.

[25] K. V. Iyer, W. P. Robbins, and N. Mohan, "Design and comparison of high frequency transformers using foil and round windings," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 3037–3043.

[26] T. B. Soeiro, J. Muhlethaler, J. Linner, P. Ranstad, and J. W. Kolar, "Automated design of a high-power high-frequency LCC resonant converter for electrostatic precipitators," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4805–4819, Nov. 2013.

Xiaofeng Sun (M'11) received the B.S. degree in electrical engineering from the Northeast Heavy Machinery Institute, Heilongjiang, China, in 1993, and the M.S. and Ph.D. degrees in power electronics from Yanshan University, Hebei, China, in 1999 and 2005, respectively.

From 2003 to 2007, he was an Associate Professor with Yanshan University, Qinhuangdao, China, where he has been a Professor and also the Director of the Key Laboratory of Power Electronics for Energy Conservation and Motor Drive of Hebei Province, Yanshan University, since 2008. He has authored or coauthored more than 70 transactions and conference papers. His current research interests include dc–dc converters, multiple-input converters, hybrid electric vehicles, microgrids, and power quality control.

Xiaoying Wu received the B.S. degree in electrical engineering from Yanshan University, Qinhuangdao, China, in 2014, where she is currently working toward the M.S. degree in power electronics.

Her current research interests include the topology and control of dc–dc converters.

Yanfeng Shen (S'16) received the B.S. and M.S. degrees in electrical engineering and power electronics from Yanshan University, Qinhuangdao, China, in 2012 and 2015, respectively. He is currently working toward the Ph.D. degree in power electronics at Aalborg University, Aalborg, Denmark.

From August 2015 to October 2015, he was an Intern with the ABB Corporate Research Center, Beijing, China. His research interests include dc–dc converters, inverters, and multiobjective life-cycle optimization of power electronics converters.

Xin Li received the B.Eng. degree in computer software and applications from Northeast Heavy Machinery College, Heilongjiang, China, in 1992. She received the M.Eng. degree in measurement technique and automation equipment and the Ph.D. degree in measurement technology and instruments from Yanshan University, Hebei, China, in 2002 and 2008 respectively.

Her current research interests include power electronics, intelligent information processing, bioinformatics and biomedical instruments.

Zhigang Lu received the B.Eng. degree in automatic control and M.Eng. degree in systems engineering from Xi'an Jiaotong University, Xian, China, in 1985 and 1988, respectively. He received the Ph.D. degree in electric power systems and automation from the North China Electric Power University of Beijing, China, in 1998.

He is the Dean of the Faculty of Electrical Engineering, Yanshan University, Qinhuangdao, China. His current research interests include economic operation and control of power system, power grid state estimation, power system planning, nature-inspired optimization algorithms and their applications on various optimization problems.