Variable-Switching-Frequency State-Feedback Control of a Phase-Shifted Full-Bridge DC/DC Converter

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***Abstract*—This paper presents a methodology to control a phase-shifted full-bridge (PSFB) dc/dc converter with variable switching frequency, as a function of the output load power. The main objective of such control is to maximize the conversion efficiency at a wide range of load power levels. By tuning the switching frequency, the net phase of the input impedance of the converter can be manipulated, and thus, at the lower load power operation, the net input impedance can be made highly inductive to achieve zero-voltage switching (ZVS) at the primary-side switches. This paper proposes an efficiency maximization method, which derives an optimum switching frequency based on the load power from a loss-minimization model. In addition, a state-feedback-based control method is proposed for maintaining a tight dynamic regulation over the converter output under a load transient. A 6-kW laboratory prototype of the PSFB converter is developed and designed to validate the proposed control algorithm. The experimental results show a conversion efficiency of 98% at full load and output voltage ripple of $\pm 1\%$, while ensuring ZVS at all operating points between 100 W and 6 kW.**

***Index Terms*—Phase shift, state-feedback control, variable frequency, zero-voltage switching (ZVS).**

I. Introduction

AMONG the traditional dc/dc converter topologies, phase-shifted full bridge (PSFB) converters have drawn significant attention in medium–high-power applications due to their simple structure and zero-voltage switching (ZVS) feature [1]–[3]. Unlike the resonant dc/dc topologies, the voltage gain of a PSFB converter does not depend on the switching frequency, rather only varies with the phase-shift angle between the duty cycles of any two diagonally located primary-side switches. One of the most important considerations to achieve a high-end conversion efficiency is to ensure ZVS at a wide range of load power. One of the biggest challenges designing a PSFB converter is maintaining ZVS at light-load conditions, since it highly depends on the value of inductance and the switching frequency at low power. Increasing resonant inductance can help achieving ZVS in light-load condition. However, increasing resonant inductance results in the duty cycle loss at the secondary side, additional dead-time conduction loss and ringing across the secondary-side rectifier [4], [5].

In order to enhance the conversion efficiency without increasing the resonant inductance, several different methods have been proposed in the literature [5]–[14]. All of these methods require an add-on auxiliary circuit to ensure ZVS in a wide load range. An additional auxiliary transformer in series between the resonant inductor and the PSFB transformer, and a capacitor connected on its secondary side is proposed in [5]. In this way, enough magnetizing energy can be supplied to the resonant inductor even at lighter load conditions. However, this additional energy will result in circulating current and conduction loss in the primary side, which may not improve the overall efficiency, even with ZVS. The circuit topology proposed in [6] utilizes an additional subcircuit consisting of two inductors and two snubber capacitors, which result in circulating current due to resonance on the primary side. For a large output current application, this circulating current might be very high, which would introduce more conduction loss and potentially degrade the overall efficiency. In order to avoid these concerns, a voltage-doubler-type rectifier is proposed in [7], which has lower circulating current and can achieve ZVS in both legs. However, it uses a very high value of leakage inductor, increasing the overall weight, and also experiences high current stresses on the secondary switches due to a larger deadtime.

Furthermore, a few methods [15], [16] are proposed in order to improve the light-load efficiency without using any auxiliary circuit components. The method presented in [15] discusses synchronous rectification (SR) turn-off schemes to create discontinuous conduction mode of operation. The method proposed in [16] minimizes the secondary-side conduction loss but does not address any approach for the overall loss minimization. Also, most of these methods need complex control and higher conduction losses in body diode of synchronous rectifiers.

A number of studies [17]–[25] have been done in improving the light-load efficiency by achieving ZVS through modifying the circuit topology [17], [18], [20] or improving the control technique [26]. Although the methods in [17], [18], and [20] enhance the overall conversion efficiency at light loads (<1 kW), the efficiency starts to fall down beyond a certain load range because of higher conduction loss in the auxiliary circuit components. This is especially true for the large output current

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applications. The method in [20] improves the efficiency by changing the dead-time over different loads but overlooks the effect of switching frequency on the overall efficiency, which does not ensure maximum efficiency. In addition, a variable-switching-frequency control of a PSFB dc/dc converter is proposed in order to enhance the conversion efficiency over a wide load range [25], [26]. Although the proposed method in [26] shows improved efficiency in comparison to the fixed-frequency control, the switching frequency calculation algorithm does not minimize the total power loss, and consequently, it does not ensure maximum efficiency at all operating load powers.

In order to address and alleviate all the aforementioned issues related to the ZVS and efficiency improvement, a variable-switching-frequency control algorithm for a PSFB dc/dc converter is proposed in this paper. The proposed algorithm calculates the switching frequency, based on a power loss minimization model. The total power loss is estimated considering switching frequency, device parameters, and component details, where the only variable parameter is the switching frequency. Thereby, a parametric minimization of the total power loss is performed, and it is found that the switching frequency at which the total power loss will be minimum does not depend on the component details, which may change over different physical conditions. Rather, it depends only on the load power level. In addition, the proposed algorithm ensures validity of ZVS condition in the determined switching frequency. Otherwise, the model derives another switching frequency at which the ZVS occurs at both the legs and ensures minimum power loss.

Furthermore, a state-feedback-based control design approach is implemented to achieve a tight dynamic regulation on the PSFB converter output at any variable load and input voltage conditions. For regulating the output voltage at a reference level during a load transient, two sensors, i.e., output voltage and load current sensors, are typically required to provide the required feedback information. One noteworthy point is that the weight of the current transformer for sensing the load current is quite high and takes a significant portion of the total weight of the converter, in the low-voltage high-current (>100 A) secondary side. As an improvement, the proposed state-feedback-based control strategy uses only one output voltage sensor and estimates the load current from the converter dynamics and switching information at the previous cycle. The detailed derivation regarding the estimation of the load resistance, and hence, the load current is carried out in this paper.

This paper is organized as follows. Section II introduces detailed operation principle of the PSFB converter. The proposed state-feedback-based control approach assuming first harmonic approximation (FHA) of the converter is described in Section III. The proposed variable-switching-frequency control approach along with the loss modeling and ZVS conditions is established in Section IV. The simulation and experimental results of the converter at different load conditions are presented in Section V. Section VI puts forward conclusions with a relevant discussion.

II. Topology Operation

A simplified circuit of the PSFB topology in a center-tapped configuration is shown in Fig. 1. MOSFETs S_1, S_2, S_3, and

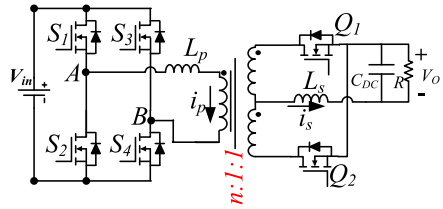

Fig. 1. Basic structure of a center-tapped PSFB dc/dc converter.

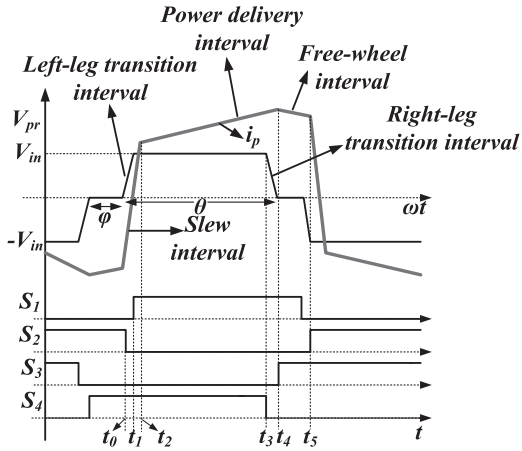

Fig. 2. Typical waveforms of primary voltage, primary current, and the gate pulses in a PSFB converter.

S_4 form the full bridge on the primary side of the transformer, T_1. S_1 and S_2 are switched with 50% duty ratio and 180° out of phase from each other. Similarly, S_3 and S_4 are switched at 50% duty and 180° out of phase with each other.

The pulse width modulation switching signals for leg S_3-S_4 of the full bridge are phase shifted with respect to those for leg S_1-S_2. Amount of this phase shift decides the amount of overlap between diagonal switches, which in turn decides the amount of energy transferred. Q_1 and Q_2 provide rectification on the secondary side, while L_s and $C_{\rm DC}$ form the output filter. Inductor L_p provides assistance to the transformer leakage inductance for resonance operation with MOSFET capacitance and facilitates ZVS. Fig. 2 provides the switching waveforms for the system in Fig. 1.

During ZVS phase-shift operation of the converter, there are five states in a half-cycle of operation. These states are briefly discussed due to the symmetric operation of the circuit.

A. Slew Interval (t_0–t_2)

This is the time interval when the primary current changes its flow direction. This time is established by primary input voltage level, load current, and the total primary-side resonant inductance, including the leakage inductance of the transformer and any additional inductance in the primary current path. Additional inductance may be required to store enough energy to displace the capacitive charge on the MOSFET output capacitance ($C_{\rm OSS}$) and to offer realistic transition delay times.

B. Power Delivery Interval (t_2–t_4)

This mode of operation is very similar to the conventional full-bridge converter operation, when either of the two diagonally

opposite switches (S_1 & S_4 or S_2 & S_3) are ON. Therefore, the applied voltage across the primary side of the transformer (including the additional leakage inductance) becomes $V_{\rm in}$ or $-V_{\rm in}$, which results in power transfer to the load. The phase shift between diagonal switches determines the output voltage and total power transfer to the load side.

C. Freewheeling Interval (t_4–t_5)

During the freewheel time, reflected load current is circulated through the FET switches S_1 & S_3 or S_2 & S_4, and the voltage across the primary is zero. The freewheeling time increases with light loads for less power transfer and decreases with heavy loads for higher power transfer. In other words, the freewheeling time is a way for the controller to idle until the next appropriate state comes along. Fig. 2 shows the droop in primary current during this time, caused by conduction losses in the circulation path and output inductor ripple current.

D. Left-Leg Transition Interval (t_0–t_1)

The process of ZVS involves the charge displacement in the drain–source parasitic capacitances of the MOSFETs and occurs differently for the two legs of the primary side. During the left-leg (S_1 & S_2) transition interval, the charge on the output capacitances of the A&B leg is displaced. For the left leg, the source of energy that displaces this charge is stored in the total primary resonant inductance. The displacement of this charge forces the voltage across MOSFET S_1 to zero (MOSFET S_2 ZVS occurs during the cycles second half), enabling ZVS to take place. The charge is displaced in a time equal to one-fourth the resonant period, given by

$$t_{\rm LL} = \frac{\pi}{2} \times \sqrt{L'_p C_R} \tag{1}$$

where $t_{\rm LL}$ = transition time for the left-leg interval; L'_p = transformer leakage inductance + additional primary inductance, and C_R = resonant capacitance, which is given by $C_R = 4xC_{\rm OSS}/3$, where The MOSFET output capacitance $C_{\rm OSS}$ is multiplied by 4/3 to approximate the average capacitance value during a varying drain-to-source voltage.

E. Right-Leg Transition Interval (t_3–t_4)

During this time interval, the full displacement of charge on the output capacitors of S_3 and S_4 happens and, thus, terminates the power transfer interval. The reflected portion of the secondary current on the primary side supplies the energy for the full charge displacement, which ensures ZVS. Unlike the left-leg ZVS, the dynamics of capacitor discharge in this mode does not follow any resonating behavior, as the reflected output current behaves like a constant current source and discharges the output capacitances of primary MOSFETs linearly. The ZVS transition time is given by the following relationship:

$$t_{\rm RL} = \frac{C_R V_{\rm in}}{I_p}. \tag{2}$$

Since the source of energy for the discharging of output capacitors is directly load dependent, it is challenging to achieve ZVS at lighter loads. However, this does not pose a serious problem, as a variable-switching-frequency-based control method can potentially ensure the ZVS occurrence even at lighter loads without adding any hardware components, as proved in the next section of this paper.

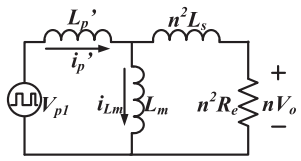

Fig. 3. Reduced equivalent circuit from FHA of a PSFB converter.

III. Phase-Shift Controller Design

In order to control a PSFB converter at any switching frequency, it is important to design a control system, which will generate the reference value of the phase shift for achieving the reference output voltage at a particular load power. Therefore, the first requirement is to determine the frequency-domain small-signal transfer function $\Delta V_o/\Delta\varphi$, which can be split as follows:

$$\frac{\Delta V_o}{\Delta\phi} = \frac{\Delta V_o}{\Delta V_{p1}} \times \frac{\Delta V_{p1}}{\Delta\phi} \tag{3}$$

where φ represents the phase-angle shift between two diagonally opposite switches, V_{p1} denotes the fundamental components of the primary voltage, and V_o is the output voltage. In order to determine the ac voltage gain of the converter, i.e., $\Delta V_o/\Delta V_{p1}$, the reduced circuit of PSFB from the FHA, shown in Fig. 3, is analyzed.

Here, L_m is the magnetizing inductance of the transformer and R_e is the equivalent reflected ac resistance on the primary side, obtained from FHA [17], i.e., $R_e = 8R/\pi^2$, where *R* is the original load resistance. Thereby, the overall voltage gain can be calculated as the following relationship, which shows a first-order variation between the fundamentals of output voltage and primary-side voltage

$$\frac{V_o}{V_{p1}} = \frac{nR_eL_m}{(L_m + L'_p)[s(n^2L_s + L_m||L'_p) + n^2R_e]}. \tag{4}$$

$\Delta V_{p1}/\Delta\varphi$, i.e., the primary voltage variation with the phase-shift angle, can be quantified by taking the ratio of the change in first harmonic amplitude of the primary voltage and the perturbation amount of the phase angle. For any phase-shift angle φ, "*m*th" harmonic amplitude of the primary voltage, i.e., a_m, can be determined as follows:

$$\begin{aligned} a_m &= \frac{1}{\pi}\int_{<2\pi>} V_{\rm pri}(t)\sin(nt)dt \\ &= \frac{V_{\rm in}}{\pi}\left[\int_0^{\pi-\phi}\sin(mt)dt - \int_{\pi}^{2\pi-\phi}\sin(mt)dt\right] \\ &= \frac{V_{\rm in}}{m\pi}[1+\cos(m\phi)]\times[1-(-1)^m]. \end{aligned} \tag{5}$$

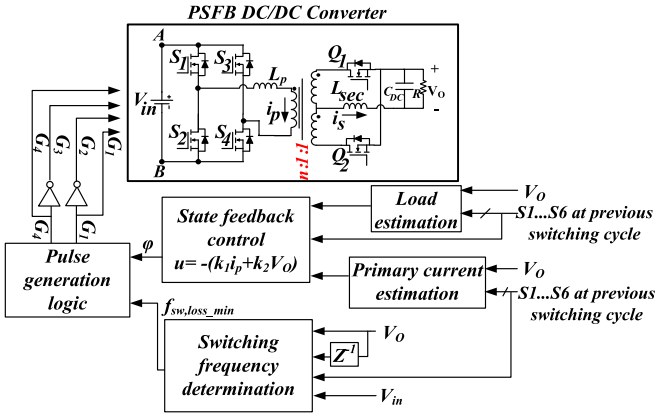

Fig. 4. Variable-switching-frequency state-feedback controller of a PSFB converter.

Accordingly, the first-harmonic amplitude of the primary input voltage is formulated by the following relationships:

$$|V_{p1}| = \frac{2V_{\text{in}}}{\pi}(1+\cos(\phi)). \tag{6}$$

Hence

$$\frac{\Delta V_{p1}}{\Delta\phi} = -\frac{2V_{\text{in}}}{\pi}\sin(\phi). \tag{7}$$

Therefore, the small-signal transfer function between the output voltage and phase-shift angle can be determined by multiplying (4) and (7), shown in (8), which is a first-order system with a pole located at $p = n^2R_e \Big/ (n^2L_s + L_m||L'_p)$

$$\frac{\Delta V_o}{\Delta\phi} = -\frac{2V_{\text{in}}}{\pi}\sin(\phi)\frac{nR_eL_m}{(L_m+L'_p)[s(n^2L_s+L_m||L'_p)+n^2R_e]}. \tag{8}$$

Hence, this relationship could be framed as a typical first-order system, as follows.

$$\frac{\Delta V_o}{\Delta\phi} = \frac{A}{1+s\tau} \tag{9}$$

where

$$A = -\frac{2V_{\text{in}}}{\pi}\sin(\phi)\frac{L_m}{n(L_m+L'_p)} \tag{10}$$

$$\tau = \frac{n^2L_s + L_m||L'_p}{n^2R_e}. \tag{11}$$

A state-feedback control algorithm is proposed for maintaining the output voltage at a fixed regulated value with a fast closed-loop system dynamics, at any transient in load power or input voltage. The control system block diagram is shown in Fig. 4, where G_{i} corresponds to the gate pulse to the switch S_i ("i" = 1 to 4). The selected state variables ($\boldsymbol{x}$) of the converter are the primary current (i_p) and the instantaneous output voltage (v_o). The control variable (u) is the phase-shift between any two diagonal switches, i.e., φ. One state-space relation in (12) can be established by using the output voltage to phase-shift transfer function in (9)

$$v_o + \tau\dot{v}_o = A\phi \tag{12}$$

$$\dot{v}_o = -\tfrac{v_o}{\tau} + \tfrac{A}{\tau}\phi. \tag{13}$$

Furthermore, from the voltage balancing at primary side, i.e., (14) and applying $v_p = V_o\varphi$, the second state-space relationship, shown in (15), can be formulated assuming $L_{\text{eq}} = n^2L_s + L_p$

$$v_p = L_p\dot{i}_p + nL_s\dot{i}_s + nv_o \tag{14}$$

$$\dot{i}_p = \frac{-n}{L_{\text{eq}}}v_o + \frac{V_{\text{in}}}{L_{\text{eq}}}\phi. \tag{15}$$

Thereby, combining (13) and (15) and comparing with the state-space equation for LTI systems, i.e., $\boldsymbol{x}' = \boldsymbol{Ax} + \boldsymbol{Bu}$, the matrices A and B are determined as follows:

$$A = \begin{pmatrix} 0 & -n\Big/L_{\text{eq}} \\ 0 & -1\Big/\tau \end{pmatrix} \tag{16}$$

$$B = \begin{pmatrix} A\Big/\tau \\ V_{\text{in}}\Big/L_{\text{eq}} \end{pmatrix}. \tag{17}$$

Substituting $\boldsymbol{u} = -kx$ (where $\boldsymbol{k} = (k_1\ k_2)^T$ is a gain matrix), in the state-space equation and taking its Laplace transformation, it is found that eigenvalues of the matrix $(\boldsymbol{sI - A + Bk})$ have to lie on the left-half plane in order to ensure stability of the system. Since the eigenvalues of $(\boldsymbol{sI - A + Bk})$ are same as the solutions of det $(\boldsymbol{sI - A + Bk}) = 0$, the Routh–Hurwitz criterion could be applied to find the conditions for obtaining negative eigenvalues [29]

$$(sI - A + Bk) = \begin{pmatrix} s + \frac{Ak_1}{\tau} & \frac{n}{L_{\text{eq}}} + \frac{Ak_2}{\tau} \\ \frac{V_{\text{in}}k_1}{L_{\text{eq}}} & s + \frac{1}{\tau} + \frac{V_{\text{in}}k_2}{L_{\text{eq}}} \end{pmatrix} \tag{18}$$

$$\det(sI - A + Bk) = s^2 + s\left(\frac{1+Ak_1}{\tau} + \frac{V_{\text{in}}k_2}{L_{\text{eq}}}\right) + \left(\frac{Ak_1}{\tau^2} - \frac{V_{\text{in}}k_1n}{L_{\text{eq}}^2}\right). \tag{19}$$

After applying the Routh–Hurwitz criterion on $\det(\boldsymbol{sI - A + Bk}) = \boldsymbol{0}$, the following constraints on the gain matrix parameters are obtained; $k_1 > 0$; $k_2 < (L_{\text{eq}}(1+Ak_1)/\tau V_{\text{in}})$. Moreover, since A and τ depend on the system variables V_{in} and R, the inequalities on k_1 and k_2 should take care of any variations in the load power and input voltage. In this case, R can be estimated from the detailed modeling of the converter dynamics and switching pulse information, as explained and derived in Section IV. A and τ would be calculated at each interrupt cycle from the measured state variables and phase-shift amount at the previous switching cycle, and accordingly, k_1 and k_2 could be updated.

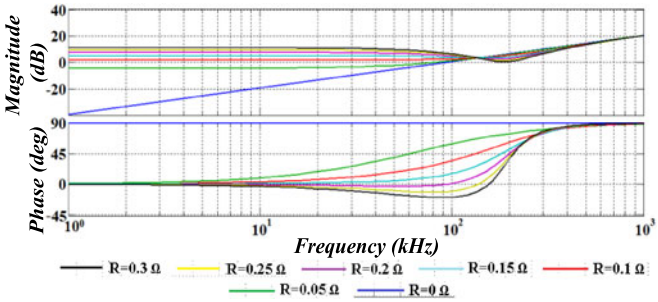

Fig. 5. Bode plot of the input impedance of a PSFB converter.

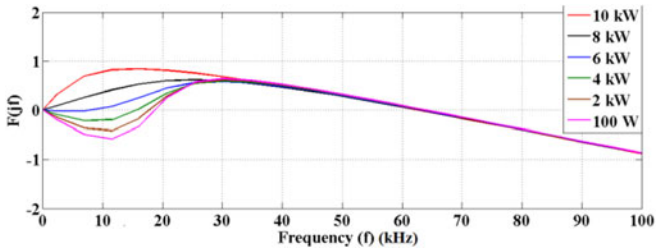

Fig. 6. Variation of cut-in frequency of ZVS occurrence in a PSFB converter.

IV. Variable-Switching-Frequency Control

For achieving ZVS at the lower load power, a higher value of inductance is required in order to sink the enough energy from the parasitic drain–source capacitances to discharge them fully. Besides increasing the inductance value for ensuring ZVS, alternatively the switching frequency can be tuned to ensure ZVS at all switches. The main objective of tuning switching frequency at different load powers is to manipulate the phase lag of the net input impedance and ensure that it is inductive in nature. Therefore, it is necessary to investigate the equivalent input impedance of the PSFB converter. Let V_1 be the instantaneous primary-side voltage, created due to linked flux, and V_p is the instantaneous voltage across the primary side of the transformer including the leakage inductance. Therefore, the following relationships can be established from the analyses on the primary and secondary sides of the transformer

$$V_p = L_p{}' \frac{di_p}{dt} + V_1 \tag{20}$$

$$\frac{V_1}{n} = L_s \frac{di_s}{dt} + V_o \tag{21}$$

$$i_s = C\frac{dV_o}{dt} + \frac{V_o}{R}. \tag{22}$$

Taking the Laplace transformation on (20)–(22) and using $i_s(s) = ni_p(s)$, the following relationship is obtained:

$$Z_{\text{in}}(s) = \frac{s^2 RCL_{\text{eq}} + sL_{\text{eq}} + nR}{sCR + 1} \tag{23}$$

where $L_{\text{eq}} = L_p' + n^2 L_s$. Therefore, the net phase lag of the input impedance can be formulated as

$$\begin{aligned}\phi_{\text{lag}} &= \tan^{-1}\left(\frac{\omega L_{\text{eq}}}{nR - \omega^2 RCL_{\text{eq}}}\right) - \tan^{-1}(\omega CR) \\ &= \tan^{-1}\left[\frac{\omega(L_{\text{eq}} - nR^2C + \omega^2 R^2C^2L_{\text{eq}})}{nR}\right].\end{aligned} \tag{24}$$

The frequency response of $Z_{\text{in}}(s)$ is shown by a Bode plot in Fig. 5, which represents that both the impedance magnitude and phase lag increase as the frequency increases. In terms of fulfillment of ZVS, minimum time lag (t_{L}) between the fundamental primary current and primary voltage must be one-fourth of a resonant cycle, i.e., $\pi\sqrt{(L'_pC_R)}/2$, where $C_R = 4xC_{\text{OSS}}/3$ and C_{OSS} is the output capacitance of each primary-side MOSFET. Hence, the condition of the inductive phase lag of the input impedance being more than ωt_{L}, i.e., (25) and (26), must be valid in order to ensure the ZVS operation

$$\tan^{-1}\left[\frac{\omega(L_{\text{eq}} - nR^2C + \omega^2 R^2C^2L_{\text{eq}})}{nR}\right] > \frac{\omega\pi}{2}\sqrt{L'_pC_R} \tag{25}$$

$$\begin{aligned}F(\omega) &= \frac{\omega\pi}{2}\sqrt{L'_pC_R} \\ &\quad -\tan^{-1}\left[\frac{\omega(L_{\text{eq}} - nR^2C + \omega^2 R^2C^2L_{\text{eq}})}{nR}\right] < 0.\end{aligned} \tag{26}$$

The cut-in frequency above which the ZVS is confirmed varies with output load power. The cut-in frequency (ω_{c}) can be determined from the equality condition of the inequality and is represented by the frequency axis intercept of *F(ω)* versus *f* (i.e., *ω/2π*) curve, shown in Fig. 6, for different load conditions.

As can be seen from Fig. 6, the frequency intercept for all the load powers ranging from 100 W to 10 kW is around 60 kHz. According to (26), *F(ω)* has to be negative as a compulsory ZVS condition. Therefore, the ZVS is confirmed at the frequencies above 60 kHz for all the load powers from 0.1 to 10 kW. In addition, as a broad objective of this work is to maximize the conversion efficiency at all operating points, it is required to perform loss modeling and minimize the total power loss by tuning the switching frequency. The main task is to determine the switching frequency, at which the total power loss would be minimum and to make the converter operate at that switching frequency if ZVS condition also satisfies simultaneously. The loss model assumes the primary-side turn-on loss to be zero assuming ZVS operation of all the switches. First priority in the process of selection of switching frequency would be to minimize the total loss and also to simultaneously ensure ZVS operation. If ZVS does not occur at the switching frequency with minimized loss, then a switching frequency satisfying (26) would be chosen. The reason is that as the frequency decreases, input impedance reduces according to (23), the current stress increases on both the primary and secondary sides, and the conduction loss increases and dominates the other losses in large output current applications. Therefore, a higher switching frequency, satisfying the ZVS condition in (26), should be selected for overall loss minimization. A flowchart depicting the switching frequency selection is shown in Fig. 7. Although the loss model is quite dependent on the design parameters of the system,

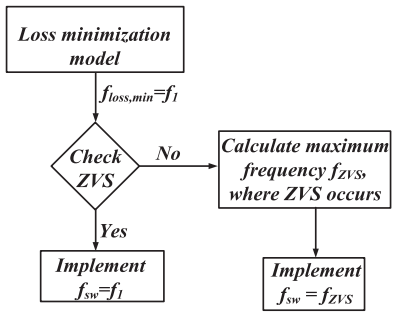

Fig. 7. Flowchart for the switching frequency selection procedure.

the calculated switching frequency for the minimized loss is proven to be independent of the device specifications and component details, and rather just a function of load power.

The total power loss, shown in (27) in the PSFB converter, could be split into four major categories, i.e., primary conduction loss ($P_{\mathrm{pri,cond}}$), secondary conduction loss ($P_{\mathrm{sec,cond}}$), transformer core loss (P_{core}), and primary-side turn-off loss (P_{off})

$$\begin{aligned} P_{\mathrm{tot}} =\ & P_{\mathrm{off}} + P_{\mathrm{pri,cond}} + P_{\mathrm{sec,cond}} + P_{\mathrm{core}} \\ =\ & \frac{V_{\mathrm{pri,rms}} I_{\mathrm{pri,rms}} t_{\mathrm{off}} f_{\mathrm{sw}}}{2} + I^2_{\mathrm{pri,rms}} R_{\mathrm{pri,cond}} \\ & + I^2_{\mathrm{sec,rms}} R_{\mathrm{pri,cond}} + k f^2_{\mathrm{sw}} \\ =\ & \frac{V^2_{\mathrm{pri,rms}} t_{\mathrm{off}} f_{\mathrm{sw}}}{2|Z_{\mathrm{in}}(s)|} + \frac{V^2_{\mathrm{pri,rms}} R_{\mathrm{pri,cond}}}{|Z^2_{\mathrm{in}}(s)|} \\ & + \frac{n^2 V^2_{\mathrm{pri,rms}} R_{\mathrm{pri,cond}}}{Z^2_{\mathrm{in}}(s)} + k f^2_{\mathrm{sw}}. \end{aligned} \tag{27}$$

Here, $V_{\mathrm{pri,rms}}$, $R_{\mathrm{pri,cond}}$, and $R_{\mathrm{sec,cond}}$ are the primary-side RMS voltage and conduction resistance of the primary and secondary MOSFETs. For a switching frequency of f_{sw}, the total power loss can be formulated as follows:

$$\begin{aligned} P_{\mathrm{tot}}(f_{\mathrm{sw}}) =\ & \frac{k_1 f_{\mathrm{sw}}}{Z_{\mathrm{in}}(f_{\mathrm{sw}})} + \frac{k_2}{Z^2_{\mathrm{in}}(f_{\mathrm{sw}})} + k_3 f^2_{\mathrm{sw}} \\ =\ & \frac{k_1 f_{\mathrm{sw}} Z_{\mathrm{in}}(f_{\mathrm{sw}}) + k_2 + k_3 f^2_{\mathrm{sw}} Z^2_{\mathrm{in}}(f_{\mathrm{sw}})}{Z^2_{\mathrm{in}}(f_{\mathrm{sw}})} \end{aligned} \tag{28}$$

where $k_1 = V^2_{\mathrm{pri,rms}} t_{\mathrm{off}}/2$; $k_2 = V^2_{\mathrm{pri,rms}} R_{\mathrm{pri,cond}}$, $k_3 = k$.

The optimum switching frequency at which the total power loss would be minimum can be determined by solving $dP_{\mathrm{tot}}(f_{\mathrm{sw}})/df_{\mathrm{sw}} = 0$. Substituting the $|Z_{\mathrm{in}}(s)|\, at\, f = f_{\mathrm{sw}}$ in the power loss expression and equating its derivative to zero, the following relationship is obtained:

$$\begin{aligned} & k_1 Z_{\mathrm{in}}(f_{\mathrm{sw}}) Z'_{\mathrm{in}}(f_{\mathrm{sw}}) - k_1 f_{\mathrm{sw}} Z_{\mathrm{in}}(f_{\mathrm{sw}}) Z'_{\mathrm{in}}(f_{\mathrm{sw}}) - \\ & 2k_2 Z'_{\mathrm{in}}(f_{\mathrm{sw}}) + k_3 Z^2_{\mathrm{in}}(f_{\mathrm{sw}}) Z'_{\mathrm{in}}(f_{\mathrm{sw}}) = 0. \end{aligned} \tag{29}$$

From the above equation, one straightforward solution could be obtained as $Z'_{\mathrm{in}}(f_{\mathrm{sw}}) = 0$, which leads to the following relationships by differentiating (23) with respect to $s = f_{\mathrm{sw}}$:

$$\frac{f^2_{\mathrm{sw}} R^2 C^2 L_{\mathrm{eq}} + 2RCL_{\mathrm{eq}} f_{\mathrm{sw}} + L_{\mathrm{eq}} - nR^2 C}{(RCf_{\mathrm{sw}} + 1)^2} = 0. \tag{30}$$

Hence

$$\begin{aligned} f_{\mathrm{sw}} =\ & \frac{\sqrt{4R^2C^2L^2_{\mathrm{eq}} + 4R^2C^2 L_{\mathrm{eq}}(nR^2C - L_{\mathrm{eq}})} - 2RCL_{\mathrm{eq}}}{2R^2C^2L_{\mathrm{eq}}} \\ =\ & \left(\sqrt{\frac{n}{CL_{\mathrm{eq}}}} - \frac{1}{RC}\right). \end{aligned} \tag{31}$$

As can be seen from (31), the commanded switching frequency from the loss-minimized model is independent of the design-dependent parameters, such as k_1, k_2, and k_3. Although there are other multiple solutions to (29), all of them are dependent on k_1, k_2, and k_3 and, thus, generate a switching frequency being dependent on the design specifications and component details. Those solutions may potentially generate misleading values of switching frequencies, upon the slight variation of component parameters with other physical parameters. Therefore, the solution from $Z'_{\mathrm{in}}(f_{\mathrm{sw}}) = 0$ is considered as the optimum switching frequency, which is only dependent on the output load power. From the established relationship in (31), it is understood that the switching frequency should be increased as the load resistance increases and vice versa. Therefore, a higher switching frequency is desired in order to reduce the total loss at a lighter load condition. Again, in order to maintain the ZVS, the switching frequency should maintain the condition mentioned in (26) (i.e., $f_{sw} > 60$ kHz for our design considerations).

Since there will be no load resistance sensing in the real-time implementation, *R* should be determined or estimated from the known measured system variables, in order to generate a frequency command according to (31). Differentiating (22) and substituting di_s/dt in (21), the relationship at (32) can be formulated and discretized at the *kth* sample in (33)

$$\frac{V_1}{n} = L_s\left(C\frac{d^2V_o}{dt^2} + \frac{1}{R}\frac{dV_o}{dt}\right) + V_o \tag{32}$$

$$\begin{aligned} & \frac{V_1(k) - V_1(k-1)}{n} \\ & = L_s\left(\frac{V_o(k) - 2\times V_o(k-1) + V_o(k-2)}{{T_s}^2}\right) \\ & \quad + \frac{L_s}{R} \times \frac{V_o(k) - V_o(k-1)}{T_s} + V_o(k) \end{aligned} \tag{33}$$

where T_{s} is the sampling time of the closed-loop implementation. From the sensor measurements, output voltages at *k*th and *(k-1)*th samples are known to us. Furthermore, $V_1(k)$ and $V_1(k-1)$ will be either V_{in} or $-V_{\mathrm{in}}$ or 0, which will be known to us from the input voltage and the primary switching pulse information. Thus, the unknown value of load resistance, i.e., *R*, could be estimated using the relationship, established in (33). Consequently, the primary current (i_{p}) at *k*th sample can also be estimated according to (34), using the fundamental relationships (20)–(22)

$$i_p(k) = \frac{i_s(k)}{n} = \frac{1}{n}\left(C\frac{V_o(k) - V_o(k-1)}{T_s} + \frac{V_o(k)}{R}\right). \tag{34}$$

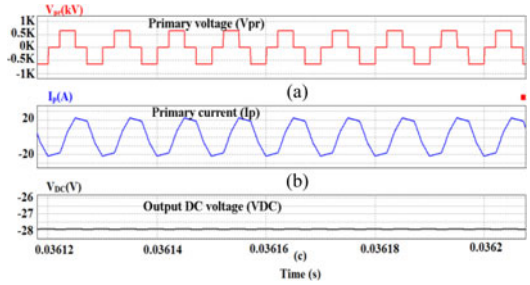

Fig. 8. Simulation results of PSFB converter. (a) Primary voltage ($V_{\rm pr}$). (b) Primary current ($i_{\rm pr}$). (c) Output dc voltage ($V_{\rm DC}$).

TABLE I
KEY DESIGN PARAMETERS AND THEIR SPECIFICATIONS

Parameters	Values	Quantity
Input voltage ($V_{\rm in}$)	650 V	-
Output voltage reference ($V_{o\_{\rm ref}}$)	28 V	-
Output power ($P_{\rm out}$)	6 kW	-
Transformer turns ratio (n)	12:1:1	-
Primary leakage inductance L'_p	8 μH	
Secondary inductor (L_s)	7.5 μH	1
DC-link capacitor ($C_{\rm DC}$)	3 mF	1
Primary MOSFETs	SiC (1.2 kV/24 A)	4
Secondary MOSFETs	FDH055N15A (145 A, 160 V)	6

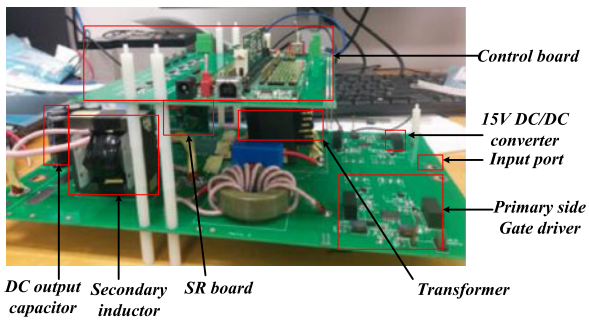

Fig. 9. Photo of the PSFB dc/dc experimental setup.

V. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the proposed control methodology, the converter is simulated with a dc voltage of 650 V at a rated nominal power of 6 kW with 28-V output dc voltage reference for the application of auxiliary power supply in a more electric aircraft. The simulation is performed in PSIM and the obtained results are shown in Fig. 8. The PSFB converter is designed based on the well-established design considerations, presented in the literature [27], [28]. The key design parameters and specifications are summarized in Table I. As a noteworthy design consideration, SR is used to drive the secondary-side MOSFETs to reduce the conduction loss and each secondary switch is realized by three MOSFETs in parallel for reducing the effective conduction resistance.

As a proof-of-concept verification to the proposed control methodology, a laboratory prototype of 6 kW (continuous)/8 kW (peak) PSFB converter, shown in Fig. 9, is designed and developed. The control algorithm is implemented in a floating-point DSP platform TMS320F28335.

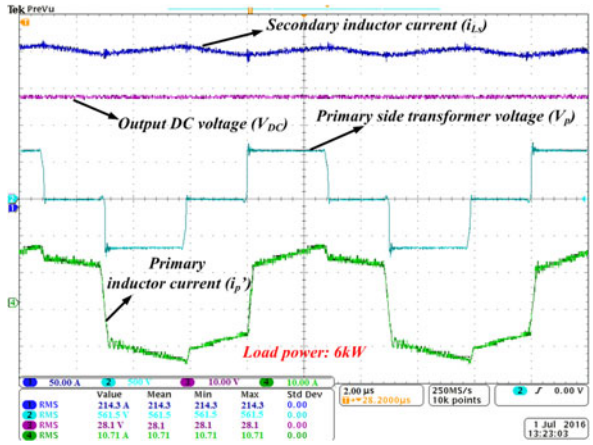

Fig. 10. PSFB waveforms at 6-kW load power; $V_{\rm in} = 650\,{\rm V}, V_{\rm O} = 28\,{\rm V}$, Output current: 214.3 A.

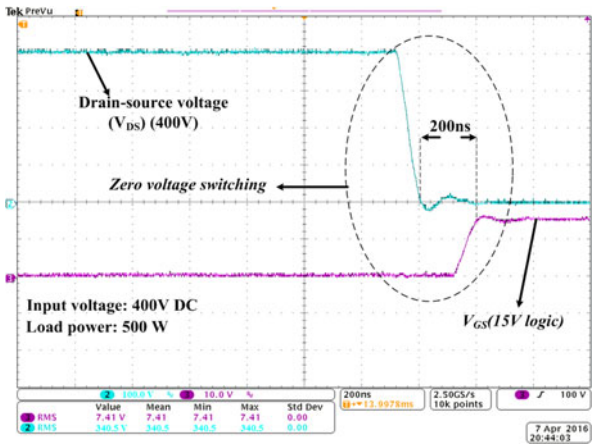

Fig. 11. ZVS in a PSFB converter at 500-W load power $V_{\rm in} = 400\,{\rm V}, V_{\rm O} = 20\,{\rm V}$, Output current: 25 A.

Fig. 10 shows the steady-state operation of the converter at 650-V DC input and 6 kW. The output dc voltage is settled at 28-V DC with a ripple within $\pm 1\%$. The secondary inductor current is averaged around 214 A with a ripple of $\pm 10\%$, and it is of twice the switching frequency, as the voltage across the inductor is rectified form of the linked secondary voltage. The ZVS occurrence of the primary-side MOSFETs is demonstrated by Fig. 11, which shows a 200-ns deadtime between complete fall of drain–source voltage and the turn-on of gate pulse.

Furthermore, the converter is also tested in different load and line conditions to check the accuracy of the proposed control logic at variable operating conditions. A 33% step increment in load from 6 to 8 kW is applied during a running condition with nominal load, and the output voltage is settled at its reference value within 5 μs with the state-feedback control approach, as shown in Fig. 12. It takes 12.5 μs to settle to the steady state under the same load transient with a PI controller, shown in Fig. 13. In addition, the undershoot in the output dc voltage under this load transient with the state-feedback and PI controller are 30% and 12% of the reference value, respectively, which prove the state-feedback control to be superior than PI in terms of dynamics and regulation of this converter. The output voltage ripple

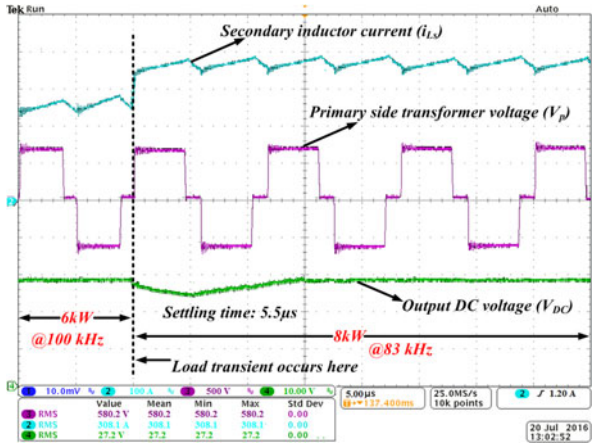

Fig. 12. PSFB waveforms at load transient from 6 to 8 kW in variable-switching-frequency state-feedback control: $V_{\rm in} = 650$ V, $V_{\rm O} = 28$ V, $f_{\rm sw} = 100$ kHz @6 kW and $f_{\rm sw} = 83$ kHz @8 kW.

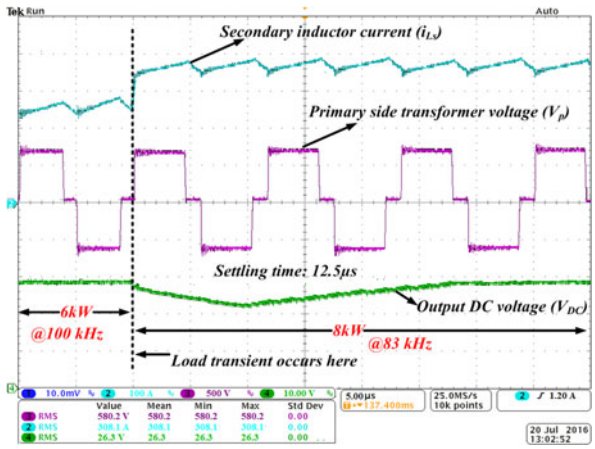

Fig. 13. PSFB waveforms at load transient from 6 to 8 kW in variable-switching-frequency PI control: $V_{\rm in} = 650$ V, $V_{\rm O} = 28$ V, $f_{\rm sw} = 100$ kHz @6 kW and $f_{\rm sw} = 83$ kHz @8 kW.

is maintained below $\pm 1\%$ at the steady state of the overload condition. It is also observed that there is a dynamic change in switching frequency from 100 to 83 kHz as soon as the load is changed from 6 to 8 kW. The fact that these frequencies match well with the optimum switching frequencies in Table II proves high accuracy of the proposed control.

The converter is tested at different operating points in a wide range of load power (from 100 W to 9 kW) and variable switching frequencies in the range of 50–220 kHz, listed in Table II, as reported by the switching frequency calculating model for maximum efficiency operation of the converter at different load conditions. The measured efficiencies at the whole load power range with the proposed control are more than the reported peak efficiency values in the previous related works, i.e., 95.6% in [26], 91% in [18], and 92.8% in [20]. This proves the justification of the effect of variable switching frequency to track the maximum attainable efficiency at a particular load. In order to validate the improved performance by the variable-switching-frequency control, a graph demonstrating a comparison of conversion efficiencies at different load powers between the proposed control and a fixed-frequency control method at 50 kHz is shown in Fig. 14, which clearly indicates an improved efficiency value at all the operating points.

TABLE II
OPTIMUM SWITCHING FREQUENCIES AT DIFFERENT LOAD POWERS AND EFFICIENCY COMPARISON WITH FIXED-FREQUENCY CONTROL AT 50 KHZ

Load power (kW)	$f_{\rm sw}$, $\rm loss_m$ in (kHz)	Efficiency at $f_{\rm sw}$, $\rm loss_m$ in	Efficiency at 50 kHz
0.1	180	95	93
1	170	97	96.2
2	158	98.1	97.1
3	145	98.2	96.9
4	130	98.15	96.8
5	114	98.1	96.8
6	100	98.1	96.65
7	92	98.1	96.6
8	83	98.05	96.6
9	75	98	96.5
10	65	97.9	96.5

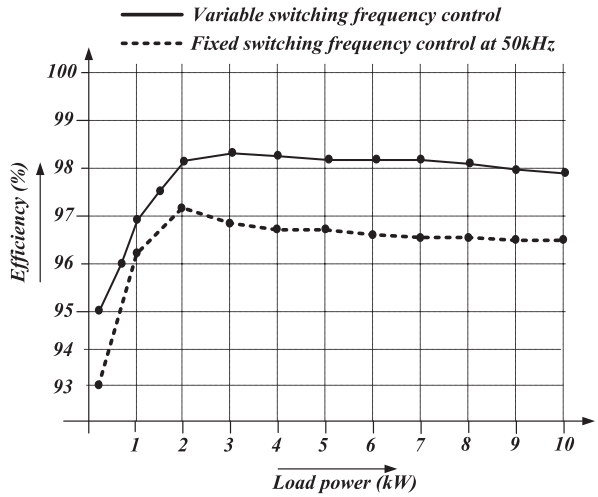

Fig. 14. Efficiency comparison between fixed- and variable-frequency control at different load power levels.

VI. CONCLUSION

In this paper, a new control methodology, incorporating variable-switching-frequency operation at different load power levels in a PSFB dc/dc converter, is proposed to maximize the conversion efficiency. In addition, a state-feedback-based control method is designed to regulate the PSFB converter at variable load and input voltage condition, with the elimination of a load current sensor. With implementation of this control, ZVS can be achieved at all power levels with just using transformer leakage inductance and removing any additional primary inductor.

As a proof-of-concept verification, a 6-kW laboratory prototype of a PSFB dc/dc converter is designed and tested with 650 V to 28 V conversion specification for the application of auxiliary power supply in a more electric aircraft. According to the experimental results, a maximum conversion efficiency of 98.1% with an output voltage ripple below $\pm 1\%$ is achieved, and the converter dynamics becomes 7 μs faster in 33% load

transient through a state-feedback control in comparison to a PI controller. Furthermore, the experimental results exhibit higher conversion efficiencies at a wide load power range (100 W–10 kW) with variable switching frequency in comparison with a fixed-switching-frequency method.

REFERENCES

[1] J. A. Sabaté, V. Vlatkovic, R. B. Ridley, and F. C. Lee, "High-voltage, high-power, ZVS, full-bridge PWM converter employing an active snubber," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1991, pp. 158–163.

[2] R. Redl, N. Sokal, and L. Balogh, "A novel soft-switching full-bridge dc–dc converter: Analysis, design considerations, at 1.5 kW, 100 kHz," *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 408–418, Jul. 1991.

[3] W. Chen, F. C. Lee, M. M. Jovanovic, and J. A. Sabate, "A comparative study of a class of full bridge zero-voltage-power deviced PWM converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1995, pp. 893–899.

[4] G. Koo, G. Moon, and M. Youn, "New zero-voltage-switching phase-shift full-bridge converter with low conduction losses," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 228–235, Feb. 2005.

[5] Y. Jang and M. M. Jovanovic, "A new PWM ZVS full-bridge converter," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 987–994, May 2007.

[6] P. K. Jain, W. Kang, H. Soin, and Y. Xi, "Analysis and design considerations of a load and line independent zero voltage switching full-bridge DC/DC converter topology," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 649–657, Sep. 2002.

[7] X. Wu, X. Xie, Chen Zhao, Z. Qian, and R. Zhao, "Low voltage and current stress ZVZCS full bridge DC-DC converter using center tapped rectifier reset," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1470–1477, Mar. 2008.

[8] W. J. Lee, C. E. Kim, G. W. Moon, and S. K. Han, "A new phase-shift full-bridge converter with voltage-doubler-type rectifier for high-efficiency PDP sustaining power module," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2450–2458, Jun. 2008.

[9] W. Chen, X. Ruan, and J. Ge, "A novel full-bridge converter achieving ZVS over wide load range with a passive auxiliary circuit," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 1110–1115.

[10] X. Zhang, X. Ruan, and K. Yao, "A novel ZVS PWM phase-shifted full-bridge converter with controlled auxiliary circuit," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 1067–1072.

[11] A. J. Mason and P. K. Jain, "New phase shift modulated ZVS full bridge DC/DC converter with minimized auxiliary current for medium power fuel cell application," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Jun. 2005, pp. 244–249.

[12] Y. Jang and M. M. Jovanovic, "A new family of full-bridge ZVS converter," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 701–708, May 2004.

[13] Z. Chen, B. Ji, F. Ji, and L. Shi, "Analysis and design considerations of an improved ZVS full-bridge DC-DC converter," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 1471–1476.

[14] B. Yang, J. L. Duarte, W. Li, K. Yin, X. He, and Y. Deng, "Phase shifted full bridge converter featuring ZVS over the full load range," in *Proc. 36th Annu. Conf. IEEE ind. Electron. Soc.*, 2010, pp. 644–649.

[15] X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved light-load efficiency for synchronous rectifier voltage regulator module," *IEEE Trans. Power Electron.*, vol. 15, no. 5, pp. 826–834, May 2000.

[16] *Green Phase-Shifted Full-Bridge Controller with Synchronous Rectification, Datasheet SLUSAI6*, Texas Instrum., Dallas, TX, USA, Mar. 2010.

[17] R. Ramachandran and M. Nymand, "Design and analysis of an ultra-high efficiency phase shifted full bridge GaN converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, Mar. 2015, pp. 2011–2016.

[18] B. Y. Chen and Y. S. Lai, "Novel dual mode operation of phase-shifted full bridge converter to improve efficiency under light load condition," in *Proc. IEEE Energy Convers. Congr. Expo.*, San Jose, CA, USA, Sep. 2009, pp. 1367–1374.

[19] J.-W. Kim, D.-Y. Kim, C.-E. Kim, M.-Y. Kim, and G.-W. Moon, "Switching control method for light load efficiency improvement in phase shifted full bridge converter," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, Melbourne, Australia, Jun. 2013, pp. 165–169.

[20] G. N. B. Yadav and N. L. Narasamma, "An active soft switched phase-shifted full-bridge DC–DC converter: Analysis, modeling, design, and implementation," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4538–4550, Sep. 2014.

[21] A. Khaligh, J. Chao, and Y. J. Lee, "A multiple-input DC-DC converter topology," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 862–868, Mar. 2009.

[22] A. Khaligh, A. M. Rahimi, and A. Emadi, "Negative impedance stabilizing pulse adjustment control technique for DC/DC converters operating in discontinuous conduction mode and driving constant power loads," *IEEE Trans. Veh. Technol.*, vol. 56, no. 4, pp. 2005–2016, Jul. 2007.

[23] A. Davoudi, J. Jatskevich, P. L. Chapman, and A. Khaligh, "Averaged-switch modeling of fourth-order PWM DC–DC converters considering conduction losses in discontinuous mode," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2410–2415, Nov. 2007.

[24] A. Davoudi, J. Jatskevich, P. L. Chapman, and A. Khaligh, "Reduced-order modeling of high-fidelity magnetic equivalent circuits," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2847–2855, Dec. 2009.

[25] Z. Lei, L. Haoyu, W. Chao, and L. Yuan, "A method of optimizing the switching frequency based on the loss analysis model," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, Dallas, TX, USA, Oct. 2014, pp. 4103–4109.

[26] Y. K. Lo, C. Y. Lin, M. T. Hsieh, and C. Y. Lin, "Phase-shifted full-bridge series-resonant DC-DC converters for wide load variations," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2572–2575, Jun. 2011.

[27] *A 50 W, 500 kHz, Full-Bridge, Phase-Shift, ZVS Isolated DC to DC Converter Using the HIP4081A, AN9506*, Intersil Intelligent Power, Apr. 1995.

[28] *UCC28950 600-W, Phase-Shifted, Full-Bridge Application Report, Datasheet SLUA560C* , Texas Instrum., Dallas, TX, USA, Sep. 2010.

[29] A. Mallik, "State feedback based control of air-fuel-ratio using two wide-band oxygen sensors," in *Proc. IEEE Asian Control Conf.*, Kota Kinabalu, Malaysia, May 2015, pp. 1–6.

[30] A. Mallik and A. Khaligh, "Control of a single-stage three-phase boost power factor correction rectifier," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2016, pp. 54–59.

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