# Three-Phase VSI Optimal Switching Loss Reduction Using Variable Switching Frequency

Oier Oñederra, Iñigo Kortabarria, Iñigo Martínez de Alegría, Jon Andreu, and José Ignacio Gárate

***Abstract*—Loss reduction in converters is one of main targets in power electronics to obtain higher efficiency and lower thermal stress, which can enhance the lifetime of devices. This paper presents a variable switching frequency technique for switching loss reduction in a three-phase voltage source inverter, obtaining similar output current quality as that of a space vector pulse width modulation (SVPWM) algorithm. This type of optimization has not been applied for a three-phase system before. Simulation and experimental results are also shown. The output current ripple rms value of three-phase SVPWM is used as the optimization constraint. Results of the optimization of the switching losses with quality constraints in the switching frequency as the variable are presented for different load angles and compared with classical SVPWM. Experimental results show that this technique can save up to nearly 19% in switching losses with similar total harmonic distortion of the output current, concluding that converter losses are reduced without reducing output current quality.**

***Index Terms*—Optimization, output current ripple, switching loss, variable frequency, voltage source inverter (VSI).**

## I. Introduction

A THREE-PHASE voltage source inverter (VSI) is one of the most widely used power electronics converter, used in application such as variable speed drives, active power filters, and uninterruptible power supplies [1]. This converter topology is well known, robust, and simple to control [2]–[4].

The most vulnerable elements in a power converter are the dc-link capacitor (30%), power semiconductors (21%), and the printed circuit board (PCB) (26%), being the high temperature the main stress source (55%), which is generated by losses in power semiconductors [5]–[8]. Power loss reduction and temperature stress reduction are two main targets in modern power converters.

Temperature of the switching devices is increased by conduction losses, leakage current losses, and switching losses (turn-ON, turn-OFF, reverse recovery, and driving). The first two sources are static losses, which depend on device technology. On the other hand, switching losses can be varied, among other factors, by modifying the switching frequency.

There are three main strategies to reduce switching losses: reducing voltage or current of the switch during commutation (soft-switching techniques) [9]–[15], varying switching time interval (advanced gate drivers) [16]–[23], or changing the number of commutations in the fundamental period of the output current (modulation and switching frequency variation techniques) [24], [25]. Soft-switching and advanced gate drivers add extra hardware, control, and complexity, reducing reliability of the system [8], [26]. However, modulation techniques and switching frequency variation can be modified without adding extra hardware; this is summarized in Table I.

Some modulation techniques, which can reduce the number of commutations, are called discontinuous pulse width modulation (PWM). These techniques avoid commutations by clamping one of the phases to upper or lower dc-link [4], [27]–[29]. However, these techniques have a lower output current quality comparing to the classical continuous space vector PWM (SVPWM), which is one of the most used modulation technique [30], [31].

Lowering the switching frequency is another method to reduce the number of commutations, but it also reduces the output current quality, which increases losses at load [32], [33]. Some studies improve this quality by varying the switching frequency during the output current period based on current harmonics [34], and other studies present other variable switching frequency (VSF) techniques, i.e., limiting the output current ripple or electromagnetic interference reduction in the three-phase VSI [32]. There is a study that uses the VSF technique to optimize switching losses for a single-phase full bridge inverter while maintaining the current ripple rms value at the same level as in a sinusoidal PWM [25]. However, experimental results of this type of optimization are not found in the three-phase VSI.

One of the objectives of VSF techniques is the reduction of the commutation number [35], [36]. According to this, the main drawback is the reduction of output current quality. In this context, the proposed method gets a commutation number reduction but with similar output current quality of a three-phase VSI system with SVPWM, by using an optimized VSF. This paper presents the proposed method with simulation and experimental results.

This paper is organized as follows: in Section II, the calculation of output current ripple is presented. Section III describes

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TABLE I
LOSSES OF SWITCHES AND POSSIBLE REDUCTION METHODS

| Losses | Switch | Diode | Loss dependence | Possible loss reduction methods | Drawbacks |
|---|---|---|---|---|---|
| • Static | • Conduction<br>• Leakage current | • Conduction<br>• Leakage current | • Voltage drop and current across the device. | • Change device/technology | • Device technology cost |
| • Dynamic | • Turn-ON<br>• Turn-OFF<br>• Driving | • Reverse recovery | • Voltage and current during commutation | • Soft-switching topologies | • Extra hardware, control complexity |
| | | | • Switching time interval<br>• Number of commutations | • Advanced gate drivers<br>• Discontinuous modulation techniques<br>• Lower switching frequency | • Extra hardware<br>• Lower output current quality<br>• Lower output current quality |

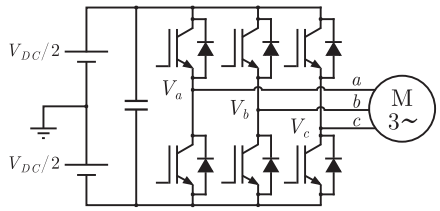


Fig. 1. Basic scheme of the three-phase VSI.

the active-set minimization algorithm objective function and constraints. Section IV presents simulation and experimental results of switching loss reduction and current ripple values for different loads.

## II. OUTPUT CURRENT RIPPLE ANALYSIS

The output current ripple has been analyzed in the literature for a three-phase VSI (see Fig. 1) with *RL* and *RLE* loads, which is useful in order to evaluate output current quality for motor-load and grid-connected applications [37]–[40]. In this analysis, the load has been considered inductive, neglecting other parameters due to $T_{\rm sw}/2 \ll \tau$, i.e., considering the switching frequency 10 kHz, the time interval is $T_{\rm sw}/2 = 1/(2 \times 10\,{\rm kHz}) = 50\,\mu{\rm s}$, and the shortest time constant is $\min(\tau) = L/R = 6\,{\rm mH}/20\,\Omega = 300\,\mu{\rm s}$.

Due to the symmetry of three phases in sinusoidal balanced currents, only one phase is studied in order to simplify the analysis, taking into account that load voltage is between a phase of the inverter and the common node. Considering the switching vectors $V_0$ to $V_7$, with the switching states (0/OFF and 1/ON) of phases $a$, $b$, and $c$ ($S_a$, $S_b$, and $S_c$) (see Fig. 1), the rate of rise and fall of current can be calculated for each applied vector, as shown in Table II. The voltage of load inductance is defined as follows:

$$v_{L_a}(t) = V_{\rm dc} \cdot \left( S_a(t) - \frac{S_a(t) + S_b(t) + S_c(t)}{3} \right) \quad (1)$$

and the resultant current ripple can be approximated as follows:

$$\tilde{i}_a(t) \approx \frac{1}{L_a} \int_0^t \left( v_{L_a}(t) - \bar{v}_{L_{a\,T_{\rm sw}}} \right) \cdot dt \quad (2)$$

where $\bar{v}_{L_{a\,T_{\rm sw}}}$ is the mean value over the switching period $T_{\rm sw}$ of load inductance voltage (given by the controller as reference: $m\cos\theta$). Both values are depicted in Fig. 2.

The ripple current is symmetrical with respect to the center point of the switching period because of the symmetry in the voltage vectors 0–7 application, such as in the SVPWM method. The current ripple waveform peak values $\Delta i_1$ and $\Delta i_2$ of Fig. 2 can be calculated as

$$\Delta i_1 = -\bar{v}_{L_{a\,T_{\rm sw}}} \frac{t_0}{2} \quad (3)$$

$$\Delta i_2 = -\bar{v}_{L_{a\,T_{\rm sw}}} \frac{t_0}{2} + \left( \frac{2V_{\rm dc}}{3} - \bar{v}_{L_{a\,T_{\rm sw}}} \right) \frac{t_1}{2} \quad (4)$$

where $t_0$ and $t_1$ are time intervals of vectors $V_0$ and $V_1$ applied, respectively. These time intervals are obtained by the modulation and carrier waveform crossing instants.

TABLE II
CURRENT SLOPES ACCORDING TO APPLIED SWITCHING VECTOR

| Switching vector | $[S_a\ S_b\ S_c]$ | Current slope $\left(\frac{di_a}{dt}\right)$ |
|---|---|---|
| $V_0$ | [0 0 0] | $-\bar{v}_{L_{a\,T_{\rm sw}}}/L_a$ |
| $V_1$ | [1 0 0] | $\left(\frac{2}{3}V_{\rm dc} - \bar{v}_{L_{a\,T_{\rm sw}}}\right)/L_a$ |
| $V_2$ | [1 1 0] | $\left(\frac{1}{3}V_{\rm dc} - \bar{v}_{L_{a\,T_{\rm sw}}}\right)/L_a$ |
| $V_3$ | [0 1 0] | $\left(-\frac{1}{3}V_{\rm dc} - \bar{v}_{L_{a\,T_{\rm sw}}}\right)/L_a$ |
| $V_4$ | [0 1 1] | $\left(-\frac{2}{3}V_{\rm dc} - \bar{v}_{L_{a\,T_{\rm sw}}}\right)/L_a$ |
| $V_5$ | [0 0 1] | $\left(-\frac{1}{3}V_{\rm dc} - \bar{v}_{L_{a\,T_{\rm sw}}}\right)/L_a$ |
| $V_6$ | [1 0 1] | $\left(\frac{1}{3}V_{\rm dc} - \bar{v}_{L_{a\,T_{\rm sw}}}\right)/L_a$ |
| $V_7$ | [1 1 1] | $-\bar{v}_{L_{a\,T_{\rm sw}}}/L_a$ |

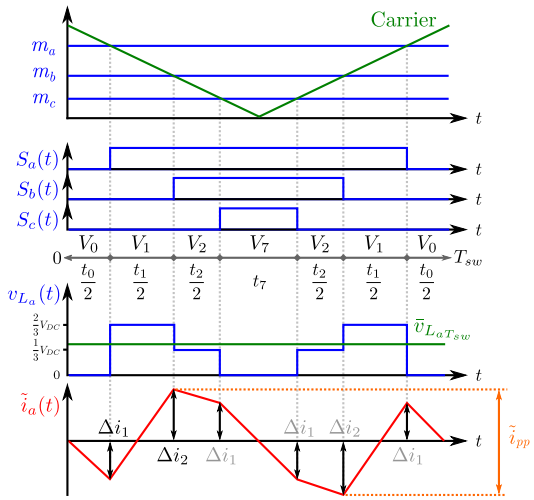


Fig. 2. Current ripple analysis.

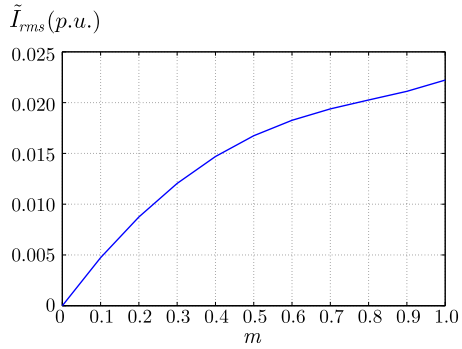


Fig. 3. Output current ripple rms values with CSF.

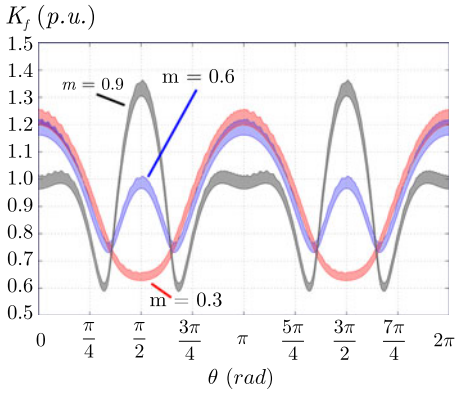


Fig. 4. Switching frequency variation over fundamental period.

The vector time intervals and $\Delta i_1$ and $\Delta i_2$ values can be used to calculate the rms value of the ripple for each switching period as (5) as shown at the bottom of this page, where $t_0$, $t_1$, $t_2$, and $t_7$ are time intervals of vectors $V_0$, $V_1$, $V_2$, and $V_7$ applied, respectively.

The rms value for a whole output period (see Fig. 3)

$$\tilde{I}_{\rm rms} = \sqrt{\frac{1}{T}\int_0^T \left(\tilde{i}_{\rm rms}(\theta)\right)^2 \cdot d\theta}. \tag{6}$$

## III. Switching Frequency Optimization

Switching losses are related to the number of commutations, device voltage, and current value in switching instants. Voltage of the switch is imposed by the dc-link ($V_{\rm dc}$), and the output current is set as a sinusoidal waveform $\left(i_a(t) = \hat{I}\cos(\omega t + \phi)\right)$ to supply a three-phase load. In this paper, the number of commutations has been reduced by changing the switching frequency over the fundamental period, giving rise to a VSF method. Defining the switching losses for each $\theta$ as

$$P_{\rm loss}(\theta) = K \cdot V_{\rm dc} \cdot \hat{I} \cdot |\cos(\theta - \phi)| \tag{7}$$

where $K$ defines switching transition times, $V_{\rm dc}$ is the dc-bus voltage, and $\hat{I}$ is the sinusoidal current peak value.

The average value of switching losses over a whole period can be calculated as

$$P_{\rm avg,loss} = \frac{2}{2\pi}\int_0^{2\pi} P_{\rm loss}(\theta) \cdot f_{\rm sw}(m,\theta,\phi) \cdot d\theta \tag{8}$$

$f_{\rm sw}(m,\theta,\phi)$ being the switching frequency function, depending on modulation index $m$, reference angle $\theta$, and load angle $\phi$, $2\pi$ being the period, and the factor of 2 being the number of commutation for each switching period.

The target of the optimization is to minimize $P_{\rm avg,loss}$. In the optimization function, all constants are avoided [$Q^*$, (9)], such as bus voltage or current peak value, because these are irrelevant for the optimization results, defined as

$$Q^*\left(f_{\rm sw}\,(m,\theta,\phi)\right) = \int_0^{2\pi} |\cos(\theta-\phi)| \cdot f_{\rm sw}(m,\theta,\phi) \cdot d\theta. \tag{9}$$

There is a tradeoff between the number of commutations and the rms value of the output current ripple when the switching frequency changes. Thus, the output current ripple rms value has been defined as a constraint [$\tilde{i}_{\rm rms}$, (11)], getting the optimization target as follows:

$$\underset{f_{\rm sw}\,(m,\theta,\phi)}{\text{minimize}}\ Q^*\left(f_{\rm sw}\,(m,\theta,\phi)\right) \tag{10}$$

$$\text{subject to } \tilde{i}_{\rm rms}(m, f_{\rm sw}(m,\theta,\phi)) = C \tag{11}$$

where $C$ is the desired rms value to be obtained. In this case, the constant $C$ has been defined as the value obtained by $\tilde{I}_{\rm rms}$ in p.u. with constant switching frequency (CSF) SVPWM in a whole period, and function of the modulation index. Summarizing, the optimized switching frequency pattern has to obey the same $\tilde{I}_{\rm rms}$ value as that of the CSF, as shown in Fig. 3.

The $Q^*\left(f_{\rm sw}\,(m,\theta,\phi)\right)$ function is minimized using an active-set minimization algorithm using the optimization toolbox of MATLAB with (10) as objective function and (11) as constraint. A varying switching frequency along the fundamental period has been obtained: $f_{\rm sw}(m,\theta,\phi)$. In order to get a normalized switching frequency, $K_f$ has been defined as

$$K_f = \frac{f_{\rm sw}(m,\theta,\phi)}{f_{\rm sw,constant}}. \tag{12}$$

With $K_f$ (see Fig. 4), any CSF can be modified into a VSF, which is optimal for loss reduction in switches. $K_f$ is highly influenced by the modulation index variation. However, it is quite insensitive to variations in the load angle (colored region involves load angles from $\phi = -\pi$ to $\pi$). Symmetry of variation over $\theta$ is noticeable.

$$\tilde{i}_{\rm rms}(\theta) = \sqrt{\frac{t_0+t_7}{T_{\rm sw}}\frac{{\Delta i_1}^2}{3} + \frac{t_1}{T_{\rm sw}}\frac{{\Delta i_1}^2 + \Delta i_1\Delta i_2 + {\Delta i_2}^2}{3} + \frac{t_2}{T_{\rm sw}}\frac{{\Delta i_1}^2 - \Delta i_1\Delta i_2 + {\Delta i_2}^2}{3}} \tag{5}$$

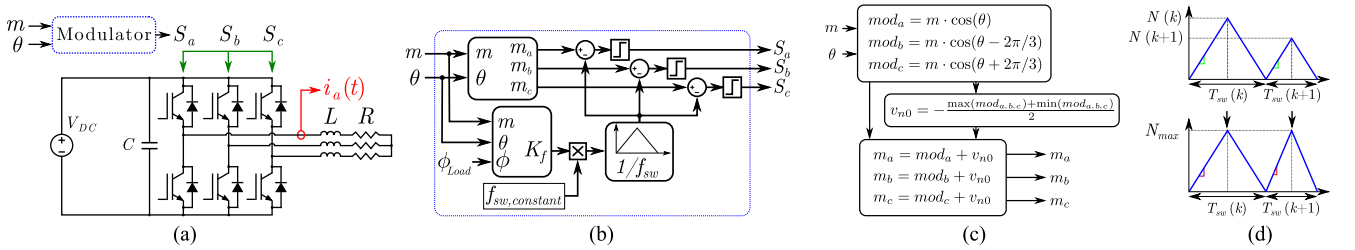


Fig. 5. VSF applied to a VSI. (a) Source, inverter, modulation system, and load. (b) Modulation system in detail. (c) Modulation waveform generator (SVPWM). (d) Carrier waveform generator.

TABLE III
PARAMETERS OF THE SYSTEM

| Parameter | Value |
|---|---|
| $V_{\mathrm{dc}}$ | 600 V |
| Inverter | SEMITOP 3 SEMIKRON |
| Modulation frequency | 95 Hz |
| CSF | 10 kHz |
| Optimized VSF | 5 − 15 kHz |
| $L_{\mathrm{Load}}$ | 6 mH |
| $R_{\mathrm{Load1}}$ | $5\,\Omega \Rightarrow \phi_{\mathrm{Load1}} = -35°$ |
| $R_{\mathrm{Load2}}$ | $10\,\Omega \Rightarrow \phi_{\mathrm{Load2}} = -20°$ |
| $R_{\mathrm{Load3}}$ | $15\,\Omega \Rightarrow \phi_{\mathrm{Load3}} = -13°$ |
| $R_{\mathrm{Load4}}$ | $20\,\Omega \Rightarrow \phi_{\mathrm{Load4}} = -8°$ |

## IV. SIMULATIONS AND EXPERIMENTAL RESULTS

Simulation and experimental results have been measured by the system depicted in Fig. 5(a) and detailed in Fig. 5(b)–(d): a dc-voltage source, a six-insulated gate bipolar transistor (IGBT) inverter, and *RL* loads with parameters listed in Table III. The VSF modulator, carrier, and switching signals are implemented in an field programmable gate array (FPGA). The modulation indexes for each phase are calculated by multiplying the modulation index $m$ with the cosine function of $\theta$ with their respective angle shifts: 0, $-2\pi/3$, and $+2\pi/3$ for $m_a$, $m_b$, and $m_c$, and adding to them the homopolar voltage ($v_{n0}$) of the SVPWM method, as shown in Fig. 5(c).

In order to get the triangular carrier wave, $K_f$ is obtained from a look-up table (LUT) according to the modulation index ($m$), reference angle ($\theta$), and load angle ($\phi$). The data of the LUT are calculated offline for each condition with the optimization process. Then, $K_f$ is multiplied by the CSF ($f_{\mathrm{sw,constant}}$) to obtain actual switching frequency. Finally, a triangular wave is generated for each switching frequency. Due to static load study, frequency patterns have been loaded for each load angle ($\phi_{\mathrm{Load}}$).

The carrier wave is implemented with an up/down counter, toggling up or down in countervalues 0 and $N$, obtaining a symmetrical triangular wave from 0 to $N$, and to 0 again. As the counterslope is programmed as constant, the switching period is varied with the peak value $N$, so this value is a function of the given instantaneous switching period or frequency. Once being able to change the carrier period, the next step is to change the peak value in order to get the same peak value for all periods [see Fig. 5(d)]. This peak value is the maximum value of the carrier wave, so the modulation waveforms fit between 0 and $N_{\mathrm{max}}$ to ensure commutation.

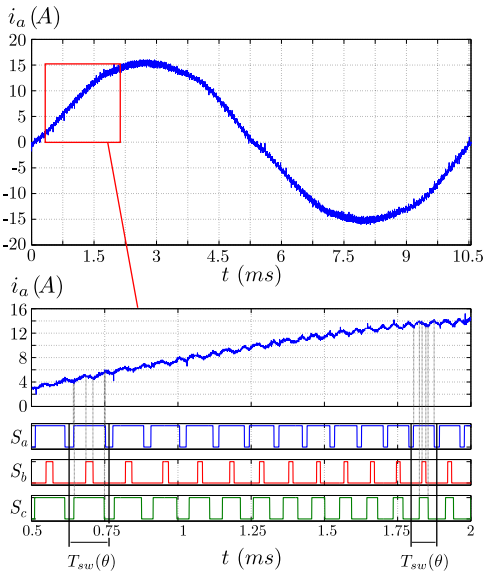


Fig. 6. Current and switching pattern of optimized VSF ($m = 0.8$, $R = 15\,\Omega$, $L = 6$ mH).

Each modulation index is compared with the triangular carrier wave to get pulses as outputs ($S_a$, $S_b$, and $S_c$). These output signals are attached to IGBT gate drivers, in order to switch them.

The implementation of $K_f$ is necessary to load in the modulator with $\Delta\theta = 2\pi/1024$ of resolution, so each $\theta$ can get an accurate value of $K_f$ to produce the desired triangular wave.

In Fig. 6, the output current of phase $a$ is shown in detail with the PWM signals ($S_a$, $S_b$, and $S_c$) for the optimized VSF ($m = 0.8$, $\phi_{\mathrm{Load3}} = -13°$). The difference between switching periods is pointed out as $T_{\mathrm{sw}}$ $(1/f_{\mathrm{sw}})$, showing up the variation in switching frequency.

In order to see the behavior of the system, some simulations have been carried out with a CSF technique, two VSF PWM techniques called VSFPWM1 and VSFPWM2 proposed in [32], and the proposed optimized VSF technique of this paper.

Considering the CSF 10 kHz and the output fundamental frequency 95 Hz, the frequency modulation index is $m_f = 10\,000/95 \approxeq 105$. Due to two commutations in each switching period per phase, the number of commutations can be approximated $2 \times m_f = 210$. But taking into account that the number

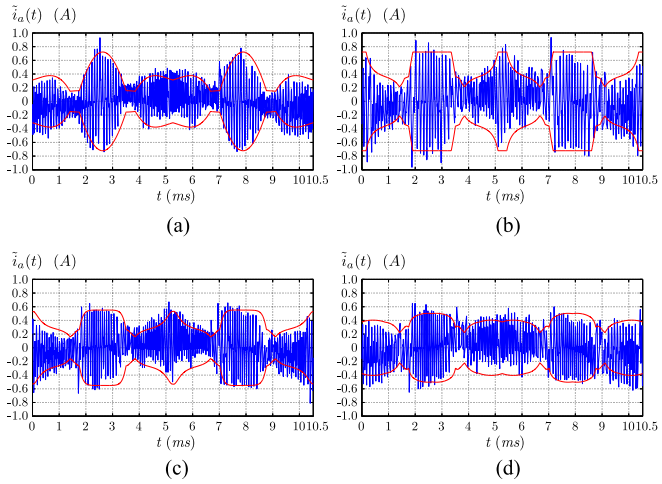


Fig. 7. Output current ripples and their envelope with different techniques ($m = 1$, $R = 20\,\Omega$, $L = 6$ mH). (a) CSF, (b) VSFPWM1, (c) VSPWM2, and (d) optimized VSF.

TABLE IV
OUTPUT CURRENT CHARACTERISTICS AND COMMUTATION PARAMETERS
($m = 1$, $R = 20\,\Omega$, $L = 6$ MH)

| Method | $\tilde{i}_{\mathrm{rms}}\,(A)$ [Analytical value] | $\max(\tilde{i}_{\mathrm{pp}})\,(A)$ | Number of commutations | $E_{\mathrm{sw}}\,(A)$ |
|---|---|---|---|---|
| CSF | 0.2381 [0.2222] | 0.7217 | 210 | 1 787 |
| VSF1 | 0.3090 [0.2494] | 0.7217 | 162 | 1 396 |
| VSF2 | 0.2300 [0.2157] | 0.5521 | 222 | 1 901 |
| Optimized VSF | 0.2419 [0.2186] | 0.5037 | 196 | 1 565 |

of commutations is not the only factor of switching losses at high power side, a sum of current switching instants is defined as

$$E_{\mathrm{sw}} = \sum_{k=1} |i(t_k)| \tag{13}$$

where $i(t_k)$ is the current value in $k$th switching instant. In Fig. 7, some simulations are shown and analyzing main characteristics of these data, a summary is shown in Table IV. Under conditions detailed in Table IV and Fig. 7, the fewest commutation number and switching loss parameter ($E_{\mathrm{sw}}$) are obtained by VSFPWM1, but with the expense of having the highest $\tilde{i}_{\mathrm{rms}}$ value, which concludes losses in load. The VSFPWM2 method gets similar $\tilde{i}_{\mathrm{rms}}$ value as CSF, but switching parameters are higher than CSF. The proposed optimized VSF method gets similar $\tilde{i}_{\mathrm{rms}}$ to CSF in simulation (lower by analytical calculation), and it obtains low switching loss parameters and the current ripple maximum value is the lowest, compared to the other methods.

In this context, Fig. 8 shows a comparison between the number of commutations in the optimized VSF against CSF. As it shows, the optimized VSF has less number of commutations. Lowering the number of commutations, driving losses are inherently reduced.

Calculating $E_{\mathrm{sw}}$ from experimental data for CSF and optimized VSF, it is possible to see the difference between them. This value is lower with optimized VSF than with CSF, independent of the load (see Fig. 9). Fig. 10 plots relative switching loss saving between both methods defined as

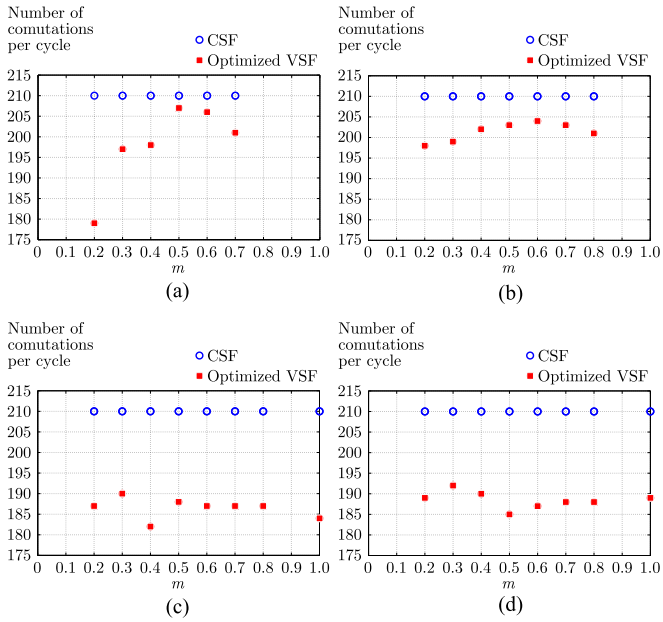


Fig. 8. Number of commutations with CSF and optimized VSF for different modulation indexes and loads. (a) Load 1 ($\phi = -35°$), (b) Load 2 ($\phi = -20°$), (c) Load 3 ($\phi = -13°$), and (d) Load 4 ($\phi = -8°$).

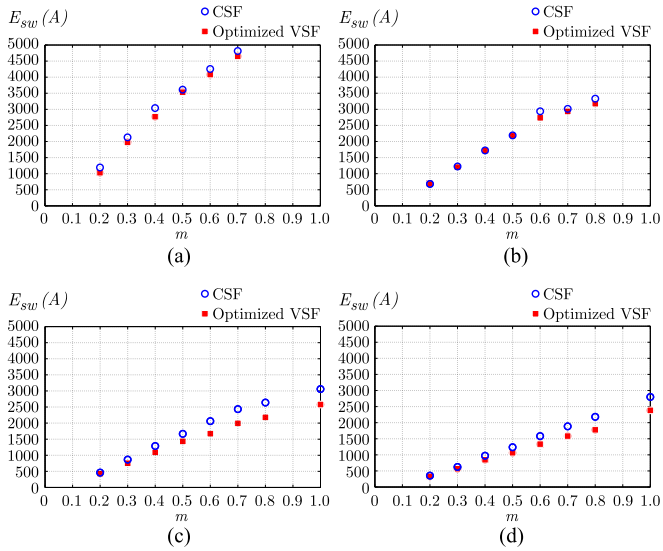


Fig. 9. $E_{\mathrm{sw}}$ values for each load and $m$ obtained from acquired data. (a) Load 1 ($\phi = -35°$), (b) Load 2 ($\phi = -20°$), (c) Load 3 ($\phi = -13°$), and (d) Load 4 ($\phi = -8°$).

$$\text{Loss saving}\ (\%) = \left(1 - \frac{E_{\mathrm{sw,opt}}}{E_{\mathrm{sw}}}\right) \cdot 100\%. \tag{14}$$

Focusing on Fig. 10, this method can save up to 19% in switching losses compared to the classical CSF SVPWM.

In Fig. 11, the output current total harmonic distortion (THD) values are shown for both systems (CSF and optimized VSF) with different loads according to the modulation index. It shows that the quality of the output current changes slightly with the

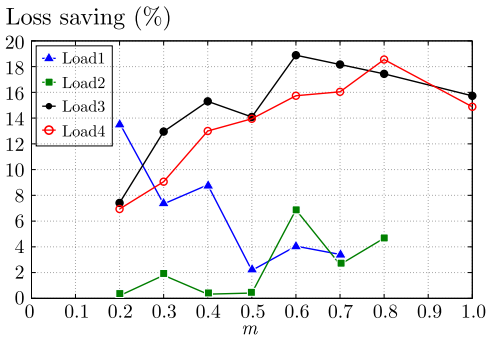


Fig. 10. Switching loss saving for different modulation indexes and loads at high power side.

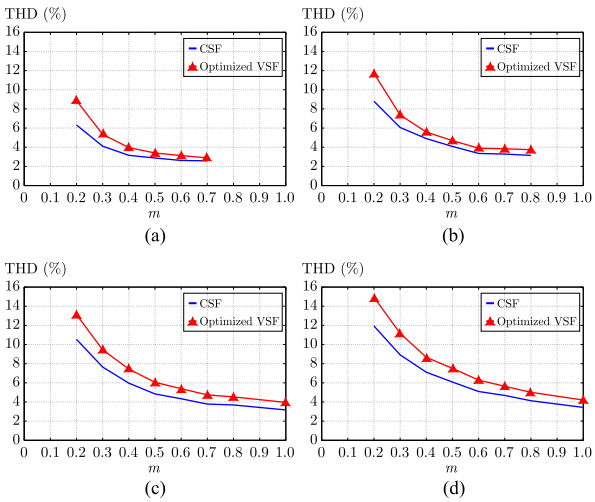


Fig. 11. Output current THD extracted from data with CSF and optimized VSF, with different loads. (a) Load 1 ($\phi = -35°$), (b) Load 2 ($\phi = -20°$), (c) Load 3 ($\phi = -13°$), and (d) Load 4 ($\phi = -8°$).

load angle, but both systems give similar results over the modulation index.

## V. Conclusion

In power converters in general, there is a tradeoff between switching losses and output current quality. In this paper, an optimal switching frequency is proposed to reduce switching losses, with nearly the same output current quality. The switching frequency is varied according to the output current ripple rms value over the whole period, concluding with a lower number of commutations.

VSF methods have been proposed for three-phase VSIs in the literature, but were not focused on optimization to reduce switching losses getting similar THD for output current. This paper tries to extend the VSF methods for three-phase VSIs.

The proposed method is extracted by mathematical optimization and has been applied to a real system with different loads and modulation indexes. It has been compared to CSF, concluding that it saves switching losses by reducing the number of commutations. With this method, high power side losses and driving losses are reduced by reducing the number of commutations, and not increasing load losses.

This technique is able to save up to 19% in switching losses (best case according to acquired data: $m = 0.6$ and $\phi = -13°$). These savings reduce the generated heat of switches, so the thermal stress gets lower, enhancing the lifetime of switches. On the other hand, focusing on the output current quality, the THD values for all applied loads and modulation indexes are still similar for both methods (CSF and VSF). Considering this, the converter losses are reduced and load losses are not increased, due to similar output current quality.

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