Single-Pulse Avalanche Mode Robustness of Commercial 1200 V/80 mΩ SiC MOSFETs

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***Abstract*—Commercialization of 1200-V silicon carbide (SiC) MOSFET has enabled power electronic design with improved efficiency as well as increased power density. High-voltage spikes induced in applications such as solenoid control, solid-state transformer, boost converter, and flyback converter can drive the MOSFET into avalanche mode operation due to high *di/dt* coupled with parasitic inductance. Avalanche mode operation is characterized by high-power dissipation within the device due to the high voltage and current crossover. This study focuses on the evaluation of two commercially available SiC MOSFETs from different manufacturers, each rated for 1200 V with an ON-state resistance of 80 mΩ, during unclamped inductive switching (UIS) mode operation. To determine device reliability, a decoupled UIS testbed was developed to evaluate the avalanche energy robustness at 22 °C and 125 °C during two specific conditions: high current and low energy, and low current and high energy. The SiC MOSFETs were evaluated using a load inductance of 1.42, 5.1, 10.5, and 15.8 mH to understand the effect of current and avalanche energy on device failure. To correlate the experimental results with the failure mechanism, estimated junction temperature and static device characteristics are presented; additionally, MOSFETs were decapsulated to examine the failure sites on the semiconductor die.**

***Index Terms*—Avalanche breakdown, failure analysis, MOSFETs, power semiconductor devices, semiconductor device reliability, silicon carbide (SiC), unclamped inductive switching (UIS).**

I. Introduction

SILICON carbide (SiC) power semiconductor technology has matured from research grade devices to commercial production. The superior semiconductor properties of SiC, as compared to Silicon (Si), make it suitable for high-voltage and high-current switching application under elevated ambient temperature condition [1]–[8]. One of the momentous breakthroughs in SiC technology is the development of the high-voltage MOSFET; as SiC fabrication continues to evolve, increased power density and reduced switching and conduction losses can be realized by the replacement of Si devices with SiC devices [9]–[12]. SiC MOSFETs can handle high blocking voltage and forward current while possessing the inherent ability to operate at high-switching frequency [13]–[17]. However, switching operation at high-current magnitude increases electrothermal stress on the power device.

Commercial SiC MOSFETs are available from major semiconductor manufacturers, however widespread acceptance of the technology has not been adopted [18], [19]. Though a promising technology for a wide variety of power electronic applications, the failure modes, and reliable operating limits under extreme operating conditions have not been fully established for commercial devices [20], [21]. Automotive applications including solenoid control, integrated-starter-alternator, and power supply topologies, such as dc–dc boost converter and flyback transformer drive, are examples of applications where the switching device experiences high-voltage spikes that can drive it into avalanche breakdown [22]. The situation is exacerbated when the high rate of change of current (i.e., *di/dt*), encountered in high-switching frequency power electronic circuits, combines with the parasitic inductance to intensify the induced voltage [23], [24]. Avalanche mode operation is encountered when switching into an unclamped inductive load, where the energy stored in the inductor must be dissipated in the switching device and is characterized by high-voltage and high-current crossover that occurs during the OFF state. Though avalanche breakdown events are unlikely during typical switching operation, due to advancements in design criteria, occurrence of any such event can result in catastrophic device destruction that may lead to system failure.

Research has been conducted in the past to evaluate the avalanche ruggedness of both commercial and research grade SiC power devices to determine device reliability during high electrical stress incurred due to avalanche breakdown. Hu *et al.* analyzed the performance of parallel connected commercial 1200-V SiC MOSFETs during the avalanche mode operation [25]. A commercial 1200-V/42 A SiC MOSFET was characterized under unclamped inductive switching (UIS) condition in [26]. Alexakis *et al.* examined the avalanche capabilities of SiC MOSFET, Si-based MOSFET, and Si-based IGBT; each rated for 1200 V with similar current ratings [27]. UIS stress testing of 1200 V normally OFF SiC JFET has been conducted in [28]. Single and repetitive pulsed evaluation of a research grade 1200 V normally ON SiC vertical JFET was conducted by Pushpakaran *et al.* and Pushpakaran *et al.*, respectively [29]–[30]. In this paper, two commercially available SiC MOSFETs, rated for 1200 V, have been compared for their avalanche performance during varying current and energy conditions; the

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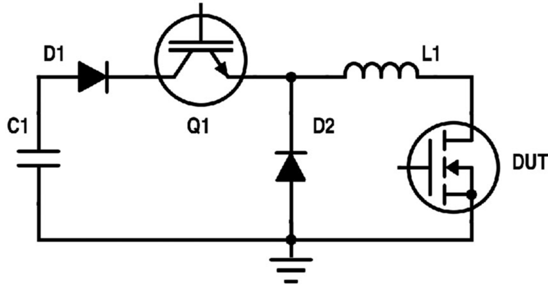


Fig. 1. Simplified UIS testbed schematic.

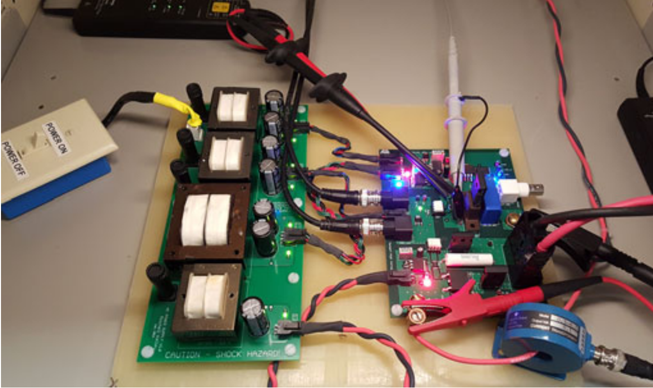


Fig. 2. Hardware setup – the load inductor and capacitor bank are not shown. The load inductor is placed outside the metal testing rack while the capacitor bank is located on the rack level directly below the testbed.

devices selected had a rated ON-state resistance of 80 mΩ. Results presented in this study are based on experiments carried out using SiC MOSFETs from CREE (C2M0080120D) and ST microelectronics (SCT30N120) to establish the avalanche robustness of two commercially available SiC MOSFETs to ensure device reliability during extreme electrical and thermal conditions, which may occur in end applications. Experimental data provided in this research not only establish maximum tolerable avalanche energy for each device, but also present static device characterization demonstrating the capabilities of SiC to withstand single-pulse avalanche events without experiencing device degradation. Additionally, an estimated junction temperature has been calculated using a simplified Z_{TH} model for both CREE and ST devices to better understand the possible failure mechanism during UIS.

II. Hardware Test Setup

Avalanche ruggedness was evaluated using a decoupled UIS testbed [29]. The decoupled UIS circuit provides two key benefits: precise current and energy control, and supply isolation. A simplified circuit schematic for the UIS testbed is shown in Fig. 1 and the hardware setup is partially shown in Fig. 2. C1, a capacitor bank consisting of four 860 μF/1150 V capacitors connected in parallel, is coupled with a 600 V/1 A dc source to provide adequate test energy for single-pulse analysis. A Si diode, D1 (IXYS DH60-16A), rated for 1600 V/60 A acts as a reverse polarity protection diode. Q1 is a 1700-V Si IGBT (IXYS IXBT42N170) that decouples the active test circuit from the source when in the OFF state. D2 (GeneSiC GB20SLT12-247), a 1200 V/50 A SiC Schottky diode, creates a discharge path to de-energize the load inductor after supply isolation. The load inductor, L1, is selected to be 1.42, 5.1, 10.5, or 15.8 mH; an air-core geometry was used for each of the four load inductors.

Q1 and DUT are normally OFF; the capacitor bank is initially charged to the testing voltage. The charging voltage of the capacitor bank was altered based on the required peak current magnitude and load inductor. Using a Spartan-3 FPGA as a signal generator, Q1 and DUT are simultaneously turned ON. Peak inductor current is then determined using (1), where I_{SS} is the steady-state current and τ is the effective RL time constant of the test circuit [30]. Coil resistance of the air-core load inductor and rated ON-state resistance of both the IGBT and DUT are factored into the calculation to realize precise current control. Stored inductor energy can then be determined using (2)

$$i_{\mathrm{peak}}(t) = I_{\mathrm{SS}}(1 - e^{-t/\tau}) \tag{1}$$

$$E = \frac{1}{2} L \cdot i^2. \tag{2}$$

At turn OFF, Q1 and DUT are triggered simultaneously. If delay exists, it is crucial Q1 be triggered prior to the DUT to decouple the capacitor bank. Avalanche mode operation occurs as both Q1 and DUT are in the OFF state. During this process, the DUT is stressed and avalanche energy can be calculated using measurements of drain to source voltage, V_{DS}, and drain to source current, I_{DS}, in (3), where the avalanche time duration is t_2 minus t_1. Avalanche time, t_{AV}, can be calculated using (4), where the avalanche time is shown to be proportional to the load inductance; I_{DS} is the measured peak drain to source current and V_{BR} is the measured peak drain to source voltage assuming the MOSFET voltage is constant during avalanche mode operation [22]

$$E = \int_{t_1}^{t_2} V_{\mathrm{DS}}(t) \cdot I_{\mathrm{DS}}(t) \cdot dt \tag{3}$$

$$t_{\mathrm{av}} = t_2 - t_1 = L \cdot \frac{I_{\mathrm{DS}}}{V_{\mathrm{BR}}}. \tag{4}$$

Measurement of V_{DS} and I_{DS} was obtained using a Keysight 10076C passive probe and Stangenes pulse current transformer. The external gate resistance was 10 Ω; turn ON and turn OFF gate voltages were 20 and -5 V, respectively. It should be noted the C2M0080120D has an internal gate resistance of 4.6 Ω and the SCT30N120 has an internal gate resistance of 5 Ω [31], [32]. Data were collected using a Tektronix DPO2024B Oscilloscope. The static characteristics of each DUT were measured prior to UIS stress testing using an Agilent B1505A Curve Tracer. Threshold voltage, V_{TH}, was measured at I_{DS} equal to 1 and 5 mA for the SCT30N120 and C2M0080120D, respectively; the gate to source voltage, V_{GS}, was set equal to V_{DS}. Forward *I–V* characteristic curves were acquired for V_{GS} between 10 and 20 V in 5-V steps; breakdown characteristics were measured with V_{GS} equal to 0 V and a current compliance limit of 100 μA.

III. Unclamped Inductive Switching

Drain to source voltage, V_{DS}, and drain to source current, I_{DS}, were measured for the DUT during UIS testing and device power

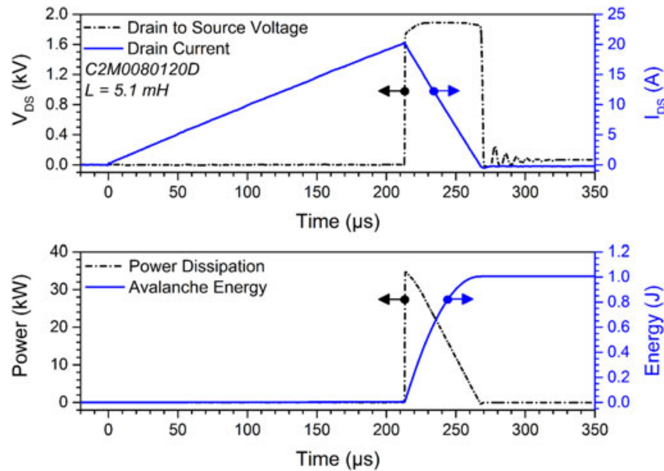


Fig. 3. Drain to source voltage and current (top), and power dissipation and avalanche energy (bottom) waveforms for 1200-V CREE MOSFET during single-pulse unclamped inductive switching with 5.1-mH load inductor.

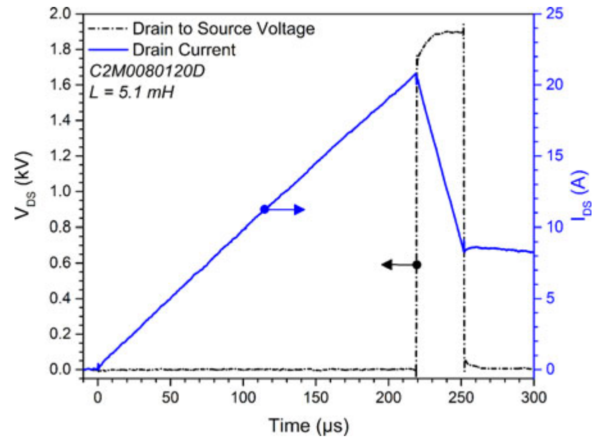


Fig. 4. Drain to source voltage and drain current waveforms pertaining to CREE MOSFET failure during single-pulse unclamped inductive switching at 22 °C with a 5.1-mH load inductor.

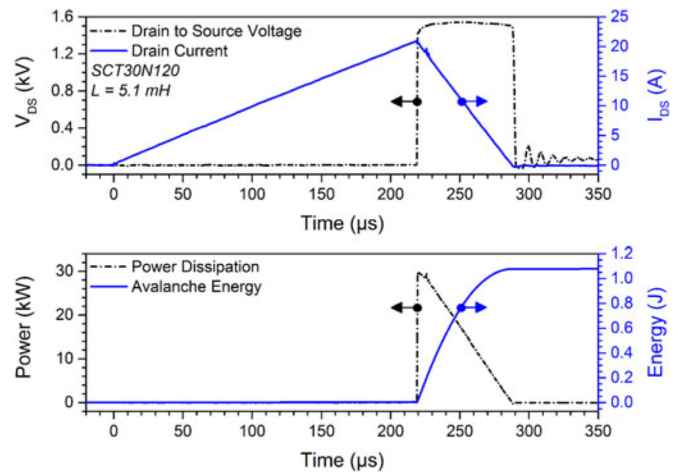


Fig. 5. Drain to source voltage and current (top), and power dissipation and avalanche energy (bottom), waveforms for the 1200-V ST MOSFET during single-pulse unclamped inductive switching with 5.1-mH load inductor.

was then calculated by multiplying V_{DS} and I_{DS} waveforms. Energy dissipated within the device during the avalanche regime was calculated by integrating the power dissipation waveform with respect to the avalanche time duration. Load inductance was varied between the minimum, 1.42 mH, and maximum, 15.8 mH, to allow for the devices to be tested under varying avalanche current and avalanche time conditions.

Measured waveforms for the CREE MOSFET, during avalanche energy testing, are shown in Fig. 3. Results in Fig. 3 were measured at 22 °C and obtained using a DUT turn ON pulse width of 213 μs, which corresponded to a peak drain current of 20.1 A with a 5.1-mH load inductor. During the avalanche regime, which lasted for 56 μs, the energy stored in the inductor discharges through the MOSFET while clamping V_{DS} to 1896 V. Under these conditions, the dissipated avalanche energy was measured to be 1 J, while the peak power dissipation was observed to be 35.3 kW.

Using a fixed load inductance, each device was tested to its failure point; this was achieved by gradually increasing the drain current, thus increasing avalanche energy. A typical single-pulse failure for the CREE device is shown in Fig. 4, where the load inductance was 5.1 mH and a pulse width of 219 μs resulted in a peak drain current of 20.8 A. During the avalanche regime, the voltage across the MOSFET reached a peak magnitude of 1900 V followed by a decrease in drain current. The avalanche regime lasted for 32.7 μs, followed by a sudden collapse in drain to source voltage that can be observed at $t \approx 252$ μs in Fig. 4. The waveforms clearly indicate complete device failure due to the loss of blocking voltage capability and the formation of a conductive path between drain and source electrodes.

Measured waveforms for the ST MOSFET during avalanche energy testing are shown in Fig. 5. Results in Fig. 5 were obtained using a DUT turn ON pulse width of 219 μs which corresponded to a peak drain current of 20.8 A with a 5.1-mH load inductor. During the avalanche regime, which lasted for 71 μs, the energy stored in the inductor discharges through the MOSFET while clamping V_{DS} to 1538 V. Under these conditions, the dissipated avalanche energy was measured to be 1.07 J, while the peak power dissipation was observed to be 30.1 kW. A typical single-pulse failure for the ST device is shown in Fig. 6, where the load inductance was 5.1 mH and a pulse width of 275 μs resulted in a peak drain current of 25.8 A. During the avalanche regime, the voltage across the MOSFET reached a peak magnitude of 1564 V followed by a decrease in drain current. The avalanche regime lasted for 44 μs, followed by a sudden collapse in drain to source voltage that can be observed at t ≈ 320 μs in Fig. 6. As with the CREE device, the measured waveforms indicate complete device failure due to formation of a conductive path between drain and source electrodes.

IV. Avalanche Energy Tolerance

Single-pulse measurements were obtained at both 22 °C and 125 °C for each of the selected four load inductances; results shown in Fig. 7 represent measurements of the CREE device and those of Fig. 8 represent the ST device. Fig. 7 shows that the

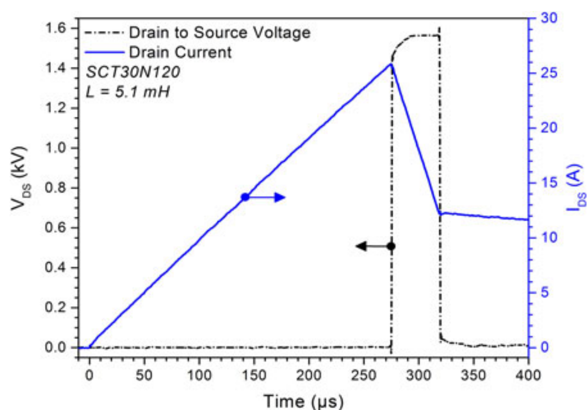


Fig. 6. Drain to source voltage and current waveforms pertaining to ST MOSFET failure during single-pulse unclamped inductive switching at 22 °C with a 5.1-mH load inductor.

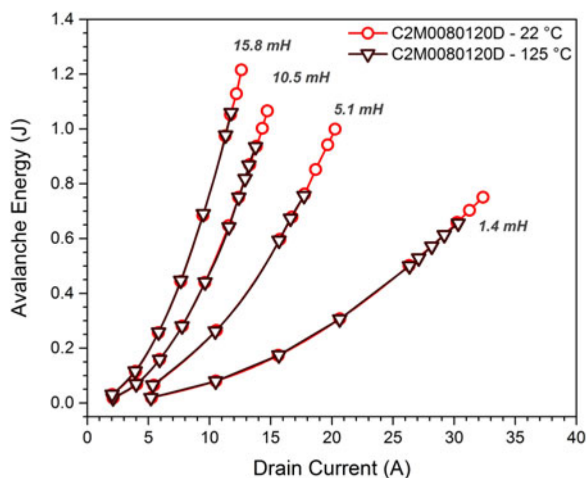


Fig. 7. Avalanche energy shown with respect to I_{DS} for the CREE device measured at 22 °C and 125 °C. The peak of each curve, shown for each load inductor, represents the maximum tolerable avalanche energy.

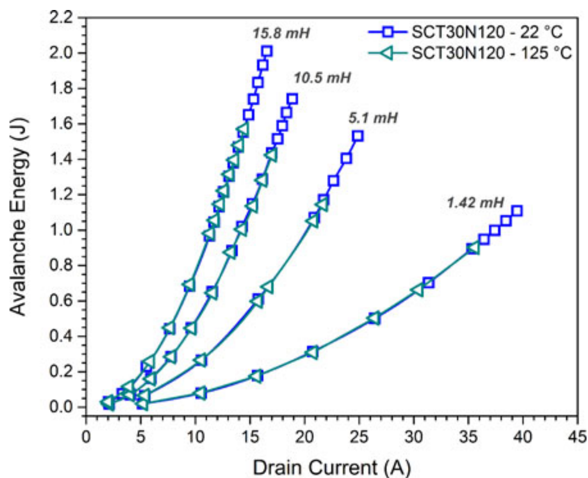


Fig. 8. Avalanche energy shown with respect to I_{DS} for the ST device measured at 22 °C and 125 °C. The peak of each curve, shown for each load inductor, represents the maximum tolerable avalanche energy.

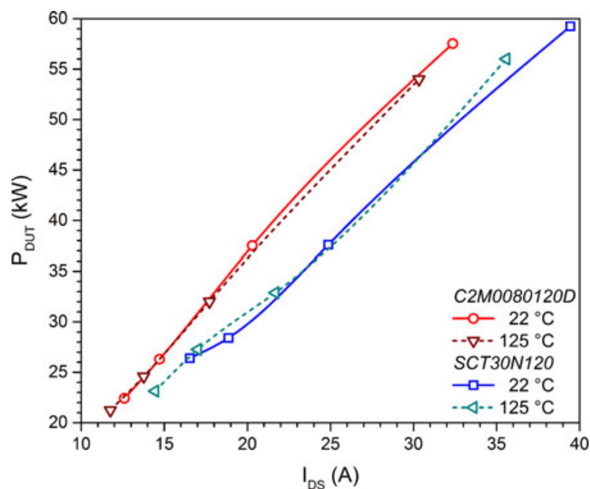


Fig. 9. Measured peak power dissipation with respect to I_{DS}. Data points represent the maximum power dissipation measured at the maximum avalanche tolerance for each of the four load inductors tested. Solid lines represent data obtained at 22 °C, and dashed lines represent data obtained at 125 °C.

maximum measured tolerable avalanche energy for the CREE device, at 22 °C, is 0.75 J resulting from a peak drain current of 32.3 A with a 1.42-mH load inductor. Also shown in Fig. 7, during longer avalanche time, the maximum measured tolerable avalanche energy for the CREE device, at 22 °C, is 1.25 J resulting from a peak drain current of 12.6 A with a 15.8-mH load inductor. Under both test conditions, high avalanche current and longer avalanche time, the avalanche energy tolerance for the CREE device was measured to decrease when the device's case temperature was increased to 125 °C.

In Fig. 8, the maximum measured tolerable avalanche energy for the ST device is shown to be higher than that of the CREE device under all test conditions. During high peak avalanche current, the maximum tolerable avalanche energy of the ST device, at 22 °C, was measured to be 1.1 J resulting from a peak avalanche current of 39.4 A with a 1.42-mH load inductance; this represents a 0.35 J increase in that measured for the CREE device. During longer avalanche time, the avalanche tolerance of the ST device was measured to be 2 J, at 22 °C, where the peak drain current was 16.5 A using a 15.8-mH load inductor. Under this test condition, the ST device yielded an avalanche tolerance 0.75 J greater than that of the CREE device. When the device's case temperature was increased to 125 °C, the ST device was also shown to exhibit a decrease in avalanche tolerance.

When tested using smaller load inductance (i.e., 1.42 mH), the avalanche time duration is lower due to the higher I_{DS} required to generate sufficient avalanche energy, thereby, increasing the peak power dissipation. Observing (4), it is shown that avalanche time is inversely proportional to the breakdown voltage, measured at I_{DS}, and therefore short avalanche duration leads to higher peak power dissipation with-in the device. A better understanding of the relationship between I_{DS} and peak power dissipation is shown graphically in Fig. 9. In Fig. 9, the maximum power dissipation, measured with each load inductor, is shown with respect to I_{DS} for measurements obtained at 22 °C

and 125 °C; each data point represents peak power dissipation measured at the maximum tolerable avalanche energy shown in Figs. 7 and 8 for the CREE and ST devices, respectively.

Even though the avalanche tolerance of the ST device was shown to be higher than the CREE device, the peak power dissipation just prior to failure is shown to increase only marginally in comparison to the avalanche energy tolerance. Avalanche energy tolerance increase, when measured with a load inductance of 15.8 mH, was 60% or 0.75 J for the ST device over the CREE device; however the peak power dissipation increased only 18%, or 4 kW at 22 °C. When measured with a load inductance of 1.42 mH at 22 °C, the increase in avalanche tolerance was 47%, or 0.35 J, yet peak power dissipation increased only 3%, or 1.7 kW.

V. Comparison of Static Characteristics

After the initial static characterization, UIS measurements were obtained for $I_{\rm DS}$ values of 10, 20, 30, and 36 A, at 22 °C using a 1.42-mH load inductor; the 36-A measurement was obtained only for the ST device. $I_{\rm DS}$ values were selected as a percentage of the maximum tolerable avalanche energy; for example, 30 A corresponds to 90% of the maximum measured avalanche tolerance of the CREE device, however 90% for the ST device occurs at 36 A. Between each UIS measurement, the initial characterization (i.e., $V_{\rm TH}$, forward IV, blocking voltage) was repeated for all test devices. A signficant variation in device performance would indicate damage to the device likely occured as a result of UIS induced energy dissipation. Results from the intial characterization and post UIS stressing are shown in Fig. 10 for the CREE device and Fig. 11 for the ST device. $V_{\rm TH}$ is shown with respect to a normalized *x*-axis representing the ratio of tested avalanche energy to the maximum tolerable presented in Fig. 7, for the CREE device, and Fig. 8 for the ST device; additionally, the intial measurement is shown at zero on the normalized axis.

Measurement results obtained after UIS stressing for the CREE device, Fig. 10, exhibited negligible deviation in device performance when compared with the initial measurements. The intial $V_{\rm TH}$ measured was 3.03 V; after measurement at approximately 90% the maximum energy tolerance, the measured $V_{\rm TH}$ was 3.04 V. Therefore, intially and after UIS, the measured $V_{\rm TH}$ remained with-in values specified in [31]. Additionally, negligible change in forward IV charactersitics or blocking voltage of the device was measured. Likewise, for the ST device, Fig. 11, no significant change in device performance was measured after UIS. Initially, $V_{\rm TH}$ was 3.35 V and measured to decrease to 3.15 V after measurement; though a larger deviation is obtained for ST device, this value remains with-in values specified in [32]. Variations observed during the measurement of $V_{\rm TH}$, at low $I_{\rm DS}$ values, could be attributed to the randomness in the surface charge distribution across the gate oxide interface as discussed in [33]. However, it is shown in both Figs. 10 and 11 that neither device exhibited a change in performance for forward or reverse mode operation as a result of $V_{\rm TH}$ changes. These results validate the robustness of both CREE and ST devices to withstand single-pulse avalanche events without any observable degredation in device performance up to 90% of tolerable measured avalanche energy.

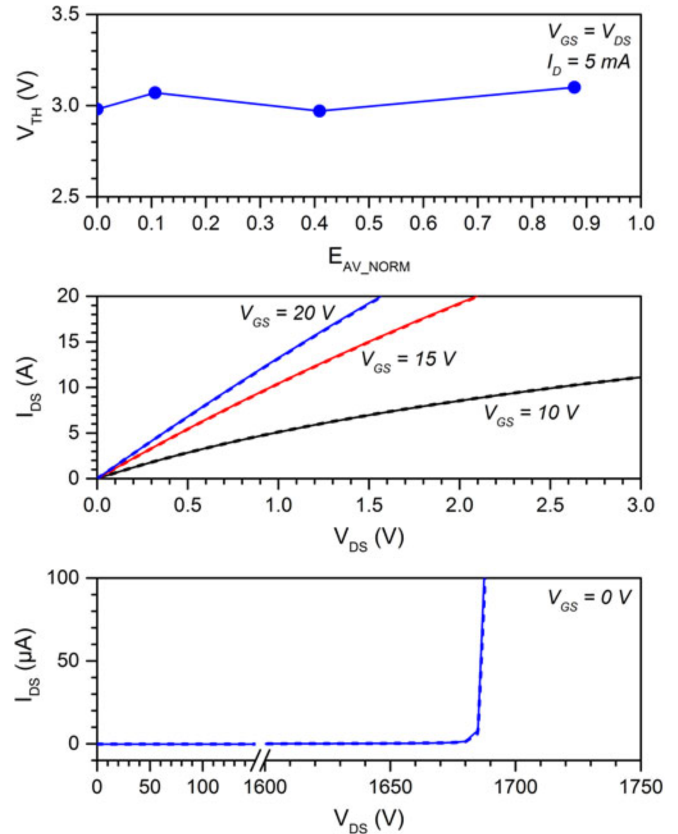


Fig. 10. Comparison on inital measurements of $V_{\rm TH}$ (top), forward IV characteristics (middle), and breakdown voltage (bottom), to those obtained after measurement at approximately 90% the maximum tolerable avalanche energy for the CREE device. Test parameters are indiciated for each measurement; in the middle and bottom plots, initial measurements are indicated with solid lines and those after UIS in bold dashes lines.

VI. Avalanche Mode Failure

In general, avalanche mode failure of a power MOSFET is caused by two factors, which are briefly discussed: turn ON of the parasitic BJT in the MOSFET structure and the attainment of intrinsic temperature limit. A simplified DMOSFET half-cell structure, shown in Fig. 12, indicates the presence of a parasitic NPN BJT formed at the junctions between the source, P-base, and drift regions as emitter, base, and collector, respectively. The turn ON of this BJT results in MOSFET latch-up, which can lead to catastrophic device failure.

The parasitic BJT turn ON is dependent on the voltage drop across the base-emitter junction (i.e., P-base and source), which in-turn is determined by the voltage drop across the resistor R_B shown in Fig. 12. Since R_B is a function of the P-base resistivity, it is directly affected by the *p*-type doping concentration used during device fabrication. In a SiC MOSFET, advanced fabrication techniques, including retrograde P-Base doping, have enabled low *p*-type doping near the surface, which is

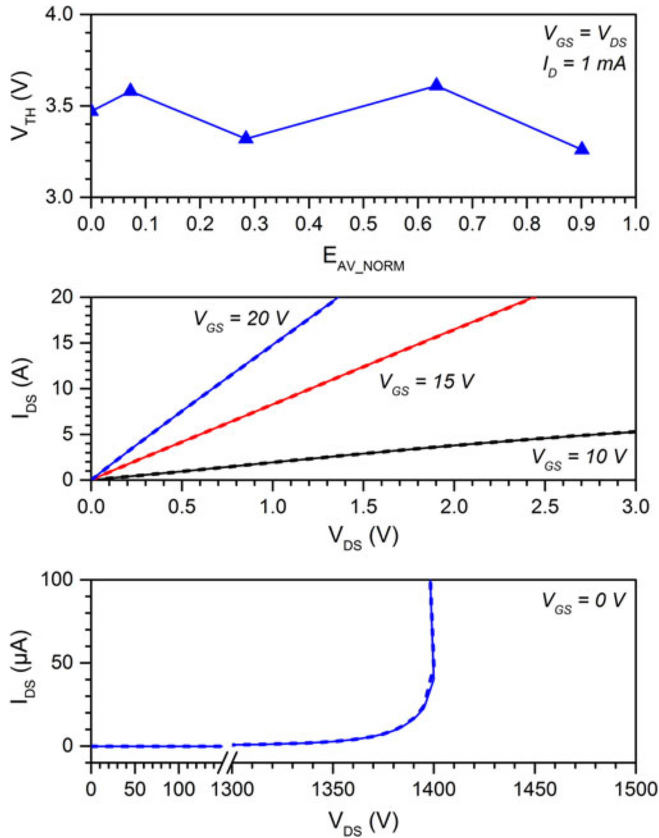


Fig. 11. Comparison on inital measurements of $V_{\rm TH}$ (top), forward IV characteristics (middle), and breakdown voltage (bottom), to those obtained after measurement at approximately 90% the maximum tolerable avalanche energy for the ST device. Test parameters are indiciated for each measurement; in the middle and bottom plots, initial measurements are indicated with solid lines and those after UIS in bold dashes lines.

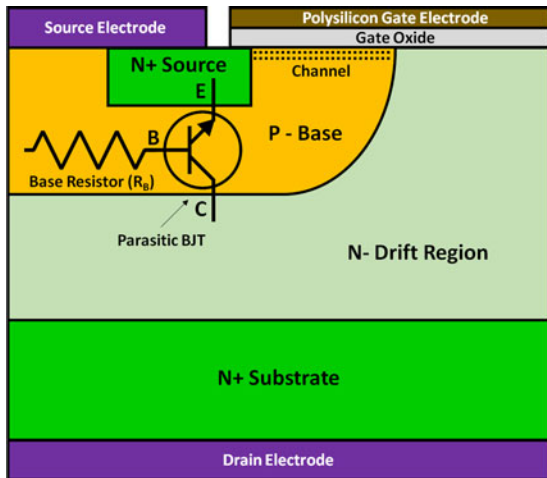


Fig. 12. Simplified vertical DMOSFET half-cell structure.

beneficial in achieving low threshold voltage and higher doping at the P-Base/Drift region interface to suppress the BJT turn ON by lowering the resistivity. Moreover, the higher built-in potential of SiC P-N junction ($\rm V_{bi}\,(SiC) \approx 3\,V$ as compared to $\rm V_{bi}\,(Si) \approx 0.7\,V$) and an extremely weak current gain for the parasitic BJT make the BJT turn ON event highly unlikely unless there is high current flow through the P-base region or substantial increase in the resistivity due to intense localized heating.

Intrinsic temperature limit of a semiconductor material can be defined as the temperature at which the intrinsic carrier concentration becomes greater than or equal to the background doping concentration. Avalanche mode power dissipation in the MOSFET can cause the lattice temperature to increase beyond the intrinsic limit, at which point the device would lose its drain to source blocking capability thereby leading to thermal runaway and eventually device failure. Due to the wider bandgap of SiC, the intrinsic carrier concentration is extremely low which enables the material to sustain its semiconductor properties even at elevated temperature. Based on the information provided in [34], a lattice temperature close to 1270 °C is required for 4H-SiC to attain an intrinsic carrier concentration of 10^{16} $\rm cm^{-3}$. However, device failure could occur prior to exceeding the intrinsic temperature limit due to metallization, dielectric, and interface degradation/failure; e.g., the melting temperature for copper doped aluminum, which is one of the material of choice for power device top metal, is around 660 °C [35]. Though both aforementioned mechanisms are a result of localized heat dissipation within the device, which leads to thermal runaway due to mesoplasma formation, bond pad, contact, and/or dielectric degradation/failure can occur prior to SiC undergoing intrinsic failure [36].

VII. Avalanche Robustness

It can be observed from the results shown in Figs. 7 and 8 that under the same test conditions, the ST MOSFET was able to withstand higher avalanche current as compared to its CREE counterpart. In this section, junction temperature and avalanche time duration are considered to analyze the difference in avalanche tolerance between both devices.

A. Junction Temperature Estimate

Single-pulse junction-to-case thermal impedance, $Z_{\rm TH}$, provided in [31] and [32], was used for the approximation of average junction temperature, $T_{J_\rm EST}$, using (5). In (5), $Z_{\rm TH}$ is a function of the measured avalanche time, $t_{\rm AV}$; $P_{\rm AV}$ is the DUT average power dissipation during the avalanche regime; $T_{\rm CASE}$ is the case temperature. $P_{\rm AV}$ is derived from the results shown in Fig. 9, for peak power dissipation, where average power is half the peak value assuming the power dissipation waveform is a reverse sawtooth pulse. Junction temperature estimates are based on the assumption that energy dissipated in the DUT is adiabatic, thereby contributing entirely to the junction temperature increase [34]; additionally, temperatures are estimated up to the measured tolerable avalanche energy

$$T_{\rm J_EST}(t_{\rm AV}) = Z_{\rm TH}(t_{\rm AV}) \cdot P_{\rm AV} + T_{\rm CASE}. \quad (5)$$

Using $P_{\rm AV}$ and the respective $Z_{\rm TH}$ value, average junction temperature estimates for the CREE device are shown in Fig. 13 for load inductances of 1.42, 5.1, and 15.8 mH, at 22 °C and 125 °C. In the case of 1.42-mH load inductance, high current, and low energy, the estimated average junction tempera-

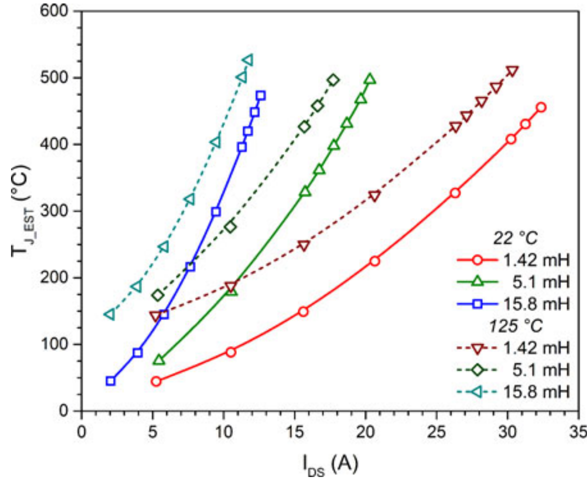


Fig. 13. Estimated average junction temperature for the CREE device with respect to I_{DS}. Estmations are shown for a case temperature of 22 °C, in solid lines, and at 125 °C, in dashed lines, for measurements obtained with load inductances of 1.42, 5.1, and 15.8 mH.

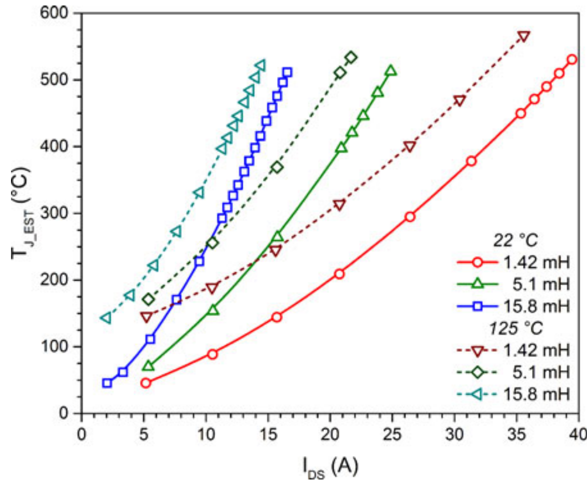


Fig. 14. Estimated average junction temperature for the ST device with respect to I_{DS}. Estmations are shown for a case temperature of 22 °C, in solid lines, and at 125 °C, in dashed lines, for measurements obtained with load inductances of 1.42, 5.1, and 15.8 mH.

ture, for 22 °C and 125 °C case temperatures, was 456 °C and 512 °C, respectively. When measured with the 15.8-mH load inductance, or low current and high energy, estimated junction temperature for both case temperatures is shown to be 474 °C and 527 °C, respectively. Averaging results from the aforementioned test cases, for all load inductances and case temperatures, yielded an average junction temperature of 494 ± 26 °C.

The estimated average junction temperature for the ST device is shown in Fig. 14 for load inductances of 1.42, 5.1, and 15.8 mH, at 22 °C and 125 °C. The aforesaid temperature estimation process was repeated for the ST device, which yielded results suggesting the ST device failed at slightly higher junction temperature. With a load inductance of 1.42 mH, at case temperatures of 22 °C and 125 °C, the estimated junction temperatures were 531 °C and 567 °C, respectively. With a 15.8-mH load inductance, the estimation was 511 °C and 527 °C,

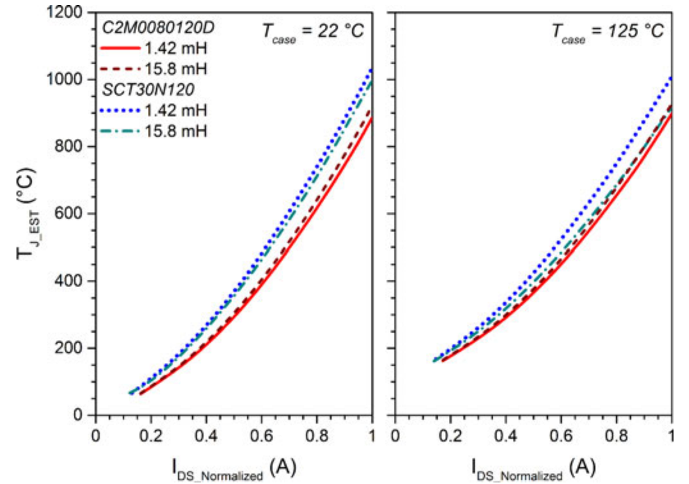


Fig. 15. Estimated peak junction temperature with respect to I_{DS} normalized. I_{DS} is normalized, in each case, to the peak I_{DS} measured at the maximum tolerable avalanche energy for each test inductor and case temperature.

respectively. Averaging results from the aforementioned test cases, for all load inductances and case temperatures, yielded an average junction temperature of 526 ± 22 °C.

Additionally, the peak junction temperature was estimated to further understand the correlation between junction temperature and failure mechanism. Peak junction temperature estimates were calculated in a similar manner as described for the average junction temperature; however, the average power dissipation was replaced with the peak power dissipation in (5). Results for the estimated peak junction temperature are shown in Fig. 15 with respect to I_{DS} normalized. The normalizing constant used for I_{DS} is the maximum I_{DS} value corresponding to the maximum tolerable avalanche energy; the normalization constant varies for each curve shown and values can be obtained from Figs. 7 and 8. These results are shown in Fig. 15 for 1.42 and 15.8 mH, at case temperatures of 22 °C and 125 °C. At a specific normalized I_{DS}, the temperature of the ST device is shown to be higher in most cases; the overall peak power dissipation in the ST device is higher than that of the CREE device and would likely generate higher junction temperatures. Estimated peak junction temperature for the CREE and ST devices, for all test conditions, yielded an average of 900 ± 48 °C and 978 ± 40 °C, respectively.

B. Impact of Avalanche Time

Assuming both devices are operating at equivalent peak power, the ratio of avalanche energy tolerance to avalanche time duration would be approximately equal for both devices; this relationship is shown in (6). Therefore, during UIS, the ST device benefits significantly from a lower V_{BR}, which increases the avalanche time duration as well as the avalanche energy tolerance due to higher I_{DS}. Avalanche time duration is shown, for all test cases, with respect to I_{DS} for both CREE and ST devices at case temperatures of 22 °C and 125 °C in Fig. 16; curves shown represent the maximum reliable single-pulse UIS operating condition with respect to I_{DS} and the resulting avalanche

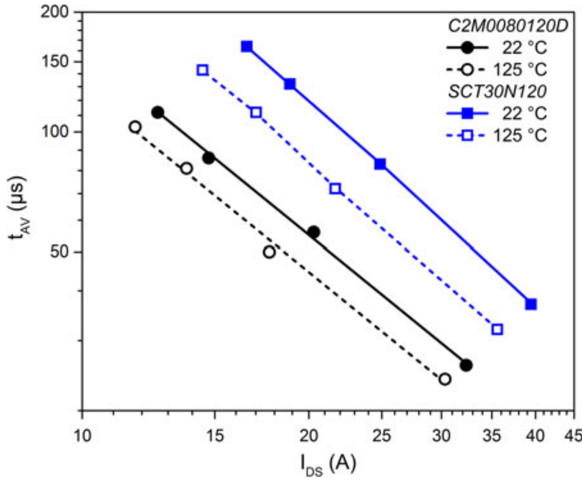


Fig. 16. Measured avalanche time for both CREE and ST devices. Both axes are represented in log scale and curves are shown for 22 °C, in solid lines, and at 125 °C, in dashes lines. Raw data points are shown with a respective best fit curve.

TABLE I
ON-STATE RESISTANCE AND BREAKDOWN VOLTAGE FOR CREE AND ST DEVICES

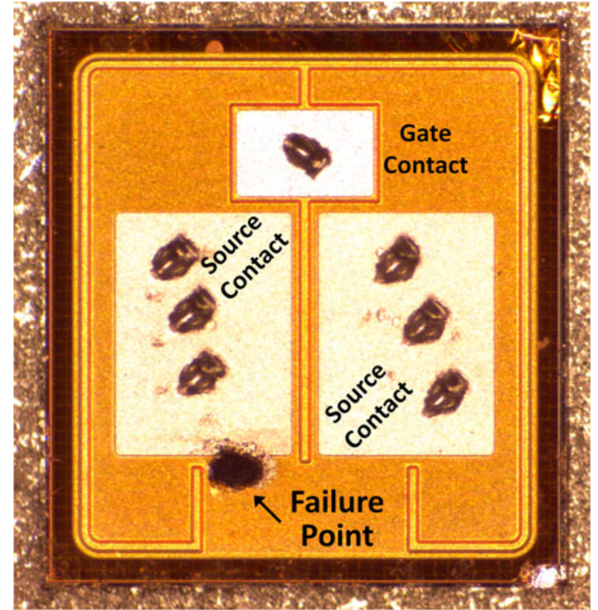
	C2M0080120D		SCT30N120	
Device Parameter	Mean	σ	Mean	σ
R_{ON} (I_{DS} = 20 A) [mΩ]	83.6	4.1	63.4	13.9
Breakdown (I_{DS} = 100 μA) [kV]	1.67	0.02	1.37	0.05

time. Both raw data and curve fit data are shown in Fig. 16

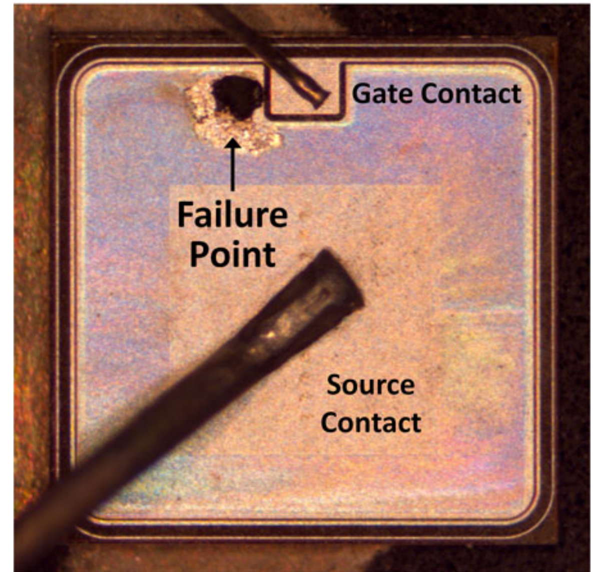
$$\frac{E_{\mathrm{ST}}}{t_{\mathrm{AV_ST}}} \approx \frac{E_{\mathrm{CREE}}}{t_{\mathrm{AV_CREE}}}. \tag{6}$$

To validate the breakdown voltage reduction of the ST device, a large sample set of devices were measured prior to UIS. The sample size is 45 for the CREE device and 35 for the ST device. ON-state resistance and breakdown voltages for CREE and ST devices are shown in Table I. Table I represents ST devices characterized in this study have a lower V_{BR} and ON-state resistance than that of the CREE devices, which leads to a higher avalanche energy tolerance.

Though the ON-state resistance of the ST devices characterized in this study were shown to be lower than the CREE devices, no direct correlation can be realized between lower ON-state resistance and avalanche tolerance. However, the lower ON-state resistance and breakdown voltage of the ST devices suggest that the effective N-drift region, shown in Fig. 12, may be more heavily doped in case of the ST device. Doping in the N-drift region strongly contributes to a devices' ON-state resistance and breakdown voltage. Breakdown voltage, however, is also strongly a function of the device geometry and fabrication methods utilized; therefore, these assumptions are made neglecting design variations that may exist between CREE and ST devices to affect these parameters.



(a)



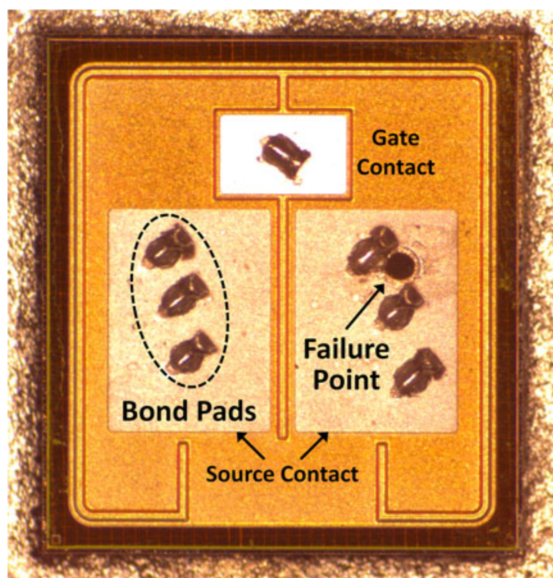
(b)

Fig. 17. (a) Decapsulated CREE device and (b) ST device. Images of devices failing during high avalanche current conditions using a 1.42-mH load inductor.

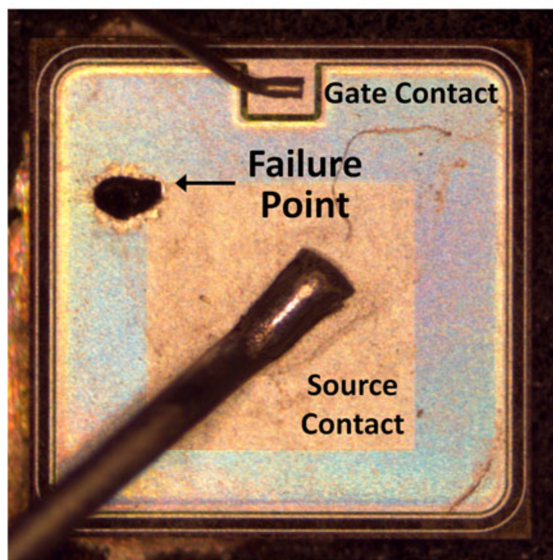
VIII. DEVICE FAILURE

Failed devices, post decapsulation, are shown in Figs. 17 and 18 for both CREE and ST devices. Die area of the CREE device was measured to be 0.104 cm^2, while the die area of the ST device was found to be 0.146 cm^2. Devices shown in Fig. 17 represent images of MOSFETs which failed during higher peak avalanche current operation, where the load inductor was 1.42 mH.

The CREE device, shown in Fig. 17(a), has slight damage to the right corners of the device which is thought to have been caused during brute force decapsulation of the device package; additionally, the solder joint of the bond wire is shown to be intact with the source contact metallization and the wire



(a)



(b)

Fig. 18. (a) Decapsulated CREE device and (b) ST device. Images of devices failing during high avalanche energy conditions using a 15.8-mH load inductor.

was detached at the joint upon package removal. Both devices, shown in Fig. 17, show failures that are highly localized in the vicinity of the source/gate metallization within the device. Devices shown in Fig. 18 represent devices which failed during longer avalanche times, where the load inductor is 15.8 mH. In both cases, failure is localized at the source terminal of the device. For the CREE device, shown in Fig. 18(a), the failure is in close proximity to one of the bond wires; for the ST device, shown in Fig. 18(b), the failure occurs at the left edge of the source metallization.

Observation of the failure sites shown in Figs. 17 and 18 reveals metallization failure; however, few observable differences between failure at high current and low energy, and low current and high energy can otherwise be inferred. Although failure locations are shown to vary, it is concluded that the mechanism of failure is equivalent for all cases and due to the formation of mesoplasma. Upon formation, mesoplasma would likely damage a smaller region of the device due to thermal runaway. Such an observable failure is shown in each case regardless of the test conditions leading to failure. In this research, a decoupled voltage source UIS circuit was utilized allowing the device failure to be observed without incurring additional device damage, which may be possible in a nondecoupled UIS circuit. Therefore, from these results it can be concluded that each device failed upon breaching a critical temperature limit for that specific device. The processing tolerances for each device plays some role in the variation of this critical temperature, but it has been shown that both devices failed with-in a small temperature window, which remained fairly consistent between CREE and ST devices.

IX. Conclusion

Single-pulse avalanche ruggedness was evaluated for commercial 1200-V SiC MOSFETs from two manufacturers: CREE and ST; devices were selected based on equivalent device specifications such as rated blocking voltage and ON-state resistance. A decoupled UIS circuit was utilized with load inductors of 1.42, 5.1, 10.5, and 15.8 mH to provide a full scope of test conditions at 22 °C and 125 °C. Each device was tested with increasing magnitude of avalanche current in order to creep up to the device's failure point. Using a 1.42-mH load inductor, the CREE device was measured up to $\mathrm{I_{DS}} = 32.3$ A resulting in an avalanche energy of 0.75 J, whereas the ST device was measured up to 1.1 J at 39.4 A. Additionally, with a 15.8-mH load inductor, the CREE device was measured up to 1.25 J with $I_{\mathrm{DS}} = 12.6$ A, while the ST device was measured up to 2 J with $I_{\mathrm{DS}} = 16.5$ A. Under both operating conditions, high avalanche current and longer avalanche time, the ST device was determined to be more tolerant during avalanche mode operation; however, the CREE device performed at the level specified within the manufacturer device datasheet.

Static device characteristics were measured prior to UIS measurement and additionally throughout UIS testing. Comparison of these results yielded no observable degradation for either CREE or ST devices tested in this research. The two common failure mechanisms during UIS, BJT latch-up and intrinsic temperature limit, were discussed; however, due to the inherent properties of wide-bandgap SiC semiconductor it is unlikely either mechanism is directly responsible for device failures presented. During UIS, high power dissipation in the DUT leads to extremely elevated junction temperatures, which would likely lead to the failure/degradation of metallization, dielectric and/or interface. Estimation of average junction temperature yielded results well below the intrinsic limit of SiC; however, estimation of peak junction temperature yielded results well above the failure limit of aluminum contacts often utilized for source/gate contact metallization. The peak junction temperature for the CREE device was estimated to be 900 ± 48 °C, while for the ST device it was estimated to be 978 ± 40 °C which is well beyond the 660 °C melting point of aluminum in both cases; though the

estimated average junction temperature was below aluminum's melting point, for both devices, localized heating could result in temperatures close to, or beyond, the estimated peak junction temperature. Decapsulation of the device package revealed the failure sites on the semiconductor die, which corroborates the aforementioned failure mechanism.

Acknowledgment

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References

[1] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. A. Hall, S. Allen, and S. Bhattacharya, "High switching performance of 1700-V, 50-A SiC Power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.

[2] B. N. Pushpakaran, A. Sarah Subburaj, S. B. Bayne, and J. Mookken, "Impact of silicon carbide semiconductor technology in photovoltaic energy system," *Renewable Sustain. Energy Rev.*, vol. 55, pp. 971–989, Mar. 2016.

[3] Q. Zhang, R. Callanan, M. K. Das, S. H. Ryu, A. K. Agarwal and J. W. Palmour, "SiC power devices for microgrids," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2889–2896, Dec. 2010.

[4] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002.

[5] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[6] J. Fabre, P. Ladoux, and M. Piton, "Characterization and Implementation of Dual-SiC MOSFET modules for future use in traction converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4079–4090, Aug. 2015.

[7] Z. Liang, P. Ning, and F. Wang, "Development of advanced all-SiC power modules," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2289–2295, May 2014.

[8] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability issues of SiC MOSFETs: A technology for high-temperature environments," in *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 418–426, Dec. 2010.

[9] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power module: A survey," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 1, pp. 80–97, Mar. 2016.

[10] S. Jahdi, O. Alatise, R. Bonyadi, P. Alexakis, C. A. Fisher, J. A. Gonzalez, L. Ran, and P. Mawby, "An analysis of the switching performance and robustness of power MOSFETs body diodes: A technology evaluation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2383–2394, May 2015.

[11] J. A. Schrock, B. N. Pushpakaran, A. V. Bilbao, W. B. Ray, E. A. Hirsch, M. D. Kelley, S. L. Holt, and S. B. Bayne, "Failure analysis of 1200-V/150-A SiC MOSFET under repetitive pulsed overcurrent conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1816–1821, Mar. 2016.

[12] J. A. Schrock, E. A. Hirsch, S. Lacouture, M. D. Kelley, A. V. Bilbao, W. B. Ray, S. B. Bayne, M. Giesselmann, H. O'Brien, and A. Ogunniyi, "Failure modes of 15-kV SiC SGTO thyristors during repetitive extreme pulsed overcurrent conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8058–8062, Dec. 2016.

[13] H. Sheng, Z. Chen, F. Wang, and A. Millner, "Investigation of 1.2 kV SiC MOSFET for high frequency high power applications," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, , Feb. 21–25, 2010 pp. 1572–1577.

[14] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Evaluation of switching performance of SiC Devices in PWM Inverter-Fed Induction Motor Drives," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5701–5711, Oct. 2015.

[15] J. O. Alatise, P. Alexakis, L. Ran, and P. Mawby, "The impact of temperature and switching rate on the dynamic characteristics of silicon carbide schottky barrier diodes and MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 163–171, Jan. 2015.

[16] N. H. Otake, T. M. Evans, T. Yoshida, M. Tsuruya, and K. Nakahara, "Three-phase LLC series resonant DC/DC converter using SiC MOSFETs to realize high-voltage and high-frequency operation," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2103–2110, Apr. 2016.

[17] H. Li, S. Munk-Nielsen, X. Wang, R. Maheshwari, S. Beczkowski, C. Uhrenfeldt, and W. T. Franke, "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[18] J. Fabre and P. Ladoux, "Parallel connection of 1200-V/100-A SiC-MOSFET half-bridge modules," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1669–1676, Mar./Apr. 2016.

[19] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett, and B. J. Blalock, "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, Feb. 2016.

[20] T. T. Nguyen, A. Ahmed, T. V. Thang, and J. H. Park, "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015.

[21] D. Peftitsis and J. Rabkowski, "Gate and base drivers for silicon carbide power transistors: An overview," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7194–7213, Oct. 2016.

[22] D. Schleisser, D. Ahlers, M. Eicher, and M. Purschel, "Repetitive avalanche of automotive MOSFETs," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2–6, 2013, pp. 1–7.

[23] M. Nymand and M. A. E. Andersen, "High-efficiency isolated boost DC–DC converter for high-power low-voltage fuel-cell applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 505–514, Feb. 2010.

[24] C. Bodeker and N. Kaminski, "Investigation of an overvoltage protection for fast switching silicon carbide transistors," *IET Power Electron.*, vol. 8, no. 12, pp. 2336–2342, Dec. 2015.

[25] J. Hu, O. Alatise, J. A. O. González, R. Bonyadi, L. Ran, and P. A. Mawby, "The effect of electrothermal nonuniformities on parallel connected SiC power devices under unclamped and clamped inductive switching," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4526–4535, Jun. 2016.

[26] L. Yang, A. Fayyaz, and A. Castellazzi, "Characterization of high-voltage SiC MOSFETs under UIS avalanche stress," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drives*, Apr. 8–10, 2014, pp. 1–5.

[27] P. Alexakis O. Alatise, J. Hu, S. Jahdi, J. O. Gonzalez, L. Ran, and P. A. Mawby, "Analysis of power device failure under avalanche mode Conduction," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, Jun. 1–5, 2015, pp. 1833–1839.

[28] C. Abbate, G. Busatto, and F. Iannuzzo, "Unclamped repetitive stress on 1200 V normally-off SiC JFETs," *Microelectron. Rel.*, vol. 52, nos. 9/10, pp. 2420–2425, Sep./Oct. 2012.

[29] B. N. Pushpakaran, M. Hinojosa, S. B. Bayne, V. Veliadis, D. Urciuoli, N. El-Hinnawy, P. Borodulin, S. Gupta, and C. Scozzie, "High temperature unclamped inductive switching mode evaluation of SiC JFET," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 526–528, Apr. 2013.

[30] B. N. Pushpakaran, M. Hinojosa, S. B. Bayne, V. Veliadis, D. Urciuoli, N. El-Hinnawy, P. Borodulin, S. Gupta, and C. Scozzie, "Evaluation of SiC JFET performance during repetitive pulsed switching into an unclamped inductive load," *IEEE Trans. Plasma Sci.*, vol. 42, no. 10, pp. 2968–2973, Oct. 2014.

[31] CREE Inc., "Silicon carbide power MOSFET C2MTM MOSFET technology," C2M0080120D Datasheet, Rev. C, Oct. 2015.

[32] STMicroelectronics, "Silicon carbide power MOSFET," SCT30N120 datasheet, Rev. 9 , Feb. 2015.

[33] S. Potbhare, N. Goldsman, A. Akturk, and A. Lelis, "Effect of random surface charge distribution on transport in 4H-SiC MOSFETs," in *Proc. Int. Semicond. Device Res. Symp.*, College Park, MD, USA, 2009, pp. 1–2.

[34] V. Pala, B. Hull, J. Richmond, P. Butler, S. Allen, and J. Palmour, "Methodology to qualify silicon carbide MOSFETs for single shot avalanche events," in *Proc. 3rd IEEE Workshop Wide Bandgap Power Devices Appl.*, Blacksburg, VA, USA, 2015, pp. 56–59.

[35] K. Banerjee, S. Rzepka, A. Amerasekera, N. Cheung, and C. Hu, "Thermal analysis of the fusion limits of metal interconnect under short duration current pulses," in *Proc. IEEE Int. Integr. Rel. Workshop*, Lake Tahoe, CA, USA, 1996, pp. 98–102.

[36] E. B. Hakim, "Hot spot mesoplasma formation in silicon planar transistors," in *Proc. 4th Annu. Symp. Phys. Failure Electron.*, Chicago, IL, USA, 1965, pp. 609–619.

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