PV-Module-Integrated AC Inverters (AC Modules) With Subpanel MPP Tracking

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***Abstract*—For small scale roof-top systems, there is a trend towards module-integrated electronics. Module integrated ac inverters (ac modules) connect each photovoltaic (PV) module separately to the single-phase grid. They feature not only increased yield due to module-level maximum power point (MPP) tracking, but also further advantages such as reduced installation cost. This work investigates the concept of subpanel-level MPP tracking for ac modules, which allows us to increase yield thanks to reduced mismatching losses. Topology concepts to realize such a converter are systematically investigated and categorized. A topology comparison identifies two promising system concepts: first a single-stage converter with a three-port power balancer and second a two-stage topology with three paralleled dc–dc converters and a pulse width modulation full bridge. The later features the advantage of a small power-decoupling capacitor and is therefore further investigated. A model-based optimization of the investigated multi-input ac module is performed, applying high performing Gallium Nitride (GaN) devices and nanocrystalline core materials to increase efficiency. The built prototype confirms the accuracy of the model-based optimization. The performed efficiency study reveals an achievable efficiency of $\eta_{EU} = 94.5\%$. In order to compete with single-input ac modules, achieving typically an efficiency of 95.5%, the efficiency of multi-input ac modules must improve beyond the level achieved with the investigated two-stage ac-module topology. Given this result, the alternative system concept with a three-port power balancer in combination with a single-stage converter seems to be more promising, as it is conceptually similar to the high efficient single-input ac modules and may achieve the same high efficiency.**

***Index Terms*—AC module, distributed MPP, PV, subpanel.**

I. Introduction

TYPICAL grid-connected PV systems consist of several PV modules and one or more PV converters. Such a system can be realized in different ways and the following basic system concepts can be distinguished [1]: centralized converters, string- and multistring converters, PV module integrated dc–dc converters, and ac modules. Whereas large scale commercial PVsystems are still designed using centralized or string converters, there is a trend towards module-integrated electronics for small scale roof-top systems. For these systems not only increased yield due to module-level MPP tracking, but also additional advantages such as reduced installation cost and safety issues become equally important [2], [3].

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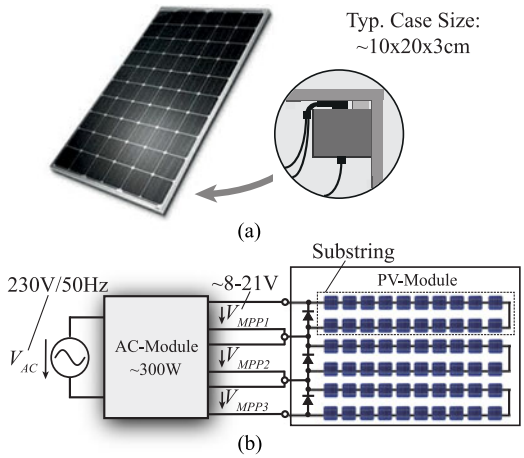

Fig. 1. AC Module. (a) Mounting. (b) Schematic.

Module integrated ac converters connect each PV module separately to the single-phase grid, providing an autonomous dc–ac converter for each PV module as illustrated in Fig. 1. The converters, designed with an appropriate low-profile housing, are mounted directly on the back side of each PV module.

Compared to string converters, ac modules feature various benefits such as full modularity of the PV system, module-level MPP tracking, low PV-system installation effort, easy monitoring, and failure detection of the PV system [3].

Unfortunately, these benefits do not come for free. AC-module converters exhibit inherent drawbacks compared to string converters. For the design of an ac module, which can compete against string and multistring converters, the following challenges persist.

1) Forming a functional unit with the PV module, ac modules need a lifetime of 20 years under harsh environmental operating conditions.
2) AC modules must step-up the voltage of a single PV module to the grid level.
3) AC modules must decouple the pulsating power delivered to the single-phase grid from the PV-side input.
4) Due to the higher number of converters, ac module PV systems have a big overhead of control- and auxiliary electronics.

For these reasons the design of a competitive ac module is very challenging. A multitude of topologies are proposed in literature aiming for an optimal tradeoff of the mentioned issues [1], [4], [5]. Currently, commercial ac modules achieve efficiencies up

TABLE I
MULTI-INPUT AC-MODULE SYSTEM SPECIFICATIONS

PV Interface	Power	$P_{\mathrm{Nom}} = 300$ W
	MPP Tracking	3 × MPPT on substring level
	MPPT Range	$V_{\mathrm{PV,MPP}} = 3 \times 8.5$–21 V
Grid Interface	Line Voltage	$V_{\mathrm{line}} = 230$ Vrms
	Line Frequency	$f_{\mathrm{line}} = 50$ Hz
	Line Current	THD max = 4%
	Reactive Power Support	Up to power factor 0.9
General	Operable Temperature	$-40°$C to $+85°$C
	Lifetime	25 years
	Volume and Dimension	PCB-size max: 160 × 100 mm
		PCB-height max: 30 mm
		Component-height max: 25 mm
Safety	Grounding	Equipment ground
	Standards	Same as single MPPT ac modules

to $\eta_{\mathrm{EU}} = 95.5\%$ and peak efficiencies slightly above 96%. The record efficiency for a commercial ac module is achieved for the North American grid and is claimed to be $\eta_{\mathrm{CEC}} = 97\%$ (Enphase S280).

Given the efficiency of transformerless string inverters in the range of 98% to 99%, ac-module technology must further catch up to the competing string converters regarding efficiency and costs. An alternative approach to make ac modules more competitive is to strengthen their advantages concerning energy yield. Even with module-level MPP tracking mismatch losses still persist on submodule level under partial shading of the PV module. Taking the MPP tracking from module to submodule level can eliminate parts of these mismatch losses. The bypass diodes contained in a junction box on the back side of the module, could be replaced by an ac module with three inputs, allowing for MPP tracking on substring level [see Fig. 1(b)]. The potential gain in annual energy yield for substring MPP tracking is estimated to be 1% for moderate and 2% for heavy shading conditions [6]. The instantaneous energy yield increase can reach 20% [7].

To improve the ac-module technology, the concept of substring-level MPP tracking for ac modules recently emerged. The works in [8] and [9] propose differential power-processing stages (DPP) as an add-on to conventional ac modules, serving as power balancers. The work in [10] deals with a specific two-input flyback topology, to achieve substring MPP tracking for a two-string PV module.

The aim of this work is to thoroughly categorize the topologies for multi-input ac modules and to identify the most promising system concepts based on a systematic topology comparison. The comparison is performed with comprehensive designs of multi-input ac modules, which are based on analytic models and measurement results for the switching losses. The system specification of the considered ac module is listed in Table I. The remainder of this paper is structured as follows. Based on a review of conventional single-input ac modules in Section II, multi-input ac-module topologies are derived in Section III. A topology comparison in Section IV helps to identify the most promising multi-input ac-module approach, for which in Section V the efficiency versus volume pareto front is calculated by model-based optimization. In addition, a prototype is presented for verifying the efficiency values.

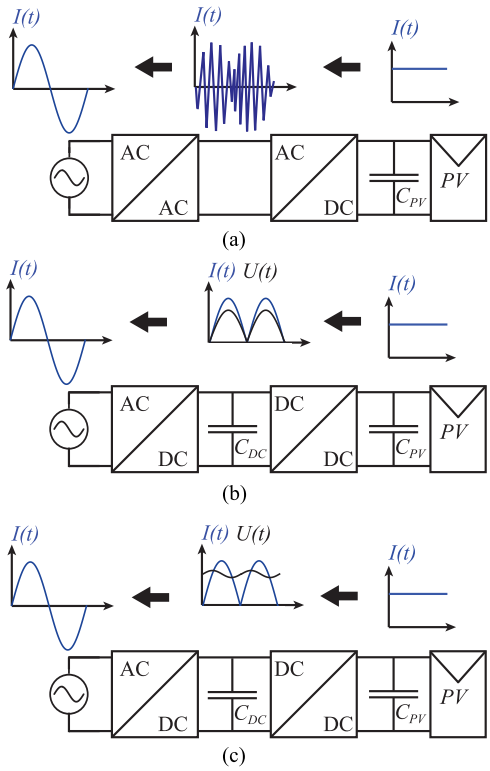

Fig. 2. AC-module topology categorization [11], [4]. (a) HF-link inverter. (b) Pseudo dc-link inverter. (c) DC-link inverter.

Finally, Section VI summarises the main findings and gives an outlook for future research on multi-input ac modules.

II. CONVENTIONAL SINGLE-INPUT AC-MODULE TOPOLOGIES

In literature, a considerable number of ac-module topologies with single MPP tracking are proposed. In order to allow an overview of the different system concepts the multitude of topologies must be structured. Reviews on module integrated PV converters [11], [4] identified the following three distinct types of inverters: the high-frequency-link (HF) inverter, the pseudo dc-link inverter, and the dc-link inverter. The categorization is based on how the dc input at the PV side is linked to the ac output.

1) *HF-Link Inverter:* As shown in Fig. 2(a), the direct current from the PV-input is transformed into a HF modulated current by a dc–ac stage, operating at HF. The following ac–ac stage directly converts this HF current into a low-frequency sinusoidal grid current.
2) *Pseudo DC-Link Inverter:* The pseudo dc-link inverter is shown in Fig. 2(b). The current from the PV input is processed by a dc–dc stage operating at HF. The dc–dc stage is modulated to output a rectified sinusoidal current to the intermediate pseudo dc link. The voltage of the pseudo dc link is pulsating with double line frequency and has the shape of a rectified sinus. The following dc–ac stage switches at line frequency and unfolds the rectified current and voltage.
3) *DC-Link Inverter:* The dc-link inverter, shown in Fig. 2(c), has an intermediate dc-link. The dc–dc stage is controlled to charge the dc link with a constant current from the PV

TABLE II
SPECIFICATIONS AND ASSUMPTIONS FOR THE TOPOLOGY COMPARISON BASED ON THE MULTI-INPUT AC-MODULE CONVERTER SPECIFICATION IN TABLE I

Specifications	
Power	$P_{\mathrm{Nom}} = 300$ W
PV Input Range	$3 \times$ MPPT: $3 \times V_{\mathrm{PV,in}} = 8.5 - 21$ V
	$1 \times$ MPPT: $V_{\mathrm{PV,in}} = 25.5 - 63$ V
Line Voltage	V_{line}: 230 Vrms/50 Hz
Line Current Ripple	$\hat{I}_{f,\mathrm{switch}} \leq 0.05 \cdot \hat{I}_{1,p_{\mathrm{nom}}}$
Assumptions	
Switching Frequency	DC–AC inverter $f_{s,\mathrm{AC}} = 20$ kHz
	DC–DC converter $f_{s,\mathrm{DC}} = 40$ kHz
	Variable $f_{s,\mathrm{avg}} = f_{s,\mathrm{DC}}$ resp. $f_{s,\mathrm{AC}}$
DC–DC Conv. current	For CCM $i\Delta_{p,p} \leq 0.2 \cdot I_{\mathrm{DC,rms}}$
Stand-By Reactive Power	$Q_{\mathrm{noload,max}} = 8$ VA (0.03 P_{nom})
Flyback	Low primary switch voltage stress [21]
Transformer Ratio	$V_{\mathrm{prim,min}} \cdot \frac{N_{\mathrm{sec}}}{N_{\mathrm{prim}}} \simeq 0.3 \cdot V_{\mathrm{sec,max}}$
Power Decoupling	$\Delta_{V_{\mathrm{dc,pp}}} = 0.25 V_{\mathrm{dc,avg}}$ [37]

input side. The dc–ac stage converts the dc current into a line frequency ac current. The intermediate dc link is controlled to a constant average value, whereas a double-line frequency ripple of typically 25% is still tolerable. Both stages operate at HF.

Another characteristic to categorize ac modules is the applied power decoupling technique. The power delivered to a single-phase grid is pulsating with double-line frequency. To match the dc-source characteristic of the PV module to the ac grid, the ac module must provide power decoupling by temporarily buffering energy in a decoupling capacitor. The power decoupling techniques can be distinguished regarding the location of the decoupling capacitor [5]:

1) at the PV side,
2) at the ac side,
3) at the dc link of a two-stage topology.

Further, power decoupling can be distinguished depending on the power flow to/from the capacitor. For passive decoupling the capacitor is directly connected and acts as a passive filter. Active decoupling is achieved by an active circuit controlling the power flow to/from the decoupling capacitor, also referred to as ripple port. The required capacitor size depends on the applied decoupling technique and voltage range. The largest decoupling capacitor is needed for passive decoupling at the PV side, because the PV-side voltage must essentially be constant for effective MPP tracking.

Among the multitude of ac modules proposed in literature a selection of single MPP tracking topologies is analyzed in this work, focusing on the topologies with the highest reported efficiency and the most promising system concepts. The considered single MPP tracking topologies are listed in Table III and will be evaluated by means of a topology comparison in Section IV-A.

III. MULTI-INPUT AC-MODULE TOPOLOGY DERIVATION

The substring MPP-tracking concepts proposed in the literature as well as commercially available products are based on dc–dc module integrated converters [7], [12], [13], [2], [8], [9].

TABLE III
SINGLE MPP-TRACKING AC-MODULE TOPOLOGIES: OVERVIEW OF THE COMPARED TOPOLOGIES

Topologies			ID:
HF Link	*LC*-Resonant and Cyclo	[24]	*I*
	Ripple-Port Push-pull	[38]	*II*
Pseudo DC Link	Flyback in BCM	[21], [39]	*III*
	$3 \times$ Interleaved Resonant Flyback	[19], [20]	*IV*
	Ripple-Port Flyback	[40], [5]	*V*
	Ripple-Port Push-pull	[41]	*VI*
DC Link	Resonant Flyback	[42]	*VII*
	Clamped Flyback	[43]	*VIII*
	Isolated Boost	[44]	*IX*
	Coupled Inductor Boost	[45]	*X*
	LC Resonant Boost	[46]	*XI*

The only exception [10], is for a two-string PV module, whereas standard mono- and multicrystalline silicon PV modules are generally grouped in three substrings.

One approach to realize a multi-input ac module is of course to combine a conventional single-input ac module with a dc–dc stage providing substring MPP tracking as proposed by Qin *et al.* [9]. In the following, the various approaches to realize such a converter are categorized and systematically compared.

A. Categorization of Realisation Possibilities

The ac-module converter topologies with three MPP-tracking inputs on substring level ($3 \times$ MPPT) are categorized by the realization of the galvanic isolation. Even though galvanic isolation is not required by the safety standards, an isolated converter topology is the most efficient way to cope with the high voltage step-up ratio of ac modules [14]. The galvanic isolation can be either realized by three two-port transformers, one multiport transformer or one two-port transformer with a nonisolated multiport stage on the PV-input side. This allows to distinguish the three types of topologies shown in Fig. 3. The galvanic isolation is in any case realized with a HF transformer, line transformers are not considered because of volume limits. Within each of these three categories, the topologies can be distinguished in the same manner as for the conventional single-input ac modules (see Section II).

1) $3\times$ *2-Port Transformer:* This type of multi-input converter can be realized in two ways. First, three single-input ac-module topologies are applied and connected either in parallel or in series. Second, a dc-link topology with three paralleled or serial dc–dc converters and one dc–ac inverter is applied.
2) $1\times$ *Multiport Transformer:* A multiport transformer can be combined with all system concepts: dc link, pseudo dc link, and HF link. The realization with a dc link is a part-count reduced version of the topology applying three paralleled dc–dc converters. The multiport transformer topologies would achieve reduced semiconductor part-count, but come along with very high design and control complexity. To find appropriate modulation and control schemes would require substantial effort.

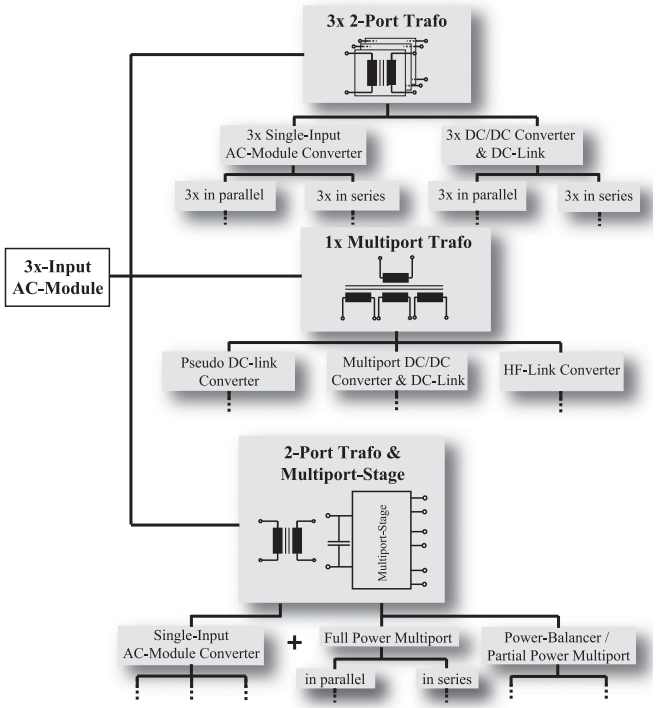

Fig. 3. Overview of the realisation possibilities for multi-input ac modules with 3×MPPT on substring-level.

3) 1× *2-Port Transformer and Multiport Stage:* A non-isolated multiport stage is applied, which features MPP tracking at each of its three inputs and one single dc output. The multiport stage is combined with a conventional single-input ac-module topology. Two different system concepts can be distinguished based on the functionality of the dc–dc multiport stage. First, the dc–dc multiport can be designed as pure power balancer with an output voltage equal to the sum of all substring voltages. The multiport only processes the unbalanced share of the panel power. This concept is also referred to as DPP, [9]. Second, the dc–dc multiport can be implemented as buck-boost converters, which process the full panel power and can be controlled to a set output voltage. An overview of PV multiport dc–dc converters and power-balancers is given in [15], [7], [12], and [16].

B. Feasible Topology Candidates

Compared to a single-input ac-module converter with MPP tracking on PV-module level, a multi-input ac module with MPP tracking on substring level comes along with the following drawbacks.

1) *Increased Part Count:* Three separate inputs demand for more active and passive components, such as semiconductors, gate drivers, auxiliary supplies, and magnetic components. This causes not only increased costs, but also leads to reduced reliability and reduced low-load efficiency due to increased quiescent supply currents.
2) *Higher Voltage Step-Up Ratio:* The voltage range of the substring MPPT inputs is one third of the PV module voltage range, requiring a three times higher voltage step-up ratio. This has a negative impact on the achievable converter efficiency.

When selecting a topology for a multi-input ac module it must therefore be taken care, that the advantage of substring MPPT is not overcompensated by the above-mentioned system drawbacks. For the topology selection, this has the consequence that only topologies with a reasonable amount of semiconductors are considered. An upper limit of 16 switches is set, which corresponds to twice the amount of most of the single-input ac-module topologies.

This restricts the feasible topology candidates, which are in the following derived:

1) 3× *2-Port Transformer*
   a) 3× *Single-Input AC Modules:* The reviewed HF-link topologies require to many switches. Pseudo dc-link inverters are a viable option, because one common unfolder can be applied for the three paralleled inverters. For power decoupling, passive PV-side decoupling must be applied. Active decoupling would require too many switches.
   b) 3× *DC–DC converter and DC-link:* A dc-link topology with dc-link power decoupling, a pulse width modulation (PWM) full bridge and three paralleled or serial dc–dc converters is a feasible topology, as long as the dc–dc stages are realized with less than four switches.
2) 1× *Multiport Transformer*
   a) *HF-link & Pseudo DC-link Converters:* HF-link and pseudo dc-link topologies can indeed be realized with the allowed number of switches, though the four-port operation brings along very high design and control complexity, such that they are not considered in this work.
   b) *Multiport DC–DC and DC-Link:* There is only one dc-link topology, which does not require too many switches: a PWM full bridge and a four-port flyback converter. Power decoupling is achieved at the dc link.
3) 1× *2-Port Transformer and Multiport Stage:*
   a) *Full Power Multiport:* A full power buck-boost multiport requires six switches and could be combined with most single-input ac-module topologies. Though in combination with a HF-link or pseudo dc-link ac-module converter, the full power multiport stage is found to cause 20%–40% of the total system losses (see Refs. [17] and [18]) and is therefore not further considered in this work.
   b) *Power-Balancer Multiport (DPP):* A three-port power balancer is typically realized with four switches and can be combined with any type of single-input ac-module topology. Depending on the number of switches of the chosen multiport and ac-module topology, the power can be decoupled either with active power decoupling or with passive PV-side decoupling.

Based on the restricted set of topologies, a set of five topology candidates is considered and evaluated in this work, which contains the most promising topology candidates, identified

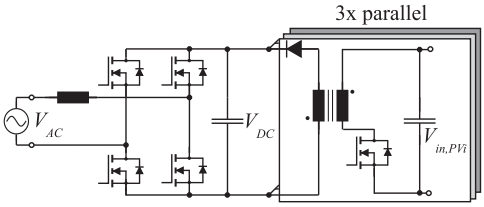

Fig. 4. $3\times$ 2-Port transformer topology: Three paralleled flyback converters and a full bridge inverter either operated as pseudo-dc link topology with unfolder (*Top.-ID: A*) or as dc-link topology with a PWM full bridge (*Top.-ID: B*).

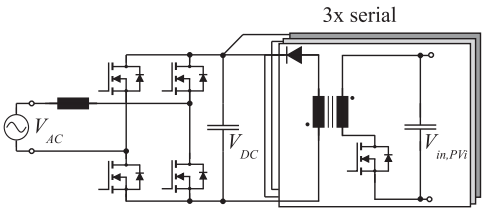

Fig. 5. $3 \times$ 2-Port transformer topology: Three serial flyback dc–dc converters and a PWM full bridge inverter (*Top.-ID: C*).

based on the review and comparison of single-input ac modules. The following sections describe the topology candidates more in detail.

1) Pseudo DC-Link With Parallel DC–DC Flyback (Top.-ID: A): The topology is shown in Fig. 4. The three paralleled flyback dc–dc converters are operated in boundary conduction mode (BCM) and output a rectified sine-waveform current. A common unfolding bridge folds the current waveforms to the correct line voltage polarity. Except the lower input voltage, the paralleled stages are operated exactly as the single-input ac module converter described in [19] and [20].

2) Parallel Flyback DC–DC & PWM Full Bridge (Top. -ID: B): Fig. 4 shows the topology with the flyback converters and the full bridge. It consists of three paralleled conventional flyback dc–dc converters operated in BCM [21]. Each flyback converter operates autonomously, performs its own MPP tracking and delivers the dc power from its PV substring into the dc link. The dc link serves as energy buffer for power decoupling and is controlled according to the control scheme proposed in [22]. A standard PWM full bridge inverter [23] with an line-inductor and single-stage LC-type differential mode filter (LCL) line filter feeds the PV power into the grid.

3) Serial Flyback DC–DC & PWM Full Bridge (Top.-ID: C): The topology is shown in Fig. 5. Three conventional flyback dc–dc converters in BCM [21], are put in series to feed into a dc link, as shown in Fig. 5. Again the dc link serves as energy-buffer for power decoupling and a PWM full bridge inverter with an LCL line filter feeds the PV power into the grid [22], [23].

4) Multiport Sequential Flyback DC–DC & PWM Full Bridge (Top.-ID: D): A four-port flyback converter is used to deliver the power from the PV substrings to the dc link. The flyback converter operates in DCM (see [21]) and the three input ports are operated sequentially one after another. The dc link serves as an energy buffer for power decoupling and a PWM full bridge inverter with an LCL line filter feeds the PV power into the grid [22], [23].

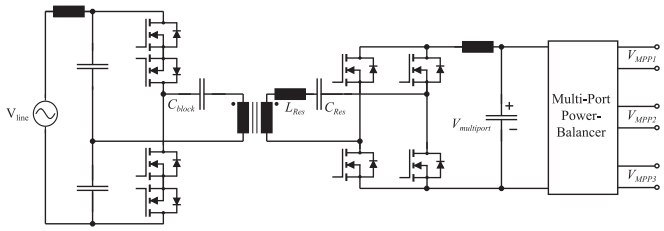

Fig. 6. $1\times$ 2-Port transformer topology: Buck boost based power-balancer multiport [9], [30] and an HF-link *LC*-resonant cyclo-converter [24], [25] (*Top.-ID: E*).

5) Power-Balancer Multiport & HF-Link type differential mode filter-Resonant Converter (Top.-ID: E): The topology is shown in Fig. 6. A power-balancer circuit is combined with the single-input HF-link LC-resonant converter described in [24] and [25]. The HF-link *LC*-resonant converter consists of a series resonant *LC* converter on the dc side combined with a cyclo converter on the ac side. The dc side is operated under variable switching frequency and phase-shift control achieving zero voltage switching (ZVS) on the dc- and ac-side. The power balancer acts as DPP stage, processing only the unbalanced share of the power. The principle of power balancers is well known from charge equalization in battery cells. A detailed discussion of these circuits is out of scope for this work. For a detailed investigation of such circuits refer to [7], [12], [16], [26], [27], [28]. The power balancer could for instance be realized as switched capacitor converters [29], [13] or as isolated bidirectional flyback converters [8]. This work considers a power balancer based on buck-boost converters as proposed in [9] and [30].

IV. AC-Module Topology Comparison

To evaluate the performance of the proposed multi-input ac-module converter topologies, a systematic topology comparison is performed, considering not only the proposed multi-input topologies but also the conventional single-input ac-module topologies. This allows us to analyze the conceptual differences between single- and multi-input ac modules and identify the most promising multi-input ac-module topologies.

The comparison is performed using six different bench marking factors based on electrical design only, in the same manner as for the topology comparisons in [31] and [32]. The semiconductor bench marking factors rely on the method in [33] (see Section III-B). The bench marking factors are as follows:

1) *Total Installed Semiconductor Power $\boldsymbol{VA}_{\mathrm{Tot}}$:* The total installed semiconductor power is an indicator for semiconductor costs. The product of the rms-current $I_{i,\mathrm{rms}}$ and the blocking voltage $\hat{V}_{\mathrm{block}}$ is summed up over all applied semiconductors N:

$$VA_{\mathrm{Tot}} = \sum_{i=1}^{N} \hat{V}_{\mathrm{block}} \cdot I_{i,\mathrm{rms}}. \tag{1}$$

2) *Total Stored Capacitive Energy $\boldsymbol{E}_{\mathbf{Cap,Tot}}$:* The capacitive energy indicates the volume and cost of the installed capacitors. The maximal voltage of each capacitor of the converter is taken into account to sum up the energy over all applied capacitors N:

$$E_{\mathrm{Cap,Tot}} = \sum_{i=1}^{N} \frac{1}{2} \cdot C_i \cdot \hat{V}_{Ci}^2. \tag{2}$$

3) *Total Stored Inductive Energy $\boldsymbol{E}_{\mathrm{Ind,Tot}}$:* The total stored inductive energy reveals the volume and cost of the applied inductors. For all inductors and flyback transformers, the maximal current flowing through the respective component is considered. The total magnetic energy is calculated by summing over all applied inductors and flyback transformers N:

$$E_{\mathrm{Ind,Tot}} = \sum_{i=1}^{N} \frac{1}{2} \cdot L_i \cdot \hat{I}_{\mathrm{Li}}^2. \tag{3}$$

4) *Transformer Area-Product $\boldsymbol{A}_{\mathrm{C-W,Trafo}}$:* To get an idea of the size of the applied transformers, the transformer area product is used as bench marking factor. The winding area is calculated assuming a current density of $S_{\mathrm{rms}} = 5$ A/mm^2, where M is the number of windings, n_i the turns number of each winding, and $I_{\mathrm{rms},i}$ the rms current of the corresponding winding

$$A_W = \frac{1}{S_{\mathrm{rms}}} \sum_{i=1}^{M} n_i \cdot I_{\mathrm{rms},i}. \tag{4}$$

The core area is calculated with the maximal value of the winding voltage integral $\int V_{\mathrm{wind}}(t)dt$ and assuming a maximal flux density of $B_s = 250$ mT (typical value for ferrite, accounting 50% margin)

$$A_C = \frac{\max(\int V_{\mathrm{wind}}(t)dt)}{B_s}. \tag{5}$$

The transformer area product is given by

$$A_{C-W,\mathrm{Trafo}} = A_C \cdot A_W. \tag{6}$$

5) *Conduction Loss Factor $\boldsymbol{\Xi}_{\mathrm{Cond}}$:* The semiconductor conduction losses are approximated with the normalized conduction loss factor Ξ_{Cond} defined in [33] (see Section III-B, Formula 3.2.6)

$$\Xi_{\mathrm{Cond}} = \sum_{i=1}^{N} \left(\frac{I_{\mathrm{rms},i}}{I_{\mathrm{line,nom}}} \right)^2 \cdot \left(\frac{\hat{V}_i}{V_{\mathrm{line,nom}}} \right)^{\beta}. \tag{7}$$

where N is the number of applied semiconductors. $I_{\mathrm{rms},i}$ and $\hat{V}_i$ denote the rms-current and the blocking voltage of each semiconductor. These values are normalized to the ac-side nominal voltage $V_{\mathrm{line,nom}}$ and current $I_{\mathrm{line,nom}}$. The semiconductor technology specific factor β accounts for the fact, that conduction losses increase with increased voltage rating.

6) *Switching Loss Factor $\boldsymbol{\Pi}_{\mathrm{Switch}}$:* The semiconductor switching losses are considered by the normalized switching loss factor Π_{Switch} defined in [33] (see Section III-B). First, the currents and voltages at commutation ($I_{\mathrm{on}}(t_k)$, $V_{\mathrm{on}}(t_k)$, $I_{\mathrm{off}}(t_k)$ and $V_{\mathrm{off}}(t_k)$) are used to calculate turn-ON and turn-OFFenergies for a specific semiconductor, which are again normalized to nominal ac-side voltage and current. For dc–ac conversion the switching energies of a given switching instant t_k vary and are therefore summed up for all switching cycles over a line period

$$\Pi_{\mathrm{on}} = \sum_{t_k=0}^{T_{\mathrm{line}}} \frac{I_{\mathrm{on},i}(t_k)}{I_{\mathrm{line,nom}}} \cdot \frac{V_{i,\mathrm{on}}(t_k)}{V_{\mathrm{line,nom}}} \tag{8}$$

$$\Pi_{\mathrm{off}} = \sum_{t_k=0}^{T_{\mathrm{line}}} \frac{I_{\mathrm{off},i}(t_k)}{I_{\mathrm{line,nom}}} \cdot \frac{V_{i,\mathrm{off}}(t_k)}{V_{\mathrm{line,nom}}}. \tag{9}$$

Second, the turn-OFFand turn-ON energies are scaled by a semiconductor technology specific factor α, which takes into account the dependence of the switching losses on the devices voltage rating. The bench marking factor is calculated by summing up the energies over all applied semiconductors N

$$\Pi_{\mathrm{Switch}} = \sum_{i=1}^{N} (\Pi_{i,\mathrm{on}} + \Pi_{i,\mathrm{off}}) \cdot \left(\frac{\hat{V}_i(t_k)}{V_{\mathrm{line,nom}}} \right)^{\alpha}. \tag{10}$$

The following assumptions are made for the design and comparison of the ac module topologies.

1) *Inductor Design for DCM:* In the case of DCM operation the inductance value is calculated, such that the converter reaches BCM at the critical operating point.
2) *Inductor Design for Continuous Conduction Mode (CCM):* When the converter operates in CCM, the allowed output current ripple is specified as percentage of the current at nominal power, I_{Nom}, being 5% for dc–ac inverters and 20% for dc–dc converters.
3) *LC Line Filter:* In case of a dc–ac inverter operating in BCM, an *LC* filter is added, to attenuate the line current ripple at switching frequency to 5% of I_{Nom}. The reactive power generated by the *LC* filter shall not surpass the limit $Q_{\mathrm{NoLoad,max}} = 8$ VA.
4) *Selection of Semiconductor Types:* All diodes are assumed to be SiC Shottky diodes. Switches are assumed to be MOSFETs, if they are operated under ZVS. Otherwise the switches are selected to be IGBTs.
5) *Model of MOSFETs for Rating Factors:* The MOSFETs are assumed to be of type Super Junction (SJ) MOSFETs, if their blocking voltage is above 250 V, and of type GD MOSFET, for blocking voltages below 250 V. Semiconductor factors α and β are determined from [34].
6) *Model of IGBTs for Rating Factors:* The IGBT semiconductor factors are derived from [31] and [35].
7) *Model of Diodes for Rating Factors:* The characteristics of SiC diodes is read out from [36].

The assumptions are summarized in Table II together with the system specification used for the comparison.

TABLE IV
MULTI-INPUT AC-MODULE TOPOLOGIES: OVERVIEW OF THE TOPOLOGY CANDIDATES

	Topologies		ID:
Pseudo DC Link	Parallel DC–DC Flyback	Fig. 4	*A*
DC Link	Parallel Flyback DC–DC	Fig. 4	*B*
	Serial Flyback DC–DC	Fig. 5	*C*
	Multiport sequential Flyback DC–DC		*D*
HF Link	Power Balancer Multiport	Fig. 6	*E*

TABLE V
SINGLE-INPUT AC-MODULE TOPOLOGY COMPARISON: CALCULATED BENCH MARKING FACTORS

ID:	VA_{Tot}	Ξ_{Cond}	Π_{Switch}	$A_{\mathrm{CW,trafo}}$	$E_{\mathrm{Ind,Tot}}$	$E_{\mathrm{Cap,Tot}}$
I	5.68 E + 3	2.05 E + 2	4.19 E + 3	1.70 E−8	2.01 E−2	1.25 E + 1
II	1.00 E + 4	2.18 E + 2	1.05 E + 5	6.60 E−8	4.56 E−2	**9.39 E−1**
III	7.26 E + 3	2.66 E + 2	4.35 E + 3	2.05 E−8	2.24 E−1	1.24 E + 1
IV	5.43 E + 3	**8.17 E + 1**	**3.89 E + 3**	2.32 E−8	**1.37 E−2**	1.24 E + 1
V	1.63 E + 4	5.75 E + 2	2.02 E + 4	3.48 E−8	1.26 E−1	2.41
VI	9.47 E + 3	1.75 E + 2	4.85 E + 3	5.06 E−8	7.97 E−2	1.33
VII	1.07 E + 4	2.54 E + 2	3.18 E + 4	6.97 E−8	1.33 E−1	4.15
VIII	7.24 E + 3	2.29 E + 2	7.42 E + 3	3.29 E−8	2.34 E−1	2.53
IX	6.47 E + 3	1.04 E + 2	1.13 E + 4	2.26 E−8	6.80 E−2	2.28
X	9.41 E + 3	3.39 E + 2	1.39 E + 4	5.54 E−8	2.52 E−1	2.81
XI	**5.03 E + 3**	1.15 E + 2	7.70 E + 3	**1.35 E−8**	5.88 E−2	2.84

A. Single-Input Topology Comparison

For each of the considered single-input ac-module topologies in Table III a system design is performed based on the common system specification in Table II. The waveforms are calculated based on a simple converter model implemented for each topology. This allows us to calculate the six bench marking factors described above.

Table V lists the calculated factors for all 11 topologies. The smaller the benchmarking factor, the better the performance of the topology. The best values of each bench marking factor, being the minimum, is highlighted in bold. The pseudo dc-link resonant flyback topology (*ID: IV*) is found to feature high efficiency of the semiconductors. In addition, it also exhibits relatively small values for the total semiconductor rating, transformer-size, and inductance energy. In comparison to the BCM flyback topology (*ID: III*), it can be seen that the interleaving of the flyback stages brings significant advantages regarding the stored inductive energy and the conduction losses. It results a well-balanced topology characteristic with high semiconductor performance and reasonable implementation effort for the passive components. An alternative topology, which achieves a comparable performance, is the HF-link *LC*-resonant & cyclo topology (*ID: I*). The resonance converter operating principle brings along an even smaller transformer factor than the resonant flyback topology and also allows for zero voltage switching. The HF-link *LC*-resonant & cyclo topology is in addition capable of delivering reactive power. The drawback of these two topologies are their high capacitive energy value, which is caused by the passive capacitive power decoupling realized with large capacitors on the PV side. These capacitors must typically be realized with electrolyte capacitors, which compromise the lifetime of the converter.

Some of the compared topologies apply active power decoupling to reduce capacitor size. Though it can be clearly seen, that power decoupling is achieved at the expense of reduced performance due to a higher-switching loss factor, transformer size, and installed semiconductor power (see *ID: II*, *ID: V* and *ID: VI*).

Alternatively to the topologies with a ripple port, the dc-link topologies provide power decoupling at the intermediate dc link. The dc-link topology with an *LC*-resonant boost converter (*ID: XI*) shows the most balanced characteristic with low bench marking factors in the same range as the pseudo dc-link resonant flyback topology (*ID: IV*) and the HF-link *LC*-resonant & cyclo topology (*ID: I*). All considered dc-link topologies apply a full bridge PWM inverter between the dc-link and the grid. This full bridge converter operates in hard switched mode, whereas most of the other compared topologies operate with ZVS. For the calculation of the switching loss factor it is not distinguished between soft switching and hard switching. The dc-link topologies are therefore subject to additional not considered switching losses, which would reduce the system performance relatively to the other compared topologies.

The topology comparison reveals the following conclusions. The first and most important decision, when designing an ac-module converter, is wether electrolyte capacitors are an acceptable component to be used or not. In literature, electrolytic capacitors were often declared as the lifetime limiting component in ac modules [1], [47], [48]. Other studies state that with a careful thermal design and overrating a 30-years lifetime of the electrolyte capacitors can easily be achieved [49], [50]. Among the commercially available ac modules there are products with [38] and without electrolytic capacitors [51], depending on the manufacturer.

1) With Electrolyte Capacitors: Passive capacitive power decoupling can be applied at the PV-input side and a single-stage topology features the best performance. Among these, the pseudo dc-link resonant flyback converter (*ID: IV*) with three interleaved flyback stages features minimal semiconductor part-count and a high performance. The comparison further identifies the HF-link *LC*-resonant & cyclo topology (*ID: I*) as a second very interesting candidate for an ac module. It features comparable performance as the flyback topology and is in addition capable of delivering reactive power.

2) Without Electrolyte Capacitors: Passive capacitive power decoupling can not be applied, due to the reduced energy-density and the high cost of alternative capacitor technologies. This decision will inherently lead to a system with reduced system performance, due to increased switching and conduction losses. There are two approaches to provide the necessary power decoupling. First with a ripple-port and second with a two stage topology and an intermediate dc-link. The two stage dc-link approach applying an *LC* resonant boost converter and a PWM full bridge appears to be the most promising candidate. Though the PWM full bridge operates under hard switched condition. As the switching loss factor does not distinguish between soft and hard switching, the switching losses of the PWM full bridge are actually underestimated relatively to soft switched topologies.

TABLE VI
MULTI-INPUT AC-MODULE TOPOLOGY COMPARISON: CALCULATED BENCH MARKING FACTORS

ID:	VA_{Tot}	Ξ_{Cond}	Π_{Switch}	$A_{CW,\mathrm{trafo}}$	$E_{\mathrm{Ind,Tot}}$	$E_{\mathrm{Cap,Tot}}$
A	4.88 E + 3	2.23 E + 2	2.25 E + 3	2.32 E−8	1.37 E−2	1.25 E + 1
B	4.88 E + 3	1.49 E + 2	9.49 E + 3	1.68 E−8	6.41 E−2	2.29
C	5.03 E + 3	1.58 E + 2	6.66 E + 3	1.67 E−8	6.41 E−2	2.35
D	7.40 E + 3	4.44 E + 2	1.53 E + 4	2.26 E−8	6.41 E−2	2.35
E	5.68 E + 3	2.05 E + 2	4.19 E + 3	1.70 E−8	2.01 E−2	1.25 E + 1

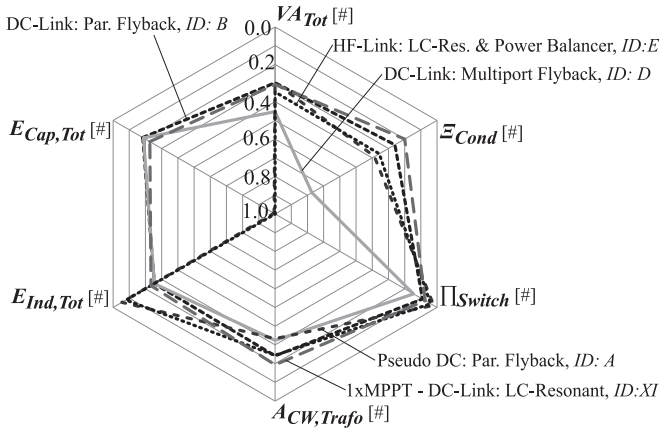

Fig. 7. Comparison of multi-input ac-module topologies.

B. Multi-Input Topology Comparison

Based on the common system specification in Table II, a system design is performed for the proposed multi-input ac-module topologies listed in Table IV.

The calculated benchmarking factors for the five multi-input topologies are listed in Table VI. The benchmarking factors are plotted on a spider plot with inverted axes, shown in Fig. 7. The benchmarking factors are normalized to the worst case value (the maximum) among all topologies compared in this work (see Tables V and VI). The serial flyback dc–dc topology (*ID. C*) exhibits similar benchmarking factors as the parallel flyback dc–dc topology (*ID. B*) and is therefore omitted in Fig. 7. In addition to the multi-input topologies also a single-input topology, the dc-link *LC*-resonant boost topology (*ID: XI*), is shown in Fig. 7.

The multiport sequential flyback dc–dc topology (*ID: D*) achieves the worst performance. Due to the sequential operation of the three inputs, the converter exhibits higher peak currents than the paralleled or serial flyback converters. This increases the semiconductor rating, the conduction losses, the switching losses, and the transformer size.

The pseudo dc-link topology with paralleled dc–dc flyback converters (*ID: A*) and the power-balancer multiport with an HF-link *LC*-resonant converter (*ID: E*) feature a small stored inductive energy, a small transformer size, and a good semiconductor performance. Power decoupling is realized with PV-side passive power decoupling, requiring electrolyte capacitors. Both topologies operate under ZVS conditions. However, the flyback topology is subject to additional not considered switching losses, caused by the transformer leakage inductance. The *LC*-resonant topology is in addition capable of delivering reactive power. Further, the power balancer multiport brings the following advantages. The voltage step-up ratio of the *LC*-resonant converter is the same as for the single-input topologies. The power-balancer is only active in unbalanced conditions, causing only minimal insertion losses in balanced conditions. This makes the *LC*-resonant topology the preferable choice among these two topologies.

The dc-link topology with paralleled flyback dc–dc converters (*ID: B*) features power decoupling at the dc-link, which enables a much smaller capacitive energy storage. Also the other benchmakring factors are relatively small, confirming an overall good performance of the dc-link topology with flyback dc–dc converters. Fig. 7 contains as a benchmark the most favorable single-input dc-link topology, being the dc-link *LC*-resonant topology (*ID: XI*). The multi-input flyback topology exhibits comparable values of the benchmarking factors as the single-input topology. However, the multi-input topology suffers from reduced performance due to the three times increased voltage step-up ratio and switching losses caused by the leakage inductance. The serial connection of the dc–dc converters (*ID: C*) exhibits slightly better benchmarking factors than the parallel connected dc–dc converters (see Table VI). Especially the switching loss factor is reduced by a factor one and a half. Though the series connection requires a much wider voltage step-up range and a more complex control, making the parallel connection preferable for a practical application.

In summary, the comparison reveals two distinct approaches to realize the multi-input converter. Which one is favorable depends again on the fundamental question, if power decoupling may be realized with electrolyte capacitors.

If electrolyte capacitors may be used, power decoupling can be realized by passive capacitive decoupling at the output of the multiport stage. The power-balancer multiport topology with an HF-link *LC*-resonant converter is the best choice. It actually consists of a conventional single-input ac-module converter combined with a power balancer dc–dc converter. The advantage of this approach is, that it minimizes the system inherent drawbacks compared to a single-input ac module and may achieve comparable converter efficiency levels.

If electrolyte capacitors are not allowed, a dc-link topology is the only feasible approach to realize power decoupling without an excessive number of switches. The topology with paralleled flyback dc–dc converters and a PWM full bridge (*ID: B*) appears to be the preferred dc-link topology. The small capacitor size is advantageous regarding converter reliability, cost, and capacitor volume. Though compared to single-input ac modules, this topology has the drawback of a three times higher step-up ratio of the dc–dc stage. Further the dc–ac PWM full bridge operates hard switched. Applying conventional semiconductors, such as MOSFETs and IGBTs, it is therefore hard to compete with soft-switched ac-module topologies. Newly available GaN-based power semiconductors feature much improved hard switching performance, compared to MOSFETs or IGBTs. With the application of GaN devices, the performance of

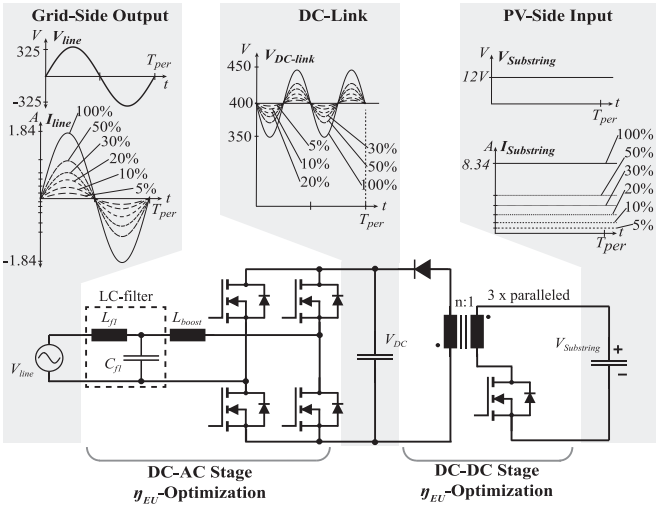

Fig. 8. Overview of the optimization procedure for European efficiency.

a hard switched dc-link topology could possibly compete with soft switched ac modules.

V. Multi Input AC-Module Design and Prototype

From the two promising topologies identified in the preceding section, the dc-link topology is investigated in the following section. A detailed model-based design and performance analysis is performed and the converter efficiency is evaluated by experimental results.

A. Investigated Multi-Input AC-Module Topology

The dc-link topology with three paralleled flyback converters (see Fig. 4) is selected for the following reasons.

1) It features a much reduced power-decoupling capacitor, overcoming a main drawback of the conventional HF-link and pseudo dc-link ac-module topologies.
2) The newly available GaN devices promise unprecedented hard switching performance of the full bridge topology. It is therefore very interesting to investigate, to which level the efficiency of the whole multi-input ac-module converter can be pushed.

The two stage topology relies on the two standard topologies, flyback converters [52] and a PWM fullbridge [23], and a control scheme for power decoupling as proposed in [53] and [22]. The three paralleled flyback stages operate completely autonomously. Consequently, also the MPP tracking on each substring is performed autonomously and state-of-the-art MPP-tracking techniques well known from single-input ac modules can be applied [54].

Fig. 8 schematically shows the operating waveforms of the two-stage converter in balanced conditions at different output power levels. The dc-link decouples the 100 Hz pulsating line power from the dc-power delivered by the PV substrings. Depending on the instantaneous line power, the excess or lacking energy is temporarily buffered in or taken from the dc-link. Consequently, the voltage V_{DC} exhibits a sinusoidal 100 Hz ripple $\Delta_{V_{\mathrm{DC}}}$ overlaid to the average dc-link voltage $\overline{V}_{\mathrm{DC}}$.

B. Converter Model & Optimization Routine

The design of the two-stage converter system is a nontrivial task due to the multitude of its design variables. The European efficiency η_{EU} serves as performance factor [55]. Furthermore the volume of the converter is defined as a constraint, to allow for the derivation of the converters efficiency versus power density, $\eta - \rho$, pareto front applying a single-objective optimization algorithm. To determine η_{EU}, the converter model must calculate the converter efficiency at the following six operating points: $P_{\mathrm{out}} = [100\%, 50\%, 30\%, 20\%, 10\%, 5\%] \cdot P_{\mathrm{nom}}$ schematically shown in Fig. 8. A wide load span optimization requires a model, which accurately models the loss components over the whole load range. Therefore, advanced magnetic models according to Refs. [56] and [57] are applied to model parasitic elements of magnetic components and their influence on operating waveforms.

As the optimization of the complete two-stage system is too complex to solve within a reasonable time with the available calculation power, the dc–dc stage and the dc–ac stage are optimized individually. The operating waveforms used for the loss models of each stage are those of the two stage system with power decoupling, as illustrated in Fig. 8. For the dc–dc flyback converter stage, a genetic algorithm is used to perform a comprehensive converter optimization including the transformer core and winding geometry. The dc–ac stage optimization routine, shown in Fig. 9, is more complex, because it contains a system-level model for the optimization of a DM output filter. A direct search method is applied to optimize the filter design [58]. Underlaid, there is a component-level model for semiconductor losses and an optimization subroutine for the inductors. Beside semiconductor and magnetic losses both converter models consider auxiliary losses for gate drive supply and measurement circuits. The complete two-stage system is derived by combining the optimization results of the dc–dc and the dc–ac stage and adding additional auxiliary losses $P_{\mathrm{syst,aux}} = 750$ mW for a microcontroller required for converter control and a line relay to comply with safety standards.

C. Model-Based Optimization

The dc–dc and dc–ac stage optimization routines are applied to calculate the volume versus efficiency pareto front of the two-stage multi-input ac module. The system specification, serving as input to the optimization routines, is given in Table VII.

1) Component and Material Selection: In the following the components and materials are described, which are considered for the model based optimization:

a) Semiconductors: For the dc–ac stage the 650 V/7A devices GS66502 B E-HEMT GaN transistors are applied. They feature total half-bridge switching losses of merely 30 μJ (at 400 V/4 A hard switching), as measured on a double-pulse prototype board. These measurements are used to accurately model the dc–ac stage switching losses. For the primary side switch of the dc–dc flyback stage the EPC2032 100 V/4 mΩ

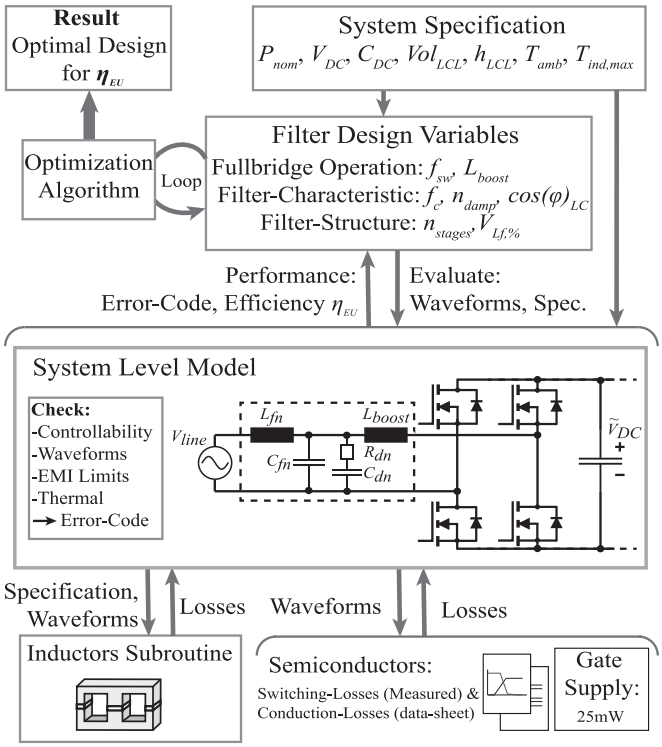

Fig. 9. DC–AC full bridge converter optimization including multistage *LC*-output differential-mode (DM) filter.

TABLE VII
DC–DC AND DC–AC STAGE OPTIMIZATION: SPECIFICATION OF SYSTEM PARAMETERS DERIVED FROM TABLE I

Output Power	P_{nom}	300 W (3·100 W)
Input Voltage	V_{substr}	12 V
DC-Link Voltage	$\bar{V}_{\mathrm{DC}}$	400 V
DC-Link Capacitor	C_{DC}	28 μF
Flyback Transformer Volume	$\mathrm{Vol}_{\mathrm{trafo}}$	30–400cm^3
Filter and Boost-Indcutor Volume	$\mathrm{Vol}_{\mathrm{LCL}}$	60–200 cm^3
Height of Magnetic Components	h_{mag}	25 mm, 37.5 mm
Ambient Temperature	T_{amb}	50°C
Max. allowed Magnetic Hotspot	$T_{\mathrm{mag,max}}$	90°C

eGaN FETs from EPC is applied. The switching losses are modeled with a V-I crossover model based on the rise- and fall-times provided in the data sheet. On the output side of the dc–dc flyback stage the 1.2 kV/2A C4D0212E SiC Schottky diode is applied due to its excellent reverse-recovery behavior and low current rating.

b) Magnetic Materials: To enable a compact design of the dc–ac stage filter and boost inductor, a core material with high-saturation flux density is required. For the boost inductor, the material must further feature low HF losses. For the model-based optimization of the boost inductor the following core materials are taken into account: amorphous Microlite DGC toroid cores (Hitachi Metals) and nanocrystalline Vitroperm 500 F gapped C-cores (Vacuum Schmelze). For the filter-inductors toroid cores of the following materials are considered: Microlite DGC cores (Hitachi Metals), HighFlux, and MPP powder cores (Magnetics). The current of the dc–dc stage flyback-transformer

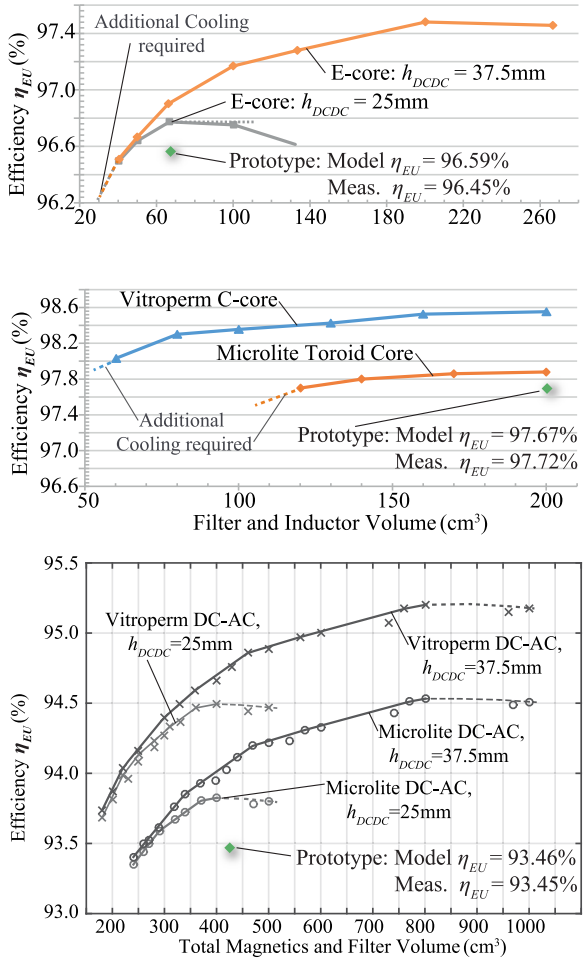

Fig. 10. Volume versus efficiency η–ρ pareto fronts calculated by model-based optimization. (a) DC–DC stage boxed transformer volume versus η_{EU}. (b) DC–AC stage boxed volume of the boost inductor and the output filter versus η_{EU}. (c) Entire two-stage multi-input ac module total magnetics and filter volume versus η_{EU}.

exhibits a large ripple at HFs. Therefore, core materials with very low HF losses, the Si-ferrites N87, N97, and N49 from Epcos are considered for the flyback transformer optimization.

c) Cooling System: All components are cooled by free convection. The magnetic components are cooled via their surface only. The semiconductors are cooled with small standard-size black anodized heat-sinks [59].

2) Optimization Results: The calculated pareto fronts are shown in Fig. 10(a)–(c) for the dc–dc stage, the dc–ac stage, and the complete multi-input ac module. The dc–dc stage pareto front [see Fig. 10(a)] reveals a strong influence of the low-profile constraint on the achievable performance. Moreover a dc–dc stage efficiency above $\eta_{\mathrm{EU}} = 96.5\%$ only comes at the expense of a highly increased volume. The dc–ac stage pareto front [see Fig. 10(b)] clearly confirms that the superior characteristic of the nanocrystalline Vitroperm material resulting in both a higher efficiency and a more compact volume. Depending on the volume, a dc–ac stage efficiency between 98% and 98.5% can be achieved. The pareto front of the complete two-stage multi-input ac module consisting of one dc–ac stage and three paralleled

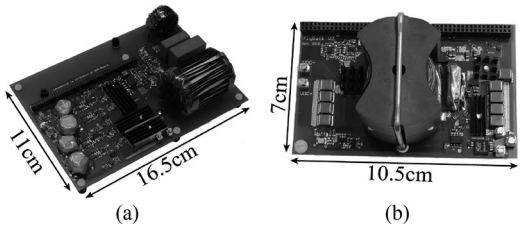

Fig. 11. Multi-input ac-module prototype. (a) DC–AC stage. (b) One of the three paralleled dc-dc stages.

dc–dc stages, is derived from the optimization results of the dc–dc and the dc–ac stage, see Fig. 10(c). With the application of a Vitroperm 500 F core as boost inductor an ac-module efficiency in the range of $\eta_{\mathrm{EU}} = 94...94.5\%$ can be achieved at a magnetics and filter volume of 200 to 300 cm^3. To increase the efficiency above 94.5% requires an ever increasing volume and a loosened height constraint of 37.5 mm for the dc–dc stage. With Microlite toroidal cores applied for the boost inductor, efficiency is ca. 0.7% lower over all volumes.

D. GaN/SiC Multi-Input AC-Module Prototype

To evaluate the results of the model-based optimization, prototypes of the dc–dc stage and the dc–ac stage has been built and tested. An MPP-tracking is not implemented, because standard MPPT techniques well known from single-input ac modules could be applied and the efficiency could also be measured without MPPT. The prototypes are shown in Fig. 11. Operating waveforms of the dc-dc and dc–ac stage are shown in Fig. 12. The line-voltage and -current exhibit some spikes at zero crossing caused by the interlocking of the full bridge, which could be mitigated by an improved modulation scheme at zero crossing. As illustrated in Fig. 10(a) and (b), the efficiencies of the designed prototypes are 0.7% and 0.2% below their respective pareto fronts. This is because suboptimal standard core sizes are applied. The pareto optimum can only be achieved with custom made core sizes. Efficiency measurements with a power analyzer show that the converter models accurately predict the efficiency (see Fig. 10(a)–(c)]. The maximal deviation between the calculated and the measured losses is below 15%.

E. Performance of the Investigated Multi-Input AC Module

For a commercial product, cost considerations limit the allowable magnetics and filter volume. With a typical volume of an ac-module converter housing in the range of 400 cm^3, the investigated two-stage multi-input ac module maximally achieves an efficiency of $\eta_{\mathrm{EU}} = 94.5\%$ at uniform power generation of all three substrings. This is 1% lower than the benchmark efficiency of the commercial ac modules being $\eta_{\mathrm{EU}} = 95.5\%$. Even with the application of the latest GaN device technology and low-loss nanocrystalline core materials, the efficiency level of the single-input ac modules can not be achieved. The main loss-contribution originates from the transformer of the dc–dc stage, which limits the dc–dc stage efficiency to 96.5%.

Under partial shading or other mismatch conditions the multi-input ac-module features increased yield. Though the crucial

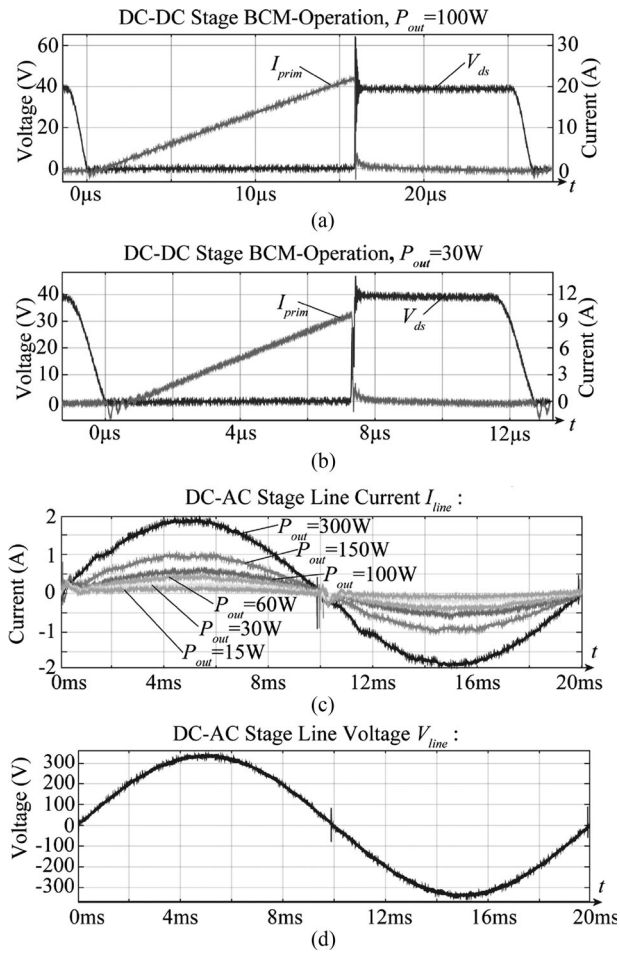

Fig. 12. Multi-input ac-module prototype waveforms. (a) and (b) Single dc–dc flyback stage transformer primary side current I_{prim} and input-side switch drain–source voltage V_{ds} at 100 W and 30 W P_{out}. (c) and (d) DC–AC stage line-current I_{line} and voltage V_{line} at various output power.

question is, how much the yield increases exactly for practical applications. A representative mismatch scenario based on which the multiinput ac module can be compared to single-input ac modules is difficult to determine. In practice, it depends very much on the specific environment, the geographic location, the quality and aging of the PV module, and it also varies with the season.

In the literature, publications proposing topologies for substring MPP tracking assume a certain arbitrary mismatch scenario to validate their proposals [8], [9]. The effectiveness of the investigated multi-input ac module may be demonstrated by using the same four scenarios as used by Bell *et al.* [8]. In their work also the MPP-tracking efficiency of a single-input ac module $\eta_{\mathrm{MPPT,single}}$ is measured for the given mismatch conditions. It is much below the MPPT-tracking efficiency under balanced conditions, being typically around 99.5%. Table VIII shows the output power for the investigated multi-input ac module and the single-input ac module Aurora Micro-0.3-I from PowerOne ($\eta_{\mathrm{CEC}} = 96.0\%$). The output power is calculated using the measured efficiencies and the detailed efficiency curves from the datasheet, respectively. An MPP voltage of $V_{\mathrm{MPP,str}} = 12$ V

TABLE VIII
COMPARISON OF THE INVESTIGATED MULTI-INPUT AC MODULE WITH THE POWERONE AURORA MICRO-0.3-I SINGLE-INPUT AC MODULE, BASED ON THE MISMATCH-SCENARIOS AND MEASURED SINGLE-INPUT MPP-TRACKING EFFICIENCY $\eta_{\mathrm{MPPT,single}}$ PRESENTED IN [8] (ASSUMPTIONS: $V_{\mathrm{MPP,str}} = 12$ V, $\eta_{\mathrm{MPPT,multi}} = 99.5\%$)

Mismatch Scenario:	Case 1	Case 2	Case 3	Case 4
$P_{\mathrm{MPP,1}}$	27.2 W	27.2 W	17.4 W	17.4 W
$P_{\mathrm{MPP,2}}$	36.9 W	27.0 W	36.9 W	17.2 W
$P_{\mathrm{MPP,3}}$	37.6 W	37.6 W	37.6 W	37.6 W
$\eta_{\mathrm{MPPT,single}}$	88.81%	92.69%	78.82%	77.97%
$P_{\mathrm{out_{single,ACmodule}}}$	86.7 W	78.4 W	78.4 W	61.4 W
$P_{\mathrm{out_{multi,ACmodule}}}$	95.8 W	86.2 W	85.7 W	67.0 W

is assumed, whereas the results are relatively insensitive to the exact MPP voltage.

In practical operation, the mismatch is much less pronounced, when considering total annual yield. There are currently not many studies, which investigate this issue in detail, due to the necessity to perform long-time experiments. A decent study, which investigates partial shading on substring level in detail is the work from Mac Alpine [6]. The annual yield is estimated to increase by 1% for moderate and by 2% for heavy shading scenarios. Under this perspective, the investigated multi-input ac module would allow for 1% annual yield increase under heavy shading conditions. For moderate shading-conditions no yield increase would result, at higher costs of the multi-input ac module due to the inherent higher part-count number and pricey, high performing semiconductor devices, and core materials.

VI. CONCLUSION

In this work multi-input ac modules with MPP tracking on substring level are investigated. Based on a review of existing single-input ac modules, possible concepts of such a multi-input ac module are derived and topology candidates are proposed. A categorization of multi-input ac-module topologies is introduced, which helps to identify the different system concepts. A systematic comparison of the multi-input as well as the single-input ac-module topologies reveals two attractive concepts to realize a multi-input ac module. The first concept is a power balancer multiport in combination with an HF-link *LC*-resonant converter topology. This approach is similar to the high-efficient single-input ac-module topologies. The power balancer serves as add-on to realize substring MPP tracking and processes only the unbalanced share of the power. The second concept is a two stage dc-link topology with three paralleled dc–dc flyback converters and a PWM dc–ac full bridge. Being a two-stage converter with intermediate dc-link, it features the advantage of smaller power decoupling capacitors.

The later is investigated in this work. A detailed loss model of this multi-input ac-module converter is derived and verified with experimental results. High performance GaN devices and nanocrystalline core materials are applied to increase efficiency. The model-based optimization reveals an achievable efficiency of 94.5%.

The concept of MPP tracking on substring level must finally compete against single-input ac modules. Considering the balance of system costs the only advantage of multi-input ac modules is the increased energy yield under partial shading. Unfortunately there exist few studies, which investigate in detail the potential yield increase of substring MPP tracking under realistic conditions. According to the available studies, the investigated topology only achieves an increased yield at heavy shading conditions [6].

Given this result, the first concept with a power balancer and an HF-link *LC*-resonant converter appears as the more appealing approach as it may achieve a comparable efficiency as the single-input ac modules. In recent publications DPP converters are proposed to realize the power balancer.

Though there is still a lot of work to do, to find the optimal topology for a power balancer, which reduces control effort, standby losses, and hardware cost. Further there is the need for more investigations on substring mismatch losses in PV modules under realistic operating conditions, for instance applying the approach proposed in [60]. Only such field measurement based studies will allow to better quantify the additional yield that can be gained from substring MPP tracking.

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