Multilevel Nonsuperconducting Fault Current Limiter: Analysis and Practical Feasibility

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***Abstract*—A new topology for nonsuperconducting fault current limiter (NSFCL) based on multilevel switching strategy is proposed in this paper. The proposed multilevel NSFCL circuit aims to control the high-level fault current by inserting different resistances in the circuit. Due to interrupting the fault current based on multilevel switching strategy which results in the decrement of switching numbers, power loss will be reduced and lifetime of the utility devices will be increased. The proposed NSFCL structure has the capability of limiting the fault current based on obtained quantities from current sensors. The proposed NSFCL topology which has no effect on voltage and load currents of the utility, ensures a high level system protection. The analysis of normal and fault conditions of the proposed multilevel NSFCL have been provided and experimental results are demonstrated to prove feasibility of the proposed structure.**

***Index Terms*—Fault current limiter (FCL), multilevel FCL, power loss, switching problem, utility protection.**

I. Introduction

CONSIDERING the rapid growth of electric power networks, their interconnections, and power demand from consumers in recent years, which have resulted to greater power capacity and lower source impedance, the probability of high rating of fault current levels have increased. As a result, failure probability of power system equipment and system collapse are increased. Due to the maximum current rating of protection devices and their requirement to several cycles for interrupting the fault current, a solution is required for solving the problem [1].

The fault current limiter (FCL) is a practical idea for preventing fault current increment from a predetermined value, which has attracted a lot of attention as a solution of the mentioned problem. Another application of FCL in power system include improving power quality [2], [3], limiting inrush current in transformers [4], [5], increasing reliability [6], [7], and enhancing power system transient stability [8], [9]. An ideal FCL should indicate zero resistance/ impedance in normal operation of the power system, and high impedance in short-circuit condition of the system. No power losses in normal operation of the system are another characteristics of an ideal FCL [10]. Moreover, rapid operation after fault occurrence and prompt recovery after fault elimination are numerated as characteristics of an ideal FCL. Besides, good reliability and low construction cost are counted as the other indication for an ideal FCL. A large number of studies have been performed in recent years on different FCL structures and several configurations have been proposed for controlling the high-fault current in power networks. Proposed FCLs in previous studies can be classified in different categories, including superconducting FCL (SFCL) [11], [12], solid-state FCL [13], [14], and magnetic FCL [15], [16].

The SFCL configurations include resistive-type SFCL [17], shielding-type SFCL [18], saturated iron-core-type SFCL [19], [20], dc reactor SFCL [21], [22], and saturated dc-reactor-type FCL [23], [24]. The requirement of SFCL for operation temperature less than their transition temperature, manifest necessity of SFCL configurations for cooling equipment. Extra operating power losses and additional costs of cooling equipment are counted as SFCL disadvantages. Besides, distortion on load voltage and network current waveform, which is due to voltage drop on SFCL instrument, are taken into account as another disadvantage of SFCL structures. Considering high technology and cost barrier of SFCL structures, different types of FCL topologies for eliminating the mentioned disadvantages have been introduced in recent years.

Recently a novel type of FCL topologies called nonsuperconducting FCL (NSFCL) structure has been introduced. NSFCL has the capability of removal of additional costs and high technologies of SFCL structures. A simple and cheap FCL circuit can be attained by placing a nonsuperconducting coil instead of superconducting coil.

In [8], Hagh and Abapour have proposed an NSFCL structure with a controllable simple topology for limiting the fault current in fault condition of the power system. Replacing superconducting coil with nonsuperconducting coil and eliminating the requirement of disconnection of distribution switches can be considered as advantages of presented NSFCL topology in this reference. A bridge-type NSFCL structure has been presented in [25], with the capability of low volume of dc reactor and low-frequency transformer with respect to topologies proposed in the previous studies. Chen *et al*. [25] have proposed the NSFCL circuit for interrupting the fault current without requirement to

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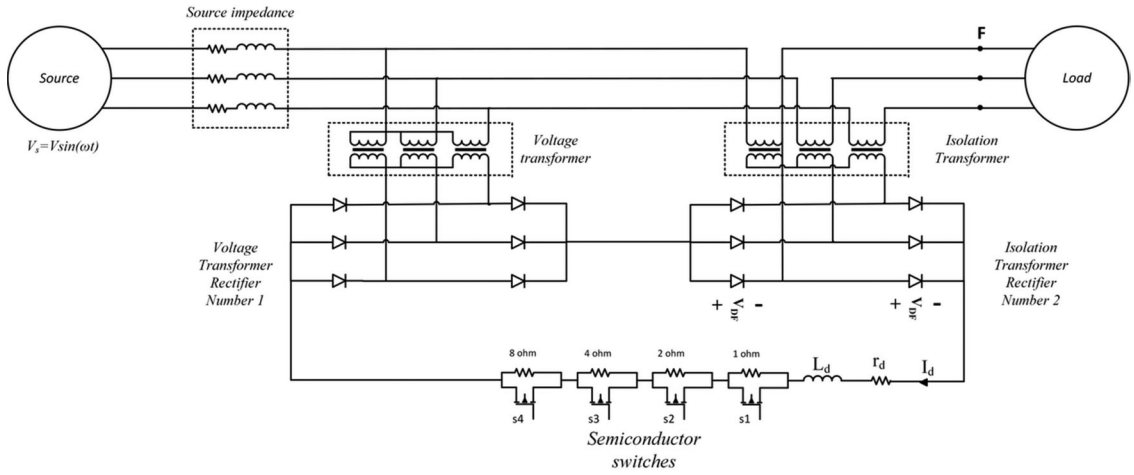

Fig. 1. Power circuit topology of the proposed FCL.

upgrading protective equipment. Chen *et al*. [1] proposed a new technique for limiting fault current by introducing a switched impedance transformer-type NSFCL structure, which is based on implementation of the introduced NSFCL structure in conjunction with other protection devices. Low power loss, simple controlling process, small size, and low construction cost are considered as advantages of the proposed NSFCL topology in this reference.

This study presents a new structure of NSFCL for interrupting the fault current, considering a multilevel switching strategy. The previous introduced structures ignored the number of switching for attaining the limited fault current, which resulted to power loss and reduced the lifetime of devices [25]. The presented NSFCL structure in this paper has the capability of fault current limitation by proposing a multilevel switching strategy. Furthermore, the proposed multilevel NSFCL circuit has a simple structure which is practical to be utilized in power networks. The simulation of circuit operation is presented in both normal and fault conditions and experienced. The provided experimental results are in good agreement with the results of simulation of circuit operation. The results obtained by simulation and experiment of the proposed multilevel NSFCL topology, ensure practicality and simple circuit structure. The contributions of this paper can be summarized as the following:

1) The switches are binary arranged in the proposed multilevel NSFCL. The switching strategy is based on inserting resistors 1, 2, 4, 8 Ω to the circuit by increment of fault current in binary arrangement instruction.
2) The number of switching is reduced, which results to switching power loss decrement with respect to previous researches reported in this area.
3) Taking into consideration the few number of switching, lifetime of switches, and FCL structure is increased.
4) By using the multilevel NSFCL structure, the voltage stress on semiconductor switches is low. So that, as an economic advantage semiconductor switches with low voltage rating is required.

The reminder of this paper is organized as follows. Power-circuit topology and operational principles of the proposed NSFCL is presented in Section II. The operation analysis with details is illustrated in Section III. Section IV represents the simulation, and experimental results are demonstrated in Section V. A discussion on different structures of NSFCL circuit is prepared in VI. Finally, the paper is concluded in Section VII.

II. Power-Circuit Topology and Operational Principles of the Proposed NSFCL

In this section, the proposed NSFCL structure, which is capable to limit the fault current level by a multi-level based switching strategy, has been analyzed. Fig. 1 demonstrates the power-circuit topology of the proposed NSFCL implementation. The proposed circuit includes three main sections which are expressed in the following:

1) Connection of a three-phase transformer as a voltage transformer and a three-phase diode-bridge rectifier which is defined as "isolation transformer rectifier number 1"; power source is provided by utilizing the three-phase diode-bridge rectifier for compensating the losses happening in the proposed circuit.
2) Connection of three sets of single-phase transformers and a three-phase diode-bridge rectifier; the three-phase diode-bridge rectifier defined as "isolation transformer rectifier number 2."
3) Four parallel connections of discharging resistors and semiconductor switches that are in series with each other and with the dc reactor.

The voltage transformer rectifier is utilized as power source for compensation of voltage. The compensating voltage can be stated as follows:

$$V_c = 2V_{\mathrm{DF}} + 4V_{\mathrm{SW}} + r_d I_d. \tag{1}$$

In which V_{SW} defines the voltage drop on each of semiconductor switches.

In the normal operation mode of the proposed power circuit, the NSFCL is ineffective to the utility. This means the proposed NSFCL has no impact on utility voltage and load current waveform in the normal condition of the utility. The semiconductor

TABLE I
CONDITION OF THE SEMICONDUCTOR SWITCHES

	Switches		Level
Ohm	Off	On	
1	1	2, 3, 4	1
2	2	1, 3, 4	2
3	1, 2	3, 4	3
4	3	1, 2, 4	4
5	1, 3	2, 4	5
6	2, 3	1, 4	6
7	1, 2, 3	4	7
8	4	1, 2, 3	8
9	1, 4	2, 3	9
10	2, 4	1, 3	10
11	1, 2, 4	3	11
12	3, 4	1, 2	12
13	1, 3, 4	2	13
14	2, 3, 4	1	14
15	1, 2, 3, 4	–	15

switch is closed in this mode and the discharging resistors are bypassed.

During the fault condition, the resistors will be added to the circuit considering current sensed by current sensor. The objective of the proposed multilevel NSFCL is to add resistors to the circuit by sensing a predetermined value by the current sensor. The basic operation of the proposed structure is adding resistors to the circuit until the current is less than the predetermined value. The proposed multilevel circuit has the capability of adding resistors from 1 up to 15 Ω for reducing the fault current.

Four different resistors, including 1, 2, 4, and 8 Ω are selected to provide a range of resistors between 1 and 15 Ω. Since the high level current will damage utility elements, it needs to be controlled. The controller circuit is required as a solution for this problem, aiming to restrict the high-level current to a predetermined value. The condition of semiconductor switches that can be turned ON or turned OFF, will be utilized for controlling the high-level current. The condition of the semiconductor switches of the proposed multilevel NSFCL structure is shown in Table I, which is identified for different levels. Each level considers a quantity of resistor for reducing the fault current at the predetermined value. The next level of the circuit will be activated if the fault current exceeds the predetermined value.

III. ANALYTICAL ANALYSIS

The analytical analysis of the utility operation considering the situation of the circuit before, during, and after fault are provided in this section. The line current before fault occurrence, during fault condition without utilizing the proposed multilevel NSFCL structure, and after fault removal can be observed in Fig. 2, in which the fault current is reached to 275 A during fault condition.

Fig. 3(a) and (b) shows the line current in presence of the proposed multilevel NSFCL circuit. Two modes of operations for circuit exist after fault occurrence as follows:

1) The fault current is less than the predetermined current level (I_d).

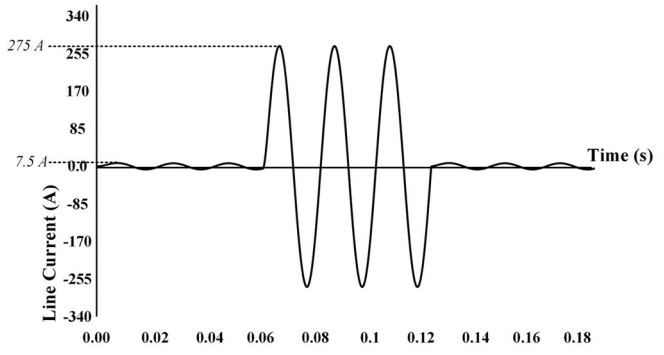

Fig. 2. Simulation results before fault occurrence, during fault condition without FCL, and after fault removal.

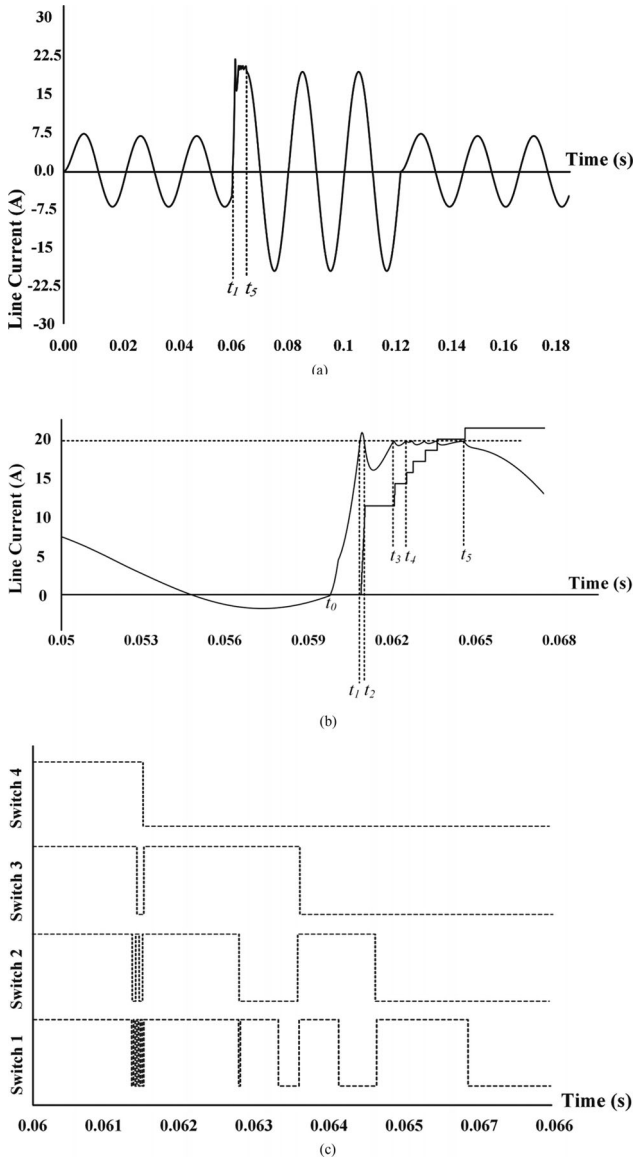

Fig. 3. (a) Simulation results of the proposed circuit before fault occurrence, during fault condition by inserting 15 Ω resistance, and after fault removal. (b) Simulation results of the proposed circuit considering different levels of resistance insert during fault condition by inserting 15 Ω resistance. (c) Simulation results of different levels of resistance insert during fault condition by inserting 15 Ω resistance.

The line currents after fault are demonstrated in Fig. 3(b), in which the short circuit happens at t_0. The control circuit recognized the increment of fault current with respect to predetermined value at t_1. During t_0 to t_1, the following equation can be introduced as the following:

$$V\sin(\omega t) = ri_L(t) + L\frac{di_L(t)}{dt}. \tag{2}$$

So the utility current can be obtained as

$$i(t) = e^{-(r/L)(t-t_0)}\left\{i_0 - \frac{V}{z}\sin(\omega t_0 - \varphi)\right\} + \frac{V}{z}\sin(\omega t - \varphi). \tag{3}$$

In which

$$\begin{aligned} r &= r_s + r_f + r_d \\ L &= L_s + L_f + L_d \\ i_L(t) &= i_d(t) = i(t) \\ z &= \sqrt{r^2 + (L\omega)^2}, \varphi = \frac{\tan^{-1}(L\omega)}{r} \\ i_0 &= i(t_0). \end{aligned}$$

2) The fault current is reached to a predetermined current level (I_d).

Considering the recognition of the control circuit of increasing the fault current with respect to the predetermined value at t_1, the resistances are added to the circuit based on multilevel switching strategy at t_1. In this mode, we have two submodes as follows:

a) Charging submode.
b) Discharging submode.

Between t_1 and t_2, the dc reactor current is similar to the line current during charging mode and can be stated as (2). Therefore, the utility and dc reactor current can be formulated as

$$i(t) = e^{-(r/L)(t-t_1)}\left\{i_1 - \frac{V}{z}\sin(\omega t_1 - \varphi)\right\} + \frac{V}{z}\sin(\omega t - \varphi) \tag{4}$$

where

$$\begin{aligned} r &= r_s + r_f + r_d + \sum r_i \\ L &= L_s + L_f + L_d \\ i_L(t) &= i_d(t) = i(t) \\ z &= \sqrt{r^2 + (L\omega)^2}, \varphi = \frac{\tan^{-1}(L\omega)}{r} \\ i_1 &= i(t_1). \end{aligned}$$

In which, resistance and inductance of fault impedance are indicated by r_f and L_f, respectively. r_i is the resistance, inserted in the circuit by the operation of the proposed multilevel NSFCL for limiting the fault current to the predetermined value.

As seen in Fig. 3(b), the inserted resistances for interrupting fault current based on multilevel strategy switching achieved a sufficient amount of current reduction at t_2, which ensures that the line current is less than the predetermined value. The line current increased from predetermined value at t_3, which manifest another resistance insert in the circuit. The interval between t_2 and t_3 can be formulated as (2). So, the line current equation is formulated as

$$i(t) = e^{-(r/L)(t-t_2)}\left\{i_2 - \frac{V}{z}\sin(\omega t_2 - \varphi)\right\} + \frac{V}{z}\sin(\omega t - \varphi) \tag{5}$$

where

$$\begin{aligned} r &= r_s + r_f + r_d + r_4 \\ L &= L_s + L_f + L_d \\ i_L(t) &= i_d(t) = i(t) \\ z &= \sqrt{r^2 + (L\omega)^2}, \varphi = \frac{\tan^{-1}(L\omega)}{r} \\ i_2 &= i(t_2). \end{aligned}$$

The line current is less than the dc current during discharging mode. Transmission of the dc reactor current through the diodes of the isolation transformer and voltage transformer rectifiers will happen in this mode. Similar to this period, the time between t_3 and t_4 and other periods up to t_5 can be analyzed.

After t_5 up to the fault removal, considering the predetermined level for interrupting the fault current based on the proposed multilevel NSFCL, the inserted resistances to the circuit remain in the circuit. During discharging submode, the line current is less than the dc reactor current, and the equation for this submode can be stated as (2). So, the line current equation is formulated as

$$i(t) = e^{-(r/L)(t-t_5)}\left\{i_5 - \frac{V}{z}\sin(\omega t_5 - \varphi)\right\} + \frac{V}{z}\sin(\omega t - \varphi) \tag{6}$$

where

$$\begin{aligned} r &= r_s + r_f + r_1 + r_2 + r_3 + r_4 \\ L &= L_s + L_f \\ z &= \sqrt{r^2 + (L\omega)^2}, \varphi = \frac{\tan^{-1}(L\omega)}{r} \\ i_5 &= i(t_5). \end{aligned}$$

In addition, the following equation can be stated in fault condition and discharging mode for dc reactor current

$$L_d\frac{di_d(t)}{dt} + ri_d(t) + 2V_{\mathrm{DF}} - V_C = 0. \tag{7}$$

So, the line current equation is formulated as

$$i_d(t) = e^{-(r/L)(t-t_5)}\left\{i_5 + \frac{2V_{\mathrm{DF}} - V_C}{r_d}\right\} + \frac{2V_{\mathrm{DF}} - V_C}{r_d} \tag{8}$$

TABLE II
SIMULATION PARAMETERS

Symbol	Contents	Value
$V_s\,(RMS)$	Source Voltage	380 (V)
r_s	Source Resistance	1 (Ω)
L_S	Source Inductance	1 (mH)
F	Power Frequency	50 (Hz)
V_{DF}	Voltage Drop Across Rectifier Diode	2 (V)
V_{SW}	Voltage Drop Across Semiconductor Switch	2 (V)
r_d	DC Reactor Resistance	0.1 (Ω)
L_d	DC Reactor Inductance	1 (mH)
r_{Load}	Load Resistance	30 (Ω)
L_{Load}	Load Inductance	0.1 (H)
r_F	Fault Resistance	0.1 (Ω)
L_F	Fault Inductance	0.1 (mH)

TABLE III
THE CIRCUIT PARAMETERS OF THESE TWO STRUCTURES

	Proposed multilevel NSFCL	Presented single switched NSFCL in [8]
Ld (DC reactor inductance)	1 mH	1 mH
Rd (DC reactor resistance)	0.1 Ω	0.1 Ω
Voltage drop over semiconductor switches	1 V	1 V
Discharge resistor	Depends on ON/OFF condition of the switches S1, S2, S3, and S4	15 Ω

where

$$r = r_s + r_f + r_1 + r_2 + r_3 + r_4$$
$$L = L_s + L_f$$
$$z = \sqrt{r^2 + (L\omega)^2}, \varphi = \frac{\tan^{-1}(L\omega)}{r}$$
$$i_5 = i(t_5).$$

IV. SIMULATION RESULTS

The power-circuit topology which is shown in Fig. 1 is simulated in the proposed study. Table II illustrates the simulation parameters of this study. In the simulations, the fault is occurred for three cycle. The control circuit samples the current with a frequency of 50 KHz.

Analysis of the fault occurrence has been done considering multiple cases and different operation performances are accomplished as follows. The fault occurred is a short circuit to ground at point F. Simulation results before fault occurrence, during fault condition without NSFCL, and after fault removal can be observed in Fig. 2. As seen in this figure, the fault current peak is reached to 275 A in the steady state of the fault condition and the current peak in the normal condition of the circuit is 7.5 A. The simulations for inserting 15 Ω resistances are provided. Performance of the proposed multilevel NSFCL topology for 15 Ω insert in the circuit is shown in Fig. 3. The control circuit is adjusted in a way that the fault current above 20 A is prohibited. As seen in Fig. 3(a), the peak value of the fault current is limited by the performance of the proposed control strategy. The proposed multilevel-based NSFCL inserted 15 Ω resistance for limiting the fault current at the predetermined value. Fig. 3(a) demonstrates the obtained simulation results for NSFCL operation performance at different conditions, including before fault occurrence, during fault condition, and after fault removal by operation of the proposed NSFCL. As seen in this figure, the short circuit is occurred in t_0, which resulted to the current increment. As mentioned earlier, the proposed multilevel-strategy-based NSFCL insert resistance until the fault current limitation in a predetermined value. The inserted resistance remains 15 Ω in this condition for reducing the fault current to the predetermined value. Considering the proposed multilevel NSFCL structure in this paper, the operation of the circuit is illustrated in more detail in Fig. 3(b). As seen in this figure, the levels of inserting the resistance in the circuit for limiting the fault current at 20 A is observable. Moreover, this figure illustrates the order of adding different levels of resistances to the circuit for interrupting the fault current at the predetermined value. The conditions of four semiconductor switches have been demonstrated in Fig. 3(c). As seen in this figure, which clearly shows the proposed multilevel switching strategy performance, the number of switching is limited which is ignored in last studies in the area of NSFCL structures.

The main advantage of the proposed multilevel NSFCL structure is the capability of detection of the fault current limitation level at a predetermined value without rapid switching during the short-circuit time interval. The advantages of altering the short circuit level are introduced in recent studies [8], [9]. For limiting the fault current with the ability of short-circuit level alteration utilizing single switched method, rapid switching during short-circuit time interval is required, which is studied in [8] and [9].

The voltage stress on semiconductor switches are compared considering the multilevel NSFCL and the presented single switched NSFCL. The circuit parameters of these two structures can be summarized as presented in Table III.

The voltage stresses on semiconductor switches are compared in two studied structures considering a current equal to 25 A in single-phase simulation. Inserting a resistance of 3 Ω by performance of the proposed multilevel NSFCL limited the fault current to 25 A, whereas the single switched NSFCL limited the current to 25 A by fast switching in which the discharge resistor is 15 Ω. It should be noted that the discharge resistor in single switched NSFCL is not permitted to be a low value, since taking into account the low amount of discharge resistor, the current will be more than the predetermined value.

For inserting a 3 Ω resistance to the circuit by multilevel NSFCL, S1 and S2 are turned OFF and S3 and S4 are ON. The voltage stress on semiconductor switches S1 and S2 are demonstrated in Fig. 4(a) and (b), respectively. As it is obvious in this figure, the maximum voltage stress on semiconductor switches S1 and S2 are 25 and 52 V. Fig. 4(c) shows the voltage stress

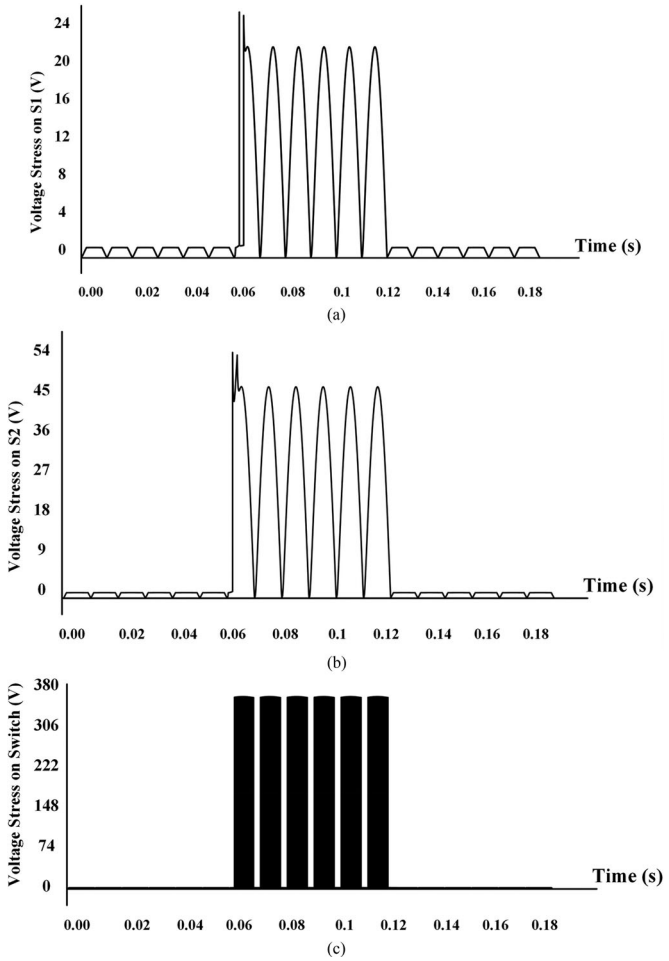

Fig. 4. (a) Voltage stress on semiconductor switch S1 considering performance of multilevel NSFCL in network current of 25 A. (b) Voltage stress on semiconductor switch S2 considering performance of multilevel NSFCL in network current of 25 A. (c) Voltage stress on semiconductor switch in single switched structure proposed in [8] in network current of 25 A.

on semiconductor switch in single switched NSFCL structure proposed in the single switched NSFCL, which has reached to a maximum amount of 360 V.

V. Discussion

The power loss discussion can be provided between the proposed multilevel NSFCL structure in this paper and the single switched NSFCL as follows:

1) Four resistors type of multilevel NSFCL structure is introduced in this paper for demonstrating the advantages of the proposed multilevel NSFCL. Three or two resistors could be utilized in order to reduce the power loss with respect to multilevel NSFCL with four resistors.
2) According to the figures and the results achieved in the previous section, voltage stress across the semiconductor switch in a single-mode resistor is much more than the multilevel NSFCL circuit. So, the semiconductor switch with high rating voltage is needed in the single switched NSFCL. Accordingly, on-state resistance of the semiconductor switch depends on the nominal voltage rate $(\mathrm{r_{ds}} \sim \mathrm{V_{ds}})$. So that, the on-state resistance in semiconductor switch in single switched NSFCL will be even more than the sum of all on-state resistance of switches in multilevel type. As a practical example, for limiting fault current of 20 A in a single switched NSFCL, usage of IRFP450 MOSFET in which $\mathrm{r_{ds}} = 0.27\ \Omega$ is appropriate. However, in the proposed multilevel NSFCL, IRFP150 MOSFET with $\mathrm{r_{ds}} = 0.055\ \Omega$ is sufficient. Considering four resistors in the proposed multilevel NSFCL, four switches in series with $\mathrm{r_{ds}} = 0.055\ \Omega$ are utilized, which equals to a resistance of $\mathrm{r_{equal}} = 0.055\ \Omega * 4 = 0.22\ \Omega$. So, the equal resistance in multilevel NSFCL is lower than the resistance of single-type NSFCL. As a result, the on-state power losses in the proposed multilevel NSFCL is lower than the single switched NSFCL.
3) In practical, the amount of fault current in power networks is high, so that the power system equipment with high tolerable current and voltage rating is needed. Requirement of semiconductor switches with high current and switch voltage rating is obvious and the maximum switch voltage for recent produced IGBTs is 3.3 kV. In other words, even usage of the single switched NSFCL requires several switches in series for tolerating the switch voltage. This fact results a high power loss in the single switched NSFCL.
4) In the single switched NSFCL, continuous switching in pulse width modulation (PWM) switching mode is obvious which results to power loss. Whereas, in the proposed multilevel NSFCL the switches are ON or OFF, and there is no PWM switching power loss.

Additionally, the time response can be discussed. As mentioned in the paper, the sampling rate of current waveform is 50 kHz. Accordingly, the available equipment such as LM311 is capable to response in 0.2 μs. Considering the switching time and total responses time, the control circuit has the ability of operation in some μs. So that, the switching resistors ON and OFF throughout fault requires insignificant time response.

In order to achieve a performance of equal arrangement similar to the proposed multilevel NSFCL, a switch which is able to handle 15 Ω resistance is required in single switched NSFCL circuit. Taking into consideration this viewpoint, a 15 V switch is more expensive than a set of 1, 2, 4, 8 V switches. Another valuable point which should be noted for cost comparison of multilevel NSFCL and single switched NSFCL is related to voltage stress on switches. By increasing the predetermined value of current limitation in single switched NSFCL, the stress voltage on the switch is increased. However, in multilevel NSFCL structure by increasing predetermined value of current limitation, all of the switches may not be turned OFF. As a result, sum of stress voltages on binary arranged switches is lower than single switched NSFCL. Considering the mentioned points and relationship between switch cost and voltage stress on the switch, the proposed multilevel NSFCL is cheaper than single switched NSFCL. As an instance, the predetermined

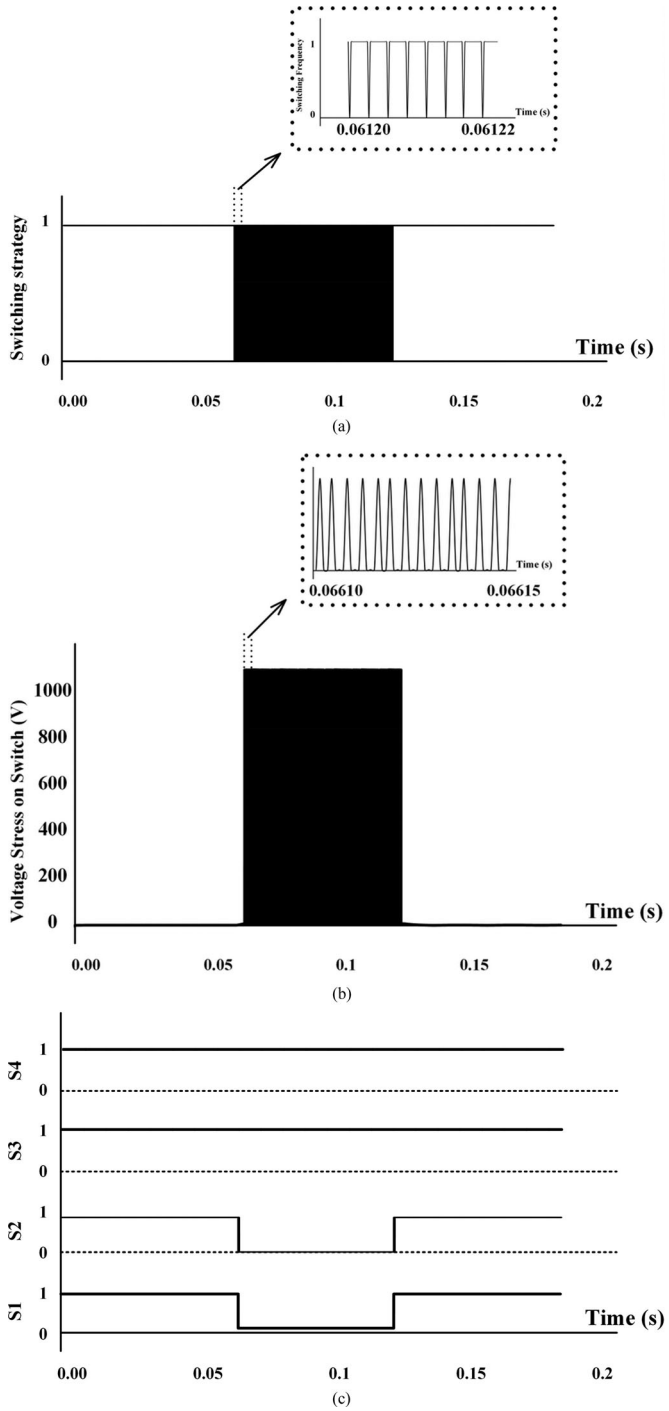

Fig. 5. (a) Switching in single switched NSFCL. (b) Voltage stress on switch in single switched NSFCL. (c) Switching in multilevel NSFCL.

value is considered equal to 70 A. The circuit is simulated for three-phase network and the simulation parameters are as tabulated in Table II. Fig. 5(a) shows the switching strategy in the single switched NSFCL. The simulation result for voltage stress on switch in the single switched NSFCL is demonstrated in Fig. 5(b). Fig. 5(c) shows the switching strategy in the proposed NSFCL. Moreover, Fig. 6(a) and (b) shows voltage stress on switch S1 and S2 in multilevel NSFCL, respectively. S3 and S4 are ON and only S1 and S2 are operated. So that, there are

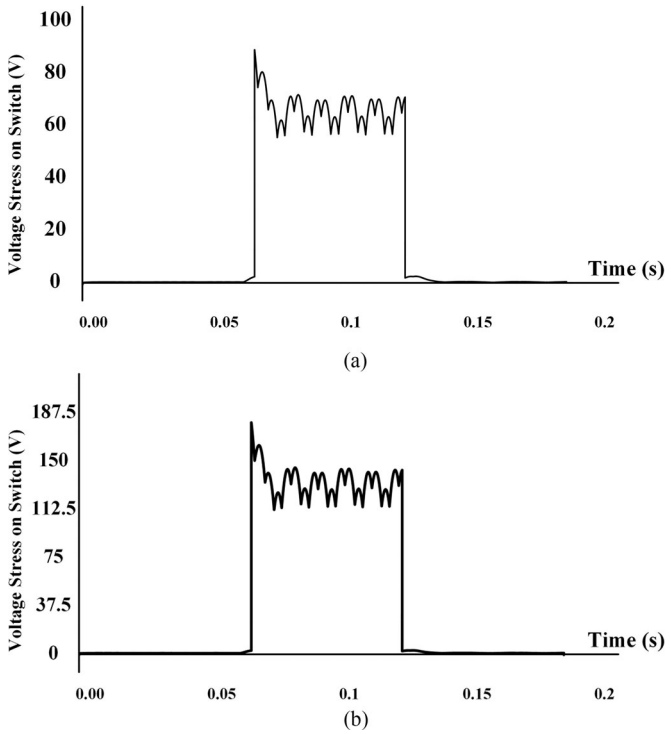

Fig. 6. (a) Voltage stress on switch S1 in multilevel NSFCL. (b) Voltage stress on switch S2 in multilevel NSFCL.

voltage stress only on S1 and S2 in fault condition. As seen in Fig. 6(a) and (b), sum of voltage stress in the multilevel NSFCL is lower than the single switched NSFCL. In this instance, the circuit requires a switch with voltage rating of 1000 V, and in the binary arranged circuit the switches with ratings of 160 and 80 V is sufficient for circuit operation. It can be numerated as another factor effecting on the circuit cost, which ensures that the proposed multilevel NSFCL is cheaper than single switched NSFCL.

As studied in this instance, switches S3 and S4 are ON and for limiting the fault current to 70 A, only two switching are needed. This fact shows the flexibility of the binary arranged FCL circuit. However, in single switched NSFCL, a similar switch and resistor exist for all limitation scenarios.

The advantages of the proposed multilevel NSFCL structure with respect to single-level NSFCL are as follows:

1) The voltage stress on semiconductor switches utilizing the multilevel NSFCL circuit is low. Accordingly, semiconductor switches with low voltage rating is needed, which can be numerated as economic advantages.
2) Taking into account lower equal on-state switch resistance in the multilevel NSFCL than the resistance of single switched NSFCL, requirement of semiconductor switches with high current and switch voltage rating, and continuous switching in PWM switching mode in the single switched NSFCL, power loss in the proposed multilevel NSFCL structure is less than the single switched NSFCL.
3) Better lifetime of semiconductor switches: Taking into account the few number of switching in fault condition, the

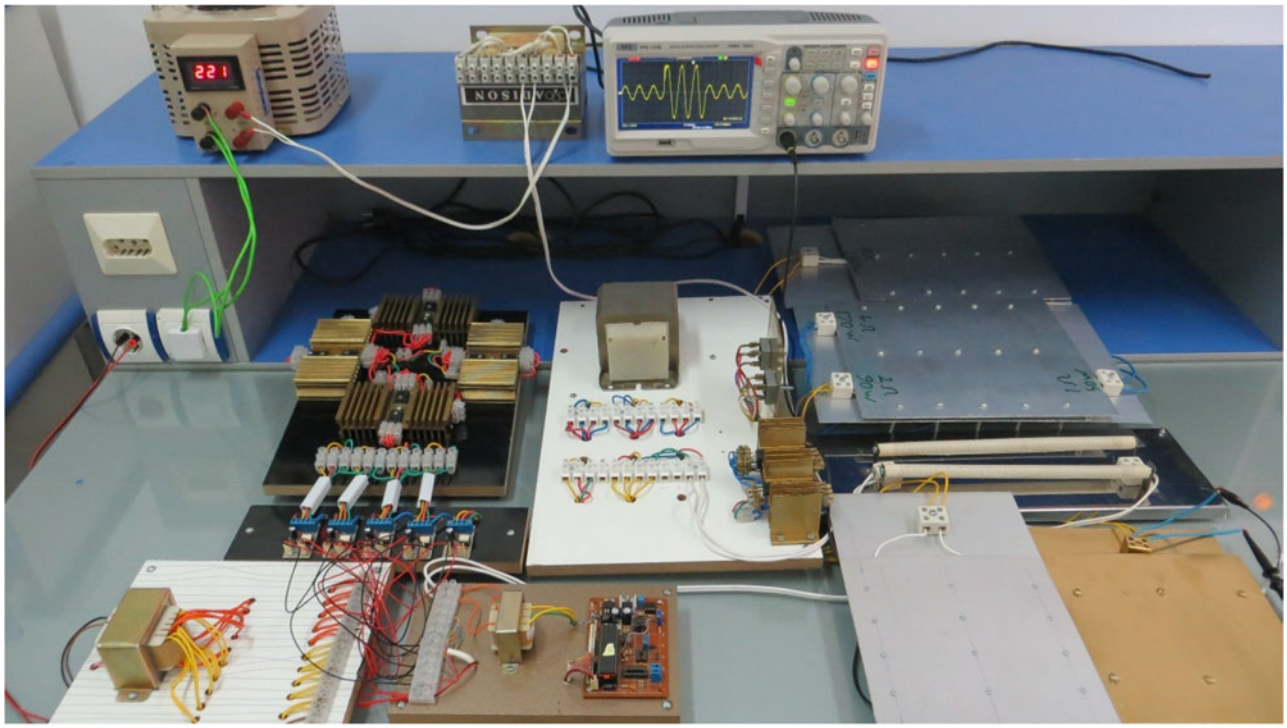

Fig. 7. Prototype of the proposed FCL topology.

TABLE IV
EXPERIMENTAL PARAMETERS

Symbol	Contents	Value
$V_s\,(RMS)$	Source Voltage	63 (V)
RS	Source Resistance	1 (Ω)
L_S	Source Inductance	1 (mH)
F	Power Frequency	50 (Hz)
V_{DF}	Voltage Drop Across Rectifier Diode	1 (V)
V_{SW}	Voltage Drop Across Semiconductor Switch	1 (V)
L_D	DC Reactor Inductance	1 (mH)
R_{LOAD}	Load Resistance	45 (Ω)
L_{LOAD}	Load Inductance	0 (H)
RF	Fault Resistance	1 (Ω)
L_F	Fault Inductance	0 (mH)
Z_{LINE}	Line Impedance	0.1 (Ω)

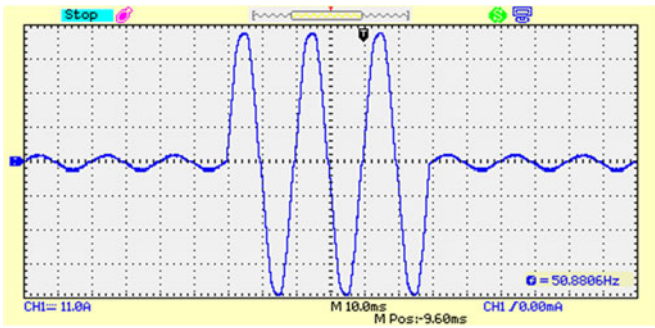

Fig. 8. Experimental results before fault occurrence, during fault condition without FCL, and after fault removal.

lifetime of switches will be increased, whereas in the single switched NSFCL, continuous switching is observed.

4) Taking into account the obtained results for network current in performance of multilevel NSFCL, current waveform distortion in fault condition is insignificant.

VI. EXPERIMENTAL RESULTS

To show feasibility of the proposed NSFCL topology, experiment of power-circuit topology of the proposed NSFCL which is shown in Fig. 1 is done. The parameters opted for experimental circuit is demonstrated in Table IV. The prototype of the proposed NSFCL topology has been shown in Fig. 7, including 1, 2, 4, and 8 Ω resistances.

For controlling the discharging resistor, metal–oxide–semiconductor field-effect transistor has been utilized. Experimental results of the proposed circuit before fault occurrence, during fault condition without presence of the proposed multilevel NSFCL, and after fault removal has been shown in Fig. 8, which is similar to the obtained result of the circuit simulation. Fig. 9(a) and (b) shows the obtained experimental results considering the 15 Ω resistance insert that are in line with simulated results provided in Fig. 3. Moreover, the provided experimental results for adding 9 Ω resistance based on the proposed multilevel NSFCL structure have been demonstrated in Fig. 10(a) and 10(b). Besides, Figs. 11 and 12 illustrate the obtained experimental results of the proposed NSFCL topology based on the multilevel switching strategy for 3 and 1 Ω insert, respectively.

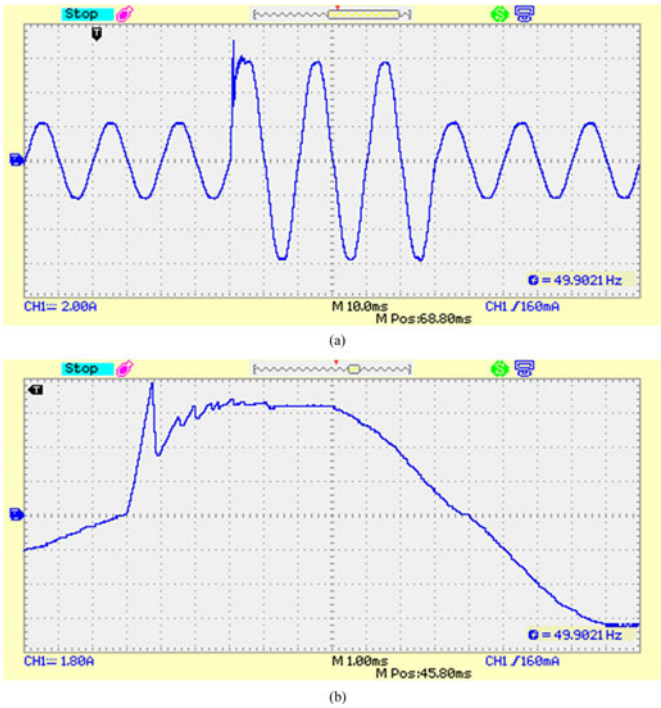

Fig. 9. (a) Experimental results of the proposed circuit before fault occurrence, during fault condition by inserting 15 Ω resistance, and after fault removal. (b) Experimental results of the proposed circuit during fault condition by inserting 15 Ω resistance.

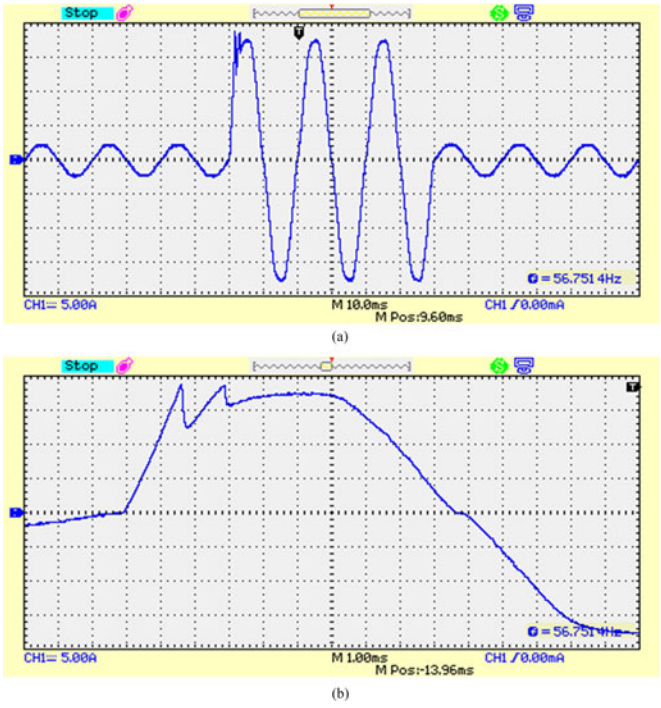

Fig. 11. (a) Experimental results of the proposed circuit before fault occurrence, during fault condition by inserting 3 Ω resistance, and after fault removal. (b) Experimental results of the proposed circuit during fault condition by inserting 3 Ω resistance.

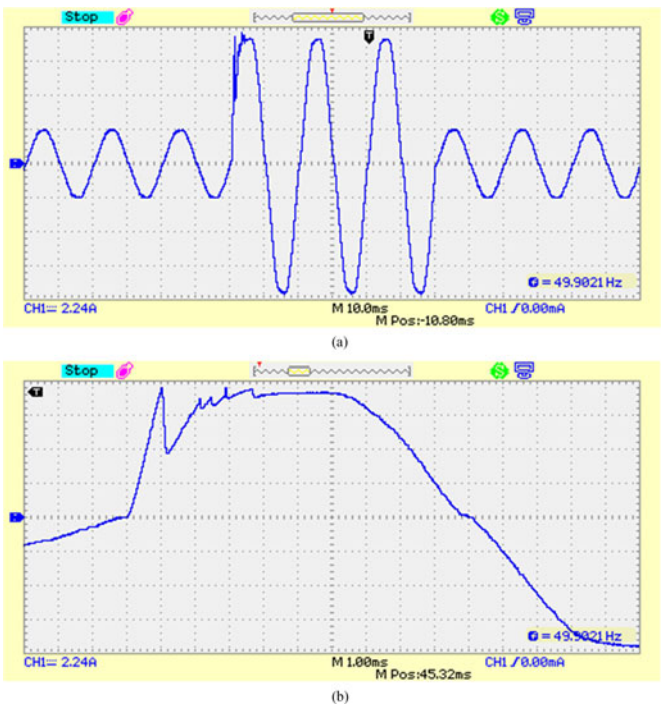

Fig. 10. (a) Experimental results of the proposed circuit before fault occurrence, during fault condition by inserting 9 Ω resistance, and after fault removal. (b) Experimental results of the proposed circuit during fault condition by inserting 9 Ω resistance.

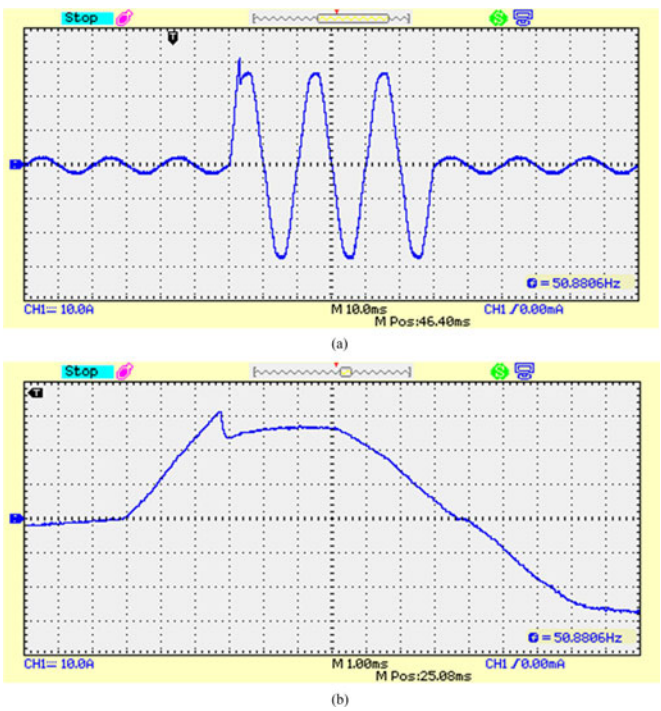

Fig. 12. (a) Experimental results of the proposed circuit before fault occurrence, during fault condition by inserting 1 Ω resistance, and after fault removal. (b) Experimental results of the proposed circuit during fault condition by inserting 1 Ω resistance.

VII. Conclusion

A novel multilevel NSFCL structure is proposed in this paper, introducing a new switching procedure which operation is based on fault current level. The proposed structure ensures fault current limitation and high protection level of the utility, which is capable to interrupt the fault current by a multilevel switching strategy. As a result, power losses are eliminated and lifetime of the utility devices is increased. Since the switching is based on a predetermined level of fault current, a few numbers of switching is required to limit the fault current, and increment of lifetime of the switching devices is attained. Moreover, by decreasing the numbers of switching for limiting the fault current, power losses are reduced. Furthermore, it should be noted that by utilizing the proposed multilevel NSFCL, requirement to superconductor technology and impact on voltage and current of the utility are eliminated. The proposed multilevel NSFCL structure is analyzed in both theory and feasibility points of view. Normal and fault conditions of the utility are analyzed and the obtained results are discussed. Simulations of the proposed multilevel NSFCL are provided and experimental results are demonstrated. Simulation and experiment of the proposed multilevel NSFCL topology show that it is practical and the structure is simple.

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