Control of a Three-Phase Boost PFC Converter Using a Single DC-Link Voltage Sensor

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***Abstract*—This paper proposes a new methodology to control a three-phase boost power factor correction (PFC) using a single dc output voltage sensor. Typically, a PFC control technique requires measurement from five independent sensors, i.e., two input voltages, one output dc voltage, and two input phase currents. Elimination of four sensors in the control system of a PFC converter is theoretically feasible and implementable without compromising stability and power quality of the converter, as analyzed and presented in this paper. The proposed control technique uses the ripple information of the measured dc-link voltage, converter dynamics, and switching states at a preceding sample in order to estimate the present state of four other unknown state variables and, thus, establishes the control method. A 2.2-kW experimental prototype of a three-phase boost PFC is developed and tested to verify the accuracy and applicability of the proposed control logic at different line and load conditions. According to the experimental measurements, conversion efficiency more than 98%, total harmonic distortion as low as 4.3%, and an output voltage ripple of $\pm 2\%$ are achieved at 2.2-kW output power.**

***Index Terms*—Boost rectifier, converter dynamics, estimation, modeling, power factor correction (PFC), sensorless control, three phase.**

I. Introduction

TRADITIONAL three-phase ac/dc rectification topologies in auxiliary power unit of airplanes, utilizing passive diode-bridge rectifiers and huge dc-link capacitors are presently being replaced by active switched-mode ac/dc converters. Power factor correction (PFC) rectifiers are one of the fundamental building blocks in active ac–dc conversion, required to supply power to different linear and nonlinear loads in the airplane. PFC stages are used to improve power quality, and are also regulate output dc-link voltages. Among the three traditional PFC topologies, i.e., buck-type, boost-type, and buck–boost-type, the three-phase active boost PFC has a simple structure, less number of semiconductor devices and capability to work in continuous-conduction mode [1]–[4].

Various methodologies to control three-phase boost PFC converters have been reported [5]–[14]. One of the most commonly used simple techniques is direct linear-phase current control, which considers each phase current as an independent state variable and stabilizes the control loop through a linear current controller for each phase [5]. Because of its simple and computationally fast implementation, higher switching frequency operation could be achieved. However, using this control strategy, it is very challenging to minimize the lower order odd harmonics of the phase currents. Therefore, input current total harmonic distortion (THD) and conversion efficiency are not comparable to advanced control methods with better modulation strategies. The inherent steady-state tracking error and the leading phase of current in this method could be potentially eliminated by the *dq*-domain space vector pulse width modulation (PWM) control strategy [6]. *dq*-domain vector control also takes care of minimizing the switching transitions and, hence, improves the input current THD content. However, *abc-dq* transformation sector determination are two major computationally complicated tasks, and thus, interrupt execution time is relatively more than the existing traditional methods. Therefore, high switching frequency designs with this control method require high-speed digital implementation platforms, such as multicore digital signal processor (DSP) or FPGA, which could increase the cost and complexity of design [7].

Moreover, in the aforementioned methods, PFC requires two input voltage sensors, one dc-link voltage sensor and two input phase current sensors. Besides obvious economic benefits of reducing sensor counts, there are several other additional advantages, such as robustness to high-frequency noise, elimination of sensor offsets, reduction of weight of the converter, and slight increase in conversion efficiency by removing the senor losses [8]. To alleviate such sensor-related issues, cheap voltage divider solutions could be applied to replace the high-frequency sensors. However, since the inductor currents and phase voltages are of low frequency, it is quite challenging to measure these variables with high accuracy. Therefore, the high-frequency sensors need to be used; however, due to the required high resolution and high sampling frequency, the cost of input current and its corresponding A/D converter is usually quite high and covers a significant portion of the entire cost of a PFC unit. In addition, these sensors introduce high-frequency noise and path delay in the control loop, which could potentially jeopardize the robustness and stability of the converter. This delay effectively works as an inductive path in the feedback loop, which could result in high-voltage spikes across the switching devices.

Additionally, using hall-effect sensors could potentially limit the duty ratio of MOSFETs due to saturation, which in turn compromises the power quality of the converter. Moreover, typical

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hall-effect phase current sensors not only add weight to the system, but also complicate the design of the control loop due to carrying high-frequency noise. To overcome these issues, different algorithms have been proposed to estimate the input phase currents from the dc-link current and/or the DC-link voltage as well as PWM states of the switches [9]–[19]. However, one of the principal difficulties associated with these methods is that the phase currents cannot be perfectly reconstructed if dc-link current consists of more than one phase currents in some switching intervals. It will also add one cycle delay in using the reconstructed phase currents in control loop, as it would take one switching cycle to compute respective estimators [20] and, hence, could lead to instability in case of an output load transient at a digital control platform. To address these critical issues, a large-signal model of boost PFC can be used to design a current observer [20]. However, the proposed control is not simply applicable to three-phase boost PFC rectifiers due to difference in topological structures.

In [21], the CT is placed in series with the MOSFET to sense the inductor current when the switch is ON. However, the idea in [21] deals with the interleaved structure of multiple boost phases; the switching noise of one phase potentially affects the sampling of the other phase, which degrades the reliability. To avoid such issues, typically low-pass filters are added in series with CT; however, this introduces more delay into the feedback loop and deteriorates the stability margins. PFC operation by removing the current sensors is presented in [22]. It is shown that a sinusoidal current can be achieved by a nominal duty ratio pattern, which is calculated in an open loop and the voltage loop controls the controllable phase of the duty ratio pattern to regulate the output voltage. However, this method is too sensitive to the circuit parameters. Also, the converter's performance degrades in light load condition due to sudden jump in zero crossings and higher THD. In [23], another current sensorless observer-based estimation approach is taken to minimize the error caused by the parasitic components. Although this method achieves high-quality input currents at heavy load, the performance deteriorates at low output power. Also, in many applications, the load value is unknown to the nonlinear observer, used in this method. Therefore, due to the lack of information, the converter loses its observability at some operating points. Moreover, similar aforementioned sensor-related issues arise in case of input voltage sensors, as input voltages are sampled at the same frequency as input currents to maintain in-phase operation. A few input voltage sensorless control strategies have been proposed; however, due to computational complexities of the suggested algorithms, switching frequency is limited, which would increase the THD of the input phase currents [24]–[27]. The idea presented in [28] estimates the input voltage from the sensed current and dynamic input impedance analysis, and proposes a voltage feed-forward control to achieve PFC. However, the input voltage estimation and the proposed control depend on the output load resistance, which makes this method inapplicable for a variable load condition.

Therefore, aiming to offer an alternative sensorless control strategy for a three-phase boost PFC converter, this paper proposes an innovative control methodology using a single dc-link voltage sensor. Four other state variables, i.e., two input voltages and two input phase currents are estimated from the dc-link voltage ripple between two consecutive samples, switching PWM states at previous cycle, and phase duty cycles at previous sample. The estimation technique involves extensively detailed mathematical modeling of the converter, and small-signal transfer functions among the state variables. The effectiveness of the control algorithm with the variability of output load power demand and line voltage conditions is addressed, analyzed mathematically, and verified through experimental results with the specifications of an avionics application (i.e., 400 Hz input ac system). Furthermore, the paper discusses the digital implementation of this control approach by comparing its execution time and computational complexity with other existing methods.

The paper is organized as follows. Section II introduces the brief description of the topology and explains the details of mathematical modeling of the converter and systematically derives the estimation algorithm for control implementation. The experimental results of applying the proposed control methodology on a 2.2-kW three-phase boost PFC prototype at variable load and line conditions are presented and analyzed in Section III. Section IV puts forward conclusions of this paper with relevant discussions.

TABLE I
LIST OF NOMENCLATURES

Symbol	Description
d_{kH}	Duty ratio of high-side MOSFET of "*k*"th phase ("*k*" is *A* or *B* or *C*)
D_{kL}	Duty ratio of low-side MOSFET of "*k*"th phase ("*k*" is *A* or *B* or *C*)
V_{kN}	Voltage between "*k*"th phase and negative terminal of dc link ("*k*" is *A* or *B* or *C*)
i_J	Instantaneous current through "*J*" phase inductor ("*J*" could be *A* or *B* or *C*)
C_o	Output capacitor value
V_{DC}	Output voltage
I_o	DC-link current
i_{out}	Current through dc load
$\Delta\tilde{i}_k$	Estimated variation in "k"th phase current over a sampling cycle
$\Delta\tilde{V}_{\mathrm{kn}}$	Estimated variation in "k"th phase voltage over a sampling cycle
A	Voltage loop PI controller output
X	Duty-averaged phase-neutral voltage
k_1	Difference between phase "A" duty and common mode duty ratio
k_2	Difference between phase "B"' duty and common mode duty ratio

II. Proposed Control Algorithm Using a Single DC-Link Voltage Sensor

For the analyses performed in rest of this section, some nomenclatures have been used and, therefore, summarized in Table I.

A. Derivation of Reference Phase Duty Ratios With All Sensors

The three-phase boost PFC converter, shown in Fig. 1 has eight different modes of operation depending upon the different switching combinations of semiconductor devices. The boost inductor for "*k*"th phase ("*k*" could be *A* or *B* or *C*) gets charged

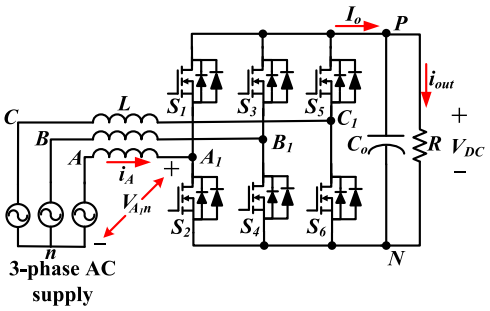

Fig. 1. Three-phase boost PFC rectifer.

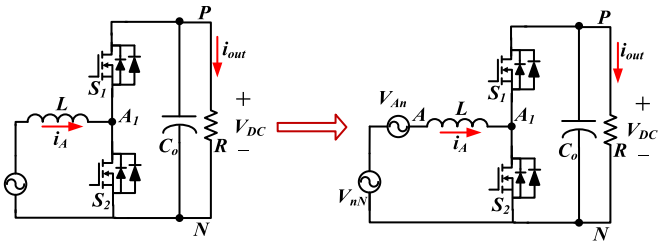

Fig. 2. One independent leg of a three-phase active boost-type rectifier.

with a rising slope of $V_{\rm kN}/L$ and discharges through top-side semiconductors with a falling slope of $(V_{\rm kN} - V_{\rm DC})/L$.

The charging and discharging times are governed by the duty ratio of the switch, which is directly determined from the individual phase duty ratios obtained from the PWM scheme. The calculation of individual phase duty ratios is based upon the analysis of the converter in terms of a coupled form of three single-phase ac–dc boost converters.

A three-phase boost PFC, shown in Fig. 1, consists of three coupled ac–dc boost converters with the same output $V_{\rm DC}$, one of which is shown in Fig. 2. According to Fig. 2, the output and input voltages of the converter are $V_{\rm DC}$ and $V_{\rm AN}$, respectively.

From volt–second balance, the generalized relationship between the dc-link voltage and any input phase voltage (phase "*k*") could be established from the principle of boost converter, according to

$$V_{\rm kN} = (1 - d_{\rm kL})V_{\rm DC} = d_{\rm kH}V_{\rm DC}. \tag{1}$$

Applying summation operator in (1) to both sides by varying phase "*k*" from *A* to *C*, the subsequent relationships are formed for a balanced three-phase ac system, i.e., $V_{\rm An} + V_{\rm Bn} + V_{\rm Cn} = 0$

$$\sum_{k=A}^{C} V_{\rm kN} = V_{\rm DC}\sum_{k=A}^{C} d_{\rm kH} \tag{2}$$

$$V_{\rm nN} = \frac{V_{\rm DC}\sum_{k=A}^{C} d_{\rm kH}}{3}. \tag{3}$$

Equation (3) provides the voltage difference between neutral point and dc-link negative terminal, which is the common coupling term among the three input voltages of the ac–dc converter. The voltage between the leg-midpoint and the negative dc-link terminal is 0 or $V_{\rm DC}$, depending on whether the corresponding lower leg switch is ON or OFF, respectively. Therefore, the switching average of the voltage across the leg-midpoint of "*k*"th phase to the negative terminal of dc link, i.e., V_{k1N} would be $d_{\rm kH}V_{\rm DC}$. Hence, for any decoupled ac/dc converter, the following relationship could be written:

$$\tilde{V}_{\rm An} + V_{\rm nN} = L\frac{di_k}{dt} + d_{\rm kH}V_{\rm DC}. \tag{4}$$

Applying summation operator to both sides of (1) and by varying phase "*k*" from *A* to *C*, the subsequent relationships are formed for a balanced three-phase system, i.e., $V_{\rm An} + V_{\rm Bn} + V_{\rm Cn} = 0$

$$(\tilde{V}_{\rm An} + \tilde{V}_{\rm Bn} + \tilde{V}_{\rm Cn}) + 3V_{\rm nN} = L\frac{d}{dt}\left(\sum_{k=A}^{C} i_k\right) + V_{\rm DC}\sum_{k=A}^{C} d_{\rm kH} \tag{5}$$

$$V_{\rm nN} = \frac{\sum_{k=A}^{C} V_{L,k} + V_{\rm DC}\sum_{k=A}^{C} d_{\rm kH}}{3}. \tag{6}$$

In a conventional linear feedback-only control with Sine-PWM technique, the instantaneous sum of all the duty modulation signals, generated from three outputs of inner-loop current compensators have 120° phase difference and, hence, add up to 0. This implies the presence of nonzero third and higher order harmonics in the inductor voltages and input currents

$$3V_{\rm nN} = V_{L,3}\cos(3\omega t) + \sum_{h\,=\,5,7,..} V_{L,h}. \tag{7}$$

Therefore, in order to eliminate the undesired third and higher order odd harmonics from the inductor current and inductor voltage waveforms, an additional duty ratio of "*x*" needs to be added to each of the current loop compensators' outputs, which can potentially nullify the effect of $V_{\rm nN}$ on the input line currents and inductor voltages. Hence, to eliminate the inductor voltage harmonics, the value of "*x*" should be $V_{\rm nN}/V_{\rm DC}$, i.e., $x = (d_{\rm AH} + d_{\rm BH} + d_{\rm CH})/3$, as implied from (6). Thus, using (1), the modified reference duty ratio of any switch is derived in discrete time domain as follows:

$$d_{\rm kH}[n] = \frac{\tilde{V}_{\rm kn} + V_{\rm nN}[n]}{V_{\rm DC\_ref}} = \frac{\tilde{V}_{\rm kn}}{V_{\rm DC\_ref}} + \frac{\sum_{k=A,B,C} d_{\rm kH}[n-1]}{3}\frac{V_{\rm DC}}{V_{\rm DC\_ref}}. \tag{8}$$

For example, in the case of phase "*A*" voltage, the final duty ratio could be formulated as follows:

$$d_{\rm AH}[n] = \frac{V_{\rm An}[n] + V_{\rm nN}[n]}{V_{\rm DC}} = K\sin(\omega n T_s) + \frac{\sum_{i=A,B,C} d_{\rm iH}[n-1]}{3}\frac{V_{\rm DC}}{V_{\rm DC\_ref}} \tag{9}$$

where $V_{\rm An}[n] = V\sin(\omega n T_s)$ and $K = V/V_{\rm DC\_ref}$. The first term in (9) denotes the phase "*A*" current compensator's (PI controller) output, and hence, the final duty reference is generated by the addition of the current controller's output and the additional common mode duty term.

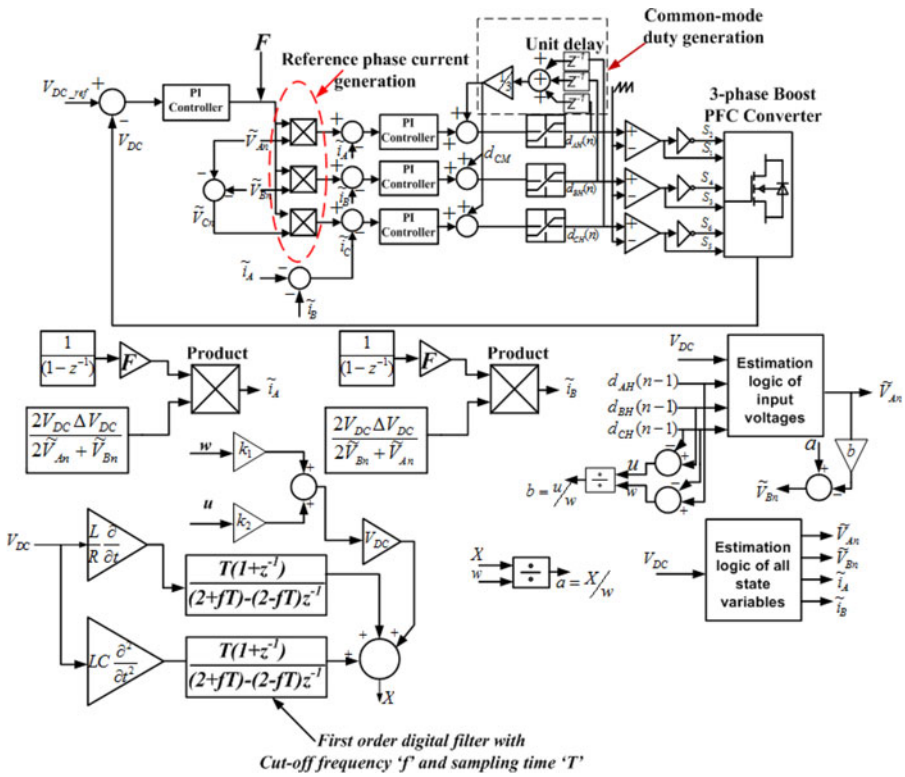

Fig. 3. Block diagram for the proposed control of a three-phase boost PFC.

Thus, the excess duty ratio term is injected additionally to each phase-current controller (PI-type) output to improve the power factor (PF). In order to eliminate four state variable measurements, used in the calculations of duty ratio derivations, it is required to estimate those using the converter dynamics and detailed time-domain modeling by maintaining the same method for control variable calculations. Detailed mathematical modeling of the three-phase boost PFC and the derivation of four estimated state variables are established in the following section.

B. Proposed Sensorless Control Algorithm

The control strategy aims at generating sinusoidal input currents to be exactly in phase with the input voltages, regulating the dc-link voltage at its reference value and maintaining a good input power quality. The proposed control logic, shown in Fig. 3, uses the information of dc-link voltage only and estimates the variation of other four state variables of the system. It overcomes the limitations of the conventional linear average current control in terms of control bandwidth and sensitivity to noise and also mitigates the observability problem at some extreme operating points in some methods [20]–[21]. In order to estimate the rest of the state variables, the time-domain mathematical equations governing the dynamics of the converter are used extensively, and thus, small-signal perturbation analyses are applied in order to determine the variation of each state variable from its previous operating point. Therefore, prior to performing perturbation analysis, it is useful to establish a thorough mathematical modeling of the converter through instantaneous time-domain relationships among all the state variables. The following parts of this section derive the method to estimate the unknown state variables from sampled value and ripple amount in the dc-link voltage. In addition, the DSP implementation with detailed time complexity of the proposed algorithm is presented in this section. In the following analyses throughout, in any discrete time-domain equation, any variable "*x*" denotes *x(n)*, i.e., its value at "*n*"th sample, if not specified exclusively.

1) Mathematical Modeling of the Converter: In a three-phase boost PFC converter, there are five state variables, i.e., dc-link voltage, two phase currents, and two input line-to-line voltages. Since different switching combinations would lead to the change in instantaneous dynamics of the converter, a switching-averaged model would be appropriate for the further analyses and modeling. Consequently, (10)–(12) could be formulated at different switching modes of PFC

$$\text{At "10\_"}, V_{\rm AB} = L\frac{di_A}{dt} - L\frac{di_B}{dt} + V_{\rm DC} \tag{10}$$

$$\text{At "01\_"}, V_{\rm AB} = L\frac{di_A}{dt} - L\frac{di_B}{dt} - V_{\rm DC} \tag{11}$$

$$\text{At "11\_" or "00\_"}, V_{\rm AB} = L\frac{di_A}{dt} - L\frac{di_B}{dt} \tag{12}$$

where the switching state of ""th phase S_i is represented as "1" if a high-side semiconductor device of the same phase is conducting and as "0" if a low-side device of the same phase is conducting and as '_', if either of the low-side or high-side device is conducting. Therefore, using these conventions, a generalized relationship between line-to-line voltages and switching states

of corresponding phases is established as

$$V_{\rm AB} = L\frac{di_A}{dt} - L\frac{di_B}{dt} + (S_A - S_B)V_{\rm DC}. \tag{13}$$

Similarly, the same concept could be applied to line voltage $V_{\rm AC}$ and could be obtained as

$$V_{\rm AC} = L\frac{di_A}{dt} - L\frac{di_C}{dt} + (S_A - S_C)V_{\rm DC}. \tag{14}$$

Since the above analyses are based on a particular switching combination in a switching cycle, it is required to make an averaged model over a switching cycle for estimating the unknown state variables, and thus, the following relationships could be formulated:

$$V_{\rm AB} = L\frac{di_A}{dt} - L\frac{di_B}{dt} + (d_{\rm AH} - d_{\rm BH})V_{\rm DC} \tag{15}$$

$$V_{\rm AC} = L\frac{di_A}{dt} - L\frac{di_C}{dt} + (d_{\rm AH} - d_{\rm CH})V_{\rm DC}. \tag{16}$$

In order to estimate the three unknown state variables in (15) and (16) (i.e., $V_{\rm AB}$, i_A, i_B), one of the vital conditions for any ideal converter dynamics will be instantaneous power balancing, which can be applied on three-phase boost rectifier, according to

$$\frac{{V_{\rm DC}}^2}{R} = V_{\rm An}i_A + V_{\rm Bn}i_B + V_{\rm Cn}i_C. \tag{17}$$

Equation (17) assumes the unity PF and lossless model of PFC. For a balanced three-phase system with an open neutral point, i.e., $V_{\rm An} + V_{\rm Bn} + V_{\rm Cn} = 0$ and $i_a + i_b + i_c = 0$; thus, (17) could be rewritten as

$${V_{\rm DC}}^2 = R[i_A(V_{\rm Bn} + 2V_{\rm An}) + i_B(V_{\rm An} + 2V_{\rm Bn})]. \tag{18}$$

Now, our aim is to estimate the small-signal changes of $\Delta V_{\rm An}$, $\Delta V_{\rm Bn}$, Δi_A, and Δi_B in terms of $V_{\rm DC}$ and $\Delta V_{\rm DC}$, which will be available from the measured data. Therefore, it is required to take a derivative of (18) with respect to time, which leads to

$$2V_{\rm DC}\frac{\partial V_{\rm DC}}{\partial t} = \frac{\partial}{\partial t}(R[i_A(V_{\rm Bn} + 2V_{\rm An}) + i_B(V_{\rm An} + 2V_{\rm Bn})]). \tag{19}$$

In the above equation, apart from $V_{\rm DC}$, rest of the four variables need to be estimated and in the following analyses, these will be represented by their respective estimators, i.e., $\tilde{V}_{\rm An}, \tilde{V}_{\rm Bn}, \tilde{i}_A, \tilde{i}_B$.

Adding (18) and (19) provides us the relationships, expressed in (20) and (21), which reduces the dependence of phase-neutral voltage by one unknown state variable. Instead of line-to-line voltage being dependent on two phase currents, a combination of the two subsequent equations make the phase-neutral voltage to only be a function of the corresponding phase current

$$\tilde{V}_{\rm An} = L\frac{d\tilde{i}_A}{dt} + \frac{3d_{\rm AH} - \sum_{i=A}^{C} d_{\rm iH}}{3}V_{\rm DC} \tag{20}$$

$$V_{\rm Bn} = L\frac{di_B}{dt} + \frac{3d_{\rm BH} - \sum_{i=A}^{C} d_{\rm iH}}{3}V_{\rm DC}. \tag{21}$$

Therefore, in order to derive the estimated instantaneous value of phase-neutral voltage, the observed perturbation in respective phase current at each cycle needs to be estimated from any related governing equation. The changes in respective phase currents are determined through the relationships obtained by performing partial differentiation of (23) with respect to the respective phase currents, shown in the subsequent relationships

$$2V_{\rm DC}\frac{\partial V_{\rm DC}}{\partial \tilde{i}_A} = R(2\tilde{V}_{\rm An} + \tilde{V}_{\rm Bn}) \tag{22}$$

$$2V_{\rm DC}\frac{\partial V_{\rm DC}}{\partial \tilde{i}_B} = R(2\tilde{V}_{\rm Bn} + \tilde{V}_{\rm An}) \tag{23}$$

$$\Delta\tilde{i}_A = \frac{2V_{\rm DC}\Delta V_{\rm DC}}{R(2\tilde{V}_{\rm An} + \tilde{V}_{\rm Bn})} \tag{24}$$

$$\Delta i_B = \frac{2V_{\rm DC}\Delta V_{\rm DC}}{R(2V_{\rm Bn} + V_{\rm An})} \tag{25}$$

$$\text{hence, } \frac{\Delta\tilde{i}_B}{\Delta\tilde{i}_A} = \frac{(2\tilde{V}_{\rm An} + \tilde{V}_{\rm Bn})}{(2\tilde{V}_{\rm Bn} + \tilde{V}_{\rm An})} \tag{26}$$

where $\Delta V_{\rm DC}$ is the dc output voltage error.

The above relation basically implies the relative change ratios of the estimated phase currents in terms of the estimated phase voltages. Equations (24) and (25) explicitly express the estimated phase current perturbations in terms of two estimated phase voltages. Therefore, if $\tilde{i}_A$, $\tilde{i}_B$ are known, the estimated phase voltages can be found out using (24) and (25). Now, the estimated changes in two phase currents would help in predicting the voltage across the boost inductors, which will again assist in estimating the phase-neutral voltages in (26) and (27). Therefore, the perturbation in phase currents obtained from (24) and (25) could be replaced in (22) and (23), and the following relationships could be established:

$$\tilde{V}_{\rm An}(n) = \frac{2LV_{\rm DC}\Delta V_{\rm DC}}{R(2\tilde{V}_{\rm An}(n-1) + \tilde{V}_{\rm Bn}(n-1))T_s} + \left(d_{\rm AH}(n-1) - \frac{\sum_{i=A}^{C} d_{\rm iH}(n-1)}{3}\right)V_{\rm DC} \tag{27}$$

$$\tilde{V}_{\rm Bn}(n) = \frac{2LV_{\rm DC}\Delta V_{\rm DC}}{R(2\tilde{V}_{\rm Bn}(n-1) + \tilde{V}_{\rm An}(n-1))T_s} + \left(d_{\rm BH}(n-1) - \frac{\sum_{i=A}^{C} d_{\rm iH}(n-1)}{3}\right)V_{\rm DC}. \tag{28}$$

Above two relationships basically demonstrate an interdependence between two estimated phase voltages. In the above two relationships, let us assume

$$k_1 = \left(d_{\rm AH}(n-1) - \frac{\sum_{i=A}^{C} d_{\rm iH}(n-1)}{3}\right) \tag{29}$$

$$k_2 = \left(d_{\rm BH}(n-1) - \frac{\sum_{i=A}^{C} d_{\rm iH}(n-1)}{3}\right). \tag{30}$$

Since, there are no measurements of phase-neutral voltages in previous *(n–1)*th samples, the estimation at *n*th sample is not feasible unless there is a known perturbation on the

corresponding phase voltage. Therefore, small-signal variation of phase voltage with other state variables is useful information and could be obtained through performing partial differentiation of (18) with respect to phase voltages. This mathematical operation would lead to the following relationships:

$$\begin{aligned} 2V_{\rm DC}\partial V_{\rm DC} &= R(2\tilde{i}_A+\tilde{i}_B)\partial\tilde{V}_{\rm An}=R(2\tilde{i}_B+\tilde{i}_A)\partial\tilde{V}_{\rm Bn} \\ &= R[(\tilde{V}_{\rm An}+2\tilde{V}_{\rm Bn})\partial\tilde{i}_B] \\ &= R[(\tilde{V}_{\rm Bn}+2\tilde{V}_{\rm An})\partial\tilde{i}_A] \end{aligned} \tag{31}$$

$$\frac{\Delta\tilde{V}_{\rm An}}{\Delta\tilde{V}_{\rm Bn}} = \frac{1+2^{\Delta\tilde{i}_B}/_{\Delta\tilde{i}_A}}{2+\Delta\tilde{i}_B/_{\Delta\tilde{i}_A}}. \tag{32}$$

From (26), substituting $\Delta\tilde{i}_B/\Delta\tilde{i}_A$ in terms of the estimated phase voltages in (32), the following relationship could be formulated:

$$\frac{\Delta\tilde{V}_{\rm An}}{\Delta\tilde{V}_{\rm Bn}} = \frac{5\tilde{V}_{\rm An}+4\tilde{V}_{\rm Bn}}{4\tilde{V}_{\rm An}+5\tilde{V}_{\rm Bn}}. \tag{33}$$

The above relationship depicts interdependence between the perturbations of estimated voltages of phases "*A*" and "*B,*" in terms of their estimated values. Therefore, once any of the two estimated values is known, the other can be found out from the relationship in (33).

By combining the above relationships, any two estimated phase voltages could be formulated by (34) and related hyperbolically to each other

$$\frac{\tilde{V}_{\rm An}-k_1\tilde{V}_{\rm DC}}{\tilde{V}_{\rm Bn}-k_2\tilde{V}_{\rm DC}} = \frac{\tilde{V}_{\rm An}+2\tilde{V}_{\rm Bn}}{\tilde{V}_{\rm Bn}+2\tilde{V}_{\rm An}}. \tag{34}$$

To determine the estimated phase voltages individually, another independent and irredundant relationship is required between them. It could be obtained from the switching averaged current through the dc link. The average dc-link current is the sum of currents through the top-side semiconductors, averaged over a switching cycle. The corresponding relationship is determined by

$$d_{\rm AH}i_A+d_{\rm BH}i_B+d_{\rm CH}i_C = C\frac{dV_{\rm DC}}{dt}+\frac{V_{\rm DC}}{R} \tag{35}$$

$$(d_{\rm AH}-d_{\rm CH})\frac{\partial i_A}{\partial t}+(d_{\rm BH}-d_{\rm CH})\frac{\partial i_B}{\partial t} = C\frac{\partial^2 V_{\rm DC}}{\partial t^2}+\frac{1}{R}\frac{\partial V_{\rm DC}}{\partial t}. \tag{36}$$

Replacing the estimated perturbations in phase currents by phase voltages from (35) and (36), another relationship, which is required to predict both phase voltages, could be established as follows:

$$(d_{\rm AH}-d_{\rm CH})\tilde{V}_{\rm An}+(d_{\rm BH}-d_{\rm CH})\tilde{V}_{\rm Bn} = X \tag{37}$$

where

$$\begin{aligned} X = {} & V_{\rm DC}[k_1(d_{\rm AH}-d_{\rm CH})+k_2(d_{\rm BH}-d_{\rm CH})] \\ & +\frac{L}{R}\frac{\partial V_{\rm DC}}{\partial t}+LC\frac{\partial^2 V_{\rm DC}}{\partial t^2}. \end{aligned} \tag{38}$$

"X" represents a known voltage term, calculated from the duty cycles, converter parameters, and measured dc-link voltage. Since the derivatives of dc-link voltage may introduce high-frequency noise into the system, a digital low-pass filter with a cutoff frequency same as switching frequency (i.e., $f=100$ kHz) is applied after each operation of time derivative in the DSP implementation, as shown in Fig. 3. Thus, by solving (34) and (37), both the unknown phase voltages could be properly estimated. The governing discrete domain relationships, which determine estimated phase voltages, are given by (39)–(43)

$$\begin{aligned} & 2(b^2-1)\tilde{V}_{\rm Bn}(n)^2+(V_{\rm DC}[(2b-1)k_1+(2-b)k_2]-4ab) \\ & \tilde{V}_{\rm Bn}(n)+(2a^2-2ak_1V_{\rm DC}+ak_2V_{\rm DC})=0. \end{aligned} \tag{39}$$

Hence, the estimated phase "*B*" voltage can be expressed as follows:

$$\tilde{V}_{\rm Bn}(n) = [-(V_{\rm DC}[(2b-1)k_1+(2-b)k_2]-4ab)+Q]/_{4(b^2-1)} \tag{40}$$

where, see (41) as shown at the bottom of this page.

The other solution of the quadratic equation in (41) will always be negative, which is not feasible and, hence, ignored. From (37), the final expression of estimated phase "*A*" voltage can be formulated in terms of the obtained phase "*B*" voltage as follows:

$$\tilde{V}_{\rm An}(n) = (a-b\tilde{V}_{\rm Bn}(n)) \tag{42}$$

$$\tilde{V}_{\rm Cn}(n) = -(\tilde{V}_{\rm An}(n)+\tilde{V}_{\rm Bn}(n)) \tag{43}$$

where

$$a = {}^{X}/_{(d_{\rm AH}-d_{\rm CH})} \tag{44}$$

$$b = {}^{(d_{\rm BH}-d_{\rm CH})}/_{(d_{\rm AH}-d_{\rm CH})}. \tag{45}$$

Therefore, any line transient in the input voltage would be reflected in terms of dc-link voltage ripple and phase duty ratios, which would help us in estimating the source disturbance through (37) and (38). The converter response to the line transient is demonstrated in Section III with experimental results. Once the phase voltage estimators are determined, the change in respective phase currents within a sample can also be calculated using (24) and (25). Then, the derived perturbation in phase currents can be integrated using a discrete domain accumulator to obtain the estimated present value of operating points. Thus, the present samples of input phase currents can be derived as

$$Q = \sqrt{(V_{\rm DC}[(2b-1)k_1+(2-b)k_2]-4ab)^2-8(b^2-1)(2a^2-2ak_1V_{\rm DC}+ak_2V_{\rm DC})} \tag{41}$$

follows:

$$\tilde{i}_A(n) = i_A(n-1) + \frac{1}{R}\frac{2V_{\rm DC}\Delta V_{\rm DC}}{2\tilde{V}_{\rm An}(n)+\tilde{V}_{\rm Bn}(n)} \quad (46)$$

$$\tilde{i}_B(n) = i_B(n-1) + \frac{1}{R}\frac{2V_{\rm DC}\Delta V_{\rm DC}}{2\tilde{V}_{\rm Bn}(n)+\tilde{V}_{\rm An}(n)}. \quad (47)$$

As the voltage loop PI output *F* corresponds to the active power of the converter [26], it could be assumed to be proportional to $V_{\rm DC}^2/R$, which is directly proportional to $1/R$ assuming a constant output voltage. From the control loop, we have the followings:

$$\tilde{i}_A(n) = F\tilde{V}_{\rm An}(n) \quad (48)$$

$$\tilde{i}_B(n) = F\tilde{V}_{\rm Bn}(n). \quad (49)$$

Plugging the phase currents from (48) and (49) into the power balancing relation (18), "*R*" can be treated in terms of "*F*" as

$$R = \frac{{V_{\rm DC}}^2}{2F(\tilde{V}_{\rm An}(n)^2 + \tilde{V}_{\rm Bn}(n)^2 + \tilde{V}_{\rm An}(n)\tilde{V}_{\rm Bn}(n))}. \quad (50)$$

Thus, the load resistance *R* can be estimated in terms of the measured variable, i.e., $V_{\rm DC}$, the estimated phase voltages and the voltage controller output, i.e., *F*, which directly indicates the active power reference. As the load profile changes from no load to full load, the value of "*F*" increases from 0 to a full-scale constant value. Substituting the obtained expression of "*R*" in (48) and (49), the load independent relationships of the estimated currents are obtained

$$\tilde{i}_A(n) = i_A(n-1) + \frac{4F(\tilde{V}_{\rm An}(n)^2 + \tilde{V}_{\rm Bn}(n)^2 + \tilde{V}_{\rm An}(n)\tilde{V}_{\rm Bn}(n))\Delta V_{\rm DC}}{V_{\rm DC}[2\tilde{V}_{\rm Bn}(n)+\tilde{V}_{\rm An}(n)]} \quad (51)$$

$$\tilde{i}_B(n) = i_B(n-1) + \frac{4F(\tilde{V}_{\rm An}(n)^2 + \tilde{V}_{\rm Bn}(n)^2 + \tilde{V}_{\rm An}(n)\tilde{V}_{\rm Bn}(n))\Delta V_{\rm DC}}{V_{\rm DC}[2\tilde{V}_{\rm Bn}(n)+\tilde{V}_{\rm An}(n)]}. \quad (52)$$

Thus, the proposed sensorless control algorithm is framed to be generalized and independent of load power. The initial values of the estimated phase currents are obtained by putting $n = 0$ in (51) and (52) and assuming $i_A(-1) = i_B(-1) = 0$.

During the start-up transient period, although unity PFC operation is not valid, there are four conditions, presented as follows which are applicable for estimating the unknown variables during this period:

1) two relationships in (20) and (21) between the estimated phase voltages and phase currents;
2) instantaneous power balance equation in (18);
3) the output capacitor current in terms of the dc voltage and phase currents.

Using these four relationships, the four variables, i.e., phase voltages and phase currents could be mathematically solved and shown in (53) and (54). Once the dc voltage ripple gets locked within a limited band with a constant average value, the steady-state analyses are used to control the converter and to maintain the PFC operation

$$\tilde{V}_{\rm Bn}(n) = \frac{-(V_{\rm DC}[(2b-1)k_1 + (2-b)k_2] - 4ab)}{4(b^2-1)} \quad (53)$$

$$\tilde{V}_{\rm An}(n) = (a - b\tilde{V}_{\rm Bn}(n)). \quad (54)$$

The estimated currents follow the same relationship with the phase voltages, as in steady-state analyses, as shown in (46) and (47).

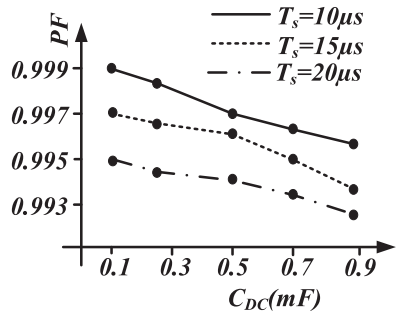

Fig. 4. PF versus output capacitor at different sampling frequencies.

C. Robustness of the Estimation Accuracy

The accuracy of the phase voltage estimation does not solely depends on $\Delta V_{\rm DC}$, rather depends on the ratio of the dc voltage ripple and the sampling time, i.e., $\Delta V_{\rm DC}/\Delta T_s$, as can be seen from (21) and (22). Therefore, even if the dc-link ripple amount is less, the same amount of estimation accuracy could be achieved if sampling frequency is increased, i.e., T_s is reduced to keep $\Delta V_{\rm DC}/\Delta T_s$ unchanged. However, T_s has a lower limit according to the execution time of the control logic, which is 5 μs in our case. Since PF is one of the appropriate justification parameters for determining the estimation accuracy, a graph plotting PF versus output capacitor at different sampling times (obtained experimentally) is shown in Fig. 4. The PF increases at a higher sampling frequency for a particular output capacitor and the PF improves with increasing sampling frequency at larger output capacitor. Therefore, there is less than1% degradation in PF for a ten times larger capacitor, i.e., 90% reduction in output voltage ripple.

The estimation accuracy is dependent on the sampling frequency; higher sampling rate improves the accuracy. Therefore, as long as the sampling frequency is fixed, reducing switching frequency will not impact the estimation accuracy. However, THD gets affected with the reduction of switching frequency. Therefore, from the viewpoint of estimation accuracy, a PFC with the proposed control is scalable upto a considerably low switching frequency (as low as 5 kHz) with a sampling frequency of 100 kHz, although the THD of the input currents deteriorates to 11%, as obtained from the simulation study.

Another noteworthy concern with this control method could be the detection of short-circuit fault at the line or load side of the converter. In a conventional control with current sensors,

the fault current could be instantaneously detected and action could be taken. In case of this proposed control, the current estimation takes one complete sampling cycle, and hence, short-circuit occurrence would be updated with one sampling cycle delay from the actual occurrence of fault. However, this delay would be in the order of few microseconds, depending on the sampling frequency. In a converter with 400 Hz ac input line and with a program execution time (i.e., sampling time) of 10 μs, the delay in reporting the fault would be 10 μs/2.5 ms $=$ 0.4% of one power cycle, which is reasonably fast for most of the applications.

D. Parameter Uncertainty Analysis

Sensitivity analyses are performed to determine the deviation of estimation accuracy with the variation of *LC* component values. The phase voltage expressions in (40) and (41) as well as the phase currents in (51) and (52) are expanded to verify the sensitivity of the voltages and currents to *LC* parameters as follows:

$$\tilde{V}_{\mathrm{An}}(n) = p_1 + q_1\sqrt{L} = r_1 + s_1\sqrt{C} \tag{55}$$

$$\tilde{i}_A(n) = p_2 + q_2\sqrt{L} = r_2 + s_2\sqrt{C} \tag{56}$$

$$\tilde{V}_{\mathrm{Bn}}(n) = p_3 + q_3\sqrt{L} = r_3 + s_3\sqrt{C} \tag{57}$$

$$\tilde{i}_B(n) = p_4 + q_4\sqrt{L} = r_4 + s_4\sqrt{C} \tag{58}$$

where p_i and q_i are independent of L and r_i and s_i ("i" $= 1$ to 4) are independent of C, as can be found from the final estimation equations of the phase voltages and currents and accordingly formulated in (59), (60), and (61) shown at the bottom of the page.

Other p_i and $q_i s$ are functions of p_1, q_1, r_1, and s_1 in the following ways: $p_2 = Ap_1$; $q_2 = Aq_1$; $r_2 = Ar_1$; $s_2 = As_1$; $p_3 = -bp_1$; $r_3 = -br_1$; $q_3 = q_1$; $s_3 = s_1$; $p_4 = Ap_3$; $q_4 = Aq_3$; $r_4 = Ar_3$; $s_4 = As_3$.

The estimation sensitivity of a variable Y with respect to a parameter "w" is generally defined as follows, i.e., the ratio between the relative changes of the two variables

$$S_w{}^Y = \frac{\partial Y/Y}{\partial w/w}. \tag{62}$$

TABLE II
ESTIMATION INACCURACY WITH *LC* PARAMETER VARIATIONS

% variation in L or C	Estimation inaccuracy (%)	Power factor
0% (no change)	0	0.999
5%	2.5%	0.996
10%	5%	0.995
20%	10%	0.99

Therefore, the following sensitivity relations can be obtained:

$$S_C{}^{V_{\mathrm{An}}} = S_L{}^{V_{\mathrm{An}}} = S_C{}^{V_{\mathrm{Bn}}} = S_L{}^{V_{\mathrm{Bn}}} = \frac{1}{2} \tag{63}$$

$$S_C{}^{i_A} = S_L{}^{i_A} = S_C{}^{i_B} = S_L{}^{i_B} = \frac{1}{2}. \tag{64}$$

This analysis implies that if a $\pm p\%$ variation is made in L and C values, the estimation accuracy could be affected by $\pm p/2\%$. Its impact on the PF, obtained from the simulation study, is detailed in Table II.

Therefore, even with 20% parameter uncertainty, the PF deteriorates by 1%, which proves the robustness of the proposed control.

The uncertainty in load resistance value R does not really affect the estimation as the proposed control does not depend on the load resistance value. This is because "R" can be treated as a function of estimated voltages and the voltage loop controller output as opposed to *LC* components, which are independent parameters. Therefore, the control method remains unaffected with the variation of R or any load transients.

E. DSP Implementation

The proposed control logic is digitally implemented in a floating point DSP TMS320F28335. The control algorithm includes a voltage-mode PI controller in discrete domain and estimation of four unknown variables using the method outlined in the earlier section. Although a conventional linear averaged current mode control with all sensor measurements uses a voltage loop PI controller, the main difference from the proposed control lies in the reference current generation and estimating the feedbacks

$$p_1 = r_1 = \frac{-(V_{\mathrm{DC}}[(2b-1)k_1 + (2-b)k_2])}{4(b^2-1)} \tag{59}$$

$$q_1 = \frac{4b - \sqrt{(V_{\mathrm{DC}}[(2b-1)k_1 + (2-b)k_2])^2 + 8(b^2-1)(2k_1V_{\mathrm{DC}} - k_2V_{\mathrm{DC}})}}{4(b^2-1)} \times \frac{V_{\mathrm{DC}}[k_1(d_{\mathrm{AH}} - d_{\mathrm{CH}}) + k_2(d_{\mathrm{BH}} - d_{\mathrm{CH}})] + \frac{1}{R}\frac{\partial V_{\mathrm{DC}}}{\partial t} + C\frac{\partial^2 V_{\mathrm{DC}}}{\partial t^2}}{(d_{\mathrm{AH}} - d_{\mathrm{CH}})} \tag{60}$$

$$s_1 = \frac{4b - \sqrt{(V_{\mathrm{DC}}[(2b-1)k_1 + (2-b)k_2])^2 + 8(b^2-1)(2k_1V_{\mathrm{DC}} - k_2V_{\mathrm{DC}})}}{4(b^2-1)} \times \frac{V_{\mathrm{DC}}[k_1(d_{\mathrm{AH}} - d_{\mathrm{CH}}) + k_2(d_{\mathrm{BH}} - d_{\mathrm{CH}})] + \frac{L}{R}\frac{\partial V_{\mathrm{DC}}}{\partial t} + \frac{\partial^2 V_{\mathrm{DC}}}{\partial t^2}}{(d_{\mathrm{AH}} - d_{\mathrm{CH}})} \tag{61}$$

TABLE III
COMPARISON AMONG DIFFERENT CONTROL METHODS IN THE SAME DSP CORE

Control technique	Interrupt execution time (μs)	Maximum possible sampling frequency (kHz)	THD (%)
Linear averaged current mode control	4 μs	250 kHz	4.4%
Vector control with SVPWM	15 μs	66 kHz	3.5%
The proposed sensorless control	10 μs	100 kHz	4.3%

TABLE IV
KEY DESIGN SPECIFICATIONS OF THE THREE-PHASE BOOST PFC

Parameters	Values	Quantity
Input voltage ($V_{\rm in}$)	120 V	-
Input frequency ($f_{\rm in}$)	400 Hz	-
Output voltage reference ($V_{\rm DC\_ref}$)	400 V	-
Output power ($P_{\rm out}$)	2.2 kW	-
Switching frequency ($f_{\rm sw}$)	100 kHz	-
Boost inductor	400 μH	3
DC-link capacitor	100 μF (= 20 μF$*$5)	5
MOSFETs	SiC (1.2 kV/24 A)	6

of phase currents. Therefore, there is a certain difference in logic complexity between these two methods. Using the same processor configuration, conventional averaged current mode control takes 4 μs for computing the program execution loop, where discrete domain implementation of three current loop PI controllers consumes 60% of total execution time. On the other hand, our proposed control logic takes 10 μs for one complete execution, where estimation of the unknown state variables and generation of current loop references take 8.5 μs, i.e., 85% of total computation time. Therefore, there should be a minimum time interval of 10 μs between two consecutive sets of samples of dc-link voltage, assuming 100% CPU utilization in a single-core DSP. As a result, the effective switching frequency should be kept below the maximum sampling frequency, which is 100 kHz in this implementation technique. Furthermore, in order to control three-phase boost PFC, space vector PWM with all the sensor measurements has been implemented in the same DSP core to make a comparison of computational complexity among different digital domain implementation methods. There are several complicated algebraic calculations and trigonometric operators, associated with the sector determination and duty cycle calculations in this modulation strategy. According to our implementation method, overall control logic with Space Vector Pulse Width Modulation (SVPWM) takes 15 μs for one complete execution of interrupt loop, whereas the sector determination itself takes more than 50% of the total time. Hence, the sampling frequency and effective switching frequency are limited below 66 kHz in a single-core DSP. Table III demonstrates the difference in time complexity, measured power quality with different control methodologies in a single-core DSP.

As can be seen from Table III, the prospective sensorless control method can achieve reasonably low THD and high switching frequency operation. In terms of power quality, the proposed

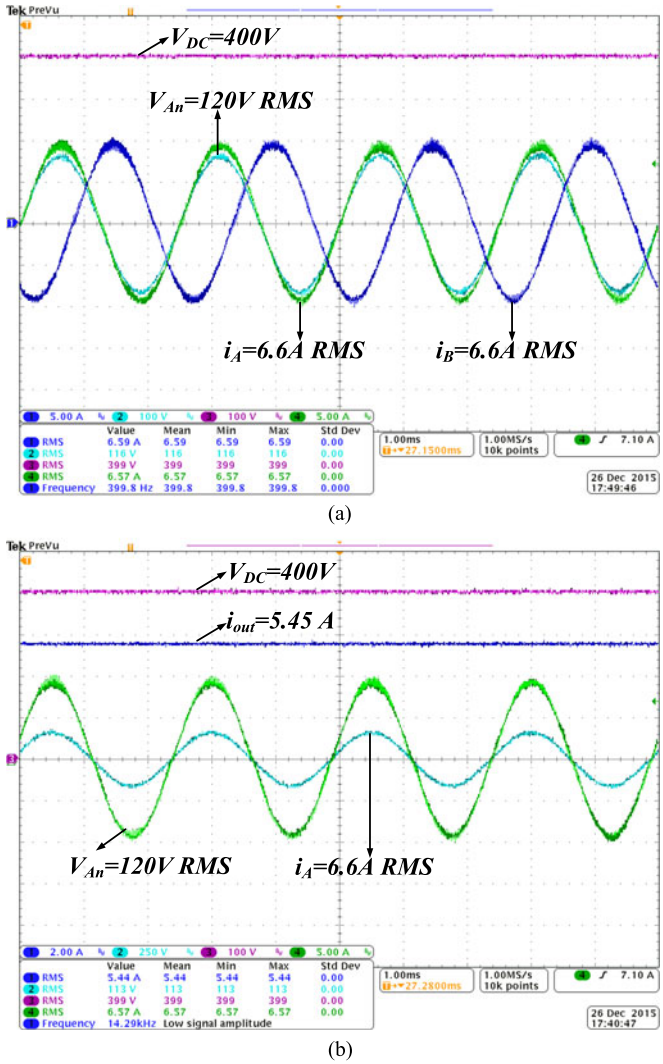

Fig. 5. Experimental waveforms of the converter at 2.18 kW. (a) $V_{\rm DC}$ = 400 V, i_A (rms) = i_B (rms) = 6.58 A, $V_{\rm An}$ (rms) = 120 V, $P_{\rm out}$ = 2.18 kW. (b) $V_{\rm DC}$ = 400 V, $i_{\rm out}$ = 5.44 A, i_A (rms) = 6.57 A, $V_{\rm An}$ (rms) = 120 V, $P_{\rm out}$ = 2.18 kW.

algorithm provides comparable results as other conventionally existing methods with an additional benefit of reducing four sensor measurements. In order to validate and establish the superiority of the prospective control, the converter performance is evaluated using the experimental results in Section III.

III. EXPERIMENTAL RESULTS

As a verification of the proposed single sensor estimation methodology, a 2.2-kW experimental prototype of a three-phase active boost rectifier is designed and developed. The PFC converter is designed for working at nominal 120-V phase-neutral 400 Hz ac input and 400 V regulated dc-link voltage. Specification details of some key design parameters of the converter are listed in Table III.

The capacitor needs to be large enough to suppress the voltage ripple [as low as 5% (Δ_v) of minimum dc-link voltage ($V_{o,\min}$)] caused by low-frequency line voltage and this is formulated in (65). Also, assuming no requirement for hold-up time, the

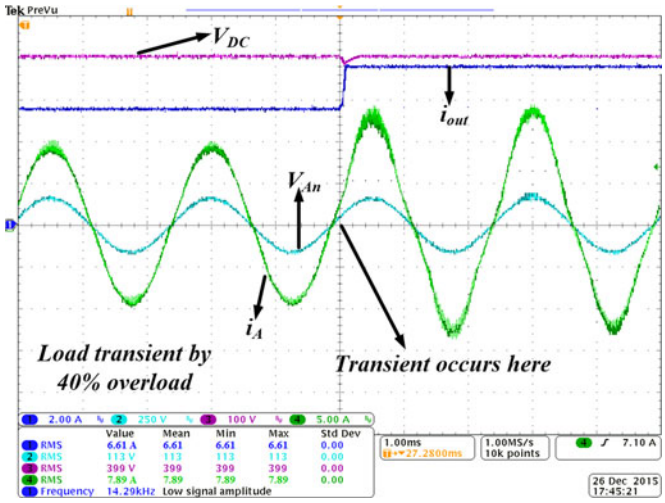

Fig. 6. Experimental waveforms of the converter under load transient from 2.25 to 3.15 kW at 400 Hz source frequency and $V_{\mathrm{An}} = 120\,\mathrm{V}$ rms, $V_{\mathrm{DC}} = 400\,\mathrm{V}$.

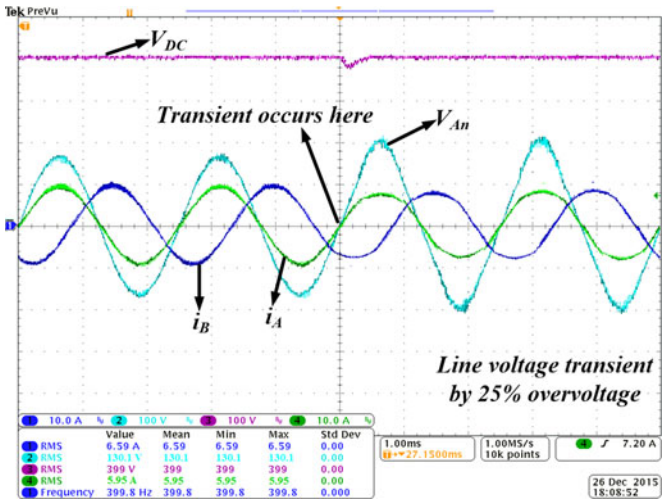

Fig. 7. Experimental waveforms of the converter under input line transient from 120 to 150 V phase-neutral rms at 400 Hz source frequency and $V_{\mathrm{DC}} = 400\,\mathrm{V}$.

dc-link capacitance value is set at 100 μF, according to the following equation:

$$C_o = \frac{P_{o,\max}}{\Delta_V 2\pi f_{\mathrm{in}} {V_{o,\min}}^2}. \tag{65}$$

The value of selected boost inductance is of 400 μH, which is required per phase to limit the maximum possible ripple amount within 5% of rms magnitude of the inductor current.

The dc-link voltage is selected based on the modulation index of the converter, which is set at 0.75, in order to avoid overmodulation effect [1]. With consideration of efficiency and power density, the switching frequency is selected at 100 kHz. The proposed sensorless control is implemented in TMS320F28335 DSP platform (floating point) and PFC hardware is tested with this control methodology up to 2.2 kW load power at 100 kHz switching frequency with the specifications listed in Table IV.

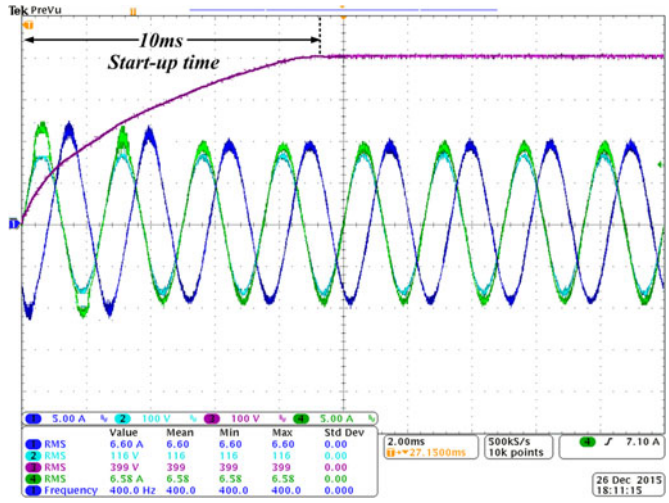

Fig. 8. Start-up waveforms of the converter with steady-state dc voltage $(V_{\mathrm{DC}}) = 400\,\mathrm{V}$.

Fig. 5(a) shows the steady-state operation of the PFC converter at 120-V phase-neutral rms, 400 Hz ac input, dc-link reference of 400 V, and 2.2 kW output power. According to Fig. 5(a), the dc-link voltage is regulated within ± 3 V ripple. Fig. 5(b) shows the load voltage along with the load current for a more accurate calculation of output power, as the load resistance value might not be exactly constant due to transients and temperature rise. Fig. 5(b) clearly demonstrates the unity PF operation of the converter, as the input phase "A" current and voltage are exactly in phase. The experimental results at 2.2 kW exhibit a conversion efficiency of 98.3% and a THD of 4.3%, which outperform the reported THD and efficiency values in some of the existing sensorless control approaches [12], [13], [18], [20], [32] and, hence, indicates a more improved power quality of the converter. The efficiency matches well to the theoretical calculations based on the loss analysis presented in [29] and [31].

Furthermore, the converter is also tested in different load and line conditions to check the accuracy of the proposed control logic at variable operating conditions. A 40% step increment in load from 2.25 to 3.15 kW is applied during a running condition with nominal load, and the output voltage is settled at its reference value within ten switching cycles, as shown in Fig. 6. Phase current amplitude increases by 40% and maintains a unity PFC operation during overload.

Also, during a 25% overvoltage line transient (from 120 to 150 V phase-neutral rms) applied at the input phase voltage, shown in Fig. 7, the proposed controller is able to accurately estimate the inductor currents and maintain the stability of the closed-loop system with an input PF of 0.997 and a settling time of 0.2 ms for dc-link voltage. The converter exhibits an output voltage ripple of $\pm 0.5\%$, an efficiency of 98.3%, and a THD of 4.3%, both before and after the line and load transients.

Fig. 8 shows the start-up transient waveforms of the converter, in order to evaluate the start-up performance of the proposed control. As can be seen from the experimental waveforms, the converter takes 10 ms (four input ac line cycles) to reach the

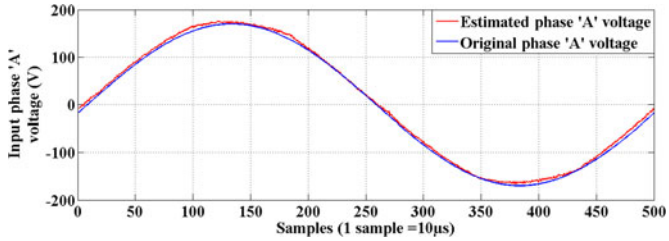

Fig. 9. Estimated and original phase "*A*" voltages.

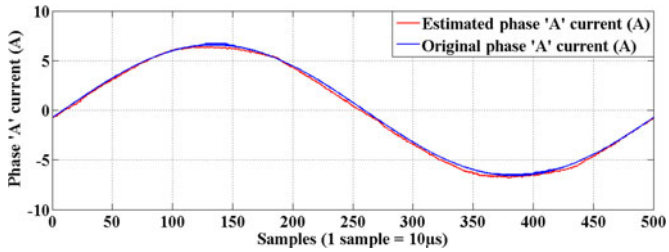

Fig. 10. Estimated and original phase "*A*" currents.

steady state with settled-down output dc-link voltage without any overshoot. Also, the start-up phase current is limited below 12 A, which is less than the double of its steady-state rms value.

Furthermore, in order to illustrate the accuracy of the voltage and current estimation, the original and estimated voltage and current of phase "A" are shown in Figs. 9 and 10. Since there is no provision of observing the estimated values in oscilloscope (as it is computed in the program), both the original and estimated values in the experiment are exported to the MATLAB and plotted. According to Figs. 9 and 10, both the estimated phase voltage and current follow their original values very closely in the experiment, which proves the high accuracy of estimation.

The maximum measured inaccuracy of both estimated voltage and current is limited below 2% of their original values.

IV. Conclusion

In this paper, a novel, cost-effective, and reliable methodology to control a three-phase boost PFC rectifier using just one voltage sensor and eliminating four other required sensors is introduced. This control principle is developed by estimating the four unknown state variables from the present state and ripple content of dc output voltage and detailed modeling of converter dynamics. The proposed sensorless estimation technique enables stable operation of the converter independent of the output load. A 2.2-kW three-phase boost PFC converter prototype is built and tested under different line and load conditions to illustrate the effectiveness of the proposed control technique. A conversion efficiency of 98.3%, THD as low as 4.3%, output voltage ripple less than $\pm 2\%$ (peak-peak), and an input PF more than 0.999 are achieved according to the test results at 120-V rms ac line input and a regulated dc-link voltage of 400 V. The prospective control logic also enables the converter to exhibit similar performance individually at 40% overload and 25% line overvoltage. Furthermore, owing to the fact that the prospective control algorithm is mainly framed on the basis of general modeling of converter dynamics, this sensorless estimation method could be potentially implemented digitally in other PFC topologies, with similar plant characteristics.

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