Characterization and Analysis of an Innovative Gate Driver and Power Supplies Architecture for HF Power Devices With High *dv/dt*

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***Abstract*—This paper presents a specific architecture for a low-side/high-side gate driver implementation for power devices running at high switching frequencies and under very high switching speeds. An electromagnetic interference (EMI) optimization is done by modifying the parasitic capacitance of the propagation paths between the power and the control sides, thanks to a specific design of the circuit. Moreover, to reduce the parasitic inductances and to minimize the antenna phenomenon, the paper studies which elements of the drivers' circuitry must be brought as close as possible to the power parts. This is important when the ambient temperature of the power device becomes critical, for instance, in automotive and aeronautic applications. Simulations and experiments validate the advantages of the proposed architecture on the conducted EMI problem.**

***Index Terms*—*dv/dt* immunity, gate driver, gate driver architecture.**

I. Introduction

NOWADAYS, robust power electronics systems are implemented in the automotive, energy management, and aeronautic applications in order to increase the performances and the working temperature of the energy conversion while being more compact. Concurrently, the classic silicon (Si) power components have reached their theoretical limitations, especially in terms of operating frequency and temperature. The wide-bandgap (WBG) semiconductors such as the gallium nitride (GaN) and silicon carbide (SiC) are excellent candidates to replace the Si-based counterparts in the coming years because these new materials allow the power converters to be smaller and more efficient at high operating temperatures [1]. SiC devices are still expensive and more suitable for high-power and high-voltage applications (above 1 kV). On the other hand, GaN devices have been improved lately and seem to be suitable for applications below $1\,\mathrm{kV}/30\,\mathrm{A}$. Moreover, today WBG power devices operate at high temperature up to 200 °C and at high switching frequencies above 1 MHz [2]–[5].

Manuscript received April 1, 2016; revised July 5, 2016 and September 2, 2016; accepted October 13, 2016. Date of publication October 21, 2016; date of current version March 24, 2017. This work was supported in part by the BPI France and the OSEO under Project MEGaN. Recommended for publication by Associate Editor B. Lehman.

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Digital Object Identifier 10.1109/TPEL.2016.2619859

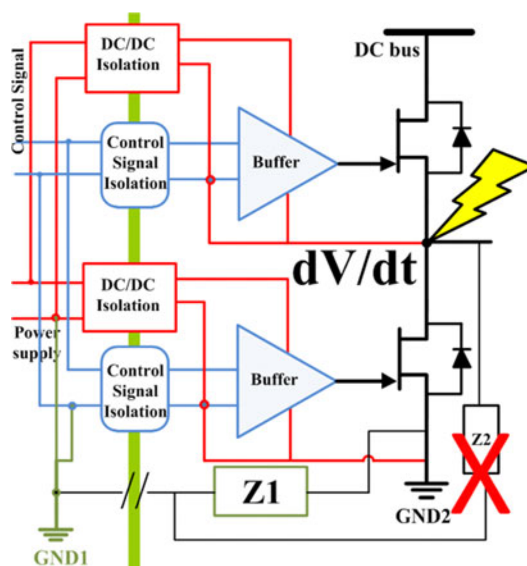

Fig. 1. Gate driver circuit with conventional architecture.

To overcome the state of the art of the power electronics devices with Si components, GaN HEMTs are good candidates. However, new gate drivers and associated supplies must be redesigned to take advantage of the capabilities of the new devices.

Fig. 1 shows that the switching transition dv/dt of advanced GaN-based active power devices increases up to $100\,\mathrm{V/ns}$ [6]–[9] at high switching frequencies. Thus, the parasitic inductances and capacitances located between the gate driver and the surrounding elements are greatly excited. As a consequence, electromagnetic interference (EMI) phenomena are conducted through the parasitic capacitances when dv/dt is generated at the middle point of the inverter leg. This causes significant disturbing currents, therefore the conducted and radiated EMI become a major problem in the system. These EMI disturbances, combined with nonadapted design of the gate driver and the supplies, limit designers in gaining a maximal benefit from the outstanding characteristics of the new generation of power devices.

Then, a special work must be engaged toward, minimizing the parasitic capacitor values, optimizing the circuit architecture

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and the gate driver IC (Integrated Circuit). The objective is to decrease the parasitic influences on the proper operation of the power converter, especially between the high-side and the low-side control modules of the gate driver.

This paper proposes an architecture with minimized EMI propagation pathways. Simulations and experiments are provided to validate the advantages of the proposed architecture on the conducted EMI problem. Following the analysis of this work, recommendations are provided stating that not only the gate driver buffer should be integrated very close to the power device. This is developed in the last section of this paper.

II. Architecture of the Gate Driver and the Supplies

A. Conventional Architecture for Gate Drivers

A conventional low-side/high-side gate driver circuit architecture, including isolation stages for power supplies and control units, is shown in Fig. 1.

In this architecture [10]–[12], two grounds are depicted. GND1 is the ground or reference potential of the remote control circuit and GND2 is the reference potential of the power circuit. Both GND1 and GND2 are isolated from each other, such as on one hand, isolated supply converters are implemented in order to enable the isolation dedicated to the power supply parts, and, on the other hand, optocouplers are used to isolate the paths for the control signals. A green barrier shows up the physical location of this strong isolation in the figures. Two important impedances are presented in Fig. 1. $Z1$ represents the nonideal isolation between GND1 and GND2 and is the sum of the parasitic impedances between both grounds. $Z2$ is the classical and often studied common mode parasitic impedance between the middle point of the power leg and the ground of the primary side of the control circuit [13], [14]. This paper will focus on the perturbations of the power circuit on the control of the drivers flowing through $Z1$.

Power converters operate by driving the high-side and the low-side gate of the power transistors with complementary signals. With the introduction of advanced power devices, higher constraints are applied to the gate driver stages such as higher switching frequencies, higher dv/dt, and higher precision in switching transition time location in order to minimize the negative impact of the conducted EMI. Overcoming these constraints would allow the GaN–GaN direct commutations [15]. As a consequence, the conventional switching cells will operate at very high switching frequencies, above several MHz with dv/dt at the middle point in the range of or above $100\,\mathrm{V/ns}$ (see Fig. 2).

In the case of the GaN HEMT transistors, which do not have body diode, the switching at HF requires an optimized dead time. Accurate propagation delays of around 10 ns are usually required but lead to the implementation of an isolation stage with poor isolation ratings and high parasitics [16]. On the other side, the parasitic inductances that cause propagation delays and magnetic couplings between the power devices and the gate drivers need to be reduced. This can be obtained by working at a packaging level and designing a specific gate driver that is

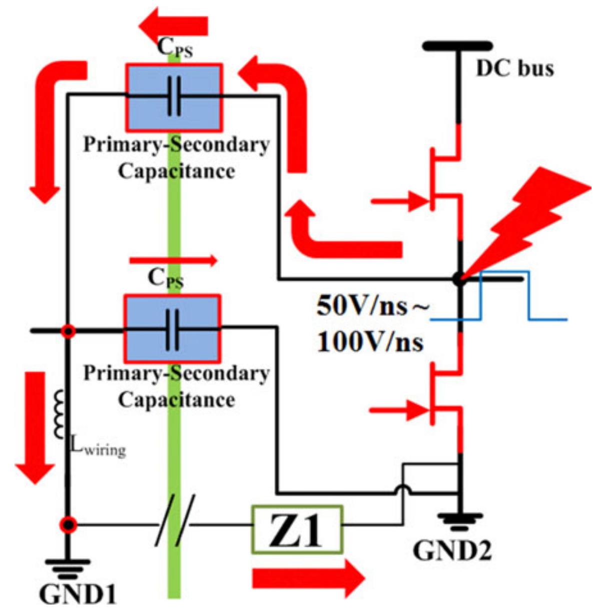

Fig. 2. Simplified circuit with power supplies + main disturbing current propagation pathway.

placed very close to the power transistors [17]–[19]. Nevertheless, parasitic propagation paths remain between the gate driver and the control parts through the gate driver supplies and the gate signal isolators. To overcome the conducted EMI problem, the parasitic capacitances need to be reduced or the propagation pathways need to be routed in a way that the high noisy currents in the common mode do not pass through the driver circuit when strong *dv/dt* occurs.

B. Proposed High-Side and Low-Side Driver and Supply Architecture for an EMI Optimization

To overcome the EMI issue at high switching frequencies and especially under high dv/dt, a new gate driver circuitry architecture for high switching speed components is depicted in Fig. 3.

Changing the EMI current paths can limit the interactions between the converter modules. The proposed approach implements the high rating isolation stages only on the low-side devices. In such a way, most disturbances circulate within the power side, especially if most of the driver elements can be integrated within the same package as the power devices. In this architecture, the control signal is transferred to the high side through the low-side gate driver components. In the same way, the input of the supply of the high-side gate driver is directly connected to the output of the supply of the low-side gate driver.

In the high-frequency (HF) equivalent circuit of the architectures in order to highlight the advantages of the proposed architecture, the effects of high dv/dt in the conventional architecture are first analyzed and detailed. Fig. 4 shows the parasitic elements around the power supplies (TRACO TMA1515S) and the isolations of the control signals (Optocoupler HPCL2211). Each power supply has two parasitic inductances on the primary

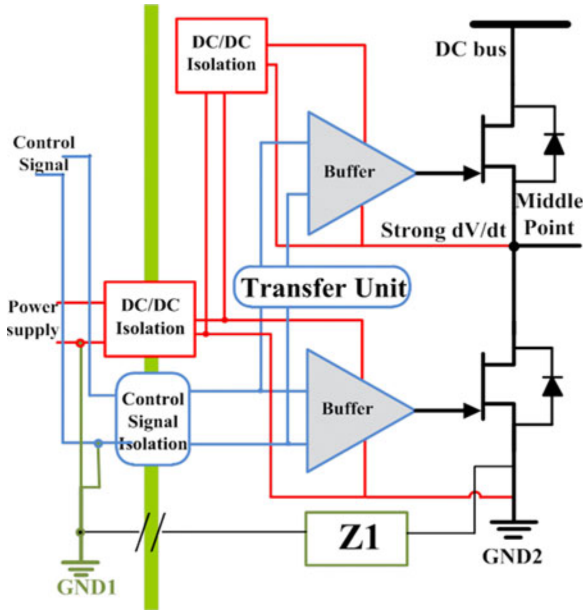

Fig. 3. Proposed architecture of the gate driver circuitry.

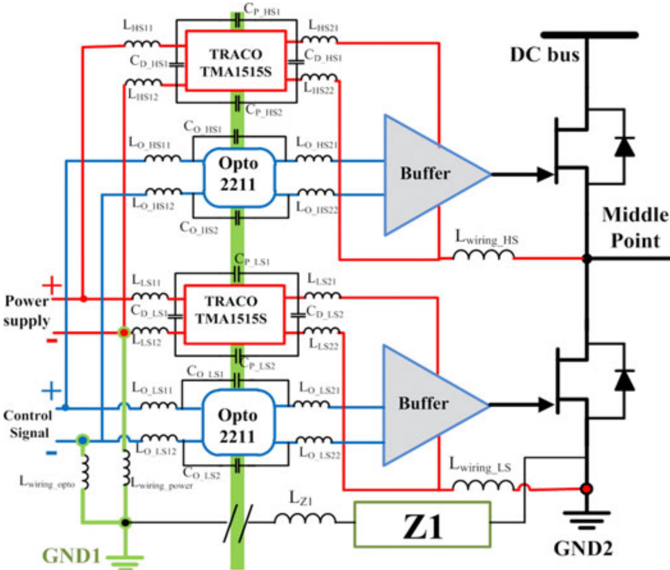

Fig. 4. Parasitic elements around the power supplies and the control signal insulators in a conventional architecture.

side and two parasitic inductances on the secondary side. There are also input and output decoupling capacitors, and two parasitic capacitors between the primary and the secondary sides. The optocouplers have a similar set of parasitic inductances as the power supply. There are also parasitic capacitances on both primary and secondary sides. In Fig. 4, the parasitic inductances between the power supplies and the source terminals of the power transistors are also considered. Furthermore, parasitic inductances have been added between the power supplies, the optocouplers, and the ground of the remote control circuitry.

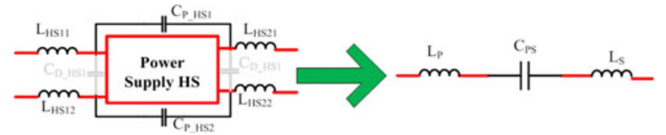

Fig. 5. HF equivalent circuit of an isolated dc–dc power supply.

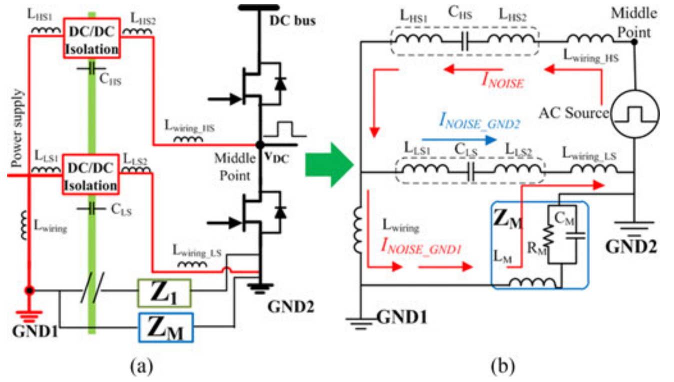

Fig. 6. Conventional architecture: (a) driver circuit with only power supplies and (b) HF equivalent circuit.

In the HF range, the input and the output capacitors of the power supplies and of the optocouplers can be shorted. Therefore, the HF equivalent model for each isolated device can be compacted as shown in Fig. 5.

In this equivalent circuit, L_P and L_S are the parasitic inductances on the primary side and secondary side, while C_PS is the parasitic capacitance across the primary side and the secondary side of the power supply.

In Fig. 6, a simplified HF equivalent circuit of the conventional architecture is presented, where only two driver supplies are taken into account.

This simplification is based on the fact that at high frequencies, the gate signal isolation stage and the gate driver supplies are in parallel and that the parasitics of the gate driver supplies are significantly larger than those of the gate signal isolation stage. To represent the dv/dt generated at the middle point of the power transistors, a trapezoidal wave voltage source is inserted between the middle point of the equivalent circuit and GND2. The impedance Z_1 in Fig. 6(a) represents the common mode impedance between GND1 and GND2. In simulations and experiments, an impedance Z_M (characterized by a large capacitor) is used to concentrate and to measure the noisy current that circulates in the driver circuit once the dv/dt is applied at the middle point of the power transistors. In brief, Z_M is an added impedance for the measurement which shorts $Z1$ to ease the conducted EMI measurements.

Table I shows all the elements of the equivalent circuit in Figs. 4–6. L_HS1 and L_HS2 are the primary and the secondary parasitic inductances of the high-side power supply, respectively. The parasitic capacitance between the input and the output of the power supply on the high side is represented by $C_\mathrm{P_HS}$. $L_\mathrm{wiring_HS}$ is the parasitic inductance of the wiring of the high-

TABLE I
ELEMENTS OF THE HF EQUIVALENT CIRCUIT IN FIGS. 4–6

$L_{\mathrm{HS1}}, L_{\mathrm{HS2}}$	Parasitic inductance on the primary and the secondary sides of high-side power supply
$C_{\mathrm{D_HS1}}, C_{\mathrm{D_HS2}}\ C_{\mathrm{D_LS1}}, C_{\mathrm{D_LS2}}$	Decoupling capacitor on the primary and the secondary side of high-side and low-side power supplies
$L_{\mathrm{wiring_HS}}\ L_{\mathrm{wiring_LS}}$	Low side and high side from gate driver circuit to power device parasitic inductors
$L_{\mathrm{LS1}}, L_{\mathrm{LS2}}$	Primary and secondary parasitic inductor of low-side power supply
$C_{\mathrm{P_HS1}}, C_{\mathrm{P_HS2}}\ C_{\mathrm{P_LS1}}, C_{\mathrm{P_LS2}}$	Parasitic capacitors between the primary and the secondary sides of the high-side and the low-side power supplies
$C_{\mathrm{HS}}\ C_{\mathrm{LS}}$	Simplified parasitic capacitor between the primary and the secondary sides of the high-side and the low-side power supplies
Z_1	Parasitic impedance between GND1 and GND2, represents totally the parasitic capacitor and the parasitics of the interconnections between GND1 and GND2
Z_M	A small impedance is added to measure the noisy current simulations and experiments
C_M, R_M, L_M	Parasitic capacitance, resistance and inductance of the measured impedance Z_M
L_{wiring}	Parasitic inductance from GND2 to devices.

side pathway. On the low side, the same parasitics are given for the power supply and the wiring: L_{LS1}, L_{LS2}, $C_{\mathrm{P_LS}}$, and $L_{\mathrm{wiring_LS}}$. On the inputs of the power supplies, a parasitic inductance L_{wiring} is added.

The noisy currents appear when high dv/dt is applied at the middle point of the half-bridge [see Fig. 6(b)]. It circulates at first in the driver through the wired devices and the parasitic elements on the high side. Then, I_{NOISE} is divided into two parts; the first component $I_{\mathrm{NOISE_GND1}}$ circulates to GND1 through the parasitic inductance of the connection L_{wiring} and the second part $I_{\mathrm{NOISE_GND2}}$ flows back to GND2 of the power part through the parasitic elements of the low-side power supply. We have

$$I_{\mathrm{NOISE}} = I_{\mathrm{NOISE_GND1}} + I_{\mathrm{NOISE_GND2}}. \quad (1)$$

As a function of the impedance ratio, without the added measured impedance Z_M and considering a first harmonic approximation, the relation of the current can be written as (2) shown at the bottom of the page.

where:

1) $f_{\mathrm{transient}}$, the transient frequency, is approximately equal to $0.35/T_{\mathrm{rise\,time}}$ where the rising time $T_{\mathrm{rise\,time}}$ is about 20 ns. Therefore, the estimated transient frequency is equal to 17.5 MHz [20], [21].
2) L_{wiring}, the parasitic inductance of the wiring connection from the ground of the remote control circuit to the input of the low-side power supply, is equal to several 10 nH, see Section II.C for the parasitic characterizations.
3) Z_{PS} is the parasitic impedance of the power supply.

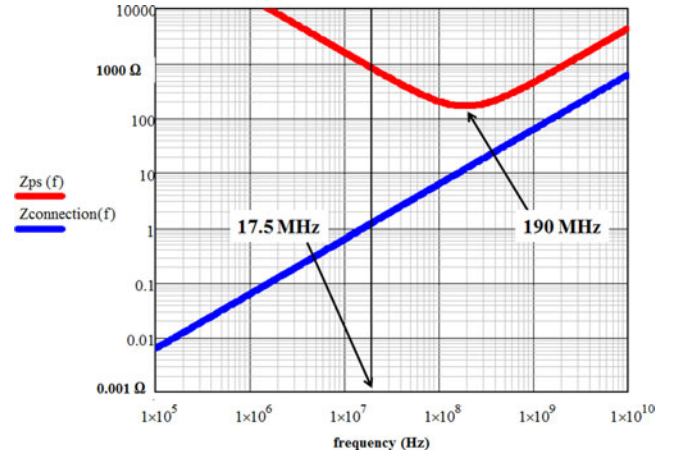

Fig. 7. Impedances Z_{PS} and $Z_{\mathrm{connection}}$ versus transient frequency.

The impedance between the low-side power supply and the connection Lwiring_LS can be expressed as follows:

$$Z_{\mathrm{PS}} = \frac{1}{2\pi f_{\mathrm{transient}} C_{\mathrm{PS}}} + 2\pi f_{\mathrm{transient}} L_{\mathrm{LS1}} + 2\pi f_{\mathrm{transient}} L_{\mathrm{LS2}} + 2\pi f_{\mathrm{transient}} L_{\mathrm{wiring_LS}} \quad (3)$$

where:

1) L_{LS1} and L_{LS2}: primary and secondary parasitic inductor of low-side power supply are estimated to 50 nH, see Section II.C for the parasitic characterizations.
2) C_{PS}: the parasitic capacitance of the power supply of the gate driver circuit, varies between 10 and 100 pF, see Section II.C for the parasitic characterizations

The impedance of the connection is given by the following equation:

$$Z_{\mathrm{connection}} = 2\pi f_{\mathrm{transient}} L_{\mathrm{wiring}}. \quad (4)$$

The impedance plots in Fig. 7 show the ratio between the Z_{PS} and $Z_{\mathrm{connection}}$.

As we can see, in the low-frequency range of the plot which is around the transient frequency 17.5 MHz, Z_{PS} is much larger than $Z_{\mathrm{connection}}$. This ratio is minimum at 190 MHz frequency that is far above the transient equivalent frequency considered in this research. Above that frequency the current ratio is represented by the parasitic inductance ratio.

According to the rise time of the power device, we can estimate the impedance contribution at the transient frequency of the primary–secondary path for parasitics for the low-side power supply as follows:

$$\frac{1}{2\pi f_{\mathrm{transient}} C_{\mathrm{PS}}} \approx \frac{20 \times 10^{-9}}{2\pi \times 0.35 \times 10 \times 10^{-12}} \approx 900\ \Omega \quad (5)$$

$$\frac{I_{\mathrm{NOISE_GND2}}}{I_{\mathrm{NOISE_GND1}}} = \frac{2\pi f_{\mathrm{transient}} L_{\mathrm{wiring}}}{\frac{1}{2\pi f_{\mathrm{transient}} C_{\mathrm{PS}}} + 2\pi f_{\mathrm{transient}} L_{\mathrm{LS1}} + 2\pi f_{\mathrm{transient}} L_{\mathrm{LS2}} + 2\pi f_{\mathrm{transient}} L_{\mathrm{wiring_LS}}} \quad (2)$$

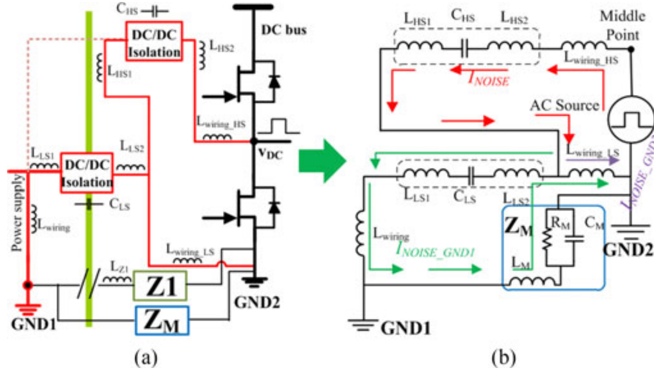

Fig. 8. Proposed architecture: (a) driver circuit with only power supplies and (b) HF equivalent circuit.

and

$$2\pi f_{\text{transient}} L_{\text{wiring}} \approx 2\pi \times \frac{0.35}{20 \times 10^{-9}} \times 10 \times 10^{-9} \approx 1\,\Omega. \tag{6}$$

Now, the estimation of the current ratio becomes

$$\frac{I_{\text{NOISE_GND2}}}{I_{\text{NOISE_GND1}}} = \frac{2\pi f_{\text{transient}} L_{\text{wiring}}}{Z_{\text{PS}} + 2\pi f_{\text{transient}} L_{\text{wiring_LS}}} \approx 10^{-3}\,. \tag{7}$$

As the estimated result of (7), $I_{\text{NOISE_GND2}}$ is much smaller than $I_{\text{NOISE_GND1}}$; almost all the noisy current I_{NOISE} in Fig. 6 goes through the ground of the primary side of the remote control part GND1.

In these driver circuits, the most important element that has effect on the noisy current is the parasitic capacitance between the primary side and the secondary side of the isolated dc–dc power supplies.

Based on the method presented above, the HF equivalent circuit of the proposed gate driver architecture is shown in Fig. 8. The wiring of the power supplies in the proposed architecture is presented in Fig. 8(a), and its HF equivalent circuit is presented in Fig. 8(b).

A noisy current appears when the voltage source generates high dv/dt [see Fig. 7(b)]. At first, the noisy current I_{NOISE} flows through the parasitic elements on the high-side supply (L_{HS1}, L_{HS2}, C_{HS}, and $L_{\text{wiring_HS}}$). Then, this current is split in two parts: the first part $I_{\text{NOISE_GND2}}$ flows to the GND2 through the parasitic inductance of the wiring $L_{\text{wiring_LS}}$, while the second part $I_{\text{NOISE_GND1}}$ circulates first through the parasitic elements of the low-side supply (L_{LS1}, L_{LS2}, and C_{LS}) and the parasitic inductance L_{wiring} toward GND1. According to (1)–(7), the relation between the currents in this architecture can be shown as follows:

$$\frac{I_{\text{NOISE_GND1}}}{I_{\text{NOISE_GND2}}} = \frac{2\pi f_{\text{transient}} L_{\text{wiring_LS}}}{Z_{\text{PS}} + 2\pi f_{\text{transient}} L_{\text{wiring}}} \approx 10^{-3}. \tag{8}$$

In this case, the estimated result of (8) is opposite to the result of (7) which means that a very small amount of the noisy current circulates from the power module to the ground of the primary side of the remote control circuit GND1.

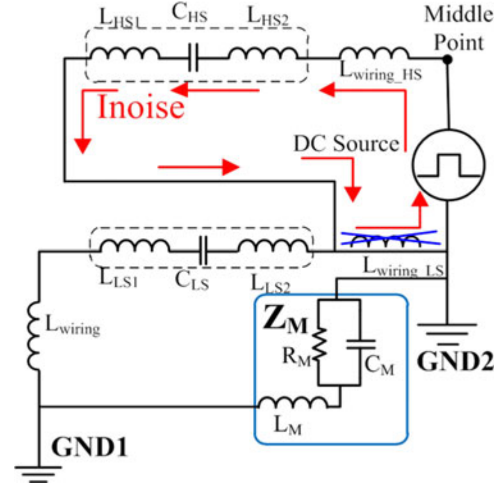

Fig. 9. HF equivalent circuit of the proposed architecture with improvement.

As a matter of fact, the current which goes to the ground of the primary side of the control circuit could be reduced even more by minimizing the parasitic inductance $L_{\text{wiring_LS}}$. In Fig. 9, an equivalent circuit without the $L_{\text{wiring_LS}}$ is depicted and the total amount of noisy current circulates in the loop of the dc source. In this case, no more current goes through GND1. The value of $L_{\text{wiring_LS}}$ could be reduced if the gate driver and the power supply of the high side are designed to be implemented as close as possible to the power transistors. But the most important issue is to limit the common traces between the low-side wiring and the connections between the low-side and the high-side devices.

To validate the presented analysis, three simulations are presented in the next section. In the first and second cases, the equivalent circuits of the conventional and the proposed architectures are simulated. Then, the value of $L_{\text{wiring_LS}}$ has been reduced in the last simulation to evaluate the decreasing of the noisy current that circulates in the remote control circuit.

C. *Simulations of the Architectures*

The values used in the simulations are derived from the experiments.

The primary to secondary equivalent impedance of the power supply TRACO TMA1515s which will be used in the experiments to supply the low side and the hide side of the gate driver is characterized in Fig. 10. At 66 kHz frequency, the impedance plot shows a capacitive impedance of 28 kΩ. Based on this measurement, the capacitor value can be derived to 86 pF. In this plot, the resonant point is at 75 MHz, therefore the inductance of the power supply TMA1515s can be determined to 55 nH.

The printed circuit board (PCB) layout of the experimental circuit has been imported into InCa3D™ [22] to evaluate the parasitic inductance $L_{\text{wiring_LS}}$, is shown in Fig. 6. Fig. 11(a) shows the complete PCB layout of the power transistors and the conventional gate driver architecture. Fig. 11(b) represents simplified PCB tracks between the output of the low-side power

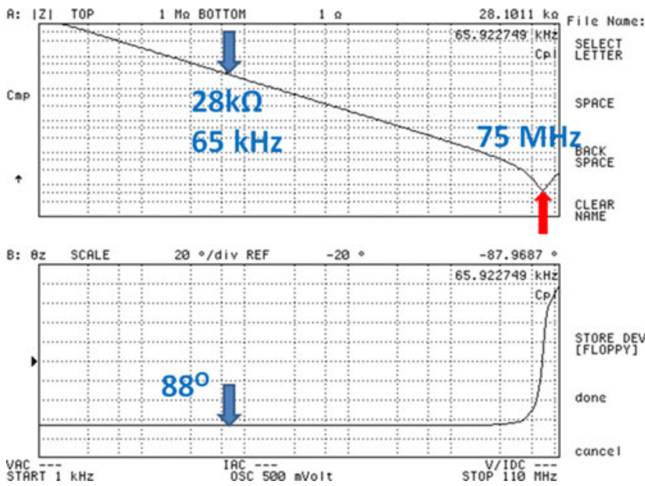

Fig. 10. Primary–secondary impedance of the power supply TRACO TMA1515S.

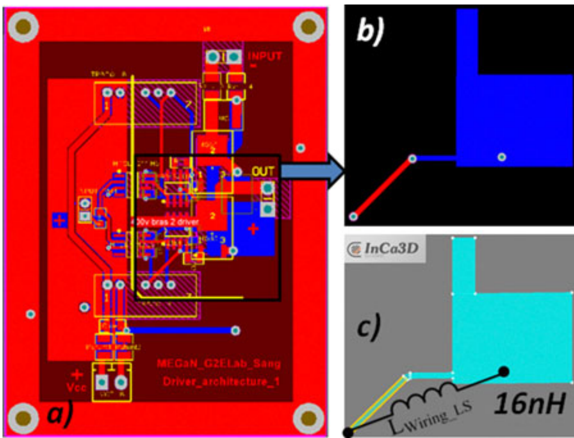

Fig. 11. Two layers PCB with 35 μm copper thickness in InCa3D to measure the $L_{\rm wiring_LS}$.

supply and the GND2. Then, Fig. 10(c) shows the modeled geometry in InCa3D of a sector of a standard two layers PCB with 35 μm copper thickness. The parasitic inductance $L_{\rm wiring_LS}$ of 16 nH has been extracted at 100 kHz in InCa3D for 18 mm of the length distance between two terminals. To simplify the value extraction in InCa3D, we decided to simulate a partial circuit then the other values are estimated through the length distance between two terminals.

Fig. 12 shows the rising edge of the waveform of the single ramp voltage source used in the experiments. The amplitude is 200 V and the rising time is 15 ns, which gives a dv/dt of 13 V/ ns that will be considered in the simulations.

Fig. 13 shows the schematic used in the software SIMPLORER to simulate and analyze the transient waveforms of the conventional architecture. The values of the parasitic elements of the high-side and the low-side power supplies are considered identical. The parasitic capacitances of the isolation $C_{\rm HS}$ and $C_{\rm LS}$ are 86 pF (as measured in Fig. 10); the parasitic inductances $L_{\rm HS1}$, $L_{\rm HS2}$, $L_{\rm LS1}$, and $L_{\rm LS2}$ on the primary side

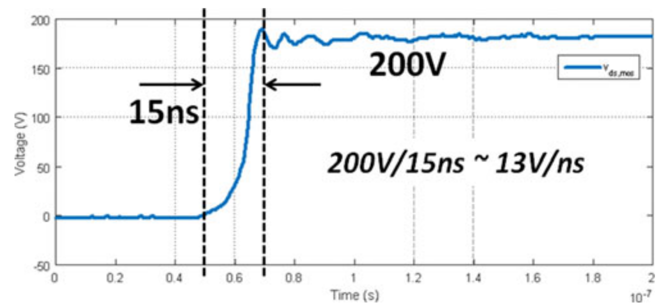

Fig. 12. Average value dv/dt of 13 V/ ns as the experimental battery voltage.

and the secondary sides of the power supplies are 27.5 nH. Thus, the total parasitic inductance is 55 nH as measured in Fig. 9. After a parasitic extraction of $L_{\rm wiring_LS}$ in InCa3D to verify the trace distance and the inductance value, the wiring parasitics $L_{\rm wiring_HS}$ is estimated to 20 nH and $L_{\rm wiring}$ is estimated to 10 nH based on the length distance between the terminals.

The fictive impedance Z_M has a parasitic inductance of 10 nH and a capacitance of 1 nF connected in parallel with a resistance of 10 MΩ. In fact, the parasitic impedance between the middle point of the power transistors and the ground of the remote control GND2 cannot be accessed by the current probe. Therefore, in both simulation and experiments, this impedance Z_M has been externally added to the circuit in order to measure the noisy current. The parasitic capacitance of the power supply is around 100 pF, thus 1 nF capacitor has been implemented between GND1 and GND2 to measure approximately 95% of the noisy current. The resistor of 10 MΩ is a parasitic resistor between the two grounds; the inductor of 10 nH represents 10 mm length of interconnections.

Fig. 14 shows the simulation schematic of the proposed architecture. A large amount of parasitic inductances is still present since the output of the power supply on the low side is directly connected to the input of the power supply on the high side. The parasitic inductance on the low-side power supply is 16 nH that corresponds to the wirings of the real circuit.

In Fig. 15, the parasitic inductance caused by the wiring on the low side has been reduced to 8 nH, thanks to an improved wire routing. The simulation takes into account this value because it always exists in a real system. In experiment, the practical improvement will be shown.

The above schematics are used in simulations to validate the analysis presented in the previous section, and to quantify the differences between the different cases. Figs. 16–18 show, respectively, simulation results of the conventional architecture, the proposed architecture, and the proposed architecture with improved wire routing.

In these simulations, at the moment $t = 0$ s, the voltage source is 0 V and there is no dv/dt. At $t = t_O$, the single ramp voltage source has generated a $dv/dt = 13$ V/ns.

As we can see in Fig. 16, in the conventional architecture, a noisy current with 2.44 A amplitude is circulating through Z_M. This current has been reduced significantly to

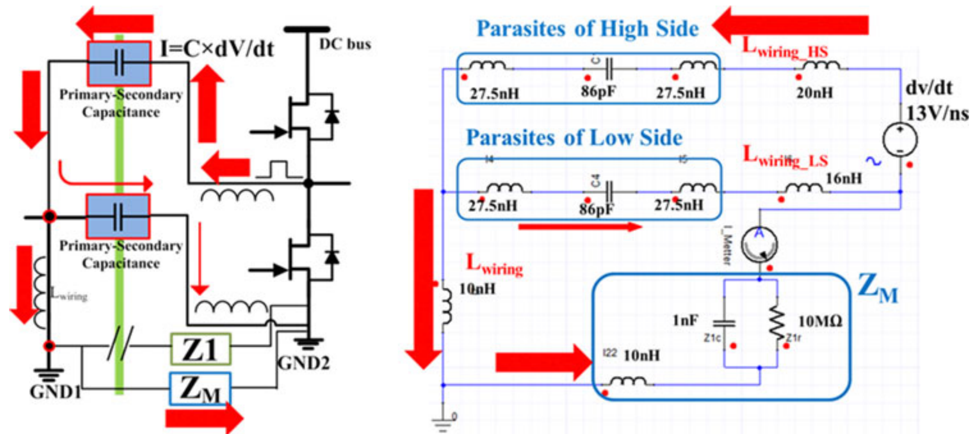

Fig. 13. Simulation of the conventional architecture. Left: schematic circuit. Right: SIMPLORER circuit.

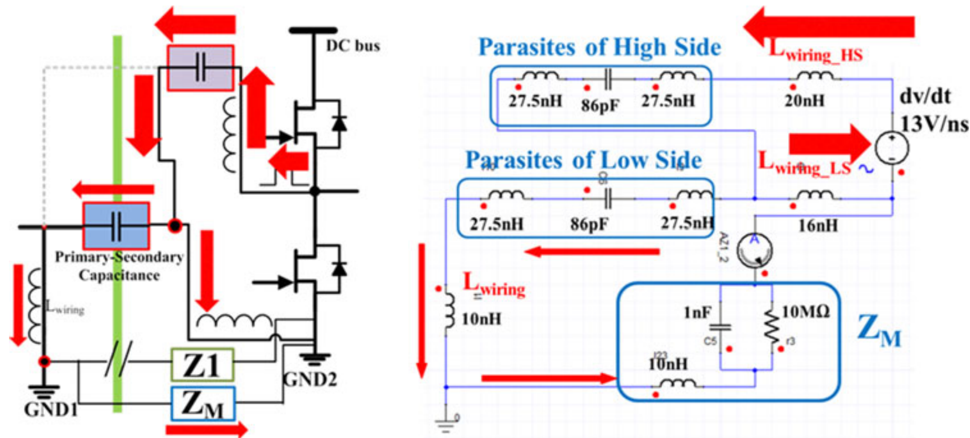

Fig. 14. Simulation of the proposed architecture. Left: schematic circuit. Right: SIMPLORER circuit.

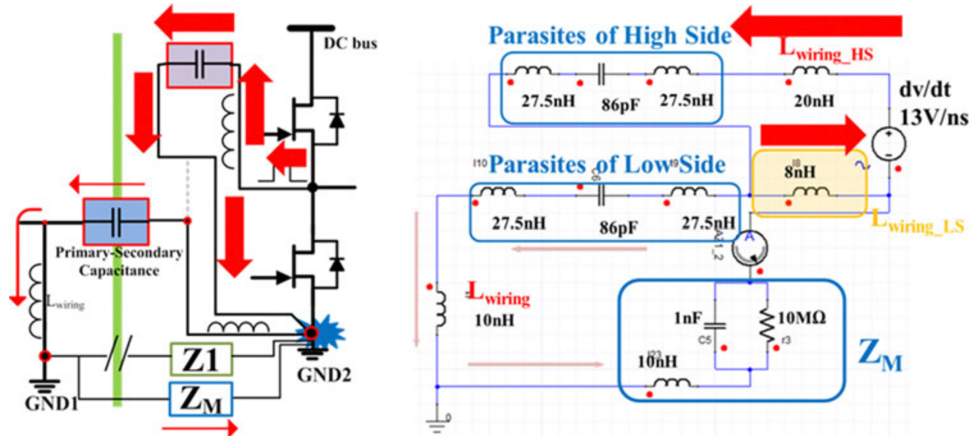

Fig. 15. Simulation of the proposed architecture with the improved routing. Left: schematic circuit. Right: SIMPLORER circuit.

0.37 A in the proposed architecture, as shown in Fig. 17, and to 0.128 A with an improved wire routing, as shown in Fig. 18. In the real system, the noisy current still circulates but through the power supplies and the control signal insulators and not anymore through GND1. These simulation results validate the advantage of the proposed architecture in terms of noisy current reduction and as a consequence of conducted EMI.

In the next section, the advantages of the proposed architecture are highlighted experimentally.

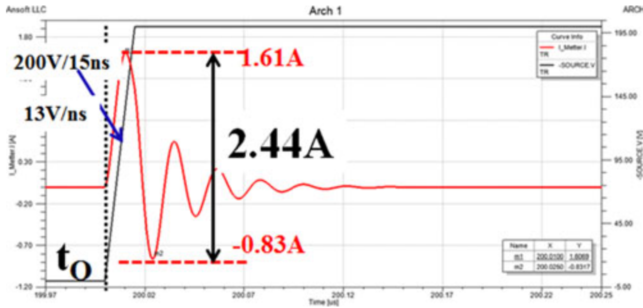

Fig. 16. Noisy current in Z_M of the conventional architecture, simulation results.

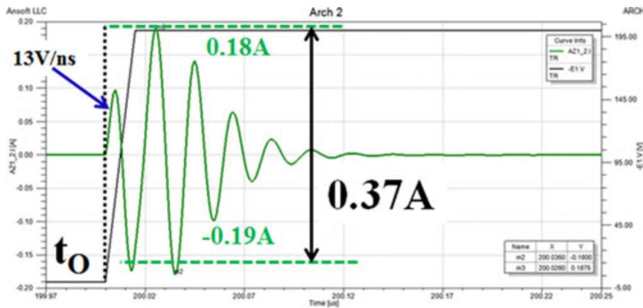

Fig. 17. Noisy current in Z_M of the proposed architecture, simulation results.

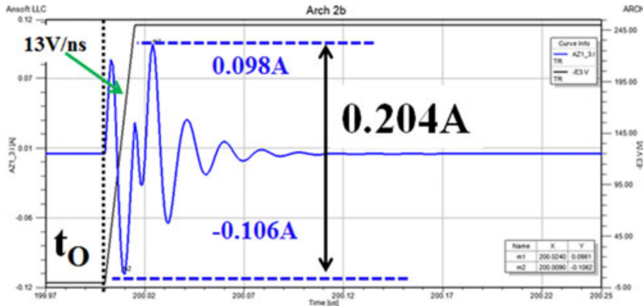

Fig. 18. Noisy current in Z_M of the proposed architecture with improved wire routing, simulation results.

D. Experimental Results of the Architectures

The noisy currents between GND1 and GND2 are measured in experimental setup shown in Fig. 19. High dv/dt can be produced by any device, not only WBG devices but also with classical Si power devices. In these robust experiments, transistors CoolMOS have been used. The dc–dc power supplies and the optocouplers make a strong isolation between the driver circuit and the power module. To physically separate the GND1 and GND2, a battery of 200 V has been used as input power for the power side. An auxiliary 15 V power supply is used for powering the driver circuit; a function generator was used to generate the control signal of the remote control part. This 15 V power supply and this function generator are powered by the grid.

The power side was supplied with batteries to ease the measurements but also to simplify the use and implementation of a function generator to produce the driving signals. A control signal pulse width modulation with 50% duty cycle and 100 kHz frequency is used to drive the power transistors. Between the GND1 and GND2, an additional artificial impedance Z_M of 1 nF and 10 MΩ has been used to emulate the impedance between GND1 and GND2. To avoid the failure of the gate driver circuit by a large current due to high dv/dt, especially in the case of the conventional architecture, the experiments are performed for only two or three periods with an inductive load.

Table II shows the list of devices used in the test circuits.

Fig. 20(a) shows the circuit with conventional architecture of the driver circuit. In this circuit, an inverter leg has been implemented with two independent control signals. Each driver is implemented with its own isolated power supply, optocoupler, and gate driver. The noisy current through the driver circuit in the conventional architecture has been measured in Fig. 20(b). As it can be observed, the dv/dt of 13 V/ns at the middle point of the power inverter leg generated 2.7 A peak to peak noisy current. This current circulates in the high-side dc/dc power supply whose nominal current is 80 mA. A higher dv/dt increases the noisy current that could alter not only the power supply but also the other elements of the driver circuit as well.

Fig. 21(a) shows a photo of the circuit of the proposed architecture. Two isolated power supplies, one optocoupler and one gate driver with integrated level shifter, have been implemented to control both low side and high side of the power inverter leg. In Fig. 21(b), the measured noisy current is reduced by a factor 6 (0.45 A) even though the wiring still causes a large parasitic inductance between the output of the low-side power supply and between the high-side power supply and GND2.

A second version of the PCB of the proposed architecture has been designed with modified track routing to minimize the undesirable parasitic inductance of the wiring on the low side [see Fig. 22(a)]. In this experiment, the parasitic inductance of the wirings can be minimized but not completely eliminated. The optimization of the wirings decrease has a significant effect on the common mode noisy current. As it can be observed in Fig. 22(b), the peak of the noisy current has been drastically reduced by a factor 10 in comparison with the conventional architecture.

In Fig. 23, the experimental results of the three circuits have been superposed in one single plot. As it can be observed, the noisy current circulating between GND1 and GND2 in the conventional architecture is significant when the dv/dt occurs.

The voltages on the output of the three studied circuits are identical. The current of the conventional architecture is in the blue color; the current of the proposed architecture is in the orange color; and the current of the proposed architecture with improved wire routing is in the red color. As we can see in Fig. 23, not only the amplitude of the current is decreased significantly but also the oscillation of the noisy current is reduced.

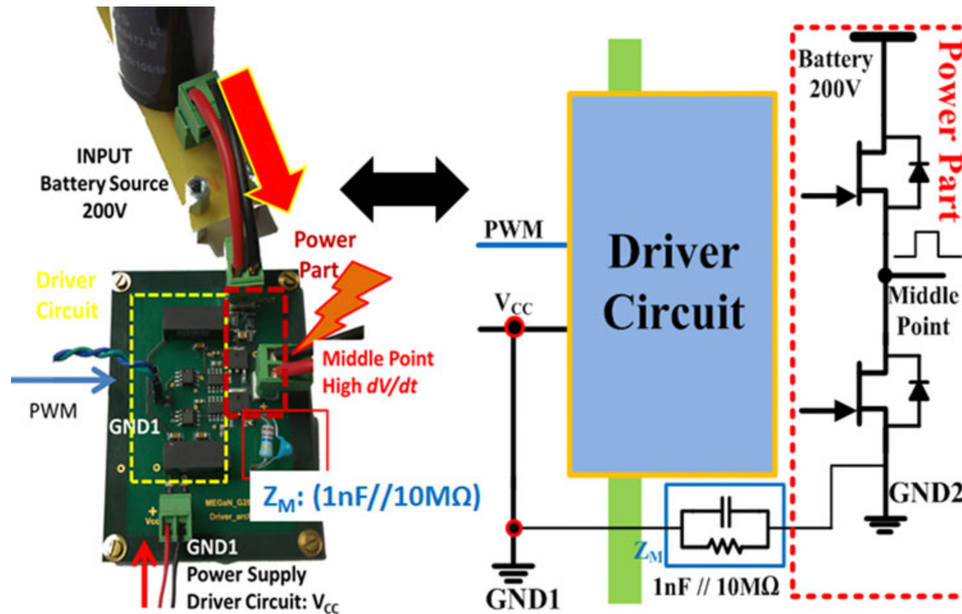

Fig. 19. Experimental setup to separate physically GND1 and GND2.

In both simulation and experimental results, the proposed architecture demonstrated significant reduction of the noisy current between GND1 and GND2. With the proposed approach, almost all noisy current returns to the power module instead circulating in the driver circuitry to the ground of the remote control circuit.

TABLE II
ELEMENTS OF EXPERIMENTS

Power part (GND2)	Power source	200 V battery bank
	Power transistors	CoolMOS–SPB11N60C2
Driver circuit (GND1)	DC–DC power supply	TRACO–TMA 1515S (Nominal current 80 mA)
	Control signal isolator	OPTO HPCL 2211
	Gate driver	IR2184
Measure	Artificial impedance Z_M between GND1 and GND2	1 nF // 10 MΩ

III. RECOMMENDATIONS FOR THE DESIGN OF HF POWER MODULES WITH HIGH dv/dt AND IN A HARSH ENVIRONMENT

This paper focuses on the improvement of the implementation of WBG devices in power modules with respect to the EMI management and especially to the conducted and radiated EMI perturbation in common mode. The system could be damaged by a large amount of the noisy current that may flow through the control parts if we do not pay high attention on the implementation of the control side of the power module. Several papers in the literature have highlighted the need to care about how gate drivers are implemented close to the power devices [17]–[19]. It is clear that the gate drivers should be as close as possible to the power devices in order to minimize the parasitic inductances limiting the speed of the gate charge and clamping for dv/dt immunity purposes. Conventional power modules with external gate driver circuits seem to be no more adapted to an effective implementation of very high speed power devices. The best solution would be to integrate the gate drivers within the power modules [23]. However, additional recommendations should be provided to really optimize their integration.

The paper has clearly shown that it is important to supply the high-side gate driver circuit and to transfer the control signals through the low-side gate driver circuitry. Cascaded circuitry with locally generated and isolated control signals and supplies would be the best solution. The paper has also highlighted that this high-side gate driver supply should be connected as close as possible to the reference potential of the power switching cell, i.e., named in this paper as GND2. In this case, four essential elements should be implemented very close to the power transistors and connected in a very specific way: two gate drivers to drive the low-side and high-side power devices, the high-side gate driver power supply, and the high-side control signal transfer unit. Each gate driver should be tightly connected to its corresponding power device. The high-side power supply should be cascaded after the low-side power supply and connected as close as possible to the reference potential of the power part GND2. The output capacitor of the low-side gate driver supply should be as close as possible to GND2 as well in order to minimize the HF common paths between the low-side and high-side circuitry. The high-side gate driver supply can be physically integrated within the power module but it does not have to be placed very close to the switching cell since it is mainly its interconnection location which is critical. On the other side, the low-side isolated gate driver supply as well as the low-side isolation units for the gate signals do not have to be specifically integrated or close to the power module.

As a matter of fact, this paper has clearly underlined that efforts must be engaged not only toward the design, the qualification, and the implementation of gate drivers but also

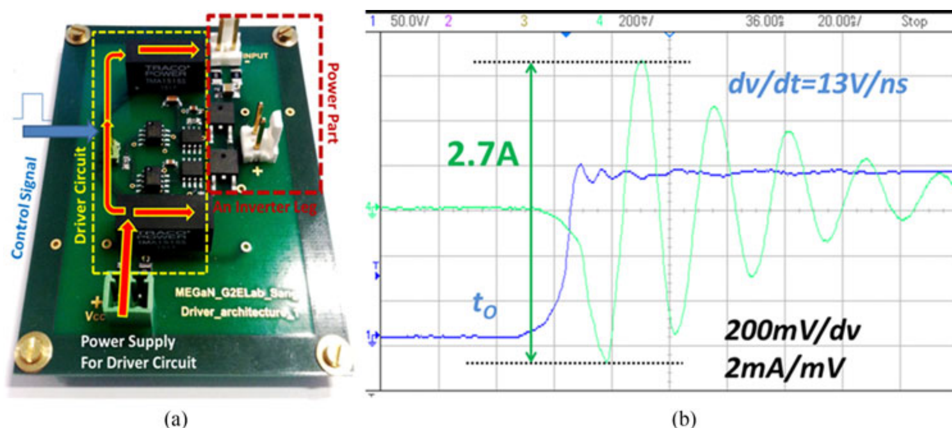

Fig. 20. Noisy current between GND1 and GND2 in conventional architecture, test circuit, and experimental results.

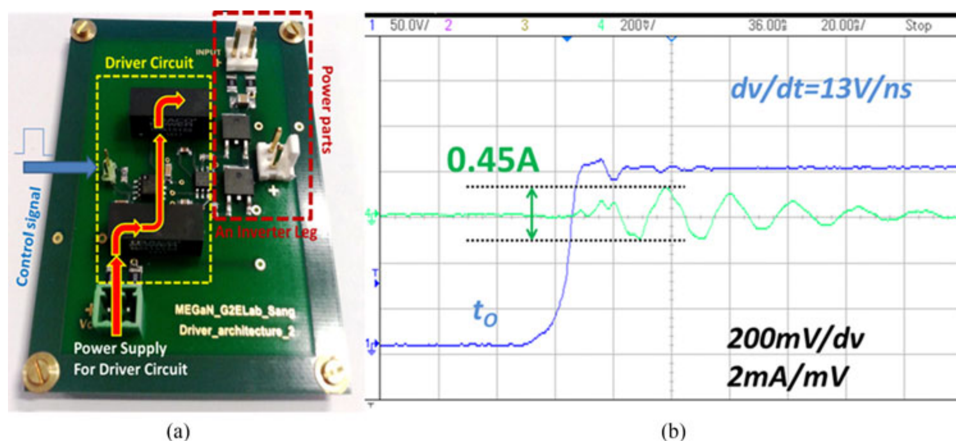

Fig. 21. Noisy current between GND1 and GND2 in the proposed architecture, actual circuit, and experimental results.

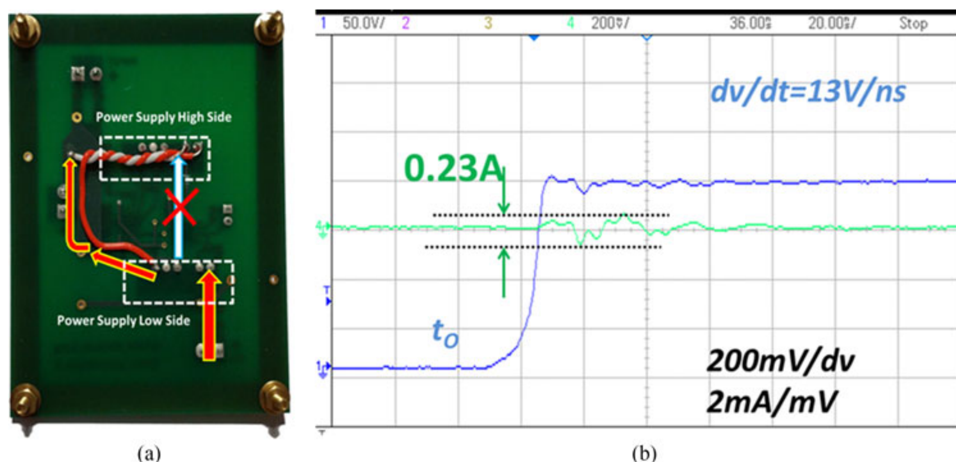

Fig. 22. Noisy current between GND1 and GND2 in the proposed architecture with improved wire routing, PCB circuit, and experimental results.

toward the gate supplies and gate signal level shifter. Moreover, in what refers to the supplies, the cascaded architecture of the gate driver supplies and control signal isolation units should also be considered as an issue for advanced and high switching speed implementation.

Fig. 24 illustrates two regions of the operating temperature and also the cascaded architectures to be implemented for proper EMI common mode path reduction. Our further works are focused on overcoming the problems of the signal transfer unit in the integrated gate driver [24].

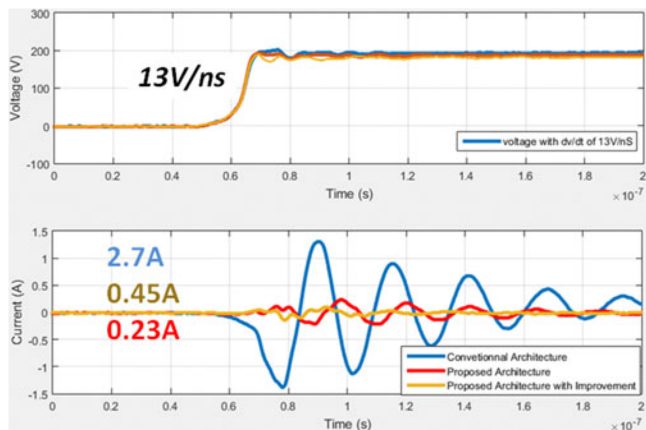

Fig. 23. Noisy currents in the three architectures and the event *dv/dt*, experimental results.

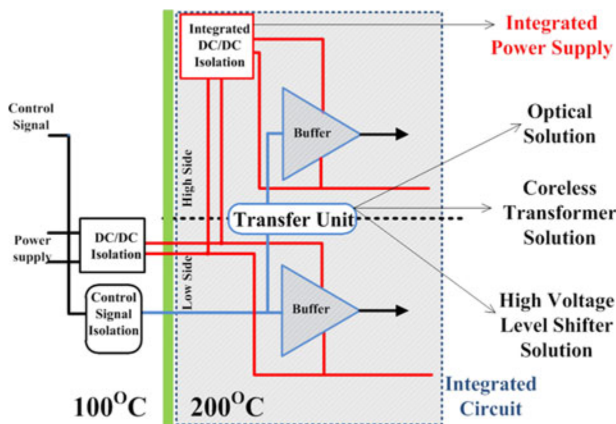

Fig. 24. Integrated circuit of the gate driver for the proposed architecture.

IV. Conclusion and Perspectives

In this paper, a proposed architecture of gate driver circuitry for HF, very high switching power devices is presented in order to minimize the EMI propagation paths out of the power module and especially through the control units. The experimental results proved its advantages regarding the optimization of the EMI disturbances under very high *dv/dt*. The analysis of the work highlighted that cascaded supply architectures as well as the integration of part of the gate drivers' circuitry as close as possible to the power transistors are required to achieve an effective WBG power module implementations.

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