Analysis, Design, and Implementation of an APWM ZVZCS Full-Bridge DC–DC Converter for Battery Charging in Electric Vehicles

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***Abstract*—An efficient power converter system plays a significant role in the design of battery charging systems for electric vehicles (EVs). In this paper, a new zero-voltage and zero-current switching (ZVZCS) full-bridge dc–dc converter is proposed to reduce the power conversion losses. The proposed converter incorporates a new asymmetrical pulse width modulation (APWM) gating technique for the dc–dc conversion stage in the battery charging system. The proposed dc–dc converter topology achieves zero-voltage switching (ZVS) for all the active switches and near zero-current switching (ZCS) for low-side active switches throughout the charging range of the battery. The proposed APWM technique can reduce the switching and conduction losses compared to the conventional phase-shift modulation (PSM) gating technique. The auxiliary inductance required to ensure ZVS with APWM can also be reduced compared to PSM. Analysis, design, and implementation of the proposed APWM ZVZCS full-bridge dc-dc converter are discussed in this paper. A 100-kHz 1.2-kW laboratory prototype is developed and the experimental results are presented. The results validate the analysis and performance of the proposed converter.**

***Index Terms*—Asymmetrical pulse width modulation, battery charging, full-bridge dc-dc converter, zero-voltage switching.**

I. Introduction

PLUG-IN hybrid electric vehicles (EVs) and plug-in EVs are potential solutions to address both the environmental and economic needs of near future urban transportation [1]. EVs use a high voltage and high energy density rechargeable battery pack for powering the traction system. The battery pack is typically charged from the utility grid, utilizing an EV battery charger. The block diagram of a power conditioning system for an on-board EV battery charger [2], [3] is shown in Fig. 1. The EV battery charger has two stages: 1) the front-end ac–dc power conversion stage that regulates the input power factor, input current total harmonic distortion (THD), and intermediate dc bus voltage; and 2) the isolated dc–dc conversion stage that regulates the output voltage and provides galvanic isolation between the utility grid and the battery pack. Galvanic isolation is required to comply with the safety standards of EV charging system listed in UL-2202 and UL-2231 [4]–[6].

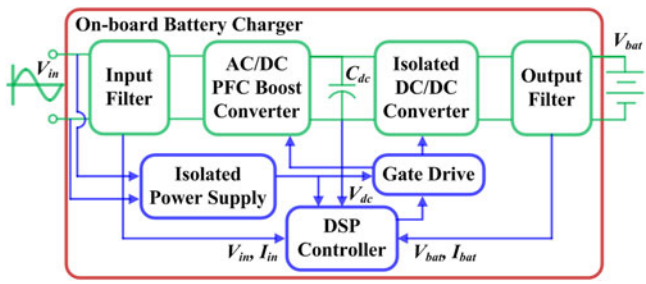

Fig. 1. Block diagram of a power conditioning system for an on-board two-stage EV battery charger.

This paper focuses on the dc–dc conversion stage of the EV battery charger. High efficiency, high reliability, high power density, isolation capability, and compliance with existing standards are the most desired features in the selection of an isolated dc–dc converter configuration. The phase-shifted full-bridge isolated dc–dc converter is a commonly preferred topology for the second stage power conversion in an EV battery charger [7], [8]. However, it has the following drawbacks: Zero-voltage switching (ZVS) for active switches in a narrow load range, high circulating current during the freewheeling period, duty-cycle loss, high-voltage spikes across the secondary rectifier diodes, and the associated electromagnetic interference (EMI). These drawbacks have to be addressed properly for EV battery charging applications to ensure the satisfactory performance of the converter over its operating range.

Several modified full-bridge dc–dc converter topologies and control methods have been proposed in [9]–[34] to overcome the drawbacks, as mentioned earlier. ZVS full-bridge converter topologies assisted with passive auxiliary circuit have been proposed and analyzed in [9]–[15]. However, the applicability of these topologies is limited by reduced effective duty cycle and

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high-voltage spikes across rectifier diodes. ZVS full-bridge converter topologies assisted with an active auxiliary circuit have been proposed and analyzed in [16]–[22]. The major drawbacks of these topologies include reduced efficiency for higher input voltage, ineffective in achieving ZVS for leading-leg switches at very light-load conditions, and increased control complexity.

Additional R-C-D snubber circuits [23], [24] and energy recovery circuits [25]–[29] have been used to mitigate the voltage spikes across rectifier diodes. The current-fed topologies with capacitive output filter proposed in [30] and [31] inherently minimize the voltage spikes and reverse-recovery losses. The converter topology proposed in [30] achieved ZVS turn-on for all the switches over wide load range and near zero-current switching (ZCS) turn-off for leading-leg switches. However, the auxiliary current in the leading leg is independent of the load conditions that increase the conduction losses of the converter in the full-load condition.

The trailing-edge pulse width modulation (PWM) and asymmetrical duty-cycle control techniques have been proposed in [31]–[34]. The trailing-edge PWM converter in [31] could achieve ZVS and ZCS for low-side switches. However, the ZVS range for low-side switches is limited and ZVS is not possible for high-side switches over the entire operating range. In asymmetrical duty-cycle controlled converters [32], [33], the diagonal switches are operated in a complementary manner with duty-cycle ratios *D* and (1 – *D*). The output voltage is regulated by varying *D* and hence resulting in a voltage across primary side of the high-frequency transformer that is asymmetric in nature. This feature increases core loss in the high-frequency transformer and the balancing inductor due to the dc-offset currents [34].

In this paper, a current-fed zero-voltage zero-current switching (ZVZCS) full-bridge dc–dc converter and a new asymmetrical PWM (APWM) gating technique are proposed. A passive auxiliary circuit is used in the converter to extend the soft-switching range of the active switches. The proposed topology ensures ZVS turn-on for all the active switches, near ZCS turn-off for the low-side active switches, and ZCS turn-off for the output rectifier diodes over the entire battery charging range. The proposed APWM controls the auxiliary inductor current to minimize the auxiliary circuit losses and conduction losses on the primary side. This feature improves the overall efficiency of the proposed converter over the battery charging range compared to the conventional phase-shift modulation (PSM) gating method. The proposed APWM gating scheme also reduces the auxiliary inductance required to achieve ZVS turn-on of all the active switches compared to the PSM. The proposed converter is designed to charge the battery using the constant current (CC) –constant voltage (CV) charging method [35].

This paper is organized as follows. In Section II, the proposed converter topology and the APWM gating technique are introduced. The operation principle of the converter is described in Section III. Steady-state analysis of the converter is given in Section IV. The converter circuit parameters design is detailed in Section V. Design procedure for the magnetics used in the converter is discussed in Section VI, followed by the experimental results in Section VII. Finally, the conclusion is presented in Section VIII.

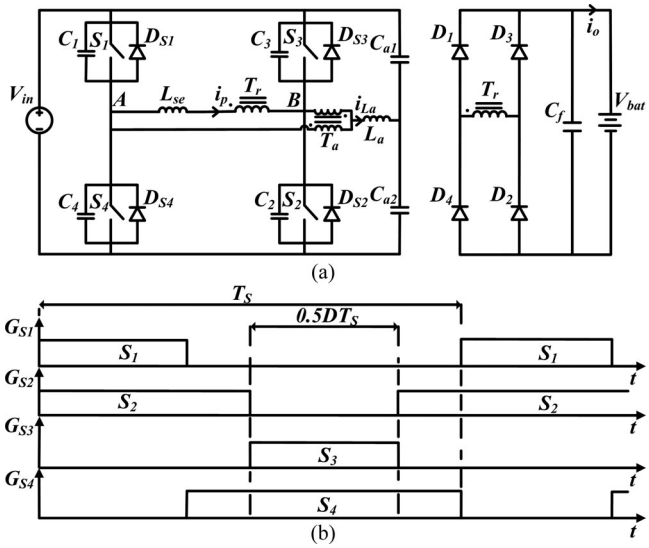

Fig. 2. Proposed APWM ZVZCS full-bridge dc–dc converter topology.

II. APWM ZVZCS Full-Bridge DC–DC Converter

The proposed ZVZCS full-bridge dc–dc converter topology is shown in Fig. 2(a). In the proposed converter circuit:

1) S_1-S_4 are the active switches;
2) $D_{S1}-D_{S4}$ are the antiparallel body-diodes for S_1-S_4, respectively;
3) C_1-C_4 are the capacitors across the active switches S_1-S_4 and the capacitances are equal to the sum of body capacitance and snubber capacitance, respectively;
4) T_r is the main high-frequency power transformer with turns ratio 1:*n*;
5) $L_{\rm se}$ is the series resonant inductor and its value is equal to the sum of the leakage inductance of T_r and external series inductance;
6) D_1-D_4 are the secondary output rectifier diodes;
7) C_f is the output filter capacitor;
8) C_{a1} and C_{a2} are the auxiliary capacitors forming a capacitive potential divider;
9) T_a is the auxiliary transformer with turns ratio 1:1; and
10) L_a is the auxiliary energy storage inductor.

The proposed APWM gating technique is shown in Fig. 2(b). $G_{S1}-G_{S4}$ are the gating signals to S_1-S_4, respectively. T_s is the switching period and *D* is the duty cycle. The inverter output voltage $V_{\rm AB}$ is symmetrical as S_1 and S_3 are gated with the same duty cycle, as shown in Fig. 2(b). This feature eliminates the dc offset which results in reduced core loss compared to the gating technique presented in [32] and [33]. The output voltage of the converter is regulated by controlling the duty cycle *D*.

The proposed APWM gating signals can be applied to S_1-S_4 in two methods to obtain the same output voltage. The first method is shown in Fig. 2(b), where the duty cycle of the high-side switches $D_{\rm SWU}$ is controlled as $0 < {\rm D_{SWU}} < 0.5$. The second method is that the duty cycle of the high-side switches is controlled as $0.5 < {\rm D_{SWU}} \leq 1$. Both the methods can be used during the converter operation to achieve an optimal thermal profile [36]. In this paper, the first gating method is analyzed.

It should be noted that the analysis presented in the following section is equally valid for the second method.

III. Operation Principle of the Proposed Converter

The steady-state operating analysis of the proposed converter over the entire battery charging range is explained here. The following assumptions are considered for ease of the analysis:

1) all the switching elements are ideal;
2) resistance and interwinding capacitance of T_r and T_a are neglected;
3) magnetizing inductance of T_r and T_a is large enough to ignore the effect of magnetizing current during the switching period;
4) resistance and winding capacitance of $L_{\rm se}$ are neglected;
5) equivalent capacitance across active switches is same $C_1 = C_2 = C_3 = C_4 = C$;
6) $C_{a1} = C_{a2} = C_a$ are large enough such that V_{ca1} and V_{ca2} are constant during the switching period;
7) C_f is large enough to assume that the output voltage is constant.

The key operational waveforms of the proposed converter are shown in Fig. 3. The operation of the converter is divided into 12 time intervals over 1 switching cycle. Time intervals $t_0 - t_6$ illustrate the positive power transfer operation and ZVS transition for S_3 and S_4. Time intervals $t_6 - t_{12}$ are similar to $t_0 - t_6$ except that it is a negative power transfer operation and ZVS transition for S_1 and S_2. The analysis for *Interval I–Interval VI* is discussed in this section. The analysis for remaining intervals, i.e., *Interval VII–Interval XII* is similar to *Interval I–Interval VI*. Therefore, it is not discussed separately.

Interval I ($t_0 \le t \le t_1$): The switch S_1 is turned ON with ZVS at the start of this interval. The body-diode D_{S1}, switch S_2, and the output diodes D_1 and D_2 are in conduction during this interval. The circuit conditions during this interval are shown in Fig. 4(a). The inverter output voltage $V_{\rm AB}$ is given by (1). The current through the primary side of the main transformer i_p rises linearly as the output rectifier diodes clamp the main transformer secondary voltage to the output voltage. The voltage across the auxiliary inductor is constant; as a result, current through L_a also rises linearly, as given by (3) and (4), respectively

$$v_{\rm AB}(t) = V_{\rm in};\ v_{\rm Tap}(t) = v_{\rm Tas}(t) = \frac{V_{\rm in}}{2} \tag{1}$$

$$i_p(t) = \frac{V_{\rm in} - V_o/n}{L_{\rm se}}(t - t_0) \tag{2}$$

$$v_{La}(t) = V_{La}^{+} = (1 - D)\frac{V_{\rm in}}{2} \tag{3}$$

$$i_{La}(t) = I_{La}(t_0) + \frac{V_{\rm in}(1 - D)}{2L_a}(t - t_0). \tag{4}$$

The current through the switches is given by

$$i_{S1}(t) - i_{\rm DS1}(t) = i_p(t) + \frac{i_{La}(t)}{2} \tag{5}$$

$$i_{S2}(t) - i_{\rm DS2}(t) = i_p(t) - \frac{i_{La}(t)}{2}. \tag{6}$$

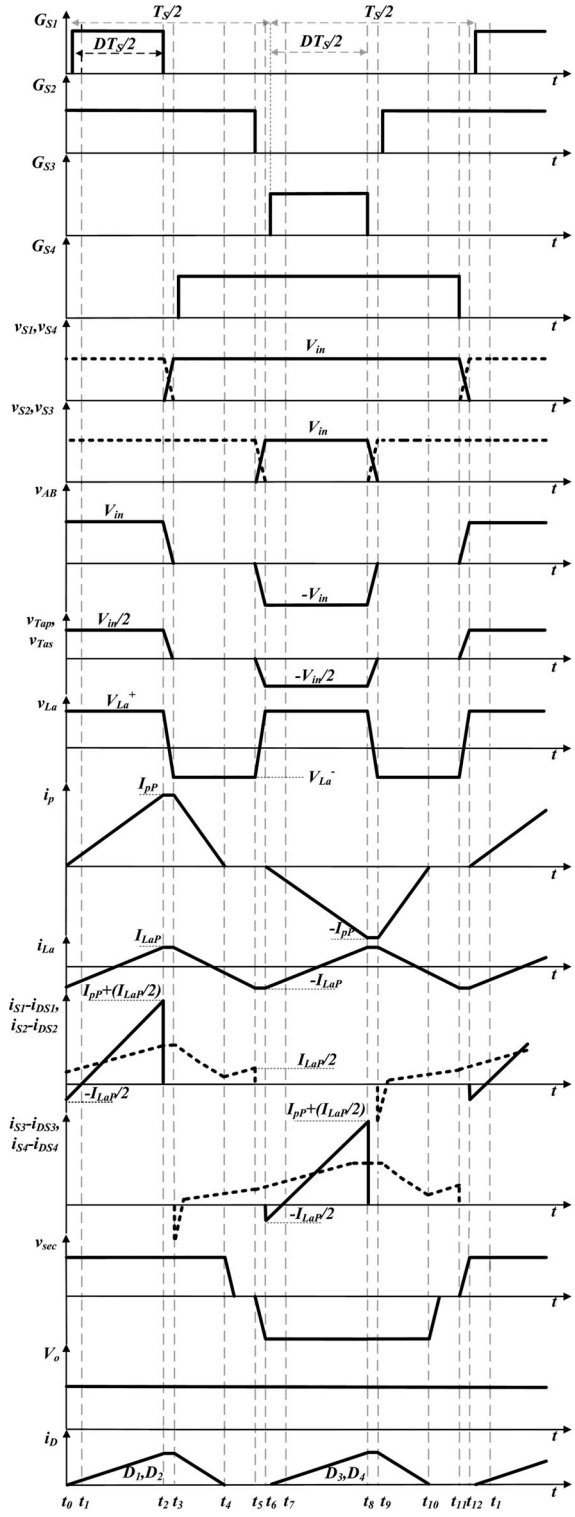

Fig. 3. Key operational waveforms of the proposed converter.

This interval ends at $t = t_1$. The switch current $i_{S1}(t) - i_{\rm DS1}(t)$ is positive at the end of this interval. The duration Δt_{1-0} of this interval is given by

$$\Delta t_{1-0} = \frac{I_{LaP}}{2\left(\frac{V_{\rm in} - V_o/n}{L_{\rm se}}\right) + \frac{V_{\rm in}(1-D)}{2L_a}} \tag{7}$$

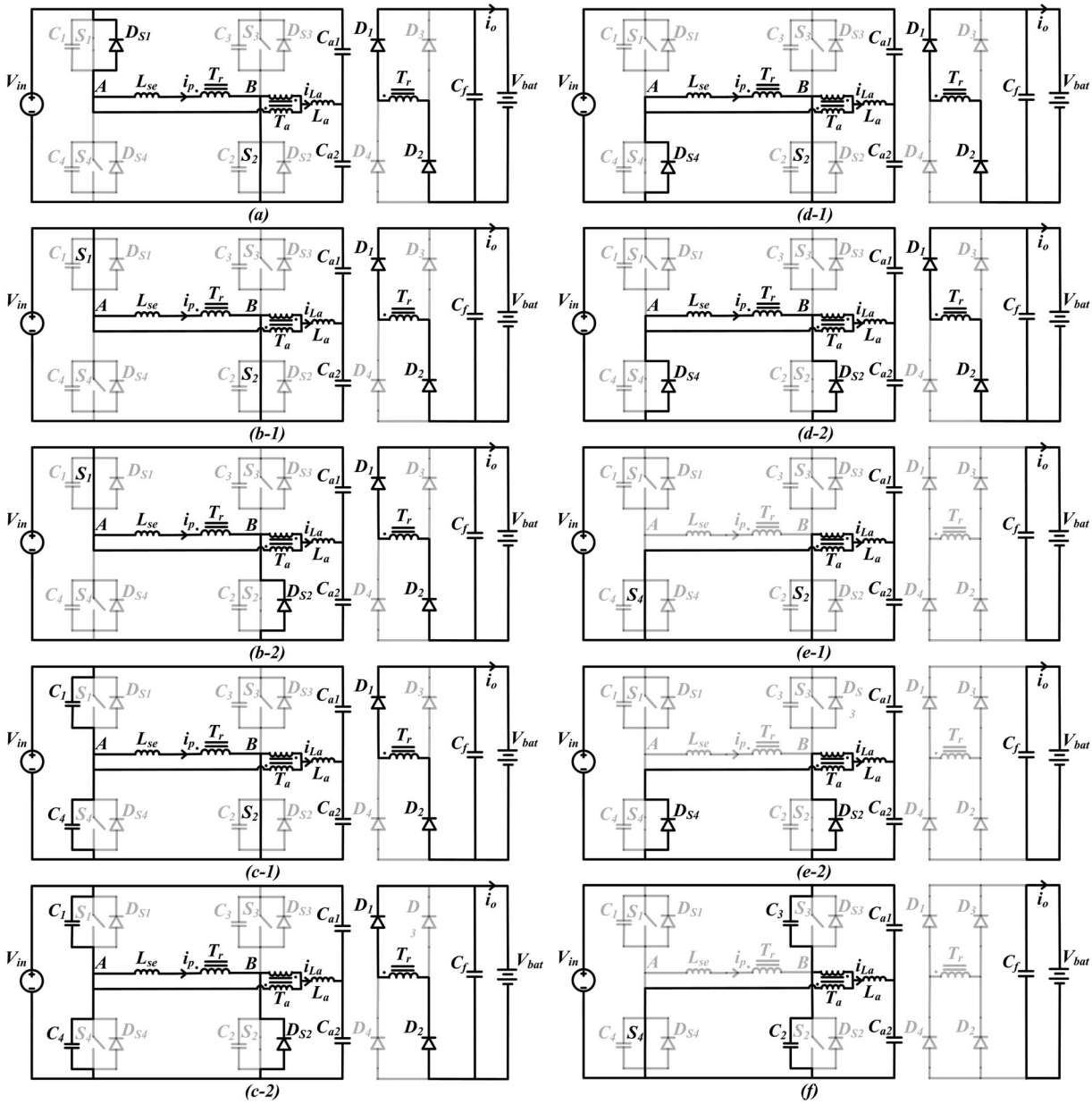

Fig. 4. Steady-state operating circuit conditions of the proposed converter. (a) $t_0 \le t \le t_1$. (b-1) $t_1 \le t \le t_2$(heavy load) and $t_1 \le t \le t_1^1$(light load). (b-2) $t_1^1 \le t \le t_2$(light load). (c-1) $t_2 \le t \le t_3$(heavy load). (c-2) $t_2 \le t \le t_3$(light load).(d-1) $t_3 \le t \le t_4$(heavy load). (d-2)$t_3 \le t \le t_4$(light load). (e-1) $t_4 \le t \le t_5$(heavy load) and $t_4^1 \le t \le t_5$(light load).(e-2) $t_4^1 \le t \le t_5$(light load). (f) $t_5 \le t \le t_6$.

where $V_{\rm in}$is the input voltage, V_o is the output voltage, $v_{\rm Tap}(t)$ and $v_{\rm Tas}(t)$ are the voltages across the primary and secondary of T_a, respectively, $i_p(t)$ is the current through the series inductor $L_{\rm se}$, and primary side of the transformer T_r, $i_{S1}(t)$, and $i_{S2}(t)$ are the currents through switches S_1 and S_2, respectively, and $i_{\rm DS1}(t)$ and $i_{\rm DS2}(t)$ are the currents through the body-diodes D_{S1} and D_{S2} currents, respectively.

Interval II ($t_1 \le t \le t_2$): In this interval the circuit conditions are dependent on load conditions. According to (6), the conduction of S_2 or D_{S2} is dependent on magnitudes of $i_p(t)$and $i_{La}(t)$. It can be understood by examining the following cases. Case 1: Under (CC) charging mode, $i_p(t)$ is always greater than $i_{La}(t)/2$, i.e., S_2 is in conduction. Case 2: Under (CV) charging mode, the power drawn from the charger is low, especially when the battery is with higher SOC. In this case, $i_p(t)$ will be less than $i_{La}(t)/2$, i.e., D_{S2} will be in conduction. A duty cycle $D_{\rm boundary}$ is defined to differentiate the heavy-load and light-load conditions. $D_{\rm boundary}$ corresponds to the same peak values of $i_p(t)$ and $i_{La}(t)/2$. Therefore, the duty cycle $D > D_{\rm boundary}$ or $I_{pP} > I_{LaP}/2$ is treated as a heavy-load condition and $D < D_{\rm boundary}$ or $I_{pP} < I_{LaP}/2$ is treated as a light-load condition. The $D_{\rm boundary}$ can be calculated by

$$D_{\rm boundary} = 1 - \frac{8L_a}{L_{\rm se}}\left(1 - \frac{V_o}{nV_{\rm in}}\right) \tag{8}$$

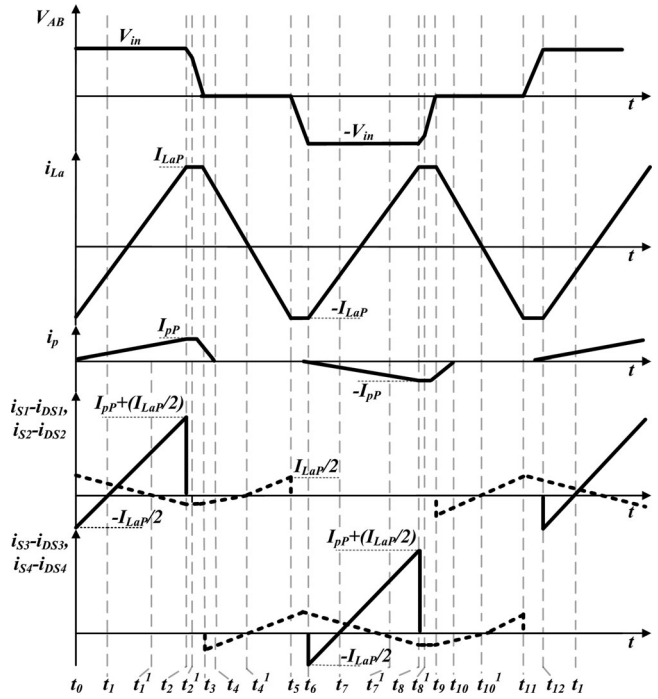

Fig. 5. Theoretical operational waveforms of proposed converter when $D < D_{\mathrm{boundary}}$.

where I_{pP} is the peak value of main transformer primary current. Therefore, the circuit conditions under different load conditions are explained as follows:

Under Heavy-Load Condition: The currents i_p and i_{La} continue to rise linearly similar to that in *Interval I*. The dc input source transfers power to the load through main switches S_1 and S_2, and output diodes D_1 and D_2. The corresponding circuit conditions are shown in Fig. 4(b-1). The duration of this interval is approximated as follows:

$$\Delta t_{2-1} = \frac{DT_s}{2} - \Delta t_{1-0}. \tag{9}$$

Under Light-Load Condition: The currents i_p and i_{La} continue to rise linearly similar to that in *Interval I,* as shown in Fig. 5. The dc input source transfers power to the load through main switches S_1 and S_2 and output diodes D_1 and D_2 until $i_p(t) > i_{La}(t)/2$. The circuit conditions are the same as shown in Fig. 4(b-1) for $t_1 \le t \le t_1^1$. The duration Δt_{1-1}^1 of this circuit condition is given by

$$\Delta t_{1-1}^1 = \frac{I_{LaP}}{\frac{V_{\mathrm{in}}(1-D)}{2L_a} - 2\left(\frac{V_{\mathrm{in}} - V_o/n}{L_{\mathrm{se}}}\right)} - \Delta t_{1-0}. \tag{10}$$

When $i_p(t) < i_{La}(t)/2$, the dc input source transfers power to the load through main switch S_1, body-diode D_{S2}, output diodes D_1, and D_2. The circuit conditions during this period are shown in Fig. 4(b-2) for $t_1^1 \le t \le t_2$. The time Δt_{2-1}^1 can be calculated using the following expression:

$$\Delta t_{2-1}^1 = \frac{DT_s}{2} - \Delta t_{1-1}^1 - \Delta t_{1-0}. \tag{11}$$

This interval ends once the switch S_1 is turned OFF at t_2. The currents i_p and i_{La} attain their peak values at t_2. At the end of *Interval II*, i.e., $t = t_2$, we obtain the following:

$$v_{C1}(t_2) = v_{C2}(t_2) = 0;\ v_{C3}(t_2) = v_{C4}(t_2) = V_{\mathrm{in}} \tag{12}$$

$$i_p(t_2) = I_{pP};\ i_{La}(t_2) = I_{LaP} = \frac{V_{\mathrm{in}} D(1-D)}{8L_a f_s} \tag{13}$$

$$i_{S1}(t_2) - i_{\mathrm{DS1}}(t_2) = I_{pP} + \frac{I_{LaP}}{2} \tag{14}$$

$$i_{S2}(t_2) - i_{\mathrm{DS2}}(t_2) = I_{pP} - \frac{I_{LaP}}{2}. \tag{15}$$

Interval III ($t_2 \le t \le t_3$): When S_1 is turned OFF at t_2, the currents i_p and $i_{La}/2$ that were initially flowing through the switch S_1 will now flow through C_1 and C_4. These currents charge the capacitor C_1 and discharge the capacitor C_4 simultaneously. The output diodes D_1 and D_2 continue to conduct the load current. The current i_{La} can be considered constant as the time duration of this interval is small and is given by

$$i_{La}(t) = I_{LaP}. \tag{16}$$

In this interval, the charging and discharging of C_1 and C_4 depends on the load conditions which are described as follows:

Under Heavy-Load Condition: The energy stored in L_{se} is sufficient to charge C_1 and discharge C_4 completely. The body-diode D_{S4} is forward-biased ensuring ZVS turn-on for S_4 by the end of this interval. The circuit conditions during this interval are shown in Fig. 4(c-1). During this interval, the current through series inductor i_p, the voltages v_{C1} and v_{C4} across capacitors C_1 and C_4, and the output voltage of the inverter v_{AB} are given by

$$i_p(t) = \left(I_{pP} + \frac{I_{LaP}}{2}\right)\cos\left(\frac{t-t_2}{\sqrt{2L_{\mathrm{se}}C}}\right) - \frac{I_{LaP}}{2} \tag{17}$$

$$v_{C1}(t) = \left(I_{pP} + \frac{I_{LaP}}{2}\right)\sqrt{\frac{L_{\mathrm{se}}}{2C}}\sin\left(\frac{t-t_2}{\sqrt{2L_{\mathrm{se}}C}}\right) \tag{18}$$

$$v_{C4}(t) = V_{\mathrm{in}} - \left(I_{pP} + \frac{I_{LaP}}{2}\right)\sqrt{\frac{L_{\mathrm{se}}}{2C}}\sin\left(\frac{t-t_2}{\sqrt{2L_{\mathrm{se}}C}}\right) \tag{19}$$

$$v_{\mathrm{AB}}(t) = v_{C4}(t);\ v_{\mathrm{Tap}}(t) = v_{\mathrm{Tas}}(t) = \frac{v_{\mathrm{AB}}(t)}{2}. \tag{20}$$

Equation (19) also implies that ZVS for low-side switch S_4 can be easily achieved because the magnitude of discharging current $i_{S1}(t_2)$ is greater than the conventional ZVS full-bridge dc–dc converter [31]. Similarly, ZVS for switch S_2 can be achieved in second half of the switching cycle ($T_s/2 \le t \le T_s$). The duration Δt_{3-2} of this interval is given by

$$\Delta t_{3-2} = \sqrt{2L_{\mathrm{se}}C}\sin^{-1}\left(\frac{2V_{\mathrm{in}}}{2I_{pP} + I_{LaP}}\sqrt{\frac{2C}{L_{\mathrm{se}}}}\right). \tag{21}$$

Under Light-Load Condition: The energy stored in L_{se} alone is not sufficient to completely discharge the capacitor C_4 as I_{pP} is very small. The proposed auxiliary inductor L_a assists in discharging C_4 completely. The body-diode D_{S4} is forward-biased

ensuring ZVS turn-on for S_4 by the end of this interval. Therefore, the transition from high-side switch S_1 to low-side switch S_4 results in two different slopes in inverter output voltage $v_{\rm AB}$, as shown in Fig. 5. The first slope is determined by i_p and i_{La} during $t_2 \le t \le t_2^1$ and the second slope is mainly determined by i_{La} during $t_2^1 \le t \le t_3$. The circuit conditions during this interval are shown in Fig. 4(c-2), where the body-diode D_{S2} conducts instead of switch S_2 as $I_{pP} < I_{LaP}/2$. The voltages v_{C1} and v_{C4} during this interval are given by

$$V_{C1}(t_2^1) = \left(I_{pP} + \frac{I_{LaP}}{2}\right)\sqrt{\frac{L_{\rm se}}{2C}}\sin\left(\frac{t_2^1 - t_2}{\sqrt{2L_{\rm se}C}}\right) \quad (22)$$

$$v_{C1}(t) = V_{C1}(t_2^1) + \frac{I_{LaP}}{4C}(t - t_2^1) \quad (23)$$

$$v_{C4}(t) = V_{\rm in} - V_{C1}(t_2^1) - \frac{I_{LaP}}{4C}(t - t_2^1). \quad (24)$$

This interval ends when the voltage $v_{\rm AB}$ becomes zero. At the end of *Interval III*, i.e., $t = t_3$

$$v_{C2}(t_3) = v_{C4}(t_3) = 0;\ v_{C1}(t_3) = v_{C3}(t_3) = V_{\rm in}. \quad (25)$$

Interval IV ($t_3 \le t \le t_4$): This interval starts when $v_{\rm AB}$ becomes zero and D_{S4} is forward-biased. During this interval, the output diodes D_1 and D_2 clamp secondary voltage of the main transformer to the output voltage. Thus, a net reflected output voltage V_o/n is applied across $L_{\rm se}$ which causes its current i_p to ramp down linearly with a slope of $V_o/nL_{\rm se}$as given by

$$i_p(t) = I_p(t_3) - \frac{V_o}{nL_{\rm se}}(t - t_3). \quad (26)$$

During this interval, a net negative voltage is applied across L_a due to V_{ca1}. Therefore, the current i_{La} ramps down from $+I_{LaP}$ with a different slope $DV_{\rm in}/2L_a$ compared to the rising slope $(1-D)V_{\rm in}/2L_a$ in *Interval I*. The auxiliary inductor current and voltage are given as

$$i_{La}(t) = I_{LaP} - \frac{DV_{\rm in}}{2L_a}(t - t_3) \quad (27)$$

$$v_{La}(t) = V_{La}^- = -\frac{DV_{\rm in}}{2}. \quad (28)$$

The output diodes D_1 and D_2 continue to conduct the load current. The circuit conditions on the primary side during this interval are described as follows:

Under Heavy-Load Condition: The circuit conditions during this interval are shown in Fig. 4(d-1), where the main switch S_2 is in conduction as $i_p(t) > i_{La}(t)/2$. Under this load condition, i_{La} reaches zero and starts to rise in the negative direction before the current i_p reaches zero.

Under Light-Load Condition: The circuit conditions during this interval are shown in Fig. 4(d-2), where the body-diode D_{S2} conducts instead of the switch S_2 as $i_p(t) < i_{La}(t)/2$ during this interval, as shown in Fig. 5.

This interval ends when the decaying primary current $i_p$reaches zero. At the end of *Interval IV*, i.e., at $t = t_4$, we obtain

$$i_p(t_4) = 0;\ i_{D1}(t_4) = 0;\ i_{D2}(t_4) = 0. \quad (29)$$

The duration of this interval Δt_{4-3} is given by

$$\Delta t_{4-3} = \left(\frac{nV_{\rm in}}{V_o} - 1\right)\frac{DT_s}{2} - \Delta t_{3-2}. \quad (30)$$

Interval V ($t_4 \le t \le t_5$): This interval starts when current through the primary side of main transformer i_p becomes zero, which indicates that the current through output diodes $i_{\rm D1}$ and $i_{\rm D2}$ is zero. The output capacitor C_f clamps the diode-bridge voltage to the output voltage and provides energy to the load during this interval. The auxiliary inductor current continues to ramp down with the same slope as observed in *Interval IV*. The circuit conditions on the primary side during this interval are described as follows.

Under Heavy-Load Condition: The circuit conditions during this interval are shown in Fig. 4(e-1). During this period, the auxiliary inductor current freewheels through S_2 and S_4. The switch S_4 conducts instead of body-diode D_{S4} as the current i_{La} is negative. During this interval, the switches S_2 and S_4, and body-diodes D_{S2} and D_{S4} currents are given by

$$i_{S2}(t) = \frac{i_{La}(t)}{2};\ i_{\rm DS2}(t) = 0 \quad (31)$$

$$i_{S4}(t) = \frac{i_{La}(t)}{2};\ i_{\rm DS4}(t) = 0. \quad (32)$$

The duration of this interval Δt_{5-4} is given by

$$\Delta t_{5-4} = (1-D)\frac{T_s}{2} - \Delta t_{4-3} - \Delta t_{3-2} - \Delta t_{6-5}. \quad (33)$$

Under Light-Load Condition: The current i_{La} ramps down to zero with a slope of $DV_{\rm in}/2L_a$ and the respective circuit conditions are shown in Fig. 4(e-2). During $t_4 \le t \le t_4^1$, the auxiliary inductor current freewheels through D_{S2}, D_{S4} as $i_{La}(t)$ is positive which is shown in Fig. 5. During this interval, the switches S_2 and S_4, and body-diodes D_{S2} and D_{S4} currents are given by

$$i_{S2}(t) = 0;\ i_{\rm DS2}(t) = \frac{i_{\rm La}(t)}{2} \quad (34)$$

$$i_{S4}(t) = 0;\ i_{\rm DS4}(t) = \frac{i_{\rm La}(t)}{2}. \quad (35)$$

The duration of this interval Δt_{4-4}^1 is given by

$$\Delta t_{4-4}^1 = (1-D)\frac{T_s}{4} - \Delta t_{4-3} - \Delta t_{3-2}. \quad (36)$$

During $t_4^1 \le t \le t_5$, the circuit conditions are similar to the heavy-load condition, as shown in Fig. 4(e-1), as $i_{La}(t)$ becomes negative with the same slope $DV_{\rm in}/2L_a$. The time duration Δt_{5-4}^1 of this circuit condition is given by

$$\Delta t_{5-4}^1 = (1-D)\frac{T_s}{4} - \Delta t_{6-5}. \quad (37)$$

This interval ends when the current i_{La} attains its negative peak value $-I_{LaP}$ and switch S_2 is turned OFF. S_2 achieves near ZCS as the turn-off current $(I_{LaP}/2)$ is smaller than the peak value of the series inductor current I_{pP}.

Interval VI ($t_5 \le t \le t_6$): This interval starts when S_2 is turned OFF at t_5. The circuit conditions during this interval

TABLE I
DESIGN SPECIFICATIONS OF PROPOSED FULL-BRIDGE DC–DC CONVERTER

Parameters	Value
Input dc voltage	300 V
Output dc voltage range	209–350 V
Maximum output dc current	3.75 A
Maximum output power	1.2 kW
Full-bridge switching frequency	100 kHz
Output voltage ripple	$< 3.5\ V_{pk\text{-}pk}$
Auxiliary capacitor voltage ripple	$< 3\ V_{pk\text{-}pk}$

are shown in Fig. 4(f). The auxiliary inductor current which was initially flowing through S_2 will flow through C_2 and C_3 during this interval. This current will charge the capacitor C_2 and discharge the capacitor C_3 simultaneously, and the respective voltages are given by (38) and (39). By the end of this interval, the capacitor C_3 is discharged completely and the body-diode D_{S3} is forward-biased ensuring ZVS turn-on for S_3. The current i_{La} can be considered constant due to the short duration of this interval

$$v_{C2}(t) = \frac{I_{LaP}}{4C}(t - t_5) \tag{38}$$

$$v_{C3}(t) = V_{\text{in}} - \frac{I_{LaP}}{4C}(t - t_5). \tag{39}$$

Equation (39) also implies that the ZVS for high-side switch S_3 can only be achieved with the auxiliary circuit current i_{La}. The ZVS mechanism for S_1 in the second half of switching period ($T_s/2 \le t \le T_s$) is similar to S_3.

This interval ends when the voltage v_{AB} becomes V_{in}. At the end of *Interval VI*, i.e., $t = t_6$, we obtain

$$v_{C3}(t_6) = v_{C4}(t_6) = 0;\ v_{C1}(t_6) = v_{C2}(t_6) = V_{\text{in}} \tag{40}$$

$$v_{La}(t_6) = V_{La}^{+} = (1 - D)\frac{V_{\text{in}}}{2}. \tag{41}$$

The duration Δt_{6-5} of this interval is given by

$$\Delta t_{6-5} = \frac{4CV_{\text{in}}}{I_{LaP}}. \tag{42}$$

IV. ANALYSIS OF PROPOSED CONVERTER

The specifications given in Table I are considered for analyzing the proposed converter. The converter operates under battery charging profile, as shown in Fig. 6 [35]. The voltage limits of the battery are based on Ford C-Max Hybrid EV battery specifications [37]. The key load points in the battery charging profile are listed in Table II. The steady-state analysis of the converter is given as follows.

A. Voltage Gain Analysis

The voltage gain of the proposed converter is determined using the volt–second balance of L_{se} and the average value of series inductor current i_p [38]. From *Interval I – Interval IV* operation analysis of the converter, it can be deduced as follows:

$$\frac{nV_{\text{in}} - V_o}{nL_{\text{se}}}(t_2 - t_0) = \frac{V_o}{nL_{\text{se}}}(t_4 - t_2) \tag{43}$$

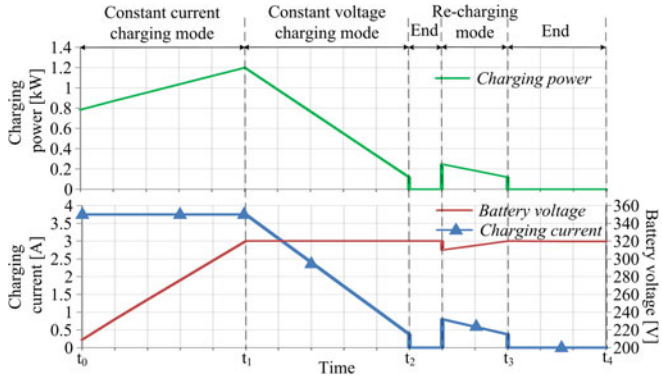

Fig. 6. Lithium-ion battery charging profile.

TABLE II
KEY POINTS IN THE CHARGING PROFILE OF LITHIUM-ION BATTERY PACK

Parameter	Start point	Nominal point	Transition point	End point	Recharge point
V_{bat} [V]	209	280	320	320	310
I_{bat} [A]	3.75	3.75	3.75	0.375	0.8
R_{ebat} [Ω]	55.73	74.67	85.33	853.33	387.5
P_o [kW]	0.78	1.05	1.2	0.12	0.25

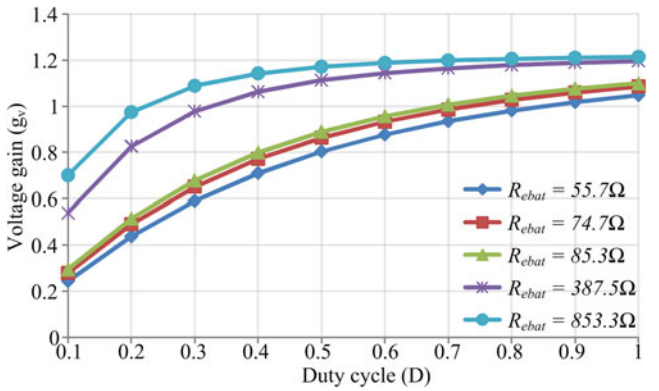

Fig. 7. Voltage gain characteristics of the converter.

$$\frac{(nV_{\text{in}} - V_o)(t_2 - t_0)(t_4 - t_0)f_s}{nL_{\text{se}}} = \frac{nV_o}{R_{\text{ebat}}} \tag{44}$$

where R_{ebat} is the equivalent load of the converter. The voltage gain of the converter can be obtained from (43) and (44), and is given by

$$g_v = \frac{V_o}{V_{\text{in}}} = \frac{2n}{1 + \sqrt{1 + \frac{4n^2 L_{\text{se}}}{f_s R_{\text{ebat}}(t_2 - t_0)^2}}}. \tag{45}$$

The voltage gain g_v of the converter at different loads with respect to the duty cycle D is shown in Fig. 7.

B. Auxiliary Circuit Voltage and Current

The auxiliary capacitors C_{a1} and C_{a2} act as constant dc voltage sources during a switching period. The respective voltages V_{ca1} and V_{ca2}, when the converter is gated with APWM and

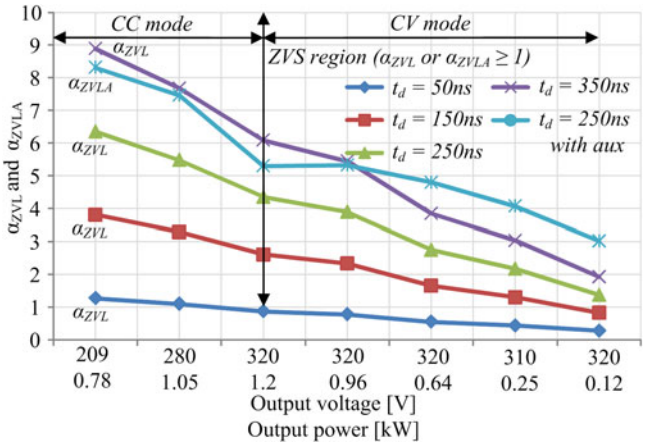

Fig. 8. ZVS range of low-side switches over battery charging profile.

PSM, are given by

$$V_{\mathrm{ca1}} = \frac{(2-D)V_{\mathrm{in}}}{2}; V_{\mathrm{ca2}} = \frac{DV_{\mathrm{in}}}{2};\ \mathrm{APWM}$$

$$V_{\mathrm{ca1}} = V_{\mathrm{ca2}} = \frac{V_{\mathrm{in}}}{2};\ \mathrm{PSM}. \tag{46}$$

The peak value of the auxiliary inductor current, when the converter is gated with APWM and PSM, is given by

$$I_{LaP} = \frac{V_{\mathrm{in}}D(1-D)}{8L_a f_s};\ \mathrm{APWM}$$

$$I_{LaP} = \frac{V_{\mathrm{in}}(1-D)}{8L_a f_s};\ \mathrm{PSM}. \tag{47}$$

C. Soft-Switching Analysis

1) Without Auxiliary Circuit: According to (19), the ZVS condition for low-side switches S_2 and S_4 depends on I_{pP}, I_{Lap}, and dead-time t_d. In this section, the ZVS analysis is carried out without considering the auxiliary circuit, i.e., the auxiliary circuit current I_{LaP} is zero. A factor called α_{ZVL} given in (48) is defined to validate the ZVS range for low-side switches. The ZVS transition for low-side switches is achieved only when $\alpha_{\mathrm{ZVL}} > 1$

$$\alpha_{\mathrm{ZVL}} = \frac{t_d}{2C}\left(\frac{V_o}{V_{\mathrm{in}}}\sqrt{\left(1-\frac{V_o}{nV_{\mathrm{in}}}\right)\frac{1}{R_{\mathrm{ebat}}L_{\mathrm{se}}f_s}}\right). \tag{48}$$

As seen in (48), α_{ZVL} is a function of switch capacitance, input and output voltages, effective load resistance on the system, series inductance, switching frequency, and dead-time. The effect of various parameters on α_{ZVL} is discussed next.

The ZVS range factor for low-side switches α_{ZVL} without the auxiliary circuit and with respect to the battery charging profile at different dead-times is shown in Fig. 8. An equivalent capacitance of $C = 0.88$ nF and a series inductance $L_{\mathrm{se}} = 18.72\ \mu$H are considered for analysis. From Fig. 8, it can be observed that a minimum t_d of 185 ns is required to achieve ZVS turn-on for low-side switches over the entire battery charging range. However, an increase in t_d requires more secondary turns to obtain the rated output voltage, which translates to higher conduction losses on the primary side.

ZCS for low-side switches S_2 and S_4 can be achieved because the main transformer T_r operates in discontinuous conduction mode (DCM). For high-voltage battery charging applications, MOSFETs switching losses can be greatly minimized by operating them with ZVS rather than ZCS. The increased ZVS range for S_2 and S_4 and ZVS for S_1 and S_3 are achieved by integrating an auxiliary circuit, as shown in the proposed converter in Fig. 2(a).

2) With Auxiliary Circuit: For the proposed passive auxiliary circuit-assisted converter, a factor called α_{ZVLA} given in (49) is defined to validate the ZVS range for low-side switches using *Interval III* analysis. The ZVS transition for low-side switches can be achieved only when $\alpha_{\mathrm{ZVLA}} > 1$

$$\alpha_{\mathrm{ZVLA}} = \frac{t_d}{2C}\left(\frac{V_o}{V_{\mathrm{in}}}\sqrt{\left(1-\frac{V_o}{nV_{\mathrm{in}}}\right)\frac{1}{R_{\mathrm{ebat}}L_{\mathrm{se}}f_s}} + \frac{D(1-D)}{16L_a f_s}\right). \tag{49}$$

α_{ZVLA} is also plotted in Fig. 8 with respect to battery charging profile at different dead-times. It can be inferred from Fig. 8 that a minimum t_d of 85 ns is required to guarantee ZVS turn-on for low-side switches S_2 and S_4. The auxiliary inductance L_a is chosen to guarantee ZVS turn-on for high-side switches S_1 and S_3. Hence, the proposed system results in ZVS turn-on for all active switches S_1–S_4 over the entire battery charging range. The design considerations for the auxiliary inductor are explained in the next section.

The low-side switches S_2 and S_4 can also achieve near ZCS as their turn-off current $(I_{LaP}/2)$ is smaller than the peak value of the series inductor current I_{pP}.

D. Features of Proposed Converter With APWM

1) ZVS turn-on for all the active switches over the entire battery charging range—from *Interval III* and *Interval VI* analyses and soft-switching analysis with the auxiliary circuit.
2) Near ZCS turn-off for low-side switches as the auxiliary circuit current is small during their turn-off transition—from *Interval V* analysis.
3) The circulating losses during the freewheeling period on the primary side are minimal due to the current-driven configuration, capacitive output filter, and APWM gating technique—from *Interval V* analysis.
4) The secondary side freewheeling losses are completely eliminated as the main transformer T_r is operated in DCM; however, the DCM operation increases the peak current of the series inductor which may affect the efficiency at heavy loads—from *Interval V* analysis.
5) The reverse-recovery and the switching losses in the output rectifier diodes are minimal as they are naturally commutated when the series inductor L_{se} current reaches zero—from *Interval V* analysis.

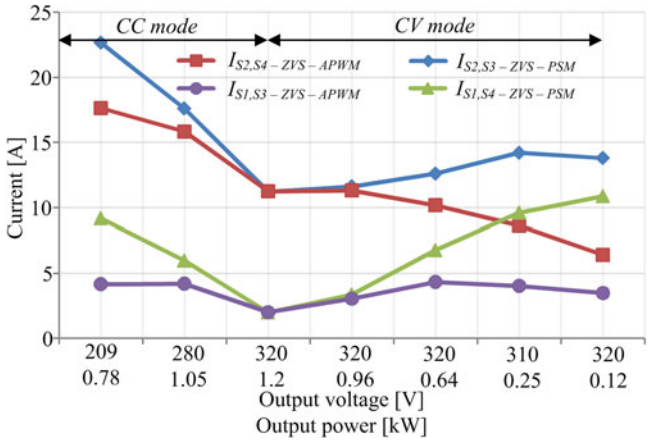

Fig. 9. Comparison of ZVS currents with APWM and PSM operated converter.

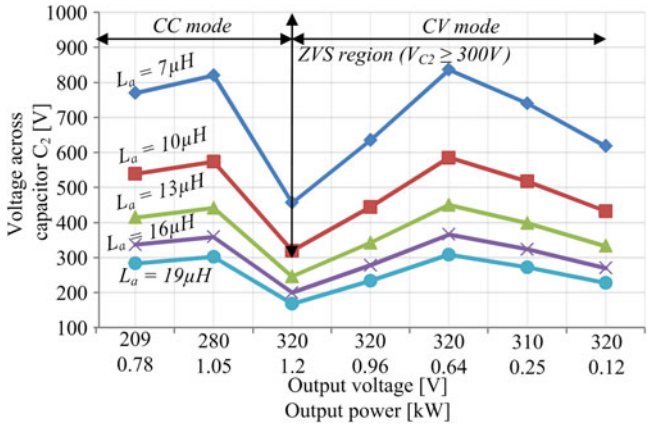

Fig. 10. Load versus V_{C2} for different values of L_a.

6) The voltage spikes across the output rectifier diodes are mitigated due to the current-driven and the capacitive output filter configuration—from *Interval V* analysis.
7) Improved EMI due to mitigation of the high voltage spikes across the output rectifier diodes—from *Interval V* analysis.
8) The output power and voltage are regulated by controlling the duty cycle of the active switches.
9) The auxiliary inductance L_a required to achieve ZVS turn-on with APWM is 25% less when compared to PSM.
10) The peak value of current through active switches during ZVS transition with APWM is smaller than PSM. The switching current for active switches is given by

$$I_{S2,S4-\mathrm{ZVS-APWM}} = V_o\sqrt{\left(1-\frac{V_o}{nV_{\mathrm{in}}}\right)\frac{1}{R_{\mathrm{ebat}}L_{\mathrm{se}}f_s}} + \frac{V_{\mathrm{in}}D(1-D)}{16L_{\mathrm{aAPWM}}f_s} \tag{50}$$

$$I_{S1,S3-\mathrm{ZVS-APWM}} = \frac{V_{\mathrm{in}}D(1-D)}{16L_{\mathrm{aAPWM}}f_s}. \tag{51}$$

The switching current for the active switches when the converter is operated with PSM is given by

$$I_{S2,\,S3-\mathrm{ZVS-PSM}} = V_o\sqrt{\left(1-\frac{V_o}{nV_{\mathrm{in}}}\right)\frac{1}{R_{\mathrm{ebat}}L_{\mathrm{se}}f_s}} + \frac{V_{\mathrm{in}}(1-D)}{16L_{\mathrm{aPSM}}f_s} \tag{52}$$

$$I_{S1,S4-\mathrm{ZVS-PSM}} = \frac{V_{\mathrm{in}}(1-D)}{16L_{\mathrm{aPSM}}f_s}. \tag{53}$$

Theoretical comparison of ZVS currents with APWM and PSM at different loads using (50)–(53) is shown in Fig. 9. It is evident that the ZVS current levels with PSM are greater than APWM operated converter. It can be concluded from this analysis that the switching and conduction losses on the primary side are substantial when the converter is operated with PSM. Therefore, the proposed APWM gating technique results in increased efficiency compared to the PSM gating technique. It is further verified with the experimental results presented in Section VII.

V. Circuit Parameters Design

A. Transformer Turns Ratio

The main power transformer T_r turns ratio n is designed for maximum output voltage at maximum duty-cycle ratio of 0.95 which is given by

$$n = \frac{V_{\mathrm{omax}}}{D_{\mathrm{max}}V_{\mathrm{in}}} = 1.23. \tag{54}$$

B. Series Inductor

The series inductance is estimated to ensure the critical conduction mode of the converter at the full-load condition. The full-load condition corresponds to the CC mode to CV mode transition point mentioned in Table II. Therefore, the series inductance value is given by

$$L_{\mathrm{se}} = \left(1-\frac{V_o}{nV_{\mathrm{in}}}\right)\frac{V_o^2}{4n^2f_sP_o} = 18.72\ \mu\mathrm{H}. \tag{55}$$

C. Auxiliary Inductor

The auxiliary inductance should be selected to ensure that the available reactive energy during switching transitions guarantees ZVS for all MOSFETs over the battery charging range of the converter. The auxiliary inductor L_a acts as a constant current source during t_d with a magnitude of I_{Lap}. This current charges and discharges the capacitor C_2 and C_3 during *Interval VI*. By using (38), the variation of voltage across capacitor C_2 during *Interval VI* with respect to different load conditions for various auxiliary inductances is shown in Fig. 10. In order to ensure ZVS, the capacitor voltage V_{C2} should be greater than the dc input voltage V_{in} over the entire battery charging range within $t_d = 250$ ns. According to Fig. 10, the voltage V_{C2} is minimum at the full-load condition. The duty cycle of the converter

corresponding to full-load condition is given by

$$D = \sqrt{\frac{16n^2 L_{\rm se} f_s / R_{\rm ebat}}{\left(\frac{2nV_{\rm in}}{V_o} - 1\right)^2 - 1}} = 0.86. \tag{56}$$

Then, the auxiliary inductance value is calculated by

$$L_a = \frac{D(1-D)t_d}{32Cf_s} = 10.7\ \mu\text{H}. \tag{57}$$

D. Auxiliary Capacitors

To ensure proper operation of the proposed converter, the two auxiliary capacitors C_{a1} and C_{a2} in the passive auxiliary circuit should behave as constant dc voltage sources over a single switching period. The auxiliary capacitances should be selected such that the peak-to-peak ripple voltage on each capacitor is small at the maximum auxiliary reactive current. The minimum required capacitance allowing a ripple of $\Delta V_{Ca} = 3$ V is estimated by

$$C_{a1} = C_{a2} \geq \frac{V_{\rm in}}{256 L_a f_s^2 \Delta V_{\rm ca}} \geq 3.65\ \mu\text{F}. \tag{58}$$

Therefore, two 4.7-μF auxiliary capacitors are selected.

E. Output Filter Capacitor

The output filter capacitor is designed based on the allowable ripple in the output voltage. The minimum filter capacitance required to maintain the voltage ripple within 1% is given by

$$C_f \geq \frac{I_o}{8 f_s \Delta V_{cf}} \geq 1.34\ \mu\text{F}. \tag{59}$$

Therefore, a 2.2-µF output filter capacitor is selected.

VI. Magnetics Design

Magnetics design for the auxiliary circuit is one of the important parts of the converter to achieve improved efficiency. The proposed converter consists of one auxiliary inductor, one auxiliary transformer, one main transformer, and one series inductor. The design steps for the auxiliary inductor are discussed as follows:

1) Select core material: Manganese-Zinc Ferrite core is chosen as it is characterized by low losses at high frequencies in the range of 100–300 kHz.

2) Set design constraint: The design constraint for the auxiliary circuit is that the maximum loss should be less than 6 W (0.5% of rated power). The maximum power loss $P_{\rm tot\_allowed}$ constraints for the auxiliary inductor and auxiliary transformer must be less than 2.5 and 3.5 W, respectively.

3) Calculate maximum volt–second product: The voltage, current, and flux density waveforms of the auxiliary inductor are shown in Fig. 11. The required inductor is a linear ac inductor as the corresponding flux density $\mathrm{B}_{La}(\mathrm{t})$ is bipolar triangular. The maximum volt–second product λ across the auxiliary inductor is the main parameter required for the design. It is given by

$$\lambda = \frac{V_{\rm in} D(1-D)}{4fs} = 187.5 \times 10^{-6}\ \text{Vs}. \tag{60}$$

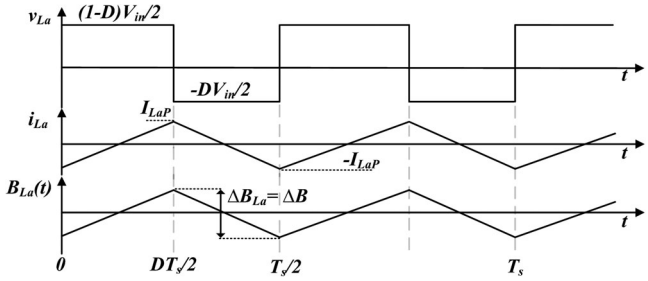

Fig. 11. Voltage, current, and flux density waveforms of L_a.

4) Calculate maximum RMS current and wire gauge: The maximum RMS current through the auxiliary inductor is given by

$$I_{La\rm RMS} = \frac{V_{\rm in} D(1-D)}{8\sqrt{3} L_a f_s} = 5\text{A}. \tag{61}$$

The Litz wire gauge for the auxiliary inductor is AWG14. It is calculated based on the maximum RMS current and current density $J = 2.5$ A/ mm^2. The AWG14 Litz wire is made of 6 strings of 40 strands of AWG38.

5) Determine core size: The core is selected to ensure that the core geometrical constant $K_{\rm geometry}$ is greater than the electrical specification constant $K_{\rm electrical}$ [38]. The constants are given by

$$K_{\rm geometry} = \frac{A_w A_e^{(2(\beta-1)/\beta)}}{(\text{MLT})(l_e^{2/\beta})}((\beta/2)^{-\beta/(\beta+2)} + (\beta/2)^{2/(\beta+2)})^{-(\beta+2)/\beta} \tag{62}$$

$$K_{\rm electrical} = \frac{\rho\lambda^2 {I_{La\rm RMS}}^2 {K_{fe}}^{2/\beta}}{4K_u {P_{\rm tot\_allowed}}^{(\beta+2)/\beta}}. \tag{63}$$

The parameters required for (62) and (63) can be found in the datasheet of the core selected. RM12 core satisfies the inequality $K_{\rm geometry}(1.5 \times 10^{-7}) > K_{\rm electrical}(2.8 \times 10^{-9})$. The critical parameters of the core are given in Table III.

6) Select number of turns: The selection of the number of turns for the auxiliary inductor depends on the peak-to-peak flux density ΔB_{La}, core winding area A_w, and the winding fill factor K_u. The optimal flux density $\Delta B_{La\rm Opt}$ to minimize the total loss in the auxiliary inductor is calculated by (64). Then, the number of turns N_{La} for L_a is estimated from (65). The number of turns selected should also satisfy the criterion that the core window area is large enough to accommodate Litz AWG calculated in step 4 and is given by (66)

$$\Delta B_{La\rm Opt} = 2\left(\frac{\rho\lambda^2 {I_{La\rm RMS}}^2 (\text{MLT})}{2K_u A_w {A_e}^3 l_e \beta K_{fe}}\right)^{1/(\beta+2)} \tag{64}$$

$$N_{La} = \frac{V_{\rm in} D(1-D)}{4\Delta B_{La} A_e f_s} \tag{65}$$

$$K_u A_w \geq N_{La} W_a. \tag{66}$$

The $\Delta B_{La\rm Opt}$ has to be coarse adjusted if the inequality (66) is not satisfied with a good margin. Finally, ΔB_{La} is coarsely

TABLE III
CRITICAL PARAMETERS OF MAGNETIC COMPONENTS

Parameter	Symbol	L_a	T_a	$L_{\rm se}$	T_r
Core type	N/A	RM12	ETD54	EE32	EE65
Core material grade	N/A	N97	3C90	N87	3C95
Saturation flux (25 °C)	$B_{\rm sat}$	0.51T	0.47 T	0.49 T	0.53 T
Relative core losses	$P_{\rm fe}$	3.6 W (100 kHz, 0.2 T)	4.8 W (100 kHz, 0.1 T)	3 W (100 kHz, 0.2T)	49.8 W (100 kHz, 0.2 T)
Core loss coefficient	K_c	$8.8896^{*}10^{-5}$W/Hz$^{\alpha}$ T$^{\beta}$	$1.7967^{*}10^{-6}$W/ Hz$^{\alpha}$ T$^{\beta}$	$7.408^{*}10^{-5}$W/ Hz$^{\alpha}$ T$^{\beta}$	$1.8641^{*}10^{-5}$W/ Hz$^{\alpha}$ T$^{\beta}$
Core loss geometrical coefficient	$K_{\rm fe}$	19 W/ cm^3 T$^{\beta}$	64.7162 W/ cm^3 T$^{\beta}$	21.4552 W/ cm^3 T$^{\beta}$	47.0806 W/ cm^3 T$^{\beta}$
Effective magnetic path length	l_e	5.7 cm	12.7 cm	7.4 cm	14.7 cm
Effective magnetic cross section area	A_e	1.46 cm^2	2.8 cm^2	0.83 cm^2	5.4 cm^2
Effective magnetic volume	V_e	8.32 cm^3	35.5 cm^3	6.14 cm^3	79 cm^3
Core window area	A_w	0.73 cm^2	3.16 cm^2	1.08 cm^2	3.94 cm^2
Mean length turn	MLT	6.1 cm	9.6 cm	6.44 cm	15 cm
Winding fill factor	K_u	0.4	0.4	0.4	0.4
Number of turns	n	10	20:20	10	13:16
Air gap length	l_g	1.7 mm	N/A	0.7616 mm	N/A
Litz wire configuration	N/A	Six AWG22 (40 strands of AWG38 wire) twisted Litz	Three AWG22 (40 strands of AWG38 wire) twisted Litz	Six AWG22 (40 strands of AWG38 wire) twisted Litz	Six AWG22 (40 strands of AWG38 wire) twisted Litz
Litz wire area	W_a	2.0268 mm^2	1.0134 mm^2	2.0268 mm^2	2.0268 mm^2
Winding resistance	R	0.068 Ω	0.196 Ω/0.196 Ω	0.068 Ω	0.208 Ω/0.256 Ω

adjusted to 0.128T, and the number of turns is selected as $N_{La} = 10$.

7) Total auxiliary inductor loss: The core loss of L_a using improved General Steinmetz equation (iGSE) [39] is given by

$$P_{Fe} = K_i|\Delta B_{La}|^{\beta}\left(\frac{2}{T_s}\right)^{\alpha}(D^{1-\alpha} + (1-D)^{1-\alpha}). \quad (67)$$

The coefficient K_i is calculated from

$$K_i = \frac{K_c}{2^{\beta-1}\pi^{\alpha-1}\left(1.1044 + \frac{6.8244}{\alpha+1.354}\right)}.$$

The peak to peak ΔB_{La} is calculated using the following equation:

$$\Delta B_{La} = \frac{2L_a I_{LaP}}{N_{La}A_e}. \quad (68)$$

The winding loss of L_a is given by

$$P_{\rm winding} = \frac{{I_{LaP}}^2 R_{La}}{3}. \quad (69)$$

The maximum auxiliary inductor loss is given by

$$P_{\rm tot} = P_{Fe} + P_{\rm winding} = 2.3\ {\rm W} \le 2.5\ {\rm W}\,(P_{\rm tot\_allowed}). \quad (70)$$

8) Air-gap length: The length of air gap l_g to obtain the required L_a is calculated from

$$l_g = \frac{\mu_o {N_{La}}^2 A_e}{L_a} = 1.7\ {\rm mm}. \quad (71)$$

Therefore, the presented design parameters satisfy the power loss constraint set for the auxiliary inductor. The auxiliary transformer is also devised in the same approach. The series inductor and main transformer are designed based on the constraint that the peak flux density ΔBmax $\le$ 0.25T to regulate the core loss and to avoid the core saturation. The final design parameters and the critical parameters of the selected cores are given in Table III.

TABLE IV
COMPONENT LIST

MOSFET Switches	IXFN64N60P
Rectifier diodes ($D_1 - D_4$)	C4D10120D
Main transformer (T_r)	E65—3C95, n: 1.23, Leakage inductance: 5.06 μH
Auxiliary transformer (T_a)	ETD54—3C90, turns-ratio—1:1
Series inductor ($L_{\rm se}$)	E32—N87, 13.7 μH
Auxiliary inductor ($L_{a\,\rm APWM}/L_{a\,\rm PSM}$)	RM12—N97, 10.7 μH/14.2 μH
Auxiliary capacitors (C_{a1}, C_{a2})	4.7 μF/300 V
Output filter capacitor (C_f)	2.2 μF/630 V
DSP controller	TMS320F28335
Gate driver IC	IXDN609SI
Optocoupler IC	ACPL-4800-300E

VII. EXPERIMENTAL RESULTS

A 1.2-kW converter prototype is developed in the laboratory to verify the theoretical analyses presented so far and validate the performance of the proposed converter and the gating technique. The designed converter specifications are given in Table I. The components used in the development of the converter are listed in Table IV. The developed prototype is shown in Fig. 12(a) and the experimental setup is shown in Fig. 12(b). PSM and the proposed APWM are developed on the TMS320F28335 controller using enhanced pulse width modulators by the up-down counter control method [40].

The ZVS results for S_3 and S_4 are shown in Figs. 13 and 14 at key load points given in Table II. The drain-to-source voltage of the switches attains zero before the respective gating signals are applied. This phenomenon confirms ZVS turn-on of switchesS_3 and S_4. As explained in Section III, the theoretical switch current $i_{\rm SW4}$ waveform shown in Fig. 3 at heavy-load conditions, i.e., $I_{pP} > I_{LaP}/2$ is similar to the measured switch current result shown in Fig. 14(a)–(c). The switch current i_{SW4} waveform shown in Fig. 5 at light-load conditions, i.e., $I_{pP} < I_{LaP}/2$ is also similar to the switch current result shown in

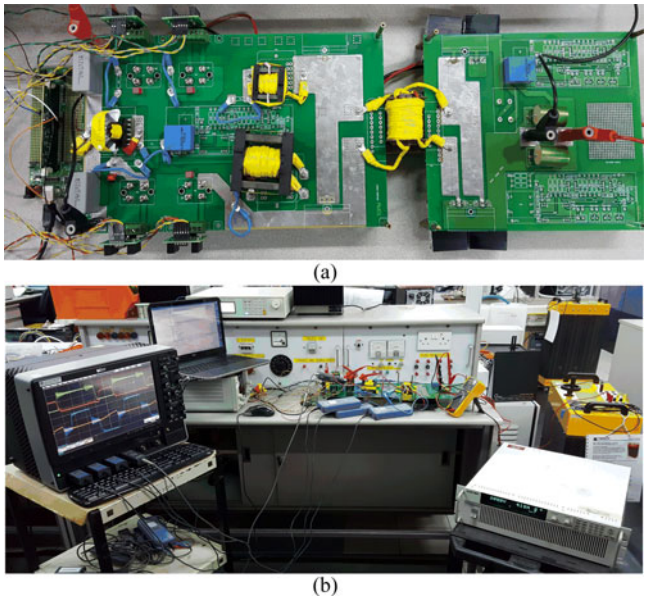

Fig. 12. (a) Proposed APWM ZVZCS converter prototype. (b) Experimental setup of the system.

Fig. 14(d)–(e). Therefore, the experimental results validate the theoretical analyses of the converter operation for heavy-load and light-load conditions.

The experimental results for the voltage across main transformer secondary $v_{\rm sec}$ and output rectifier diode $v_{\rm D1}$ at transition and end load points are shown in Fig. 15. It is clearly evident from Fig. 15 that the high-voltage spikes on rectifier diodes are mitigated in the proposed converter.

The auxiliary inductor voltage v_{La} and current i_{La} results of the converter with the proposed APWM and PSM techniques at transition and end load points are shown in Figs. 16 and 17, respectively. The experimental results for the peak values of i_{La} at different load conditions with APWM and PSM are compared in Fig. 18. It can be observed from Fig. 18 that the peak value of i_{La} with APWM is significantly lesser than PSM especially at light-load conditions.

The measured switches current during the ZVS transition with APWM and PSM at different load points are compared in Fig. 19. It can be observed from this figure that the peak value of ZVS current with APWM is significantly lesser than PSM, especially at light-load conditions.

Fig. 20 shows the efficiency of the converter over the battery charging profile under the following scenarios:

1) APWM converter without auxiliary circuit (conventional converter);
2) PSM converter with auxiliary circuit, $L_a = L_{a\rm PSM} = 14.2\ \mu$H;
3) APWM converter with auxiliary circuit, $L_a = L_{a\rm APWM} = 10.7\ \mu$H.

From Fig. 20, it is evident that the proposed converter topology with the proposed APWM achieves superior efficiency when compared to the PSM and conventional converters. According to Fig. 20(b), the APWM converter efficiency is higher

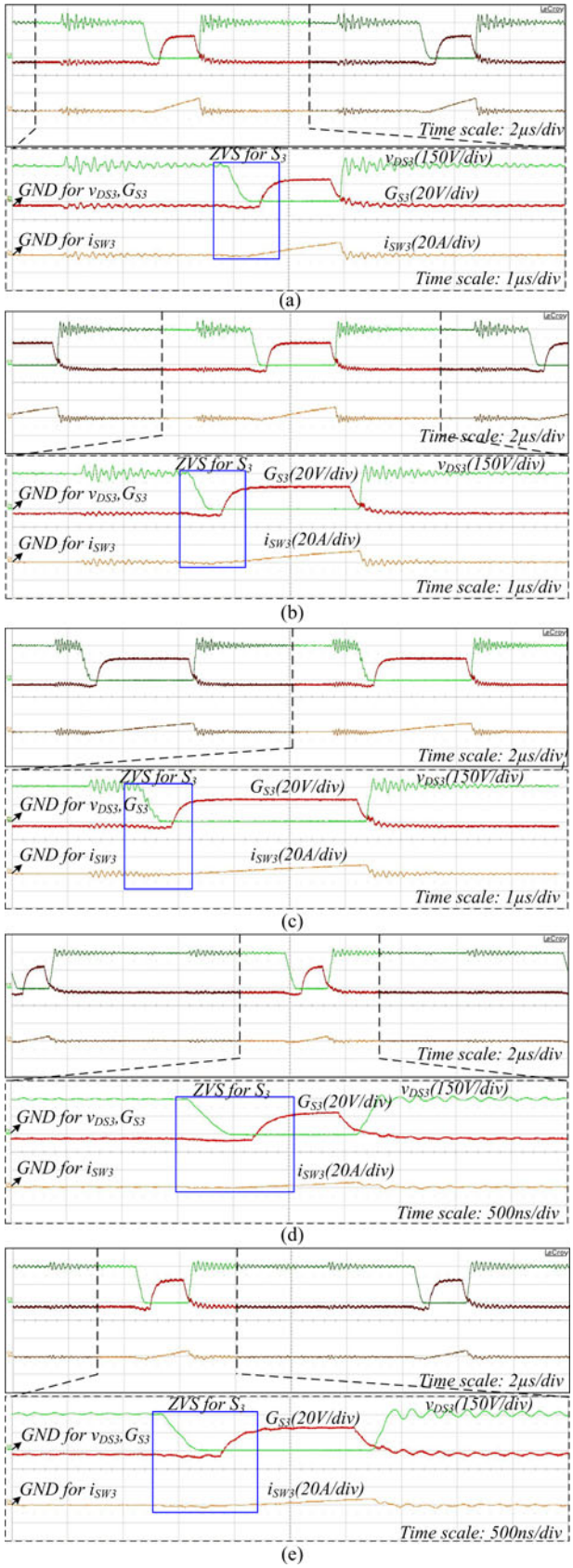

Fig. 13. ZVS waveforms for high-side switch S_3. (a) At start point. (b) At nominal point. (c) At transition point. (d) At end point. (e) At recharge point.

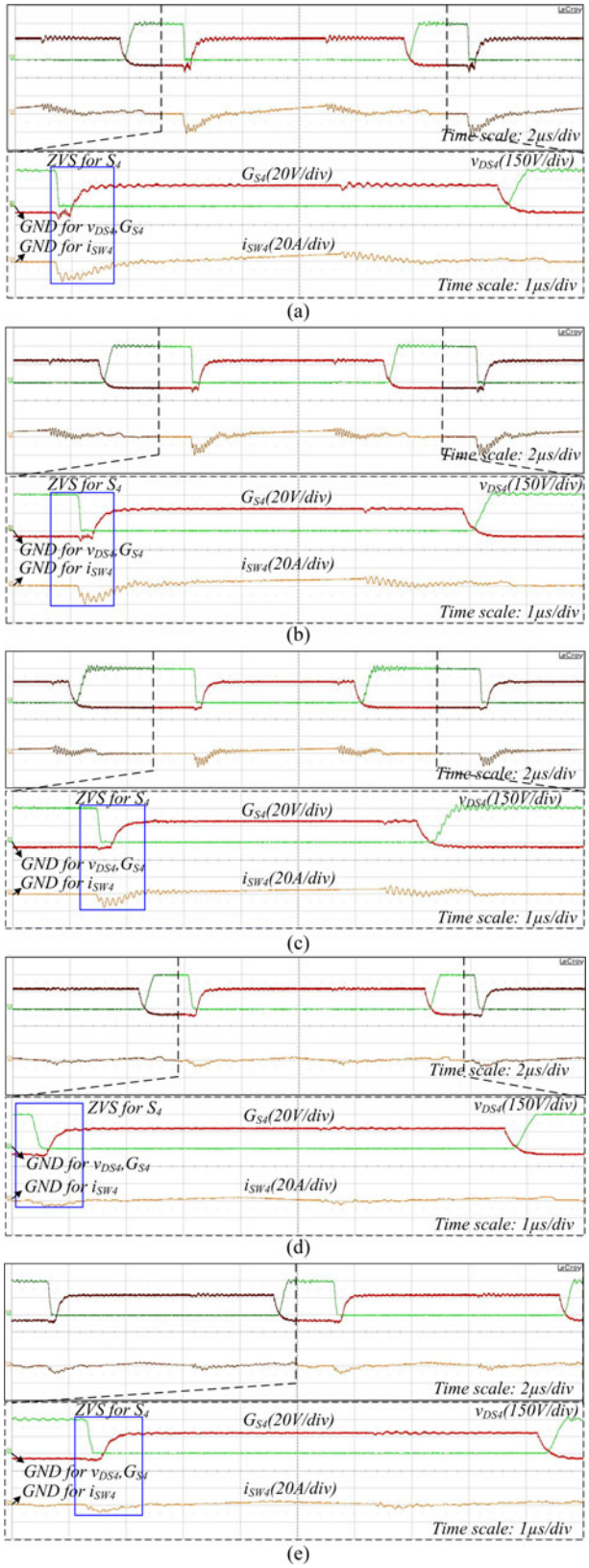

Fig. 14. ZVS waveforms for low-side switch S_4. (a) At start point. (b) At nominal point. (c) At transition point. (d) At end point. (e) At recharge point.

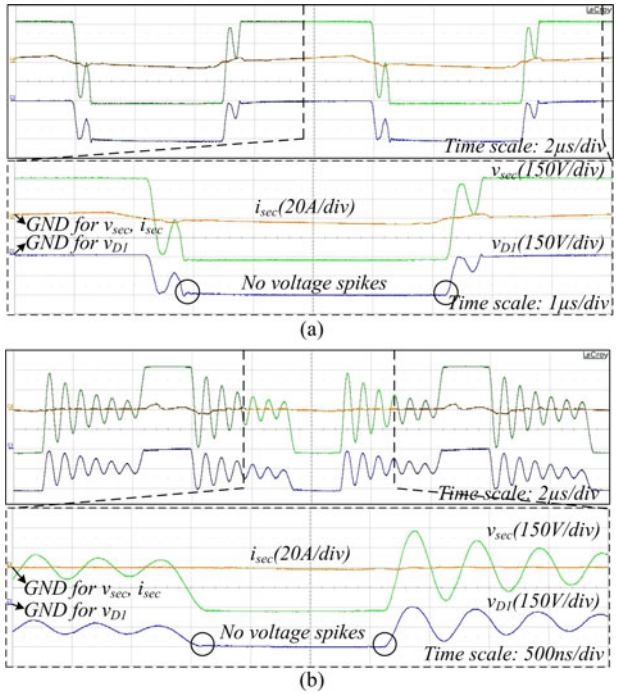

Fig. 15. T_r secondary operating waveforms. (a) At transition point. (b) At end point.

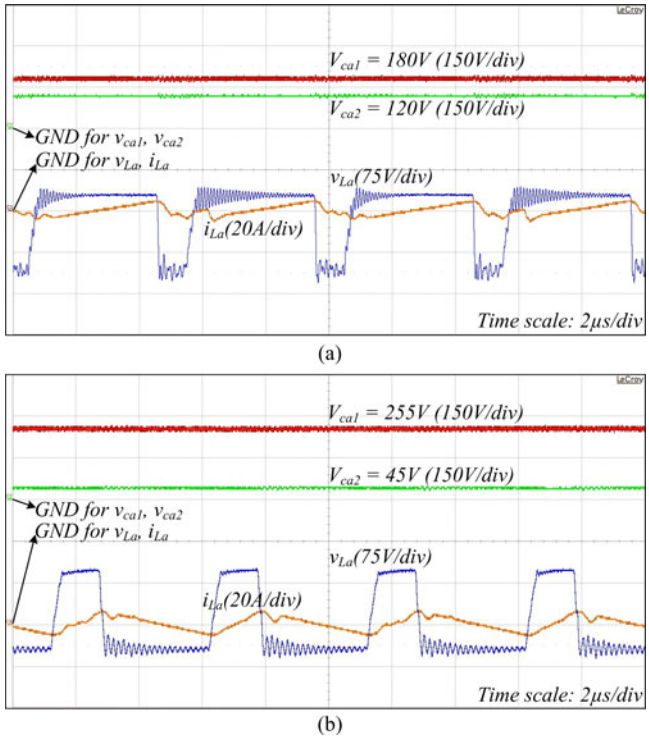

Fig. 16. Auxiliary circuit waveforms with APWM. (a) At transition point. (b) At end point.

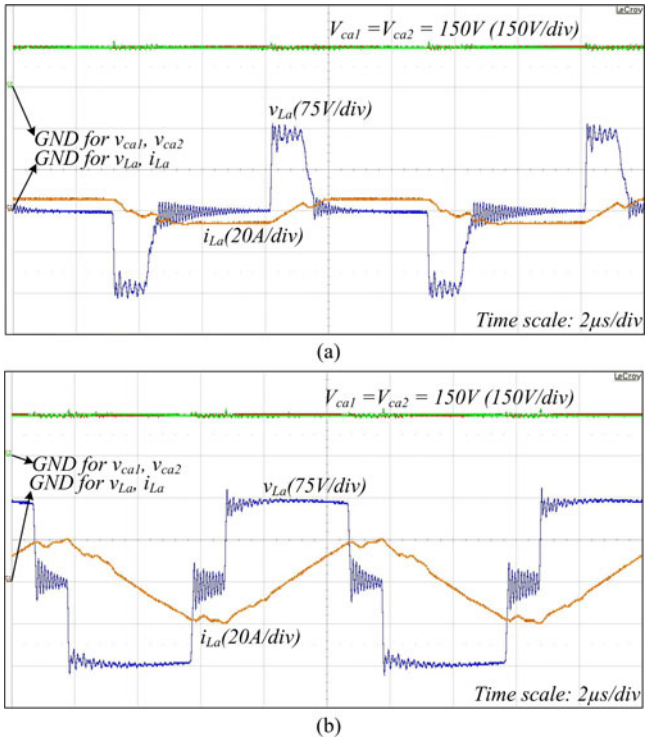

Fig. 17. Auxiliary circuit waveforms with PSM. (a) At transition point. (b) At end point.

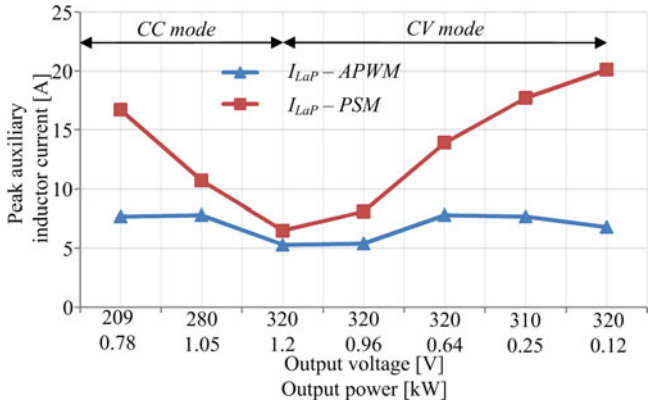

Fig. 18. Comparison of peak auxiliary inductor current with APWM and PSM over battery charging profile.

especially at light-load conditions due to the reduced switching and conduction losses of main switches, auxiliary circuit losses, low circulating current, and elimination of reverse-recovery losses of output rectifier diodes.

Table V shows the comparison between the proposed APWM ZVZCS converter and the other converters [15], [30], [31]. The other converter systems are the half-bridge integrated full-bridge converter in [15], two symmetric auxiliary poles assisted PSM converter in [30], trailing-edge PWM converter in [31], and the proposed PSM converter. The converters [15] and [30] have more number of components compared to the proposed converter. The converter in [15] requires additional snubber circuit to mitigate the voltage spikes across the output rectifier diodes

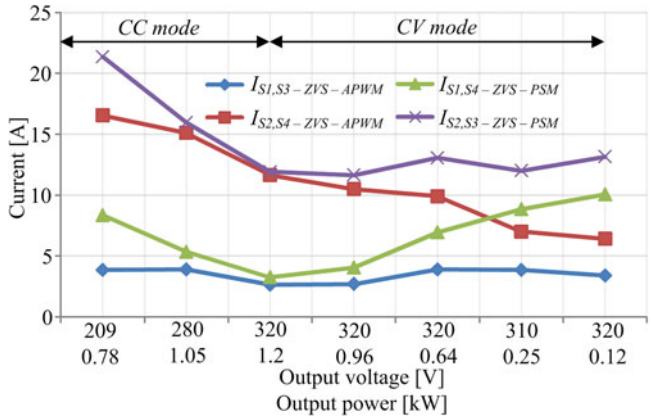

Fig. 19. Comparison of ZVS switches current with APWM and PSM over battery charging profile.

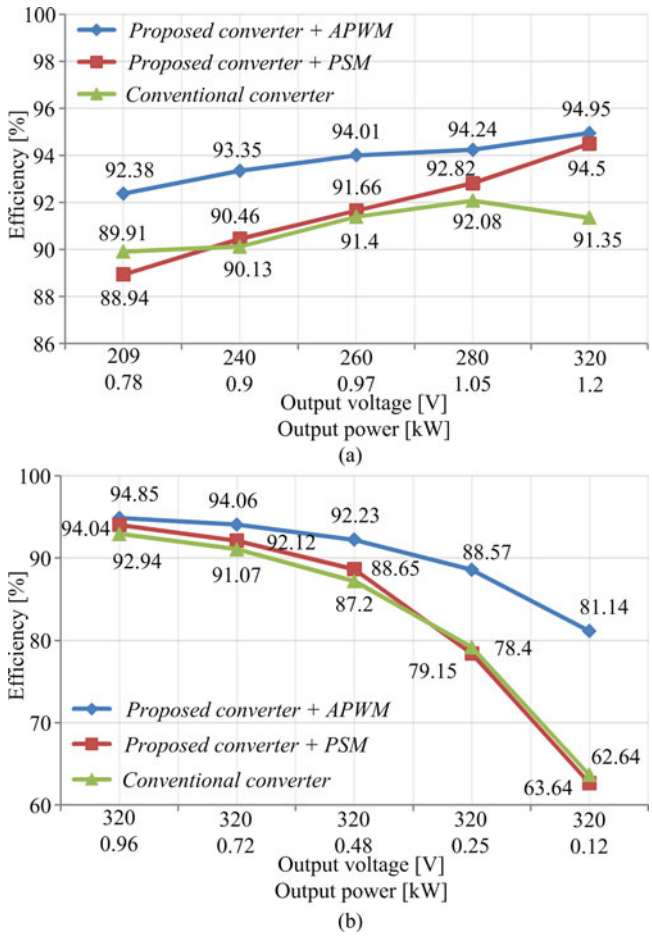

Fig. 20. Efficiency of the converters over battery charging profile. (a) CC charging mode. (b) CV charging mode.

compared to proposed APWM ZVZCS converter. The converter in [31] can only achieve ZVS for two switches whereas the proposed APWM converter achieves ZVS for all (four) switches. In the case of ac inductor design, the volt–second product is the key design parameter to determine the physical size of the inductor core [38]. According to Table V, it can be observed that the auxiliary inductor size (volt-second) required for ZVS

TABLE V
COMPARISON OF FULL-BRIDGE DC–DC CONVERTERS

Converter topology	Topology in [15]	Topology in [30]	Topology in [31]	Proposed topology	
Modulation method	PSM	PSM	Trailing-edge PWM	PSM	APWM
Number of auxiliary components	2	6	Not applicable	4	4
Total number of components	16	17	11	15	15
Auxiliary inductor size (volt–second)	$\frac{V_{\text{in}}}{8}\frac{D}{f_s}$	$\frac{V_{\text{in}}}{8}\frac{1}{f_s}$	Not applicable	$\frac{V_{\text{in}}}{8}\frac{(1-D_{\max})}{f_s}$	$\frac{V_{\text{in}}}{8}\frac{D_{\max}(1-D_{\max})}{f_s}$
Auxiliary circuit peak current rating	$\frac{V_{\text{in}}D}{8L_{\text{maux}}f_s}$	$\frac{V_{\text{in}}}{8L_a f_s}$	Not applicable	$\frac{V_{\text{in}}(1-D)}{8L_a f_s}$	$\frac{V_{\text{in}}D(1-D)}{8L_a f_s}$
ZVS	All switches $(S_1 - S_4)$	All switches $(S_1 - S_4)$	Two switches $(S_2,\ S_4)$	All switches $(S_1 - S_4)$	All switches $(S_1 - S_4)$
ZCS	Not applicable	Two switches $(S_1,\ S_4)$ –near ZCS	Two switches $(S_2,\ S_4)$	Two switches $(S_1,\ S_4)$ – near ZCS at fullload	Two switches $(S_2,\ S_4)$ – near ZCS
Additional snubber circuit	Required	Not required	Not required	Not required	Not required
Voltage spikes across output rectifier diodes	Minimized	Mitigated	Mitigated	Mitigated	Mitigated

in [15] and [30] is larger compared to the proposed APWM ZVZCS converter. The proposed PSM converter auxiliary inductor size is also greater than the proposed APWM ZVZCS converter.

VIII. CONCLUSION

In this paper, a ZVZCS full-bridge dc–dc converter and a new APWM gating technique have been proposed for battery charging applications in EVs. Theoretical operation of the converter for achieving the ZVS turn-on of the main switches has been discussed. The circuit parameters design and magnetics design have been presented. The results have verified the capability of the proposed converter to achieve ZVS condition over the entire battery charging range. The proposed converter showed significant reductions in switching losses, auxiliary circuit losses, and required auxiliary inductance. The high voltage spikes on output rectifier diodes have been mitigated. The features have been validated by the experimental results from the laboratory-scale 1.2-kW converter prototype. The efficiency results have proved the improved performance of the proposed APWM converter over the proposed PSM converter and the conventional ZVZCS converter.

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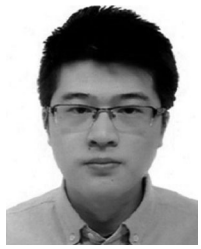

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