A Modular Multilevel DC–DC Converter Topology With a Wide Range of Output Voltage

Qiang Ren, Chi Sun, and Fei Xiao

***Abstract*—To solve some problems caused by the ac control method used for the existing modular multilevel dc–dc converter (MMDC), this paper has proposed a new MMDC topology with a wide range of output voltage by means of dc control. By reconstructing the submodule structure, the converter has a power branch and an auxiliary balance branch, which are used to transmit dc power and balance the capacitor voltage, respectively. Both dc analysis and control method are adopted to establish a mathematical model so as to deduce the mathematical relationships between the key electrical parameters. Moreover, what have been done include analyzing the self-balancing principle of the capacitor voltage and the mechanism of the auxiliary balance branch, calculating the related parameters of the capacitor voltage fluctuation, and presenting a dc closed-loop control strategy based on a small-signal model. The analyses of the steady and dynamic states in combination with simulation and experiment show that the proposed converter can stably operate in the mode of dc control, with a large adjustable range of output voltage, a small fluctuation in voltage of the capacitor, and the ability of the inductor to suppress the spike of the auxiliary balance current effectively so as to reduce the impact on the device.**

***Index Terms*—Capacitor voltage self-balancing, dc control method, dc–dc converter, modular multilevel converter (MMC), power electronics.**

I. Introduction

With the expanded application of the concept of energy Internet, the planning and construction of a smart microgrid integrated with new renewable energy sources is of great importance to energy storage, resource sharing, and the construction of a multiport distributed open power system [1]–[3]. Especially, the smart microgrid based on the dc transmission and distribution technology has advantages over the traditional grid based on the ac transmission and distribution technology in regard to reactive power, transmission loss, and stable operation. Its practical value lies in being able to improve the reliability of power supply, absorb renewable energy fully, and meet the needs for new-type dc power-supply loads [4]–[6].

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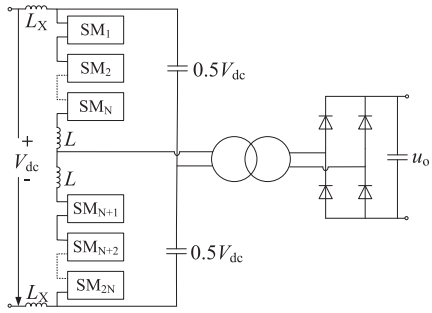

Fig. 1. Topology of isolated two-level unidirectional dc converter.

As the medium-high-voltage dc power conversion is limited by the low-voltage level and power capacity of a single power switching device, the main solutions to the problem are the series–parallel connection of power switching devices, the series–parallel combination of modules, and the multilevel conversion technique. However, as far as the structure of conventional series–parallel devices is concerned, it is difficult to control the sharing of voltage and current in a dynamic or static state of the devices. For the multimodule series–parallel converter, it is difficult to control the sharing of voltage on the series side and the sharing of the current on the parallel side. Besides, the number of devices increases sharply but the extendibility decreases when the conventional clamped multilevel converter varies with an increase in level. As the cascaded H-bridge multilevel converter needs multiple independent power supplies, it is very difficult to design a high-capacity multiwinding complex transformer as required. For those reasons, the use of the conventional structures for energy conversion is not an optimal option in the aspects of high-voltage, high-power density, modular design, high reliability, and maintainability.

Since the modular multilevel converter (MMC) came into being, it has become popular in the academic field for its being of advantages to high-voltage application, high-level modular design, and ideal multilevel output, so it is considered to be one of the main trends toward the high-capacity power conversion technology [7]–[9]. Recently, MMC has mainly used for high-voltage dc transmission and high-power electric drive. With an increasing demand for the medium-high-voltage dc converter in view of dc transmission and distribution, the solution to a dc–dc converter based on the modular multilevel structure has become a hot topic.

In [10] and [11], the topology of an isolated dc–dc converter with MMC—transformer–rectifier was proposed, as shown in

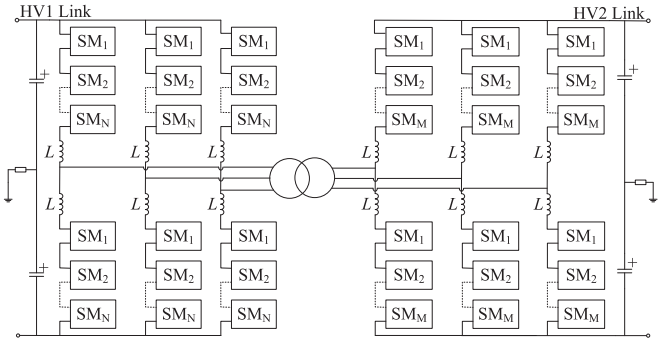

Fig. 2. Topology of isolated two-stage bidirectional dc–ac–dc converter.

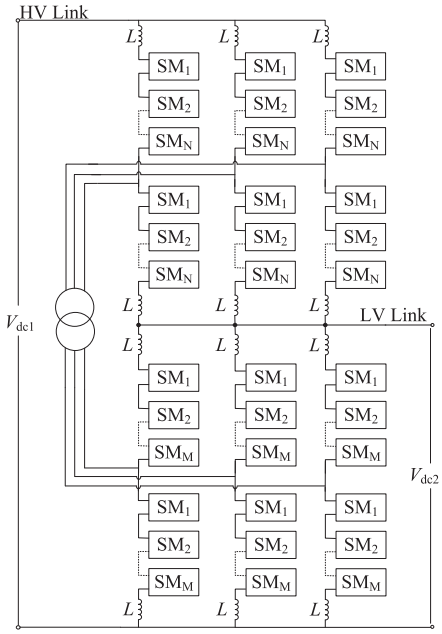

Fig. 3. DC autotransformer topology.

Fig. 1. It uses a two-level ac square wave as an intermediate coupling variable to make the power flow unidirectional. Its structure is compact and easy for analysis and control. However, the advantage of multilevel output of MMC has not been brought into play, and the high dv/dt of the square wave increases the insulation of the transformer windings.

An isolated bidirectional dc–ac–dc converter used for interconnecting the dc grids was analyzed in [12]–[16], as shown in Fig. 2. Using the coupling transformer, it is possible for the medium-high-frequency ac link to isolate the input and output MMC subconverters, and meanwhile, the capacity and volume of the passive devices and the design cost can be reduced, but in this two-stage conversion structure, the dc power to be transmitted needs to go through dc/ac conversion twice, which will increase the power conversion loss. As only half of the switching devices are in operation, the utilization of the devices is low.

To solve the problem of high loss of the two-stage conversion structure, Schon *et al.* [17]–[20] proposed a dc autotransformer, as shown in Fig. 3. Not only is the dc power transmitted through the ac link but also through the dc path so as to reduce both the capacity and conversion loss of the ac link. While performing

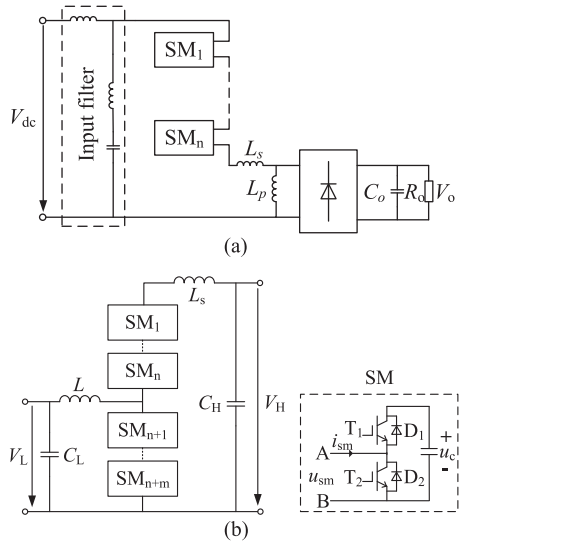

Fig. 4. Resonant dc–dc converter topologies. (a) Resonant converter topology 1. (b) Resonant converter topology 2.

power transmission, the ac link can redistribute the energy between the arms and balance the submodule capacitor voltages, but in this converter, there is a coupling relationship between the subconverters, leading to the complexity of control and a small range of output voltage.

A resonant dc–dc converter analyzed in [21] and [22] generates the resonance by use of the leg inductor and the inserted submodule capacitors and rectifies the dc voltage, as shown in Fig. 4(a). The submodule is equivalent to the switching device of the conventional buck/boost converter in [23] and [24], as shown in Fig. 4(b). It can achieve the capacitor voltage balance and control the output voltage by using the resonance of the output-side inductor and the inserted capacitors, but the resonance will cause an increase in the reactive power of the converter, a large loss of the device, and a big fluctuation in the output voltage.

According to the principle of Fourier series, nonsinusoidal voltage and current can be expressed as the sum of sinusoidal components at different frequencies. The mean value of the power component obtained from the product of voltage and current at different frequencies is zero. In other words, the power components with different frequencies are orthogonal. Power can be delivered at one frequency and absorbed at another, and the energy of the power conversion unit can be kept balanced [25] and [26]. Therefore, a control concept is proposed, which refers to a primary power loop and a secondary balance loop for the conventional MMC, as shown in Fig. 5. The primary power loop is used for power transmission, and the secondary balance loop is used for voltage balance of the submodules. However, the artificial injection of ac circulation increases the reactive power, the current stress of the devices becomes high, and obvious fluctuations appear in the capacitor voltages and output voltage.

As seen by the main topologies and control methods of the MMDC, the unidirectional current in dc power conversion results in a unidirectional change in the capacitor voltage of the submodule. For this reason, an ac control method is adopted to redistribute the energy between the arms and balance the capaci-

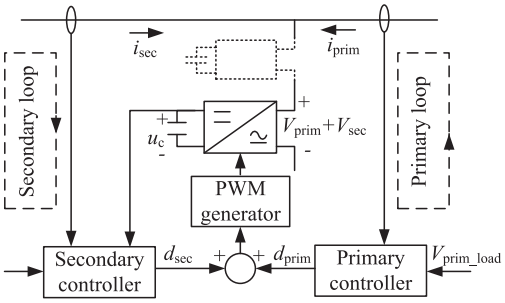

Fig. 5. Primary/secondary loop control diagram.

tor voltages. However, the method also leads to greater difficulty in analysis and control, larger reactive power, higher current stress of the switching device, and lower conversion efficiency. In order to overcome the aforementioned problems, this paper has presented a new MMDC topology based on the concept of dc control—the topology with a wide range of output voltage [30]. After the submodule is reconstructed, the converter will have both a power branch and an auxiliary balance branch. The power branch can perform the dc power transmission and help the auxiliary balance branch achieve the self-balancing of the capacitor voltages. The basic working principle and control become simple by use of the classical dc analysis and control method. Compared with the currently accepted topologies and ac control methods, the proposed converter topology and its dc control method are characterized by innovation to a certain extent.

For the proposed converter, this paper consists of the following sections. Section II analyzes the basic principles of the new MMDC. Section III proposes a closed-loop control strategy based on the model analysis. Section IV verifies the basic principles by simulations and experiments. The results show the proposed converter is useful and effective.

II. Basic Principles of the New MMDC

A. Topology of the New MMDC

As shown in Fig. 6, the MMDC proposed in this paper includes the cascading structure, which consists of an upper arm and a lower arm with N submodules. As for every submodule, its capacitance is C and its rated voltage is u_c. The submodule is a four-terminal heterogeneous full-bridge structure composed of a power half-bridge and an auxiliary balance half-bridge. Both of them share the storage capacitor. Unlike the conventional two-terminal half-bridge or full-bridge submodule, the proposed four-terminal submodule contains two capacitor charge–discharge paths. The charge–discharge current can form a loop through the power half-bridges, that is called power branch, or a loop through the auxiliary balance half-bridges, that is called the auxiliary balance branch. The power branch of the upper and lower arms is connected in series through the inductors, which are used to filter out the high-frequency ripples from the voltage, buffer the unbalance between the leg voltage and the dc voltage, and limit the rising rate of the dc short-circuit current in order for the converter to have time for self-protection. The series inductors of auxiliary balance branch are used to suppress

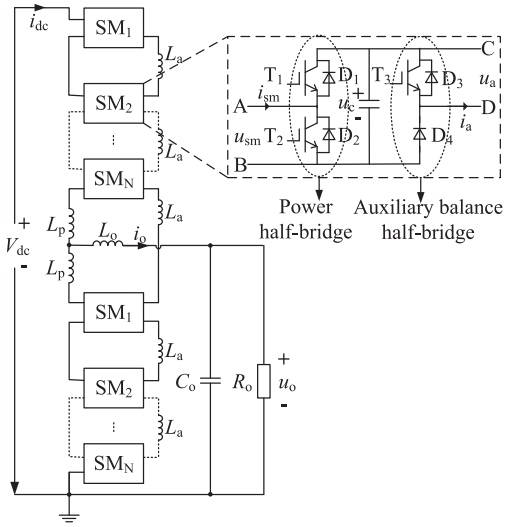

Fig. 6. Proposed topology of MMDC.

the surge currents generated in the power transmission between the submodules and prevent large surge currents from damaging the switching devices.

Each submodule can output two kinds of voltage u_c and 0 by controlling its power half-bridge switches to insert or bypass the capacitor. The converter can output different voltages through different combinations of inserted submodules of the power branch. However, the unidirectional branch current at the time of the dc power conversion causes a unidirectional change in the capacitor voltages. In order to maintain the balance of capacitor voltages, the balance power transformation can be fulfilled through the parallel connection of adjacent submodule capacitors in the upper and lower arms and between the arms, for the purpose of compensating for the voltage unbalance caused by dc power transmission. On this basis, the adoption of the conventional dc analysis and control method can make it possible to stabilize the output voltage, which is only related to the states of the power half-bridges.

For the same voltage level and power level of a single-phase N-level bidirectional MMDC, the key electrical parameters of the proposed converter, the conventional nonisolated MMDC in [25] and [26], and the isolated MMDC in [12]–[16] are compared, as shown in Table I. The conversion ratio is the ratio of output voltage to dc voltage. The sign d denotes the duty ratio of the switches, i_{rat} is the rated arm current with the converter being under rated power, n is the transformer turn ratio, and p_{semi} is the expenditure of the semiconductors.

As can be seen from Table I, the semiconductor devices of the isolated MMDC and the proposed MMDC are almost twice those of the conventional nonisolated MMDC, while the current stress of the devices decreases almost one half. As pointed in [26], the expenditure of the semiconductors is one of the main factors to measure the cost and loss of a converter and the semiconductor expenditure is proportional to the device current. So the expenditures of the semiconductors of the three converters are almost equal. In addition, the proposed converter needs $n-1$ balance branch inductors to suppress the surge currents

TABLE I
COMPARISON OF ELECTRICAL PARAMETERS OF THE THREE CONVERTERS

Electrical parameters	Nonisolated MMDC	Isolated MMDC	Proposed MMDC
Number of IGBTs	$4N$	$8N+4$	$6N$
Number of diodes	$4N$	$8N+4$	$8N$
Number of capacitors	$2N$	$4N$	$2N$
Current stress of IGBT	$\approx 2i_{\text{rat}}$	$\approx i_{\text{rat}}$	$\approx i_{\text{rat}}$
Voltage stress of IGBT	$\approx(1+10\%)u_c$	$\approx(1+5\%)u_c$	$\approx(1+5\%)u_c$
Fluctuation of capacitor voltage	$\approx 10\% u_c$	$\approx 5\% u_c$	$\approx 5\% u_c$
Having circulation or not	Yes	Yes	No
Having transformer	No	Yes	No
Number of inductors	3	4	$N+2$
Conversion ratio range	$[d, 1-d]$	$[nd/2,\ n(1-d)/2]$	$[d/N,\ 1-d/N]$
Expenditure of semiconductors	$\approx p_{\text{semi}}$	$\approx p_{\text{semi}}$	$\approx p_{\text{semi}}$

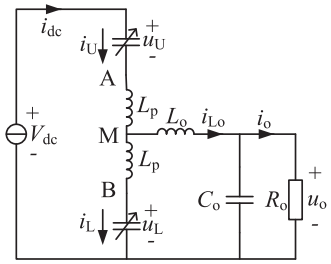

Fig. 7. Mathematical model of the proposed MMDC.

when the capacitors are in parallel. The inductance is microhenry level, which can almost be reached by use of the stray inductance. Therefore, an increase in the number of inductors does not lead to extra cost.

In the proposed converter, one half of switching devices are used to form an auxiliary balance branch so as to separate the balance current from the dc power current and simplify the system analysis. Compared with the conventional nonisolated and isolated converters which use ac control method, the proposed converter can effectively reduce the reactive power and loss by use of the dc control method, with small ripples in the submodule capacitor voltages and output voltage. Using the structure of paralleling the output stage with the lower arm, it is possible to achieve a wide range of output voltage through a change in the number of insertion submodules in the arm.

B. Analysis of a Mathematical Model

Suppose the devices of the converter are ideal and the capacitor voltage of each submodule is kept balanced through the self-balancing mechanism. The upper and lower arms are equivalent to controllable voltage sources. The mathematical model is shown in Fig. 7.

According to the Kirchhoff voltage law, it can be expressed as

$$V_{\text{dc}} = u_U + u_L + L_p \frac{di_U}{dt} + L_p \frac{di_L}{dt} \tag{1}$$

$$u_o = u_L + L_p \frac{di_L}{dt} - L_o \frac{di_{\text{Lo}}}{dt}. \tag{2}$$

According to the volt–second balance of the inductor, voltage drops on power branch inductors and output filter inductor are neglected in a steady state. For a MMDC with N levels, the submodule insertion coefficients of the upper and lower arms are, respectively, n_U and n_L, and the conversion ratio is k, then

$$u_o = u_L = kV_{\text{dc}} = V_{\text{dc}} n_L / N. \tag{3}$$

From (3), it can be seen that the output voltage is equal to the sum of the inserted capacitor voltages of the lower arm. The output voltage can be regulated by adjusting the insertion coefficient of the lower arm.

With the switching period as an interval, the submodules can be inserted or bypassed in turn by a round-robin modulation method. In (3), when n_L is an integer, the number of the inserted submodules of the lower and upper arms are n_L and $N - n_L$, respectively, and the involved submodules are switched on during the whole period. When n_L is a decimal, there will be a change in the number of the inserted submodules. In the lower arm, there are $[n_L]$ submodules switched on during the whole period, except only one operating with a duty ratio of d. Accordingly, there are $N - n_L - 1$ submodules switched on during the whole period, and there is only one operating with a duty ratio of $1 - d$ of the upper arm. $[n_L]$ represents the integral part of n_L. The duty ratio d equals

$$d = n_L - [n_L]. \tag{4}$$

Thus, the following can be obtained:

$$u_o = (d + [n_L])u_c = V_{\text{dc}}(d + [n_L])/N. \tag{5}$$

According to (5), the output voltage of the new MMDC is a square wave with bias voltage of $[n_L]u_c$, and the step voltage is u_c. Its output voltage has smaller amplitude in step and harmonics compared with the two-level square-wave output voltage from the traditional buck converter. The output voltage waveforms of the two types of converters are shown in Fig. 8.

When $[n_L]$ is zero, the output voltage is

$$u_o = V_{\text{dc}}\, d/N. \tag{6}$$

Under the condition of the same switching duty ratio, the effective conversion ratio of the new MMDC is N times smaller than that of $u_o = dV_{\text{dc}}$ in the buck converter. Thus, the new converter can achieve a wider range of voltage regulation, with the loss of switches, the capacity of inductors, and the limitation of duty ratio taken into consideration.

Meanwhile, according to the Kirchhoff current law, the current formula of steady state is derived as follows:

$$i_U - i_L = i_o. \tag{7}$$

Then, the power relationship between the upper and lower arms can be deduced from the conservation law of input and

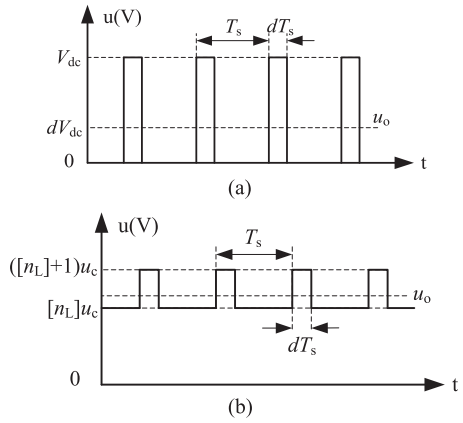

Fig. 8. Output voltage waveforms of the conventional buck converter and the new converter. (a) Two-level square waveform of the buck converter. (b) Square waveform with dc bias of the new converter.

output power $V_{\rm dc} i_U = u_o i_o$

$$u_U i_U = -u_L i_L. \tag{8}$$

Equation (8) indicates that the input power of the upper arm is equal to the output power of the lower arm at any time and that the powers of the arms are complementary to each other. Part of the load power is provided by the dc power supply directly through the upper arm and the other part is provided by the submodule capacitors of the lower arm. The lost power of the lower arm is compensated by the balance power transferred from the upper arm that is, fulfilled by the self-balancing of the capacitors. The orderly insertion or bypass of the submodules of the auxiliary balance branch provides the paths for local balance power transformation, thereby ensuring the balance of the capacitor voltages. According to the law of conservation of energy, the analysis of the equivalent model is proved to be correct.

According to the input and output power conservation, the relational expression can be obtained through power P_b transferred from the balance branch and powers P_U and P_L of the upper and lower arms

$$P_b = P_U = -P_L = (1-k)P_{\rm load}. \tag{9}$$

Under the condition of invariable conversion ratio, the powers of the upper and lower arms increase with the load power. The increased balance power will lead to a bigger fluctuation of submdule capacitor voltage and a larger balance branch current. Under the condition of invariable output power, the powers of both the arms and the balance power decrease as the conversion ratio increases. The capacitor voltage fluctuation and the balance branch current are also reduced accordingly. The ratio of the power component provided by the lower arm to the load is gradually reduced, while the ratio of the power provided to the load by dc power through the upper arm is gradually increased.

C. Self-Balancing Principle of Submodule Capacitor Voltage

The basic requirement of the MMC is to maintain the balance of submodule capacitor voltage. The new MMDC adopts a heterogeneous full-bridge structure, which is composed of a power branch and an auxiliary balance branch. The power branch is used to provide instruction for output voltage and to transfer dc power. The auxiliary balance branch is used to form current loops for power transfer and voltage balance between the submodules. The control of both the branches leads to the charging and discharging of the capacitors. Thus, the converter can perform the power conversion while maintaining the self-balancing of the capacitor voltages. Because of sharing the same storage capacitor, there is a coupling relationship between the two half-bridges of the submodule. When power conversion is carried out by controlling the power half-bridge switches, the corresponding auxiliary balance half-bridge switching states are restricted. With the submodules $n-1$ and n of the upper arm as objects of analysis, the self-balancing principle of capacitor voltages and the inherent relationships between the switching states are analyzed.

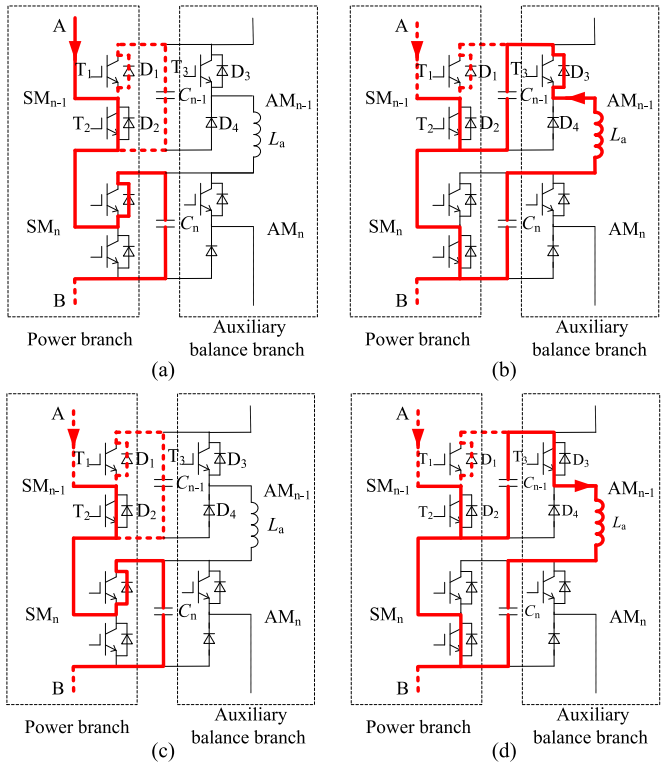

Fig. 9. Diagrams of switching states of power branch and auxiliary balance branch. (a) Switching state 11 or 01 when $u_{n-1} < u_n$. (b) Switching state 10 or 00 when $u_{n-1} < u_n$. (c) Switching state 11 or 01 when $u_{n-1} > u_n$. (d) Switching state 10 or 00 when $u_{n-1} > u_n$.

Suppose State 1 represents the upper insulated gate bipolar transistor (IGBT) is switched on and the lower IGBT is switched off in a half-bridge, and State 0 represents the complementary states of IGBTs. In order to keep the submodules working normally without being short-circuited, when the switching states of the power branch of two adjacent submodules are, respectively, 11, 10, 01, and 00, those of the corresponding power branch and auxiliary balance branch states should be such as shown in Fig. 9.

TABLE II
RELATIONSHIPS BETWEEN SUBMODULE SWITCHING STATES

SM_{n-1} switch state	SM_n switch state	AM_{n-1} switch state	Relationship of two capacitors
1	1	0	Series
1	0	1	Parallel
0	1	0	Separation
0	0	1	Parallel

Because of the small line resistance, in order to prevent the capacitor of submodule $n-1$ from being short-circuited, its auxiliary balance switching state must be $\mathrm{AM}_{n-1}=0$ when the submodule n is inserted or $\mathrm{SM}_n=1$. The half-bridge diode D_4 has a reverse cut-out after the inductor current is zero. The two capacitors are in series or in a discrete state, without any power exchange between them, as shown in Fig. 9(a) and (c). When submodule n is bypassed or $\mathrm{SM}_n=0$, the state of submodule $n-1$ is expressed as $\mathrm{AM}_{n-1}=1$ and the two adjacent capacitors are connected in parallel. According to the capacitor voltages $u_{n-1}<u_n$ or $u_{n-1}>u_n$, the auxiliary balance branch current flows through the antiparallel diode D_3 or the switch T_3 to transfer power between the two capacitors, as shown in Fig. 9(b) and (d). Then, the current is reduced to zero after the two capacitor voltages are equal. Because of a voltage drop in the inductor L_a, the power current does not flow through the auxiliary balance branch after the capacitor voltages are equal. Thus, the balance current flows through the auxiliary branch only, decreasing power capacity and loss of the branch.

Similarly, the self-balance of the capacitor voltages of the lower arm and the relationship between its switching states can be achieved. Moreover, the self-balancing mechanism can be introduced into a converter with multiple submodules.

For different switching states of power branch, the corresponding auxiliary balance branch states are shown in Table II.

As known from the above analysis, to balance the capacitor voltages and transmit power between the submodules in different switching states of the power branch, the auxiliary balance switching state of submodule $n-1$ is complementary to the power switching state of submodule n

$$\mathrm{AM}_{n-1}=!\mathrm{SM}_n. \tag{10}$$

Thus, the pulse signal of the auxiliary balance switch of submodule $n-1$ can be obtained by inverting the pulse signal of the power branch switch of submodule n. The balance of capacitor voltage is an independent behavior and there is no need for a special balance controller as the conventional MMDC does for the capacitor voltage balance. The optimal control of the converter is focused on the control of the power half-bridges, and each submodule has the ability of self-balancing its capacitor voltage.

Meanwhile, the parallel equivalent circuit of the adjacent submodule capacitors can be drawn according to the proposed topology, as shown in Fig. 10.

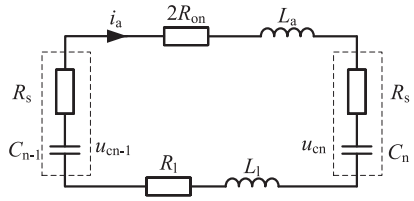

Fig. 10. Diagram of parallel equivalent circuit of submodular capacitors.

In Fig. 10, R_l, L_l, R_s, R_{on}, and L_a are the line resistance, line inductance, capacitor equivalent series resistance, IGBT conduction resistance, and series inductance of the auxiliary balance branch, respectively. The parallel equivalent circuit is a second-order circuit considering R_l, L_l, and R_s are small enough to be ignored. In order to reduce the surge current and the device capacity of the auxiliary balance branch, the series inductance should be as large as possible. However, a larger inductance will, to a certain extent, hinder the power transmission, thus causing a larger fluctuation in capacitor voltage and in turn increasing the surge current. Therefore, it is necessary to make a compromise in choosing a series inductor according to the magnitude of surge current and the fluctuation of capacitor voltage so that the capacitor voltage is kept within the rated range when the switching device is subjected to a certain impact current.

In order to prevent the second-order circuit from resonance, the inductor should simultaneously meet the condition for the equivalent circuit to form a critically damped system or an overdamped system. Suppose the chosen inductor satisfies the equivalent circuit as a second-order overdamped system and the initial voltage difference between the two parallel capacitors is Δu. According to the principle of the second-order circuit, it is possible to obtain the range of inductance, the maximum surge current $i_{\max}$, and the power transfer time Δt needed by the voltage difference which is within $\xi\Delta u$

$$L_a \le \frac{CR_{\mathrm{on}}^2}{2} \tag{11}$$

$$i_{\max}=\frac{C\Delta u x_1 x_2}{2(x_1-x_2)}\left[\left(\frac{x_2}{x_1}\right)^{\frac{x_2}{x_1-x_2}}-\left(\frac{x_2}{x_1}\right)^{\frac{x_1}{x_1-x_2}}\right] \tag{12}$$

$$\Delta t=\frac{1}{x_1-x_2}\ln\frac{x_1}{\xi x_2} \tag{13}$$

where x_1 and x_2 are the two solutions to the characteristic equation of the second-order circuit, respectively. ξ is the voltage balance coefficient. According to the input and output specifications, the switching loss of the auxiliary balance branch can be estimated, and the selection of devices and the design of heat dissipation also can be made.

In addition, according to the voltage conservation and charge conservation of the submodule capacitor, the variable quantity of charges under the action of the power branch current is equal to that under the action of the balance branch current in steady-state conditions; that is, the periodical average current i_p is equal to i_{pb} in Fig. 11

$$\langle i_p\rangle_{T_s}=\langle i_{\mathrm{pb}}\rangle_{T_s}. \tag{14}$$

Therefore, the periodical average current of the power half-bridge switching devices is identical with that of the auxiliary balance half-bridge switching devices. Unlike the switching

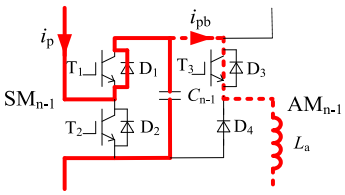

Fig. 11. Diagram of charge conservation of the submodule capacitor.

current containing both power current and balance current in the conventional single-leg MMDC, the power current and the balance current in the proposed converter flow through the power branch and the added balance branch, respectively, so as to decrease the electric stress on an individual element.

D. Capacitor Voltage Fluctuation and Parameters Calculation

The voltage balance control of the submodule capacitor is one of the main control goals of the MMDC. Under normal operating conditions, the submodule maintains the dynamic balance of capacitor voltage by the self-balancing control. However, the instantaneous fluctuation of a capacitor voltage is closely related to the capacitor capacity, modulation mode, switching frequency, and load. The balance power transferred from top to bottom also leads to a stepwise decrease in capacitor voltages.

Suppose that the capacitor voltage balance is achieved through power transfer of the two paralleled submodules. Due to the stepwise power transfer, the quantity of charges to be transferred is ΔQ_{cUi} when the submodule i is in parallel with the submodule $i+1$ in the upper arm

$$\Delta Q_{\mathrm{cUi}} = i(1-d)i_U T_s, i = 1, 2...N \tag{15}$$

i_U is the average current of the power branch of the upper arm, and T_s is the switching period.

For the two submodules in the middle of the leg (SM_N of the upper arm and SM_1 of the lower arm), the upper arm capacitor is charged by the power branch current, while the lower arm capacitor is discharged by the branch current. When the two capacitors are in parallel, their powers are supplementary to each other. Suppose the power transfer can be finished in an instant when the capacitors are in parallel, and the initial capacitor voltages are u_c. According to the power conservation (8), the average capacitor voltages u_{cUN} and u_{cL1} can be abstained after one-time power transfer of the two paralleled capacitors

$$u_{\mathrm{cUN}} = u_{\mathrm{cL1}} = \frac{\Delta Q_{\mathrm{cUN}} + Q_c + \Delta Q_{\mathrm{cL1}} + Q_c}{2C} = u_c. \tag{16}$$

It can be known that the average voltage of the two submodules in the middle of the leg is kept in the range of the rated value through the power transfer. On this basis, the voltage of the submodule $N-1$ can be obtained after the power transfer of paralleled capacitors of submodule $N-1$ and submodule N for j times

$$u_{\mathrm{cUN-1(j)}} = u_c + \frac{(2^j - 1)\Delta Q_{\mathrm{cUN-1}}}{2^j C}. \tag{17}$$

When $j \to +\infty$, the stable average voltage of submodule $N-1$ can be expressed as

$$u_{\mathrm{cUN-1}} = u_c + \frac{(N-1)(1-d)i_U T_s}{C}. \tag{18}$$

Thus, the stable capacitor voltage of submodule i of the upper arm can be derived

$$u_{\mathrm{cUi}} = u_c + \frac{(N-i)(N+i-1)(1-d)i_U T_s}{2C}. \tag{19}$$

Similarly, the stable capacitor voltage of submodule i of the lower arm can be obtained.

$$u_{\mathrm{cLi}} = u_c - \frac{(i-1)(2N-i)di_L T_s}{2C}. \tag{20}$$

Equations (19) and (20) show that the average voltage deviation of each submodule is related to its position, power branch current, and capacitance. There is the largest capacitor voltage deviation in the submodule 1 of the upper arm and the submodule N of the lower arm

$$\Delta u_{\mathrm{cU\,max}} = \Delta u_{\mathrm{cL\,max}} = \frac{N(N-1)k(1-k)i_o T_s}{2C}. \tag{21}$$

It is known from the above analysis that the minimum capacitor capacity can be achieved by setting the voltage fluctuation index of the submodule capacitor as ε, so that the fluctuation of the capacitor voltage is kept in a given range, namely $\Delta u_c \le \varepsilon u_c$

$$C \ge \frac{N(N-1)k(1-k)i_o T_s}{2\varepsilon u_c}. \tag{22}$$

In (22), the capacity of the submodule capacitor is inversely proportional to its switching frequency and rated voltage but is proportional to the load current when the capacitor voltage is maintained in a certain range of fluctuation. The higher the frequency is, the more often the energy exchange between the adjacent submodules, the smaller change of the capacitor energy in every switching period, and the smaller the fluctuation of the capacitor voltage. Furthermore, the larger the load current, the more sharply the capacitor charges and discharges, or the more strongly the capacitor voltage fluctuates.

On the other hand, the round-robin modulation mode is used to generate the pulse signals in sequence of inserting submodules, during which a relatively large fluctuation of instantaneous capacitor voltages caused by both different parameters of the devices and difficulties in power transfer of each submodule is ignored. Based on the self-balancing mechanism, the mode can be optimized so as to decrease the voltage fluctuation and increase the control accuracy of the output voltage. Thus, the priority indexes of the submodues can be obtained according to the instantaneous capacitor voltages and their degrees of difficulty in power transfer of the upper and lower arms. The submodules can be selectively inserted according to priority after the insertion coefficients of the arms are obtained at the beginning of a switching period. According to (10), the noninserted submodules are in parallel with each other for power transfer; therefore, causing that the ones with higher voltages to be discharged and the ones with lower voltages to be charged. Compared with the round-robin modulation, the selective insertion method is capable of decreasing the fluctuations of capacitor voltages.

Thus, a smaller fluctuation in capacitor voltage and a better steady-state performance can be achieved according to the capacitor capacity calculated by (22).

Meanwhile, the charge capacity of submodule capacitors of the upper and lower arms is kept in balance in a steady state. The inserted capacitors of the upper arm are charged by the arm current, with an increase in the capacitor charge Δq_U, whereas the inserted capacitors of the lower arm are discharged, with a decrease in the capacitor charge Δq_L. The increased charge capacity of the upper arm is equal to the decreased charge capacity of the lower arm

$$\Delta q_U = \Delta q_L. \tag{23}$$

According to the conservation of charge, the changed charge capacity of the upper or lower arm is equal to the charge capacity transferred from the upper arm to the lower arm. Under extreme condition, the transferred charge capacity is the smallest when the bottom submodule of the upper arm is only in parallel connection with the top one of the lower arm. In this situation, according to the change in voltage of the submodule, the quantity of the changed capacitor charges obtained after one-time power transfer can be expressed as

$$\Delta q_N = C(\Delta u_U - \Delta u_L)/2 \tag{24}$$

where Δu_U and Δu_L represent average changes in the capacitor voltages of the upper and lower arms. According to $\Delta q_U = \Delta q_N$, it can be derived

$$i_o = \frac{(\Delta u_U - \Delta u_L)CV_{\rm dc}u_c}{2(V_{\rm dc} - u_o)u_oT_s} = \frac{\varepsilon CV_{\rm dc}{u_c}^2}{(V_{\rm dc} - u_o)u_oT_s}. \tag{25}$$

According to (25), the maximum output current is proportional to the switching frequency and the capacitor capacity. Increasing the frequency can effectively improve the ability of an output power.

III. Small-Signal Module and Control of the New MMDC

According to the mathematical model in Fig. 7 and the complementation of the insertion coefficients n_U and n_L, the inductor voltages of the upper and lower arms are

$$u_{\rm LU} = -u_{\rm LL}. \tag{26}$$

So it can be deduced that the potentials of A and B are the same

$$V_A = V_B. \tag{27}$$

The equivalent circuit obtained from the output side is shown in Fig. 12, in which the voltage of the lower arm is equivalent to a controllable voltage source u_L and $L_e = L_p/2 + L_o$. The output voltage is linear to the equivalent voltage of the inserted submodules of the lower arm. Therefore, by use of the classical dc control method, the control of the equivalent voltage of the lower arm can result in the stabilization of the output voltage.

Assuming that the capacitor voltage of each submodule is in dynamic balance, the voltage of an equivalent voltage source

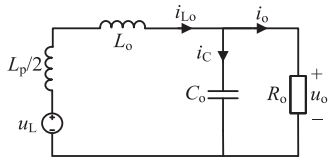

Fig. 12. Diagram of converter output equivalent circuit.

that can be obtained in a switching period T_s is expressed as

$$u_L = \begin{cases} ([n_L]+1)u_c & 0 \le t \le dT_s \\ [n_L]\,u_c & dT_s \le t \le T_s \end{cases}. \tag{28}$$

The average switching-period method is used to establish the state equation of the inductor voltage in Fig. 12

$$L_e\frac{d\langle i_{\rm Lo}(t)\rangle_{T_s}}{dt} = n_L(t)\langle u_c(t)\rangle_{T_s} - \langle u_o(t)\rangle_{T_s}. \tag{29}$$

In the same way, the state equation of the capacitor current is established

$$C_o\frac{d\langle u_o(t)\rangle_{T_s}}{dt} = \langle i_{\rm Lo}(t)\rangle_{T_s} - \frac{\langle u_o(t)\rangle_{T_s}}{R_o}. \tag{30}$$

According to the volt–second balance of the inductor and the charge balance of the capacitor, the periodical average values of the inductor voltage and the capacitor current are zeros in a stable state. Thus, the steady relationships of the equivalent circuit are obtained

$$\begin{cases} \langle u_o(t)\rangle_{T_s} = n_L(t)\langle u_c(t)\rangle_{T_s} \\ \langle i_{\rm Lo}(t)\rangle_{T_s} = \langle u_o(t)\rangle_{T_s}/R_o \end{cases}. \tag{31}$$

Equation (31) shows that the output voltage can be adjusted by changing the insertion coefficient of the lower arm and that the load current is irrelative to $n_L(t)$ and is only related to the parameters in (25).

Based on the state equations (29) and (30), the use of the perturbation method to deal with the dynamic small-signal model of the converter leads to

$$L_e\frac{d\hat{i}_{\rm Lo}(t)}{dt} = N_L\hat{u}_c(t) + V_c\hat{n}_L(t) - \hat{u}_o(t) \tag{32}$$

$$C_o\frac{d\hat{u}_o(t)}{dt} = \hat{i}_{\rm Lo}(t) - \frac{\hat{u}_o(t)}{R_o} \tag{33}$$

where N_L and V_c are, respectively, the insertion coefficient and capacitor voltage of the lower arm in a steady state; $\hat{i}_{\rm Lo}(t)$, $\hat{u}_c(t)$, $\hat{n}_L(t)$, and $\hat{u}_o(t)$ denote the perturbations of the filter inductive current, capacitor voltage, lower arm insertion coefficient, and output voltage, respectively.

The transfer function of the converter is deduced by converting the time-domain small-signal model into the frequency-domain one. The equation is

$$u_o(s) = \frac{N_Lu_c(s) + V_cn_L(s)}{L_eC_os^2 + \frac{L_e}{R_o}s + 1}. \tag{34}$$

It can be found from (34) that the converter is a zero-type system. The output voltage is only related to the insertion

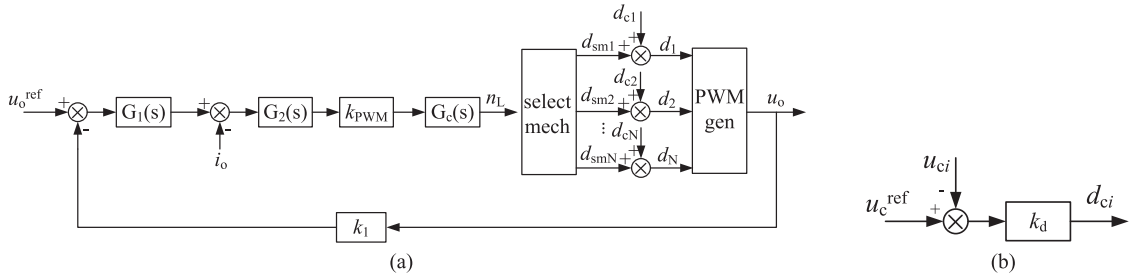

Fig. 13. Block diagram of closed-loop control. (a) Block diagram of voltage–current double closed-loop control. (b) Block diagram of capacitor voltage disturbance correction.

coefficient of the lower arm. The conventional proportional integral regulator can eliminate the steady-state error of the output voltage.

In addition, considering instantaneous fluctuations in the capacitor voltages have influence on the control precision and dynamic performance of the converter, the instantaneous error of each capacitor voltage is treated as a disturbance to adjust the control variable. The specific method is that after the insertion coefficient of the lower bridge arm in the next switching period is obtained, each submodule is determined to insert or bypass according to the selective modulation method and its reference duty can be obtained too; according to the instantaneous disturbance of each capacitor voltage, the adjustment of the duty results in the proper one; the disturbance correction of the capacitor voltage is done by the proportional regulator.

The combination of the control method of the voltage–current double closed-loop of the conventional buck converter and the disturbance correction method of the submodule capacitor voltage leads to a new control method, as shown in Fig. 13.

In Fig. 13, k_1 is the sampling coefficient of output voltage; $G_1(s) = k_{p1} + k_{i1}/s$ and $G_2(s) = k_{p2} + k_{i2}/s$ represent the voltage-loop regulator and the current-loop regulator, respectively; k_{PWM} denotes the gain of pulse width modulation modulator; $G_c(s)$ denotes the transfer function from control to output of the dc–dc converter. The control parameters k_{p1}, k_{p2}, k_{i1}, and k_{i2} are related to the real circuit. k_{d} denotes the regulating coefficient of the submodule capacitor voltage disturbance.

IV. Experiment and Analysis

According to the proposed MMDC, the basic principle is simulated and analyzed based on PLECS. Meanwhile, a two-level dc converter prototype for experiment is built to verify the dc power conversion characteristics. The prototype is shown in Fig. 14.

The heterogeneous full-bridge submodule is composed of the intelligent power module (IPM) PM75RLA060 of MITSUBISHI, the energy- storage film capacitor, and the related driving circuit. The load of the converter is a resistor. The input dc source comes from the voltage regulator. The corresponding experimental parameters are shown in Table III.

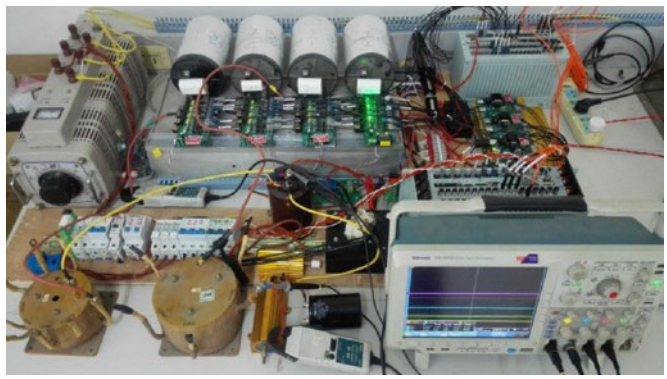

Fig. 14. Platform of experimental prototype.

TABLE III
Experimental Parameter

Parameters	Value
Input DC voltage	$V_{\mathrm{dc}} = 200$ V
Number of submodules	$N = 2$
Power branch inductor	$L_{\mathrm{p}} = 0.1$ mH
Rated voltage of submodule	$u_{\mathrm{c}} = 100$ V
Filter inductor	$L_{\mathrm{o}} = 0.5$ mH
Filter capacitor	$C_{\mathrm{o}} = 2.2$ mF
Switch frequency	$f_{\mathrm{s}} = 10$ kHz
Auxiliary balance branch inductor	$L_{\mathrm{a}} = 1.6$ mH
Modulation mode	Round-robin and selective insertion modulations

When the conversion ratio k has a step change from 0.7 to 0.2, the steady and dynamic waveforms of the key electrical parameters are shown in Fig. 15.

Fig. 15(a) shows the steady and dynamic voltage at the time of a step change appearing in the conversion ratio. The use of the proposed closed-loop control method leads to a fast dynamic response of the converter and its stable output voltage, thereby eliminating the steady-state error of the output voltage due to voltage fluctuations in the submodule capacitors and an addition of dead time between the switching pulses, and the output voltage error is within 3%. Fig. 15(b) shows the input and output current waveforms. Because of the buffer effects of the power branch inductors, the inductors are charged and discharged periodically. The input current has a small fluctuation on the dc bias when there is a change in the number of inserted submodules

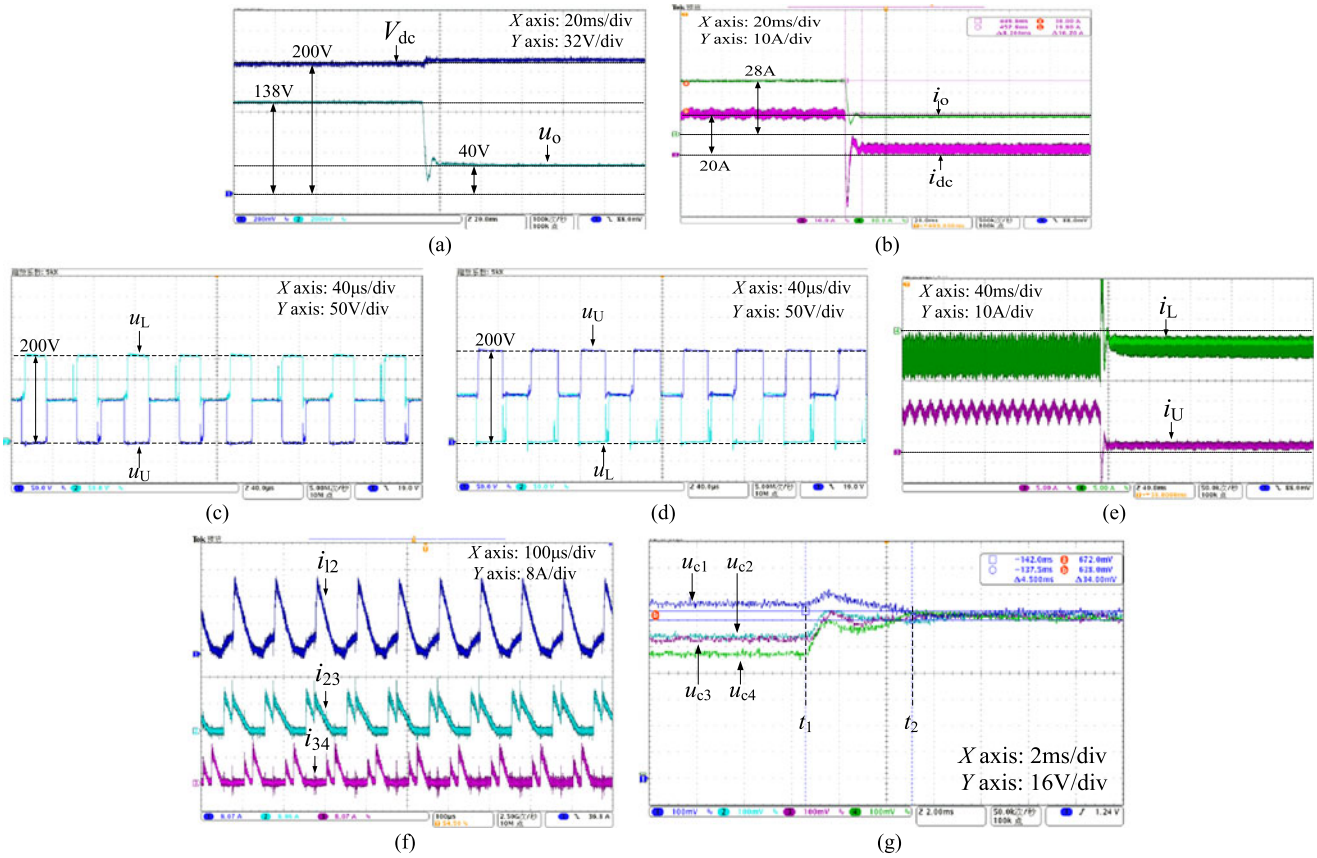

Fig. 15. Experimental waveforms of key parameters. (a) Input–output voltage. (b) Input–output current. (c) Voltages of upper and lower arms when $k = 0.7$. (d) Voltages of upper and lower arms when $k = 0.2$. (e) Currents of upper and lower arms of the power branch. (f) Currents of auxiliary balance branches. (g) Voltages of submodule capacitors.

of the arms. When there is a step change in the output voltage, the energy stored in the inductors can make the capacitors overcharged. The converter feeds power back to the power supply, thereby causing a reverse current spike in the input current. Fig. 15(c) and (d) shows the voltage waveforms of the upper and lower arms at the time of different conversion ratios. It can be seen that although the conversion ratios are different, the voltages of the arms are also different, their voltages are always complementary and their sum equals the dc voltage. In the case of different ratios, the output voltage is obtained by chopping the voltage with different dc bias, which can reduce the output voltage ripples and the needs for the output filter. Fig. 15(e) shows the currents of the upper and lower power branches. In the dc operation mode, the currents are dc. Because the output voltage comes from the lower arm voltage which is chopped, there are triangle fluctuations in the currents. Fig. 15(f) shows the current waveforms of auxiliary balance branch between the adjacent submodules. In each switching period, the connections between the capacitors change with the operating states of the inserted submodules. When the submodules are connected in parallel, the difference in capacitor voltages will generate current to transfer power. Because the time constant of the parallel circuit is smaller than the switching period, the power transfer can be fulfilled in a short time. The current of the branch is a discontinuous surge current, which is suppressed effectively by the series inductor. As a short-time surge current is only needed, the switching loss and the capacity of the devices of the auxiliary balance branch are decreased. Fig. 15(g) shows the self-balancing voltage waveforms of the four submodule capacitors $u_{c1} - u_{c4}$. At the beginning of t_1, there are deviations in voltages of the four capacitors. During $t_1 - t_2$, power exchanges between the submodules are performed through the parallel connection of the capacitors, and the capacitor voltages have their self-balancing ability without the need for a special balance controller. In the end, the average voltage fluctuations are within 5%.

According to (5), the conversion ratio of the proposed MMDC is N times smaller than that of the conventional buck converter. In the case of the minimum duty ratio of the switching device, the converter has a wider range of output voltage. Fig. 16 shows the wide-range output voltage of the converter and the voltage waveform of its lower arm. In (a), the modulation ratio of the converter is 0.05. In (b), the modulation ratio is 0.95. Suppose the minimum duty ratio of the device is $d_{\min} = 0.1$. The round-robin modulation method is used to make the two submodules of the upper or lower arms operate in turn, and the minimum duty ratio of each switch is 0.1 (10 μs).

The output voltage is the filtered voltage of the lower arm. When the conversion ratio is very small, the output instruction voltage is low. In one switching period, one submodule of the

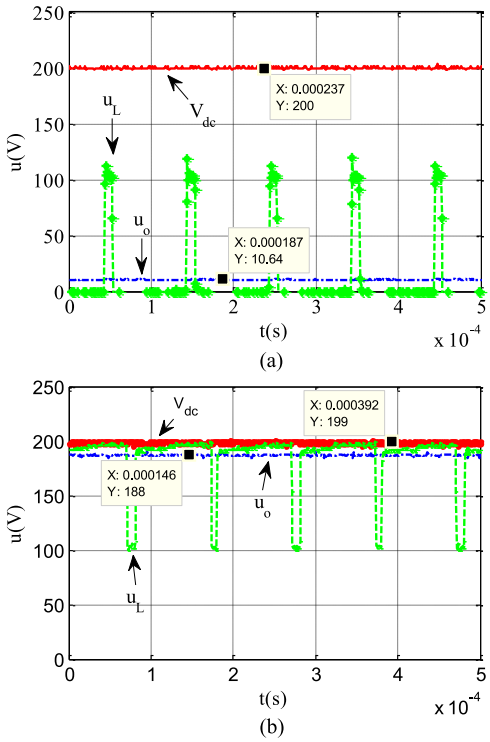

Fig. 16. Experimental waveforms of wide-range output voltage. (a) Input–output and lower arm voltage waveforms of modulation ratio 0.05. (b) Input–output and lower arm voltage waveforms of modulation ratio 0.95.

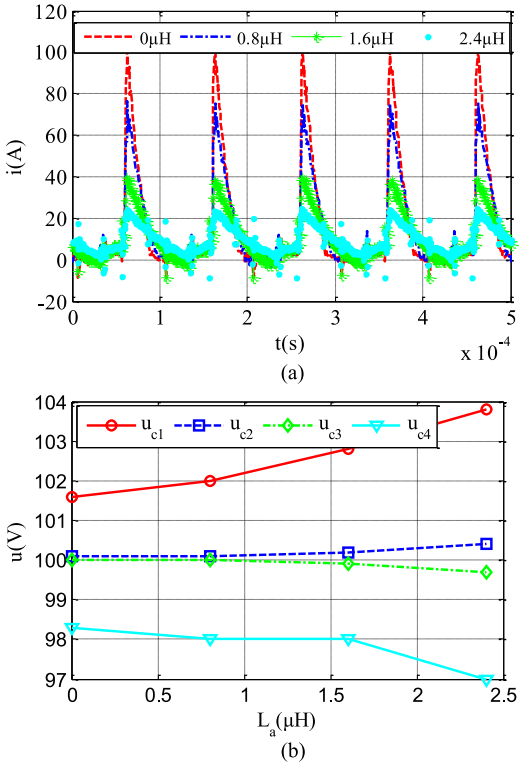

Fig. 17. Experimental diagrams of series inductor of auxiliary balance branch. (a) Auxiliary balance branch current i_{12}. (b) Capacitor voltages of the four submodules.

lower arm is bypassed, and the other one operates with the minimum duty ratio. The operating states of the arms are complimentary to each other. The lower arm voltage as a single capacitor voltage fluctuates periodically, as shown in Fig. 16(a). When the conversion ratio is large, the output instruction voltage is high. In one period, one submodule of the lower arm is constantly switched on, and the other one operates with the maximum duty ratio. The lower arm voltage is a square wave with a dc bias u_c, and its fluctuation is only a capacitor voltage, as shown in Fig. 16(b). The filtered output voltage has smaller fluctuation and higher stability than that of the conventional buck converter. For the same minimum duty ratio $d_{\min}$, the output voltage range of the proposed MMDC expands from $[V_{\rm dc}d_{\min}, V_{\rm dc}(1-d_{\min})]$ to $[V_{\rm dc}d_{\min}/N, V_{\rm dc}(1-d_{\min}/N)]$. With an increase in the number of the submodules, its output voltage range is wider, and the capacity and volume of the filter needed for output are smaller.

The auxiliary balance branch provides current paths for the parallel connections of the adjacent submodule capacitors so as to achieve the self-balancing of the capacitor voltages under the condition of dc power conversion. However, the voltage difference between the paralleled capacitors and the small-line impedance will lead to a surge current in the branch and a large electric stress on the devices. The series inductor of the branch can effectively suppress the current. According to changes in inductance, the corresponding experimental waveforms of the branch currents and the capacitor voltages are shown in Fig. 17.

With an increase in series inductance of the auxiliary balance branch, the surge current is decreased obviously. An increase in time constant of the equivalent circuit will lengthen the duration of current. While suppressing the surge current, the inductor hinders the power transfer between the submodules, and the voltage fluctuations of the capacitors will increase when the current continues. Therefore, a suitable inductor can not only suppress the current but also keep the branch current discontinuous when the capacitor voltages are in a rated range. As a result, the device capacity required by the auxiliary balance branch can be reduced.

Fig. 18 shows the experimental waveforms of the maximum capacitor voltage fluctuations. When the conversion ratio is constant, voltage fluctuation increases with the output current. The calculation value basically coincides with the experimental one, as shown in Fig. 18(a). With an increase in conversion ratio, the experimental value is smaller than the calculated value when several submodules are in parallel to transfer power, as shown in Fig. 18(b).

Furthermore, the basic principle of the converter shows that the capacitor voltage is inversely proportional to the switching frequency. The higher the frequency is, the more times the submodules in parallel connection transmit power in a unit time and the smaller the fluctuation of the capacitor voltage is. Changing the switching frequency can obtain the average voltage of each capacitor, as shown in Fig. 19.

It can be seen from Fig. 19 that as the frequency decreases, the capacitor voltage fluctuation increases. The average capacitor voltage is gradually decreased according to the submodule position from top to bottom of the leg. The capacitor voltage fluctuations of the submodules located at both ends of the leg

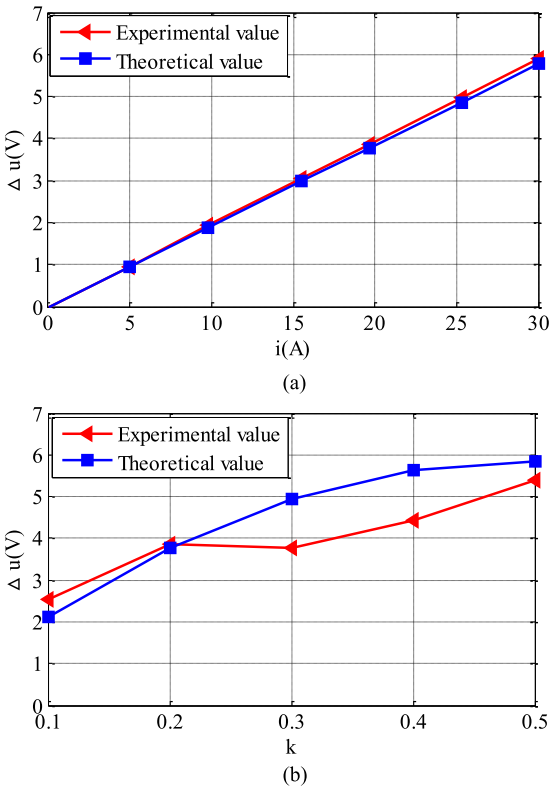

Fig. 18. Experiment waveforms of the max capacitor voltage fluctuation. (a) Max capacitor voltage fluctuation when $k = 0.2$. (b) Max capacitor voltage fluctuation when $i_o = 20$ A.

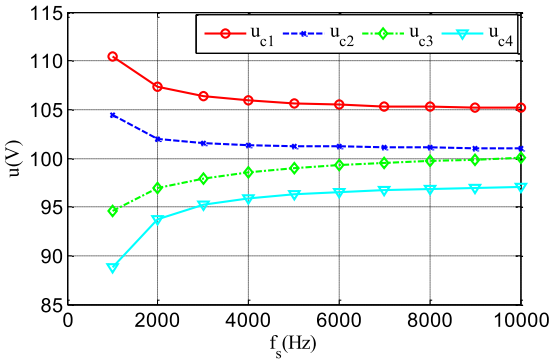

Fig. 19. Simulation waveforms of the capacitor voltages with different switching frequencies.

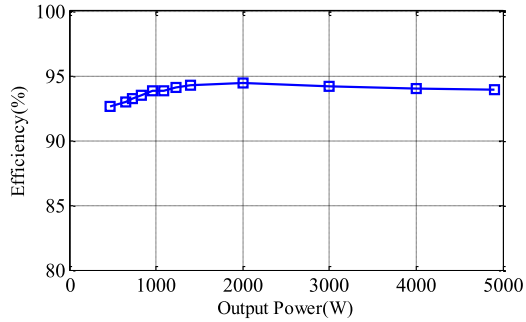

Fig. 20. Efficiency curve of the MMDC.

are larger than that of the middle ones. The reason is that the power transmission of those end submodules is more difficult than that of the intermediate submodules. The corresponding experimental results are in agreement with theoretical analysis.

In order to study the loss of the converter, the efficiency of different output power is tested on the 5-kW prototype, and the results are shown in Fig. 20. When the output power is small, the switching loss is high, and the efficiency is low. With an increase of the output power, the efficiency is gradually increased, and the maximum is achieved at the power of 2 kW. As the power level of the prototype is small, the converter loss is high and the efficiency is relatively low. When the power level is increased, the efficiency will be improved.

V. Conclusion

Because the currently used MMDC with ac control is relatively complex, the reactive power is large, and the electric stress on the device is high, this paper has proposed a new MMDC topology based on the concept of dc control. By changing the conventional two-terminal full-bridge submodule into a four-terminal one, the converter contains a power branch and an auxiliary balance branch. Based on the analysis of the mathematical model, the self-balancing principle of the capacitor voltage, the capacitor voltage fluctuation, and the small-signal model, this paper has presented a closed-loop control strategy. The simulations and experiments verify the dynamic and static performance. The results show that the proposed MMDC can work stably due to good dynamic and static characteristics under the classical dc control, the capacitor voltage has self-balancing ability and small fluctuation, and the adjustable range of output voltage is wide. The proposed topology and its dc control method are characterized by simple analysis and control as well as novelty, compared with the commonly used ac control method. All this is of some reference value to the future research of the topologies and control methods of the MMDC. Considering the comprehensive energy efficiency characteristics, the new MMDC can be used as a technological option for the dc power conversion in medium-voltage vessel integrated power system.

In conclusion, as far as the proposed converter is concerned, continuous and deep researches on optimizing modulation mode, states of continuous and discontinuous currents, as well as the bidirectional power conversion are of great importance to improve the theoretical analysis and guiding practical application. The above related contents will be continuously studied.

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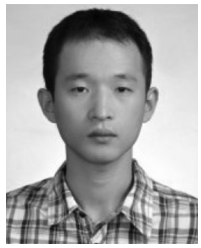

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