Ultrahigh Step-Down Converter With Wide Input Voltage Range Based on Topology Exchange

Y. T. Yau, *Member, IEEE*, W. Z. Jiang, *Student Member, IEEE*, and K. I. Hwu, *Member, IEEE*

***Abstract*—To overcome the traditional buck converter, which is difficult to achieve a high step-down gain with an appropriate duty cycle, a coupled-inductor-based step-down converter, named ultrahigh step-down converter, is proposed by Hwu *et al.* [11]. As compared with the buck converter, the ultrahigh step-down converter can achieve a much higher step-down gain, which can be determined by not only the duty cycle but also the turns ratio of the coupled inductor. However, the ultrahigh step-down converter is designed at a fixed input voltage of 48 V. In the telecommunication applications, the high dc bus voltage varies in a wide range, not kept at a fixed nominal voltage of 48 V. The experimental results show that as the input voltage increases, the efficiency of the ultrahigh step-down converter decreases. Therefore, in this paper, an improved ultrahigh step-down converter with a wide input voltage range is presented. According to the topology exchange, the voltage gain can be changed to a suitable one when the input voltage changes. By doing so, as compared with the ultrahigh step-down converter [11], the duty cycle of the proposed converter can be extended, and hence the efficiencies of the proposed converter can be improved. The proposed converter is verified by a wide input voltage (18–54 V), with an output voltage of 1.2 V and a rated output current of 10 A.**

***Index Terms*—Buck converter, coupled inductor, topology exchange, ultrahigh step-down converter, wide input voltage.**

I. Introduction

Up to now, the switching power has gotten attractive in the world [1], [2]. In today's telecommunication applications, the distributed power systems (DPSs) have been widely used [2]- [5]. The general architecture for the DPS is shown in Fig. 1. From Fig. 1, it can be seen that there are three stages. The first stage is an ac–dc converter, which transfers the ac input to a 48-V dc voltage bus; the second stage is a dc–dc converter, also called bus converter, which converts 48V to 12V and provides galvanic isolation; the third stage is a nonisolated dc–dc converter, called point of load (POL), which steps down 12 V to the low voltage to meet the load requirements.

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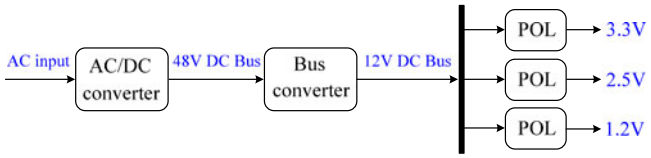

Fig. 1. Architecture of the DSP for telecommunication.

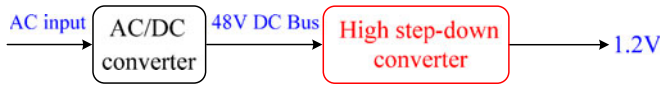

Fig. 2. Direct voltage-step-down from 48-V DC bus to load using the high step-down converter.

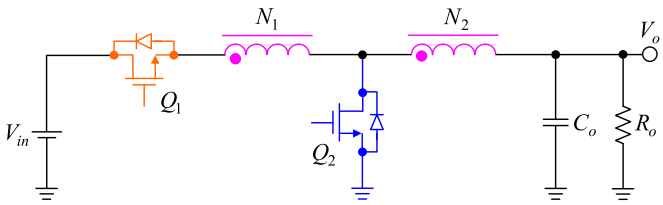

Fig. 3. Tapped-inductor buck converter [9] with voltage gain equal to $DN_2/(N_1 + N_2 - DN_1)$.

The synchronously rectified (SR) buck converter is commonly used for the POL converter due to its simple structure and control [6]- [8]. The voltage of 48 V is converted to the low required voltage via two stages. Thus, the efficiency is the product of individual efficiencies of two stages. To improve the efficiency, one stage is another solution as shown in Fig. 2. Moreover, since the voltage gain of the buck converter is equal to its duty cycle, it is difficult to obtain a high efficiency for high voltage step-down applications due to its narrow duty cycle. Therefore, to obtain a suitable duty cycle, the tapped-inductor buck converter is an alternative solution for high voltage step-down applications [9], [10] as shown in Fig. 3. The tapped-inductor buck converter has two freedoms: turns ratio and duty cycle. Thus, as compared with the buck converter, the duty cycle of the tapped-inductor buck converter can be extended. However, the tapped-inductor buck converter still suffers from some problems. First, the leakage inductance causes high voltage spikes across the switches. Second, the high voltage spikes result in high switching loss. Third, high voltage rating switches are required due to the high voltage spikes. To improve the above disadvantages, a high step-down converter, named ultrahigh step-down converter, is presented [11] as shown in Fig. 4. From Fig. 4, it can be seen that the ultrahigh step-down converter is constructed by

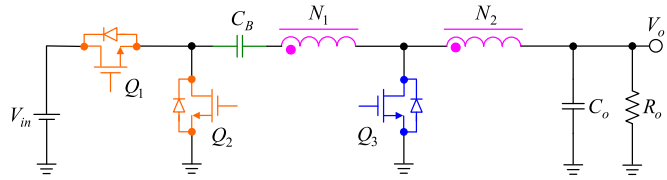

Fig. 4. Ultrahigh step-down converter [11] with voltage gain equal to $DN_2/(N_1+N_2)$.

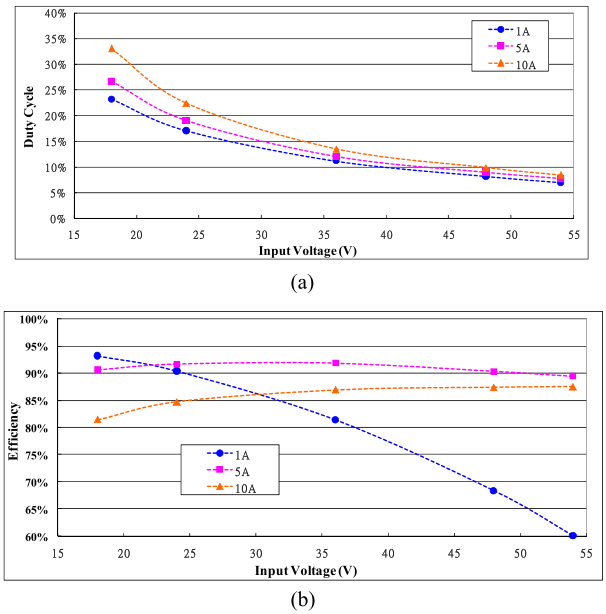

Fig. 5. Experimental results of the ultrahigh step-down converter [11] under different input voltages with output voltage of 3.3 V and $N_1 : N_2 = 24 : 8$ and switching frequency of 100 kHz: (a) duty cycle versus input voltage and (b) efficiency versus input voltage.

adding one additional switch and one additional capacitor to the tapped-inductor buck converter. Therefore, the coupled inductor in the ultrahigh step-down converter works in a different way as compared with the tapped-inductor buck converter. In the ultrahigh step-down converter, when Q_1 is turned on, C_B and the coupled inductor are storing energy, while when Q_2 and Q_3 are turned on, C_B resonates with the leakage inductor of the coupled inductor. Therefore, the soft switching and low-voltage spike can be achieved. Moreover, if Q_1 is broken, a high voltage will not appear in the output terminal. This is because the energy-transferring capacitor C_B is connected with the output capacitor C_o serially. If Q_1 is broken, the input voltage will be almost across C_B because C_B is usually chosen to be much smaller than the output capacitor C_o.

In [11], the ultrahigh step-down converter is design at a fixed input voltage. However, in telecommunication applications, the high dc bus voltage varies in a wide range, not kept at a fixed nominal voltage of 48 V [4], [12]. In general, the high dc bus voltage range ratio is 2:1. Fig. 5 shows the experimental results under a wide input voltage range of 18–54 V and an output voltage of 1.2 V. From Fig. 5(a), it can be seen that the duty cycle decreases with increasing the input voltage. When the input voltage is increased to 54 V, the corresponding duty cycle is decreased to about 6.8%. Consequently, the small turn-on

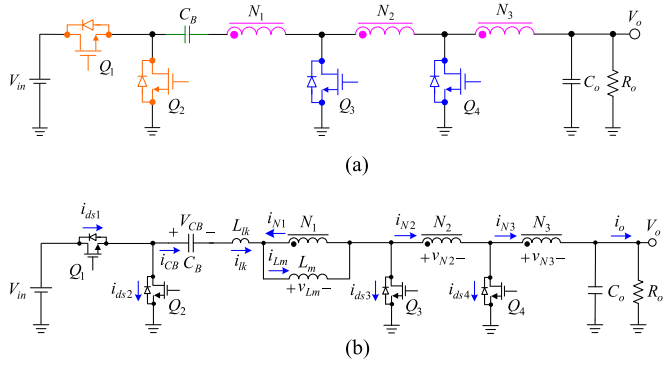

Fig. 6. Proposed converter: (a) main structure and (b) equivalent circuit model.

period will cause high switching loss and make the control difficult. Fig. 5(b) shows the efficiency curves with different input voltages and output currents. From Fig. 5(b), it can be seen that the efficiencies under half and rated loads can be maintained at reasonable values; however, at light load, the efficiency drops dramatically when the input voltage approaches to a high value of 54 V. This is because at light load, the zero voltage switching (ZVS) of Q_1 will be lost; thus, the switching loss is more severe, especially at high input voltage.

In this paper, the major objective focuses on the efficiency improvement of the ultrahigh step-down converter with a wide input voltage range. Therefore, an improved ultrahigh step-down converter with a variable voltage gain is proposed. When the input voltage of the proposed converter varies, the voltage gain can be changed to a suitable one to make the high step-down converter operate at higher efficiency. By the way, the pros and cons of the existing POLs and the proposed converter are shown in Appendix A.

II. Proposed Converter

For the circuit shown in Fig. 4, most of the energy is transferred to the load during the turn-off period of Q_1, but small portion of the energy is transferred to the load during the turn-on period of Q_1. The larger the duty cycle D is, the higher the peak value of i_{N2}, thereby causing the conduction loss and copper loss to be increased significantly. Accordingly, the duty cycle is suggested not to be too large. In addition, if the duty cycle is too small, the switching loss will be high and hence the duty cycle cannot be too small. Therefore, the aforementioned description is the reason why the topology exchange is used in this paper. As the input voltage range is large, the duty cycle should be controlled under a suitable range such that a better efficiency will be obtained.

Fig. 6(a) shows the proposed converter, which contains four switches Q_1, Q_2, Q_3, and Q_4, one energy-transferring capacitor C_B, one coupled inductor having three windings N_1, N_2, and N_3, and one output capacitor C_o. Moreover, the input voltage is denoted by $V_{\rm in}$, the output voltage is signified by V_o, and the output resistor is represented by R_o.

The equivalent circuit of the proposed converter is shown in Fig. 6(b). The coupled inductor is modeled as an ideal transformer with three windings N_1, N_2, and N_3. The magnetizing

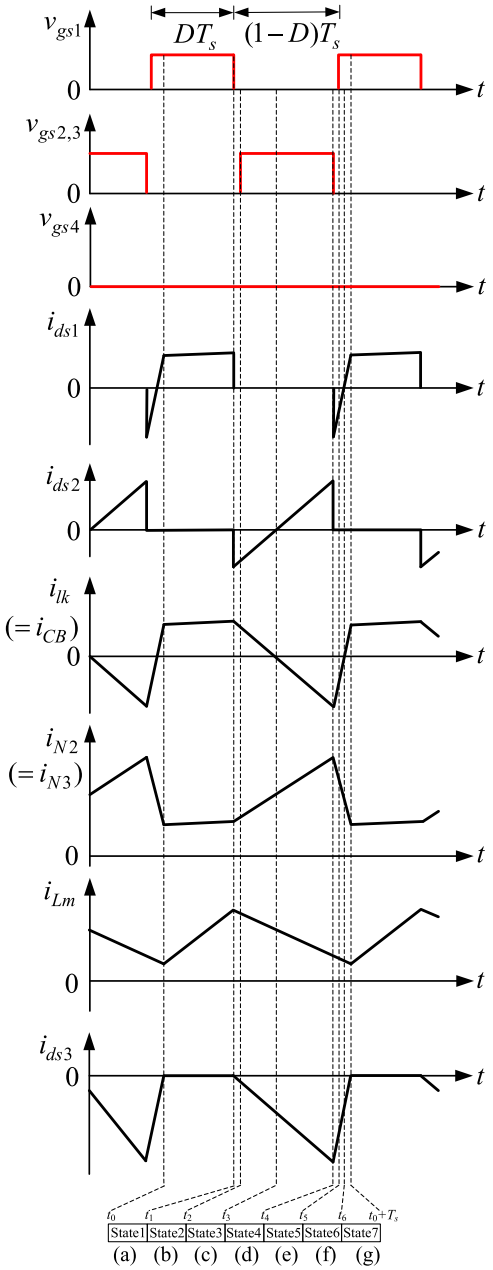

Fig. 7. Waveforms for the proposed converter in the low step-down gain mode.

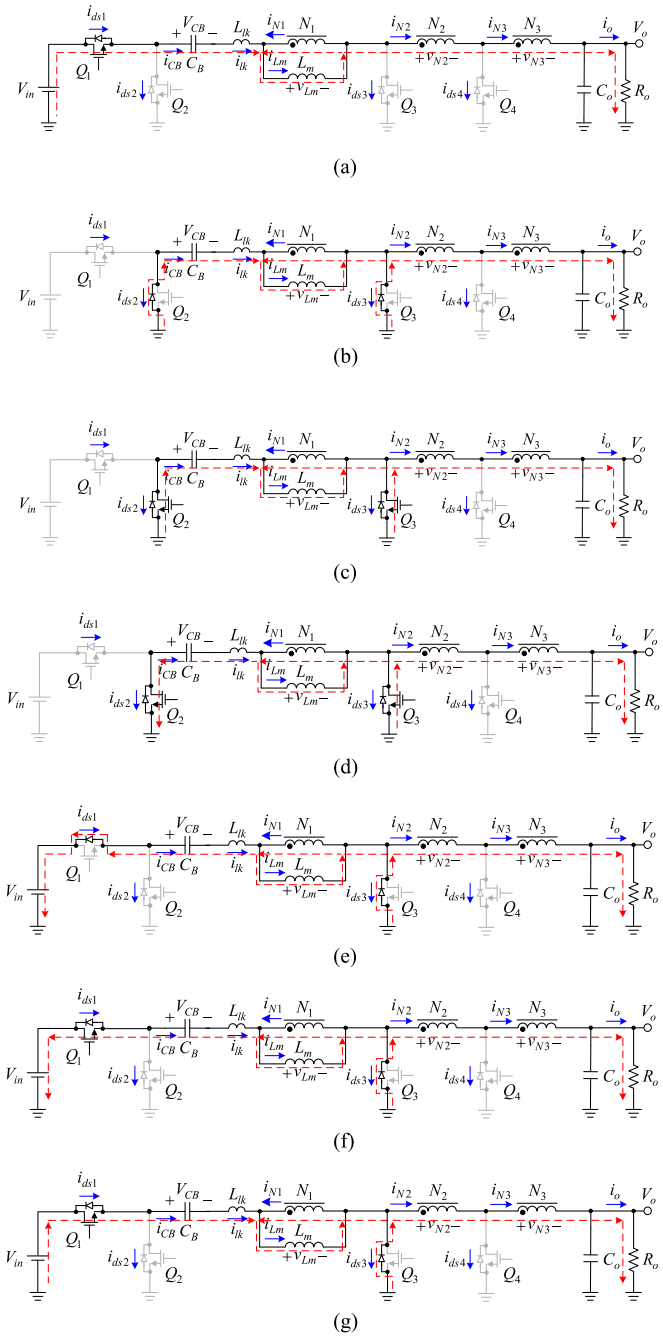

Fig. 8. Operating circuits over one switching period in the low step-down gain mode: (a) state 1, (b) state 2, (c) state 3, (d) state 4, (e) state 5, (f) state 6, and (g) state 7.

inductor L_m is connected in parallel with N_1, and a leakage inductor $L_{\rm lk}$ is connected in series with N_1.

The currents flowing through Q_1, Q_2, Q_3, Q_4, C_B, N_1, N_2, N_3, L_m, $L_{\rm lk}$ and R_o are signified by $i_{\rm ds1}$, $i_{\rm ds2}$, $i_{\rm ds3}$, $i_{\rm ds4}$, $i_{\rm CB}$, i_{N1}, i_{N2}, i_{N3}, $i_{\rm Lm}$, $i_{\rm lk}$ and i_o, respectively. Furthermore, the voltage across L_m or the N_1 winding is signified by $v_{\rm Lm}$, the voltages across the N_2 and N_3 windings are represented by v_{N2} and v_{N3}, respectively. The voltage across C_B is indicated by $V_{\rm CB}$. As to the control scheme for the proposed converter, it can be seen in Appendix B.

III. Basic Analysis

In order to make the analysis of the proposed converter easier, there are some assumptions to be made as follows: 1) all the switches and components are assumed to be ideal except for the coupled inductor as mentioned in Fig. 6(b); and 2) the voltages across the capacitors are constant.

The basic operating principles of the proposed converter include: 1) the high step-down mode; and 2) the low step-down mode. For the high step-down mode due to the high voltage range, Q_3 is always off and Q_4 is used as a freewheeling rectifier. In this case, N_1 and N_2 are regarded as connected in series, and hence the turns ratio n is equal to $N_3/(N_1+N_2)$, implying that the voltage step-down gain is high and the duty cycle can be

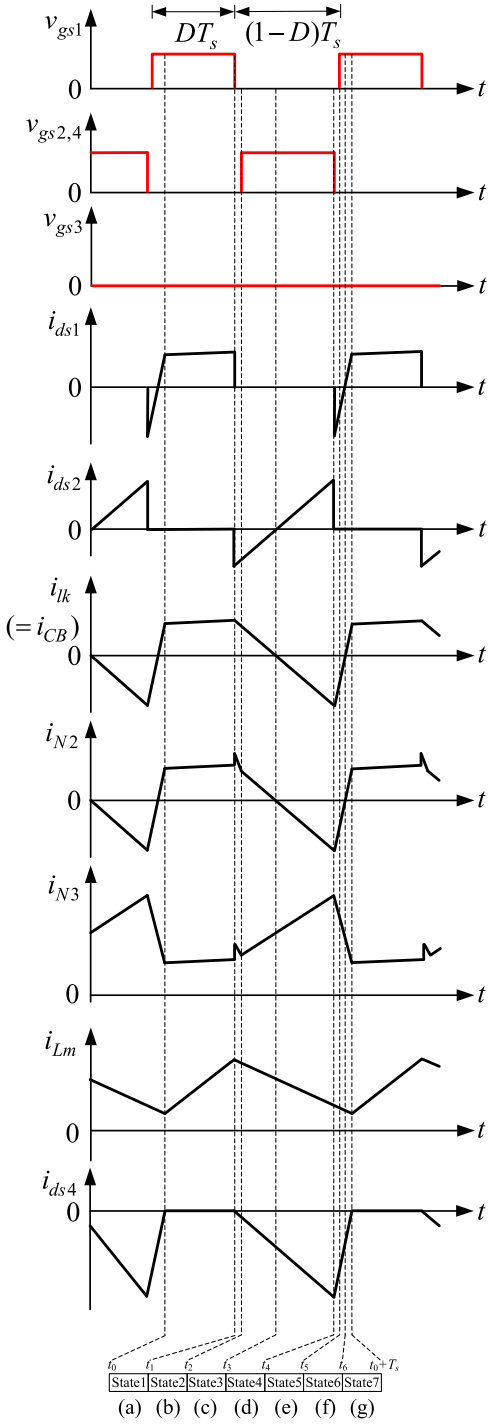

Fig. 9. Waveforms for the proposed converter in the high step-down gain mode.

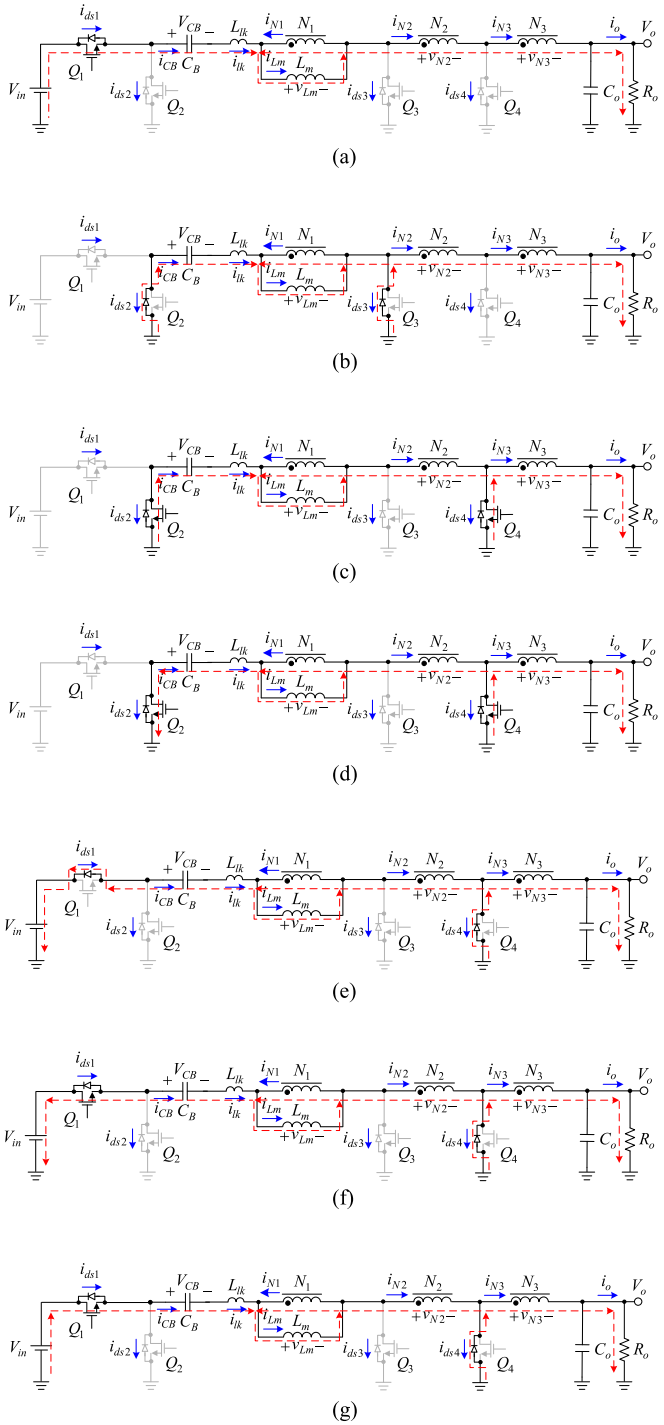

Fig. 10. Operating circuits over one switching period in the high step-down gain mode: (a) state 1, (b) state 2, (c) state 3, (d) state 4, (e) state 5, (f) state 6, and (g) state 7.

increased. For the low step-down mode due to the low voltage range, Q_4 is always off and Q_3 is used as a freewheeling rectifier. In this case, N_2 and N_3 are regarded as connected in series, and hence the turns ratio n is equal to $(N_2+N_3)/N_1$, implying that the voltage step-down gain is low and the duty cycle can be decreased. Via the two methods, the duty cycle all over the input voltage range can be controlled under a reasonable range.

The following analyses contain:

1) operating principles (low step-down gain mode and high step-down gain mode);

2) voltage gains (low step-down gain mode and high step-down gain mode); and

3) boundary conditions of the magnetizing inductor (low step-down gain mode and high step-down gain mode).

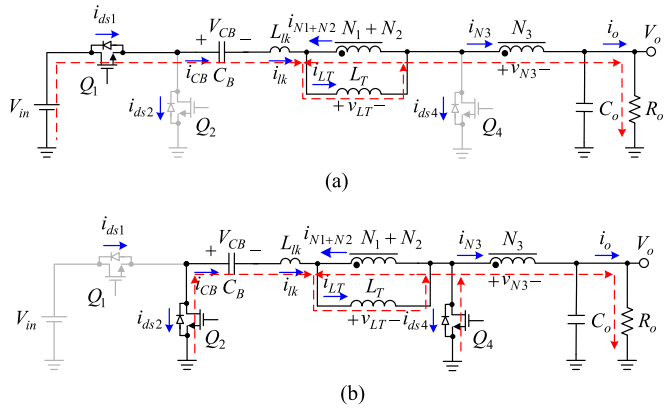

Fig. 11. Equivalent circuits from Fig. 10(a) and (c).

TABLE I
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Input voltage ($V_{\rm in}$)	18–54 V
Output voltage (V_o)	1.2 V
Rated output current ($I_{o,\rm rated}$)	10 A
Minimum output current ($I_{o,\rm min}$)	1 A
Switching frequency (f_s)	100 kHz
Mode switching point	36 V

TABLE II
COMPONENTS USED IN THE PROPOSED CONVERTER

Components		Product name
MOSFET switches	Q_1, Q_2	AON6248
	Q_3	AON6512 × 2 (cascaded)
	Q_4	BSC014NE2LSI
Energy-transferring capacitor	C_B	10 μF/50-V MLCC capacitor × 2
Output capacitor	C_o	1000-μF OSCON capacitor × 1, 10 μF MLCC × 6
Coupled inductor		Core: CH203125 × 2 $N_1 : N_2 : N_3 = 18 : 3 : 6$ $L_m = 60\mu$H, $L_{\rm lk} = 9.39\mu$H

A. Operating Principles for Low Step-Down Gain Mode

In the low step-down gain mode, the switch Q_4 is always turned OFF. The gate driving signal for Q_1 has the duty cycle of D, and the gate driving signals for Q_2 and Q_3 have the duty cycle of $1-D$. For the proposed converter operating in the low step-down gain mode, there are seven operating states to be described later. Fig. 7 shows the waveforms over one switching period, and the equivalent circuit in each state is shown in Fig. 8.

1) *State 1* $[t_0, t_1]$*:* As shown in Fig. 8(a), the switch Q_1 is turned ON, and the switches Q_2, Q_3 and Q_4 are turned OFF. During this state, the three windings are serially connected, which can be regarded as a single inductor whose equivalent value is $\{[(N_2+N_3)/N_1]+1\}^2 \cdot L_m + L_{\rm lk}$. A positive voltage $V_{\rm in} - V_{\rm CB} - V_o$ is imposed on the equivalent inductor. Thus, the currents $i_{\rm ds1}$, $i_{\rm lk}$, i_{N1}, i_{N2} and i_{N3} increase slowly. The magnetizing inductor L_m is also magnetized, and hence the current $i_{\rm Lm}$ increases. This state ends when Q_1 is turned OFF at $t = t_1$.
2) *State 2* $[t_1, t_2]$*:* As shown in Fig. 8(b), the switch Q_1 becomes turned OFF, but the switches Q_2, Q_3 and Q_4 still keep turned OFF. During this dead time period, the body diodes of Q_2 and Q_3 are forward-biased due to the coupled inductor freewheeling. C_B and $L_{\rm lk}$ start to resonate, and the resonating current $i_{\rm lk}$ or $i_{\rm CB}$ decreases. Meanwhile, the negative voltage $-V_o \cdot [N_1/(N_2+N_3)]$ is imposed on L_m. Thus, $i_{\rm Lm}$ starts to decline gradually. This state ends when Q_2 and Q_3 are turned on at $t = t_2$.

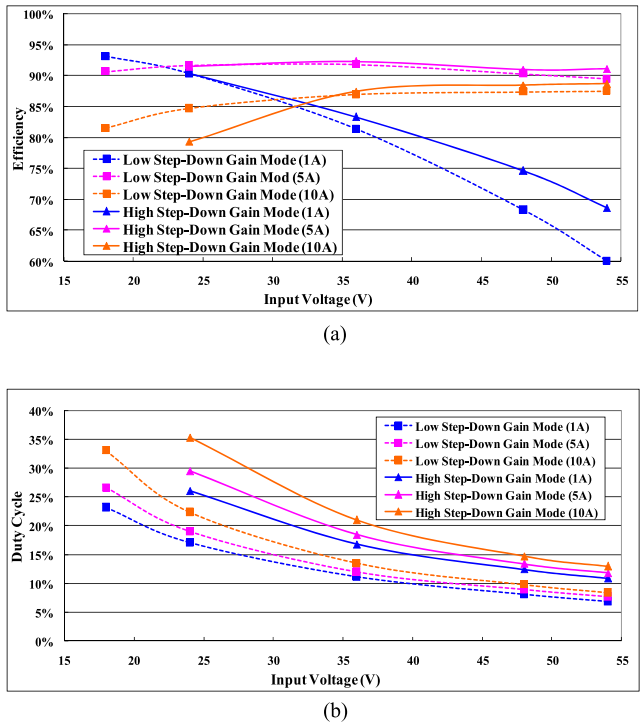

Fig. 12. Experimental results of the proposed converter under different input voltages with output voltage of 1.2 V and $N_1 : N_2 : N_3 = 18 : 3 : 6$ and switching frequency of 100 kHz: (a) efficiency versus input voltage and (b) duty cycle versus input voltage.

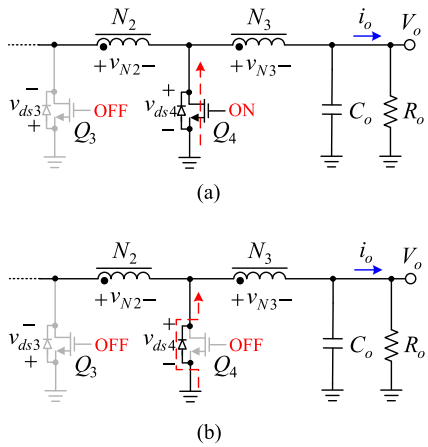

Fig. 13. Equivalent circuits in the high step-down gain mode: (a) turn-on state of Q_4 and (b) turn-on state of the body diode of Q_4.

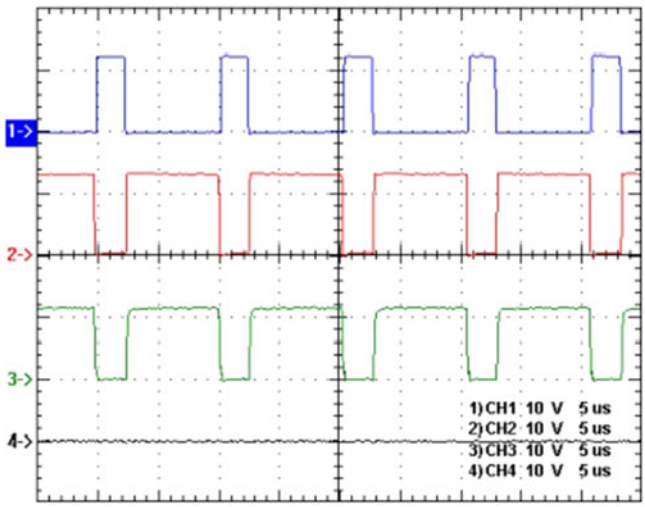

Fig. 14. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of 1 A: $v_{\rm gs1}$ (10 V/div); (2) $v_{\rm gs2}$ (10 V/div]; (3) $v_{\rm gs3}$ (10V/ div); and (4) $v_{\rm gs4}$ (10 V/div).

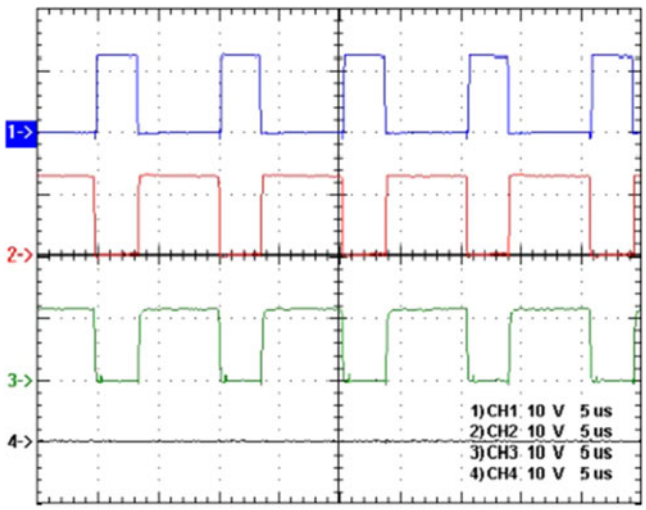

Fig. 15. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of : (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm gs2}$ (10 V/ div); (3) $v_{\rm gs3}$ [10V/ div] ; and (4) $v_{\rm gs4}$ (10 V/ div).

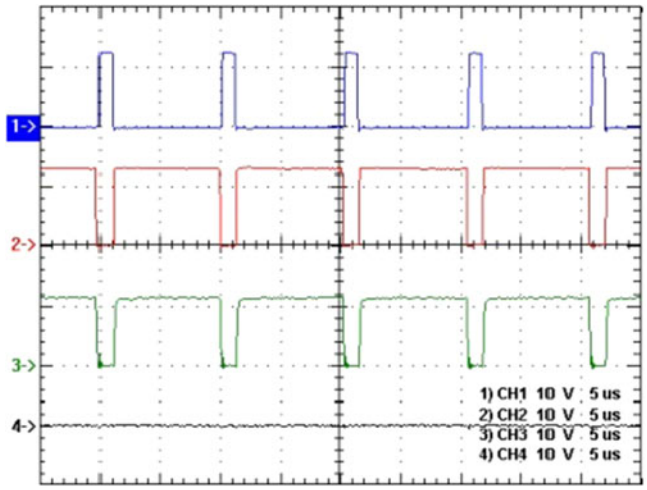

Fig. 16. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 1 A: $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm gs2}$ (10 V/ div); (3) $v_{\rm gs3}$ (10 V/ div); and (4) $v_{\rm gs4}$ (10 V/ div).

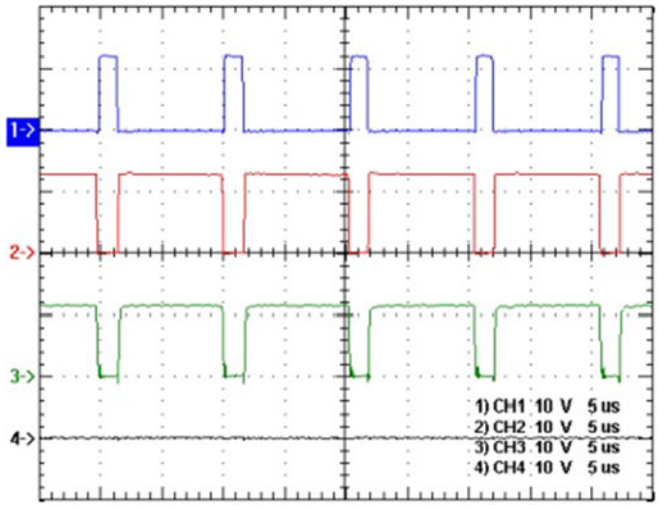

Fig. 17. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 10 A: $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm gs2}$ (10 V/ div); (3) $v_{\rm gs3}$ (10 V/ div); and (4) $v_{\rm gs4}$ (10 V/ div).

3) *State 3* $[t_2,\ t_3]$*:* Before the state 3 begins, the body diodes of Q_2 and Q_3 are conducted. Thus, Q_2 and Q_3 are turned ON with ZVS as shown in Fig. 8(c).The resonating current $i_{\rm lk}$ continually decreases, and $i_{\rm Lm}$ still decreases. Once $i_{\rm lk}$ falls to zero, this state ends at $t\ =\ t_3$.
4) *State 4* $[t_3,\ t_4]$*:* As shown in Fig. 8(d), the switches Q_1 and Q_4 keep turned OFF, and the switches Q_2 and Q_3 keep turned ON. The resonating current $i_{\rm lk}$ changes the direction, and is increasing in the opposite direction. C_B discharges the energy to the output via the coupled inductor windings. Thus, i_{N2} and i_{N3} continually increase. L_m is still demagnetized. This state ends when Q_2 and Q_3 are turned OFF at $t\ =\ t_4$.
5) *State 5* $[t_4,\ t_5]$*:* As shown in Fig. 8(e), the switches Q_1 and Q_4 keep turned OFF, and the switches Q_2 and Q_3 become turned OFF. During this dead time period, the body diode of Q_1 is forward biased by $i_{\rm lk}$, and the body diode of Q_3 is forward biased due to coupled inductor freewheeling. Meanwhile, $i_{\rm lk}$, i_{N2} and i_{N3} start to decrease, and L_m is continually demagnetized. This state ends when Q_1 becomes turned ON at $t\ =\ t_5$.
6) *State 6* $[t_5,\ t_6]$*:* Before state 6 begins, the body diode of Q_1 is forward biased. Thus, Q_1 is tuned ON with ZVS as shown in Fig. 8(f). The resonating current $i_{\rm lk}$ continually decreases, and L_m is continually demagnetized. This state ends when $i_{\rm lk}$ reaches zero at $t\ =\ t_6$.
7) *State 7* $[t_6,\ t_0+T_s]$*:* As shown in Fig. 8(g), Q_1 still keeps turned ON, and Q_2, Q_3 and Q_4 still keep turned OFF. During this state, $L_{\rm lk}$ and C_B form a series resonant circuit, and $i_{\rm lk}$ increases from zero. At the same time, i_{N2} and i_{N3} continually decrease. As soon as $i_{\rm lk}$ is equal to i_{N2}, $i_{\rm ds3}$ falls to zero, and this state ends at $t\ =\ t_0+T_s$.

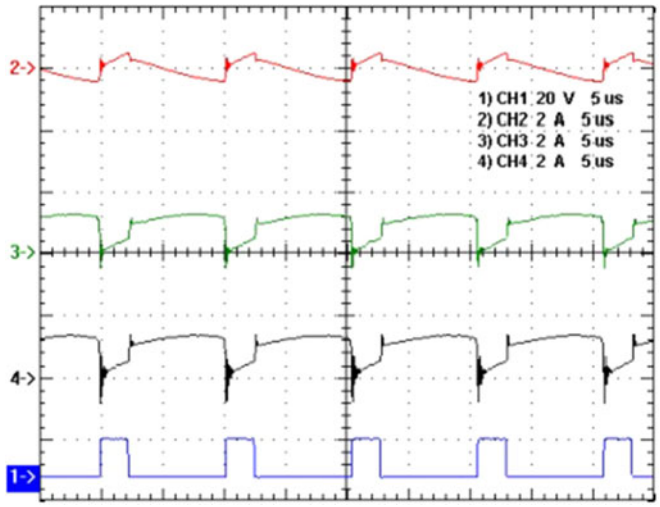

Fig. 18. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of 1 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (2 A/ div); (3) i_{N2} (2 A/ div); and (4) i_{N3} (2 A/ div).

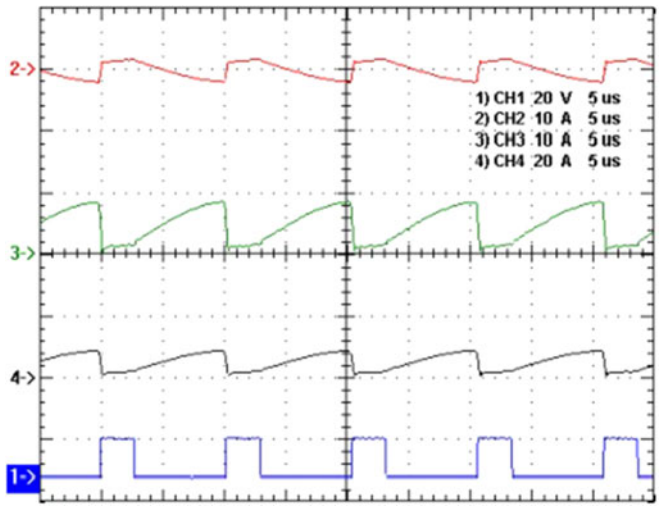

Fig. 19. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of 5A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20 A/ div).

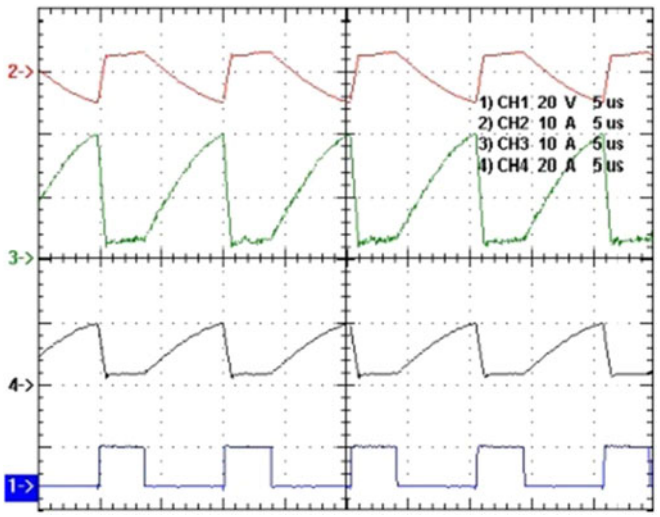

Fig. 20. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of 10 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20A/ div).

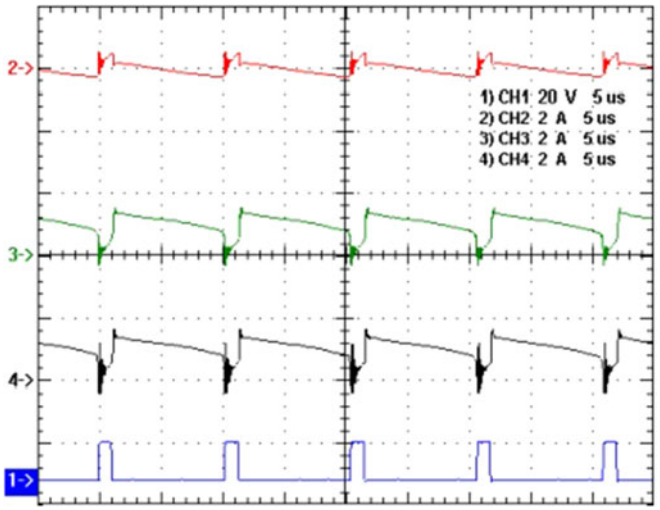

Fig. 21. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 1 A: (1) $v_{\rm gs1}$ (20V/ div); (2) $i_{\rm lk}$ (2 A/ div); (3) i_{N2} (2 A/ div); and (4) i_{N3} (2 A/ div).

B. Operating Principles for High Step-Down Gain Mode

In the high step-down gain mode, the switch Q_3 is always turned OFF. The gate driving signal for Q_1 has the duty cycle of *D*, and the gate driving signals for Q_2 and Q_4 have the duty cycle of $1-D$. For the proposed converter operating in the high step-down gain mode, there are seven operating states to be described below. Fig. 9 shows the waveforms over one switching period, and the equivalent circuit in each state is shown in Fig. 10.

1) *State 1* $[t_0, t_1]$*:* As shown in Fig. 10(a), the switch Q_1 is turned ON, and the switches Q_2, Q_3 and Q_4 are turned OFF. During this state, the three windings are serially connected, which can be regarded as a single inductor whose equivalent value is $\{[(N_2+N_3)/N_1]+1\}^2 \cdot L_m + L_{\rm lk}$. A positive voltage $V_{\rm in}-V_{\rm CB}-V_o$ is imposed on the equivalent inductor. Thus, the currents $i_{\rm ds1}$, $i_{\rm lk}$, i_{N1}, i_{N2} and i_{N3} increase slowly. The magnetizing inductor L_m is also magnetized and $i_{\rm Lm}$ increases. This state ends when Q_1 is turned off at $t = t_1$.
2) *State 2* $[t_1, t_2]$*:* As shown in Fig. 10(b), the switch Q_1 becomes turned OFF, but the switches Q_2, Q_3 and Q_4 still keep turned OFF. During this dead time period, the body diodes of Q_2 and Q_3 are forward-biased due to the coupled inductor freewheeling. C_B and $L_{\rm lk}$ start to resonate, and the resonating current $i_{\rm lk}$ or $i_{\rm CB}$ decreases. Meanwhile, the negative voltage $-V_o \cdot [N_1/(N_2+N_3)]$ is imposed on L_m. Thus, $i_{\rm Lm}$ starts to decline gradually. This state ends when Q_2 and Q_4 are turned ON at $t = t_2$.
3) *State 3* $[t_2, t_3]$*:* Before the state 3 begins, the body diode of Q_2 is conducted. Thus, Q_2 is turned ON with ZVS as shown in Fig. 10(c). Meanwhile, Q_4 becomes turned ON. The resonating current $i_{\rm lk}$ continually decreases, and $i_{\rm Lm}$ still decreases. Once $i_{\rm lk}$ falls to zero, this state

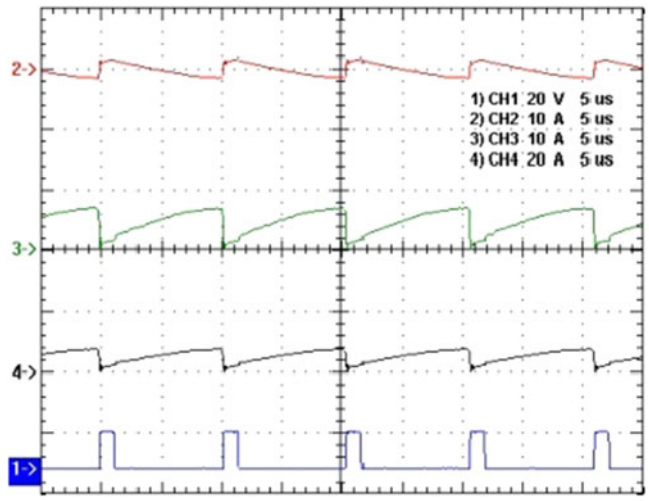

Fig. 22. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 5 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20 A/ div).

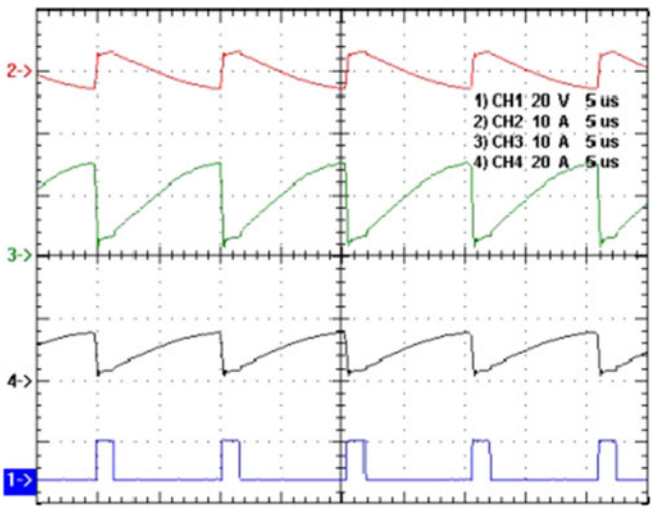

Fig. 23. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 10 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20 A/ div).

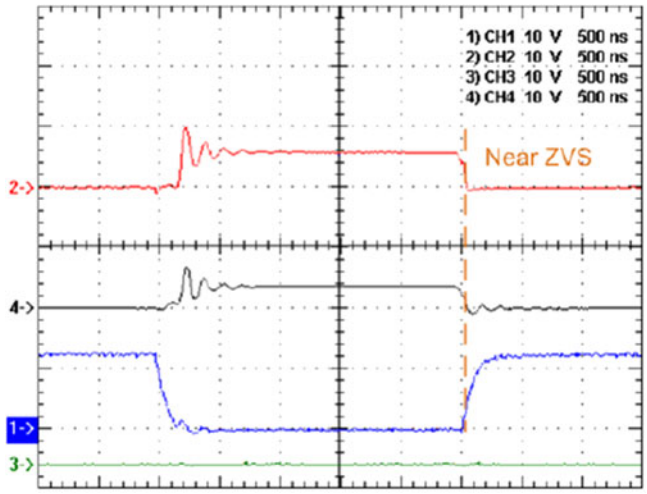

Fig. 24. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of 1 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

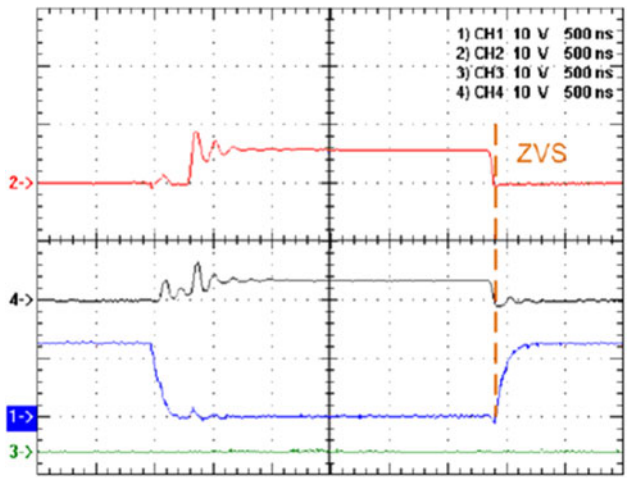

Fig. 25. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of 5 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

ends at $t = t_3$. During this state, N_1 and N_2 are serially connected and the equivalent magnetizing inductance is $[(N_2/N_1)+1]^2 \cdot L_m$. It should be noted that during this state, although the body diode of Q_3 has a positive voltage drop between its anode and cathode, this diode must be turned OFF. This is because the voltage drop is smaller than the forward voltage of the body diode of Q_3. If this voltage drop is larger than the forward voltage of the body diode of Q_3, the coupled inductor will be short-circuited.

4) *State 4* $[t_3, t_4]$*:* As shown in Fig. 10(d), the switches Q_1 and Q_3 keep turned OFF, and the switches Q_2 and Q_4 keep turned ON. The resonating current $i_{\rm lk}$ changes the direction, and is increasing in the opposite direction. C_B discharges the energy to the output via the coupled inductor windings. Thus, i_{N3} continually increases. L_m is still demagnetized. This state ends when Q_2 and Q_4 are turned OFF at $t = t_4$.
5) *State 5* $[t_4, t_5]$*:* As shown in Fig. 10(e), the switches Q_1 and Q_3 keep turned OFF, and the switches Q_2 and Q_4 become turned OFF. During this dead time period, the body diode of Q_1 is forward biased by $i_{\rm lk}$, and the body diode of Q_4 is forward biased due to the coupled inductor freewheeling. Meanwhile, $i_{\rm lk}$, i_{N2} and i_{N3} start to decrease, and L_m is continually demagnetized. This state ends when Q_1 becomes turned on at $t = t_5$.
6) *State 6* $[t_5, t_6]$*:* Before state 6 begins, the body diode of Q_1 is forward biased. Thus, Q_1 is tuned on with ZVS as shown in Fig. 10(f). The resonating current $i_{\rm lk}$ continually decreases, and L_m is continually demagnetized. This state ends when $i_{\rm lk}$ reaches zero at $t = t_6$.
7) *State 7* $[t_6, t_0 + T_s]$*:* As shown in Fig. 10(g), Q_1 still keeps turned ON, but Q_2, Q_3 and Q_4 still keep turned OFF. During this state, $L_{\rm lk}$ and C_B form a series resonant circuit, and $i_{\rm lk}$ increases from zero. i_{N2} and i_{N3}

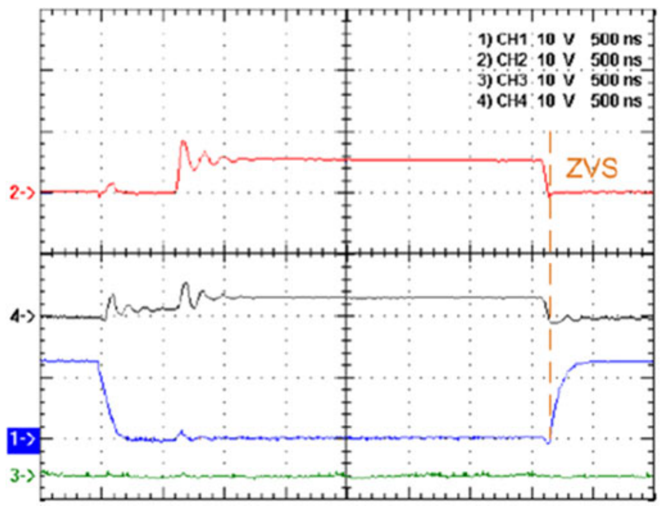

Fig. 26. Waveforms in the low step-down gain mode at input voltage of 18 V and output current of 10 A: (1) v_{gs3} (10 V/ div); (2) v_{ds3} (10 V/ div); (3) v_{gs4} (10 V/ div); and (4) v_{ds4} (10 V/ div).

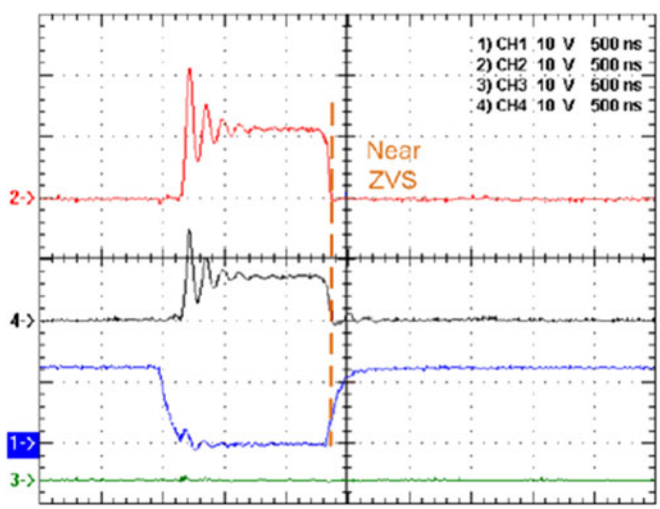

Fig. 27. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 1 A: (1) v_{gs3} (10 V/ div); (2) v_{ds3} (10 V/ div); (3) v_{gs4} (10 V/ div); and (4) v_{ds4} (10 V/ div).

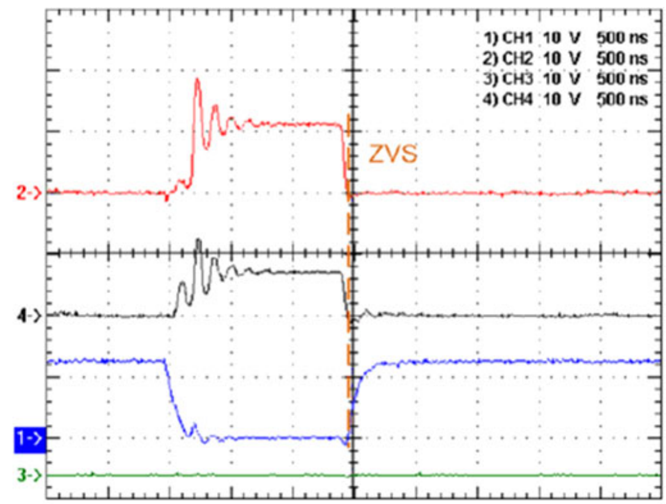

Fig. 28. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 5A: (1) v_{gs3} (10 V/ div); (2) v_{ds3} (10 V/ div); (3) v_{gs4} (10 V/ div); and (4) v_{ds4} (10 V/ div).

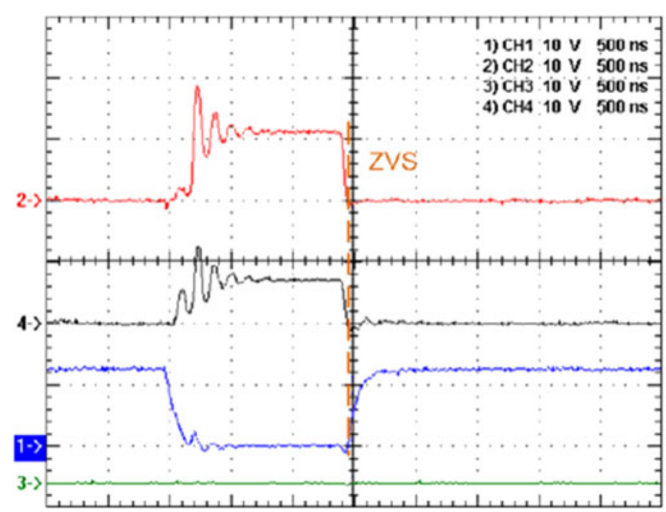

Fig. 29. Waveforms in the low step-down gain mode at input voltage of 36 V and output current of 10 A: (1) v_{gs3} (10 V/ div); (2) v_{ds3} (10 V/ div); (3) v_{gs4} (10 V/ div); and (4) v_{ds4} (10 V/ div).

continually decrease. As soon as i_{lk} is equal to i_{N3}, i_{ds4} falls to zero and this state ends at $t = t_0 + T_s$.

C. Voltage Gain in Low Step-Down Gain Mode

In order to obtain the voltage gain and the voltage across C_B, only states 1 and 3 are considered, and the dead times and the leakage inductance L_{lk} are ignored. From state 1 as shown in Fig. 8(a), v_{Lm} can be found to be

$$v_{\mathrm{Lm}}^{(1)} = (V_{\mathrm{in}} - V_{\mathrm{CB}} - V_o) \cdot \left(\frac{N_1}{N_1 + N_2 + N_3}\right). \quad (1)$$

From state 3 as shown in Fig. 8(c), v_{Lm} can be found to be

$$v_{\mathrm{Lm}}^{(3)} = -V_{\mathrm{CB}} = -V_o \cdot \left(\frac{N_1}{N_2 + N_3}\right). \quad (2)$$

By substituting V_{CB} as shown in (2) into (1), $v_{\mathrm{Lm}}^{(1)}$ can be expressed to be

$$v_{\mathrm{Lm}}^{(1)} = \left(V_{\mathrm{in}} - V_o \cdot \frac{N_1}{N_2 + N_3} - V_o\right) \cdot \left(\frac{N_1}{N_1 + N_2 + N_3}\right). \quad (3)$$

Based on (2) and (3), and by applying the voltage-second balance principle to L_m over one switching period, the following equation can be obtained:

$$D \cdot \left(V_{\mathrm{in}} - V_o \cdot \frac{N_1}{N_2 + N_3} - V_o\right) \cdot \left(\frac{N_1}{N_1 + N_2 + N_3}\right) = (1 - D) \cdot V_o \cdot \left(\frac{N_1}{N_2 + N_3}\right). \quad (4)$$

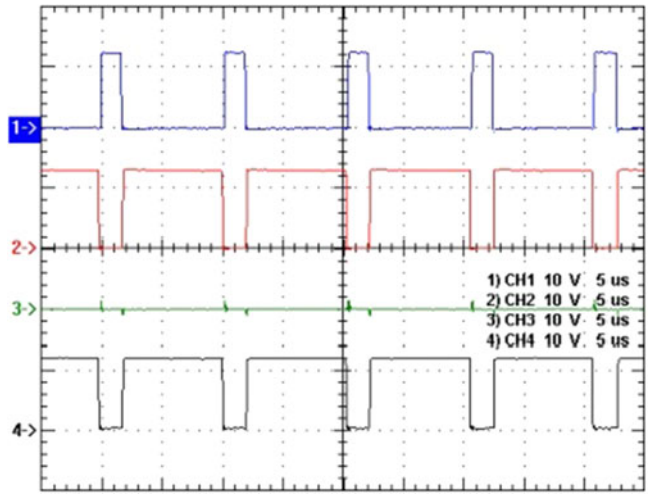

Fig. 30. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 1 A: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm gs2}$ (10 V/ div); (3) $v_{\rm gs3}$ (10 V/ div); and (4) $v_{\rm gs4}$ (10 V/ div).

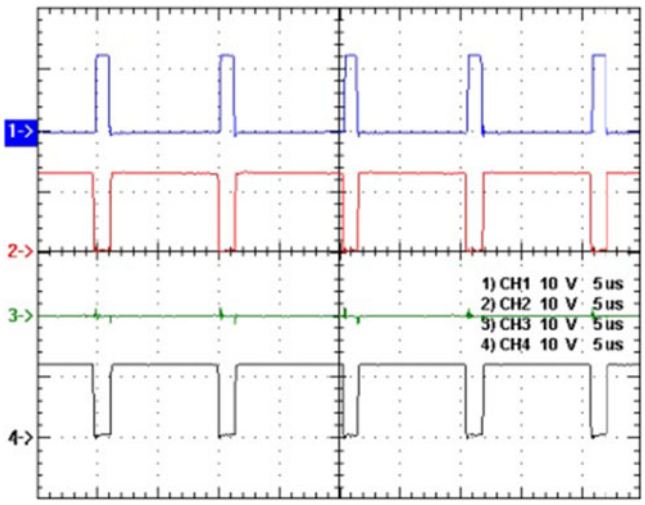

Fig. 32. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 1 A: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm gs2}$ (10 V/ div); (3) $v_{\rm gs3}$ (10 V/ div); and (4) $v_{\rm gs4}$ (10 V/ div).

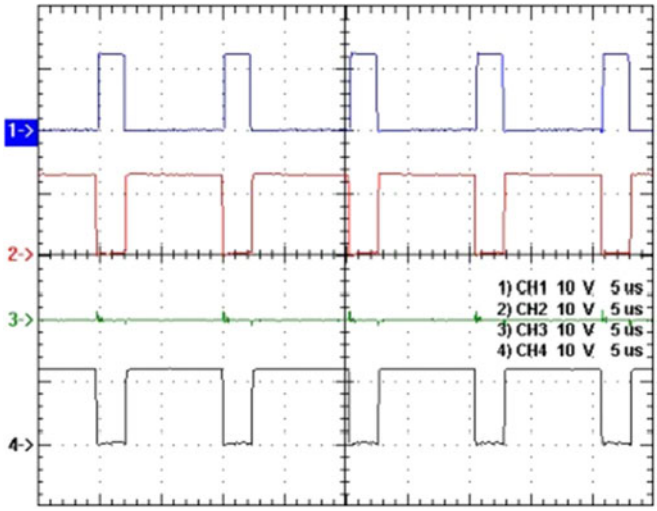

Fig. 31. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 10 A: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm gs2}$ (10 V/ div); (3) $v_{\rm gs3}$ (10 V/ div); and (4) $v_{\rm gs4}$ (10 V/ div).

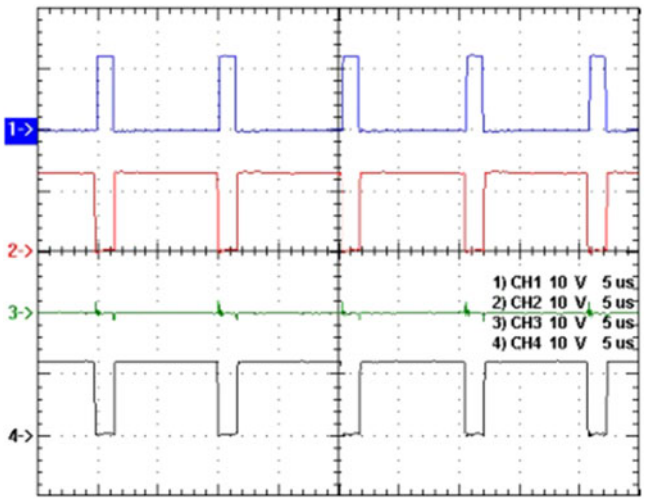

Fig. 33. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 10 A: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm gs2}$ (10 V/ div); (3) $v_{\rm gs3}$ (10 V/ div); and (4) $v_{\rm gs4}$ (10 V/ div).

By rearranging the aforesaid equation, the corresponding voltage gain can be obtained as follows:

$$\frac{V_o}{V_{\rm in}} = D \cdot \left(\frac{N_2 + N_3}{N_1 + N_2 + N_3} \right). \tag{5}$$

D. Voltage Gain in High Step-Down Gain Mode

In order to obtain the voltage gain and the voltage across $C_{\rm B}$, only states 1 and 3 are considered, and the dead times and the leakage inductance $L_{\rm lk}$ are ignored. In Fig. 10(a) and (c), the windings N_1 and N_2 can be combined and the equivalent magnetizing inductance $L_T = [1 + (N_2/N_1)]^2 \cdot L_m$. Thus, the circuits can be redrawn as shown in Fig. 11(a) and (b).

From state 1 as shown in Fig. 11(a), $v_{\rm LT}^{(1)}$ can be found to be

$$v_{\rm LT}^{(1)} = (V_{\rm in} - V_{\rm CB} - V_o) \cdot \left(\frac{N_1 + N_2}{N_1 + N_2 + N_3} \right). \tag{6}$$

From state 3 as shown in Fig. 11(b), $v_{\rm LT}^{(3)}$ can be found to be

$$v_{\rm LT}^{(3)} = -V_{\rm CB} = -V_o \cdot \left(\frac{N_1 + N_2}{N_3} \right). \tag{7}$$

By substituting $V_{\rm CB}$ as shown in (7) into (6), $v_{\rm LT}^{(1)}$ can be expressed to be

$$v_{\rm LT}^{(1)} = \left(V_{\rm in} - V_o \cdot \frac{N_1 + N_2}{N_3} - V_o \right) \cdot \left(\frac{N_1 + N_2}{N_1 + N_2 + N_3} \right). \tag{8}$$

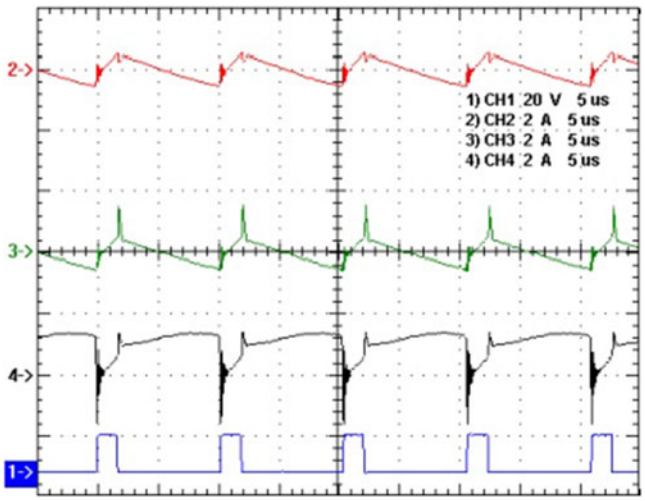

Fig. 34. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 1 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (2 A/ div); (3) i_{N2} (2 A/ div); and (4) i_{N3} (2 A/ div).

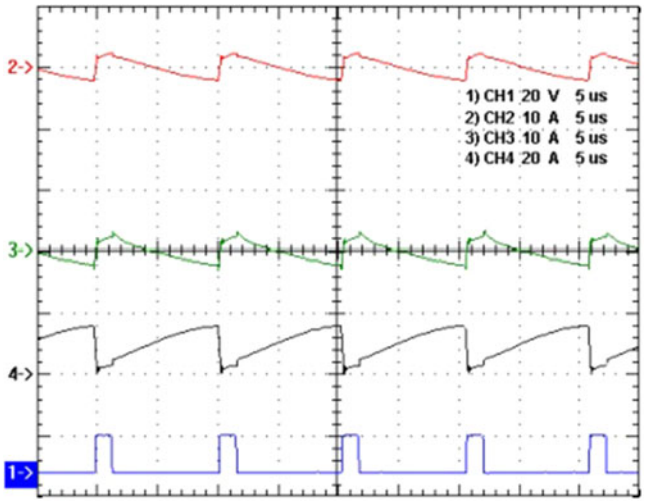

Fig. 36. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 10 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20 A/ div).

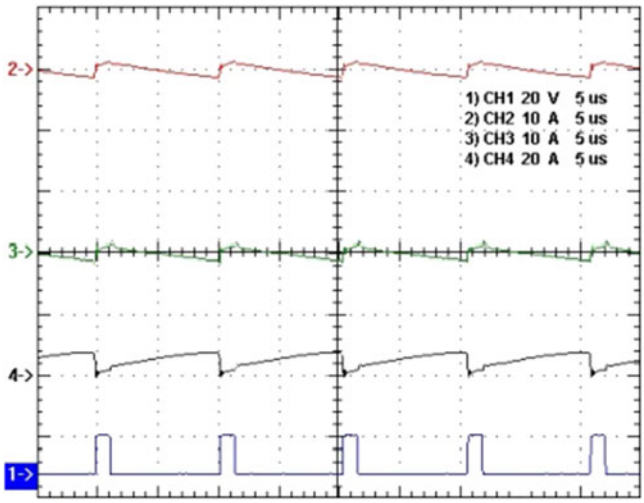

Fig. 35. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 5 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20 A/ div).

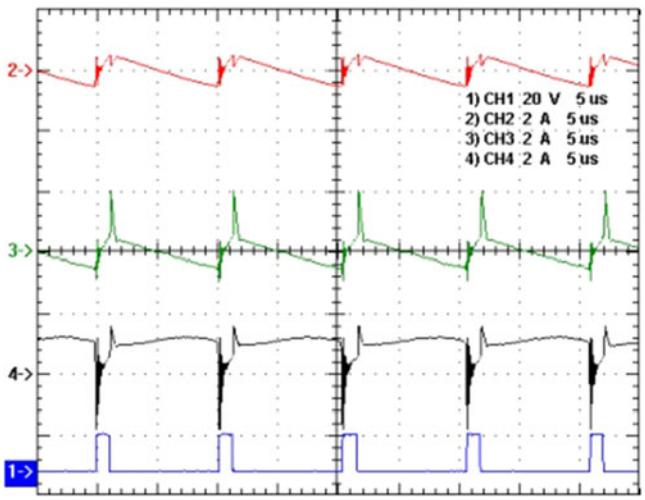

Fig. 37. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 1 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (2 A/ div); (3) i_{N2} (2 A/ div); and (4) i_{N3} (2 A/ div).

Based on (7) and (8), and by applying the voltage-second balance principle to L_T over one switching period, the following equation can be obtained:

$$D\cdot\left(V_{\rm in}-V_o\cdot\frac{N_1+N_2}{N_3}-V_o\right)\cdot\left(\frac{N_1}{N_1+N_2+N_3}\right)=(1-D)\cdot V_o\cdot\left(\frac{N_1+N_2}{N_3}\right). \tag{9}$$

By rearranging the aforesaid equation, the corresponding voltage gain can be obtained as follows:

$$\frac{V_o}{V_{\rm in}}=D\cdot\left(\frac{N_3}{N_1+N_2+N_3}\right). \tag{10}$$

E. Boundary Condition of Magnetizing Inductor in Low Step-Down Gain Mode

The condition for the output inductor L_m operating in positive current region or negative current region is described as follows:

$$\begin{cases}2I_{\rm Lm}\geq\Delta i_{\rm Lm}, & \text{positive\_current\_region}\\ 2I_{\rm Lm}<\Delta i_{\rm Lm}, & \text{negative\_current\_region}\end{cases} \tag{11}$$

where $I_{\rm Lm}$ and $\Delta i_{\rm Lm}$ are the dc component and peak-to-peak value of ac component of $i_{\rm Lm}$, respectively.

In the low step-down gain mode, the magnetizing inductance current of the coupled inductor can be derived as

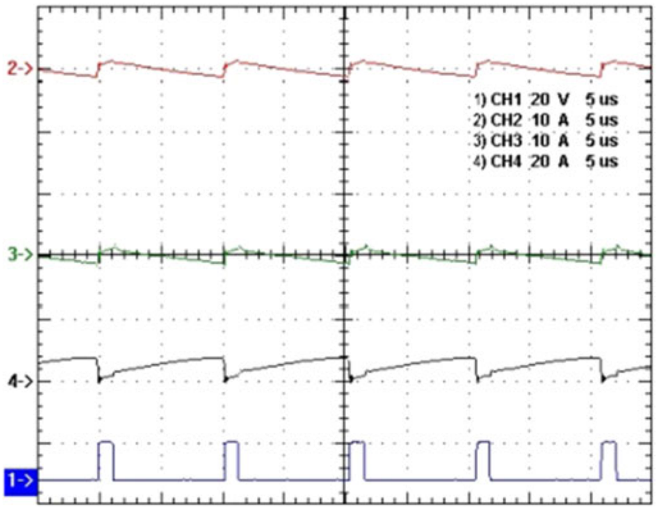

Fig. 38. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 5 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20 A/ div).

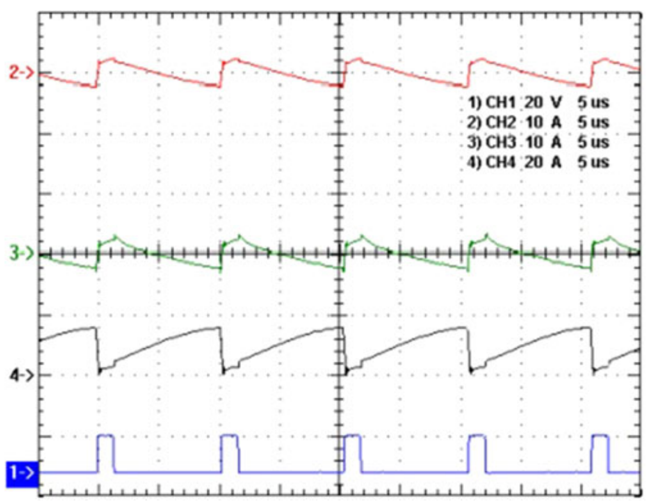

Fig. 39. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 10 A: (1) $v_{\rm gs1}$ (20 V/ div); (2) $i_{\rm lk}$ (10 A/ div); (3) i_{N2} (10 A/ div); and (4) i_{N3} (20 A/ div).

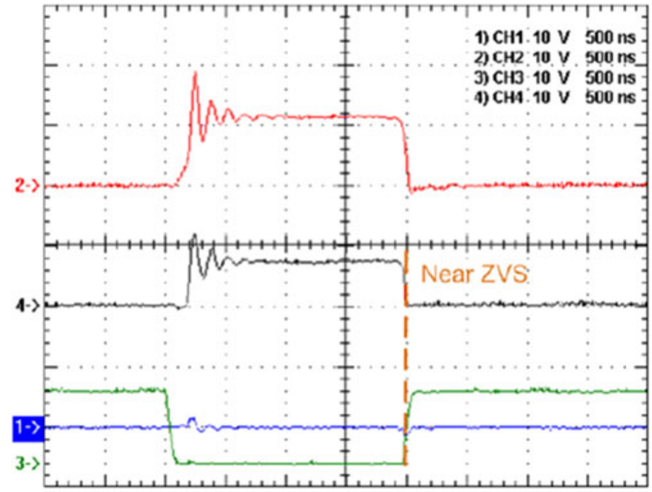

Fig. 40. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 1 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

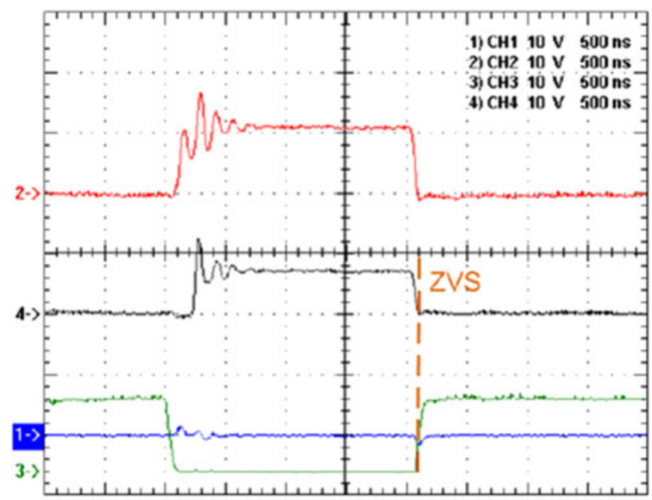

Fig. 41. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 5 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

follows:

$$i_{\rm Lm} = i_{N1} + i_{\rm CB} = \frac{N_2 + N_3}{N_1} \cdot i_{N2} + i_{\rm CB}. \tag{12}$$

According to the ampere-second balance, the average value of the current in C_B is zero. Therefore,

$$\langle i_{\rm Lm} \rangle = \frac{N_2 + N_3}{N_1} \cdot \langle i_{N2} \rangle + \langle i_{\rm CB} \rangle . \tag{13}$$

The above equation can be rewritten as

$$I_{\rm Lm} = \frac{N_2 + N_3}{N_1} \cdot I_{N2} \tag{14}$$

where $\langle i_{\rm Lm} \rangle$ or $I_{\rm Lm}$, and $\langle i_{\rm CB} \rangle$ are the average values of $i_{\rm Lm}$ and $i_{\rm CB}$, respectively.

Since I_{N2} is equal to I_o, (14) can be expressed to be

$$I_{\rm Lm} = \frac{N_2 + N_3}{N_1} \cdot I_o. \tag{15}$$

Replacing I_o with V_o/R_o yields the following equation:

$$I_{\rm Lm} = \frac{N_2 + N_3}{N_1} \cdot \frac{V_o}{R_o}. \tag{16}$$

Also, $\Delta i_{\rm Lm}$ can be expressed in the following:

$$\Delta i_{\rm Lm} = \frac{v_{\rm Lm} \Delta t}{L_m} = \frac{\frac{N_1}{N_2+N_3} \cdot V_o \cdot (1-D)T_s}{L_m}. \tag{17}$$

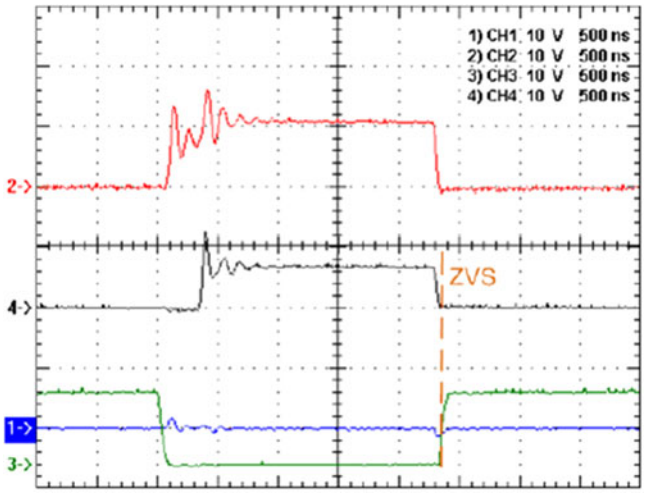

Fig. 42. Waveforms in the high step-down gain mode at input voltage of 36 V and output current of 10 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

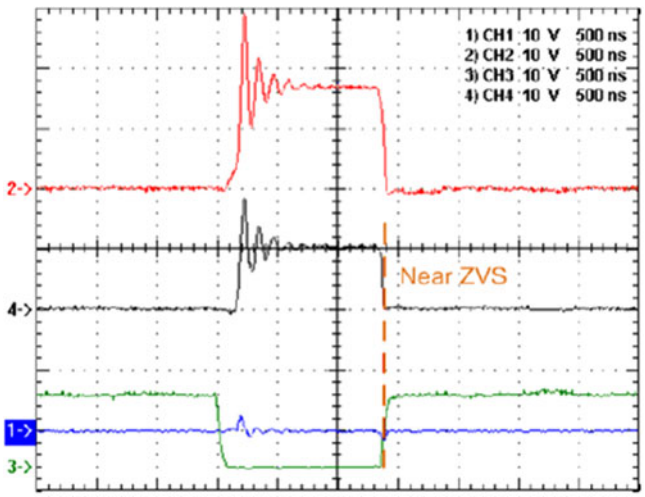

Fig. 43. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 1 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

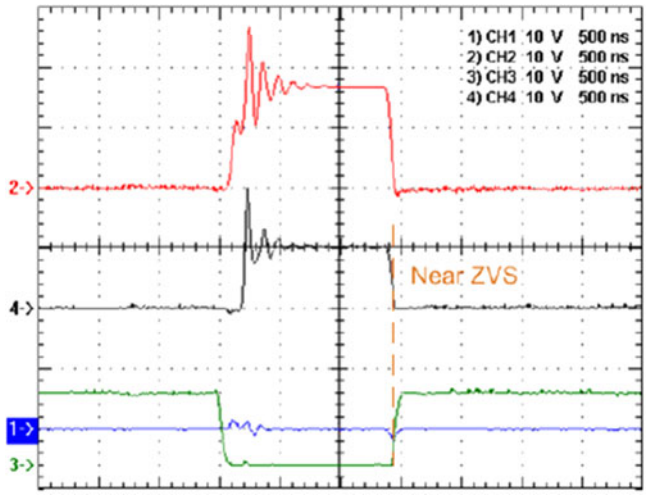

Fig. 44. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 5 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

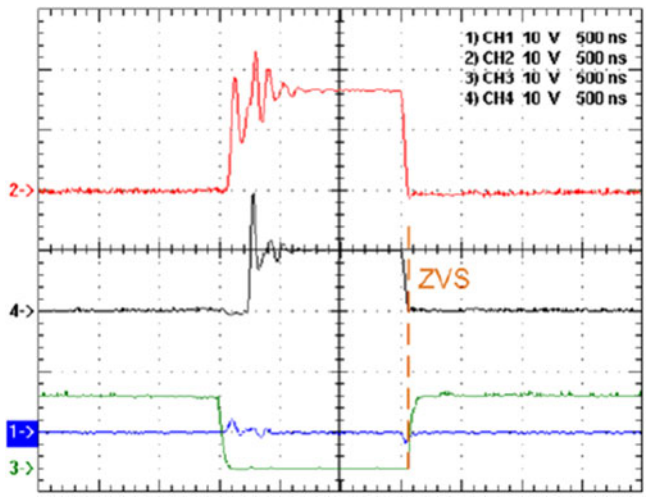

Fig. 45. Waveforms in the high step-down gain mode at input voltage of 54 V and output current of 10 A: (1) $v_{\rm gs3}$ (10 V/ div); (2) $v_{\rm ds3}$ (10 V/ div); (3) $v_{\rm gs4}$ (10 V/ div); and (4) $v_{\rm ds4}$ (10 V/ div).

Therefore, the condition for L_m operating in the positive current region is shown as follows:

$$\begin{aligned} & 2I_{\rm Lm} \geq \Delta i_{\rm Lm} \\ & \Rightarrow 2 \cdot \left(\frac{N_2+N_3}{N_1} \cdot \frac{V_o}{R_o} \right) \geq \frac{\frac{N_1}{N_2+N_3} \cdot V_o \cdot (1-D) T_s}{L_m} \\ & \Rightarrow \frac{2L_m}{R_o T_s} \geq \left(\frac{N_1}{N_2+N_3} \right)^2 (1-D) \\ & \Rightarrow K_1 \geq K_{\rm crit1}(D). \end{aligned} \tag{18}$$

That is to say, in (18), if K_1 is larger than $K_{\rm crit1}(D)$, L_m operates in the positive current region; otherwise, L_m works in the negative current region.

F. Boundary Condition of Magnetizing Inductor in High Step-Down Gain Mode

As shown in Fig. 11, the magnetizing inductance current of the coupled inductor in the high step-down gain mode can be derived as follows:

$$i_{\rm LT} = i_{N1+N2} + i_{\rm CB} = \frac{N_3}{N_1+N_2} \cdot i_{N3} + i_{\rm CB}. \tag{19}$$

According to the ampere-second balance, the average value of the current in C_B is zero. Therefore,

$$\langle i_{\rm LT} \rangle = \frac{N_3}{N_1+N_2} \cdot \langle i_{N3} \rangle + \langle i_{\rm CB} \rangle. \tag{20}$$

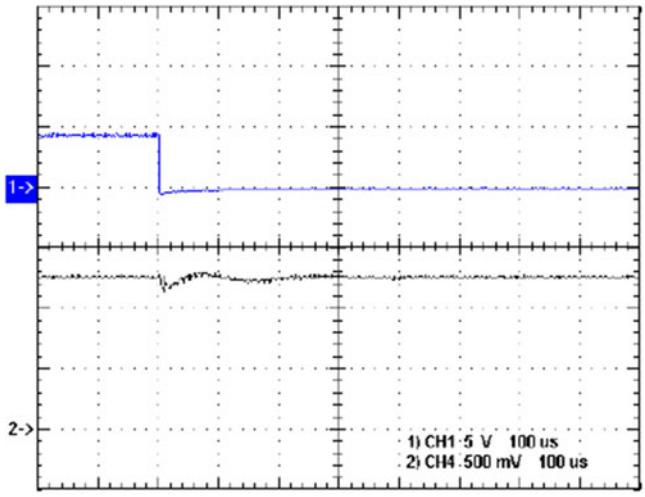

Fig. 46. Mode exchange transient response from low step-down gain to high step-down gain at the input voltage of 36 V and output current of 1 A: (1) Enable (5 V/div) and (2) v_o (500 mV/div).

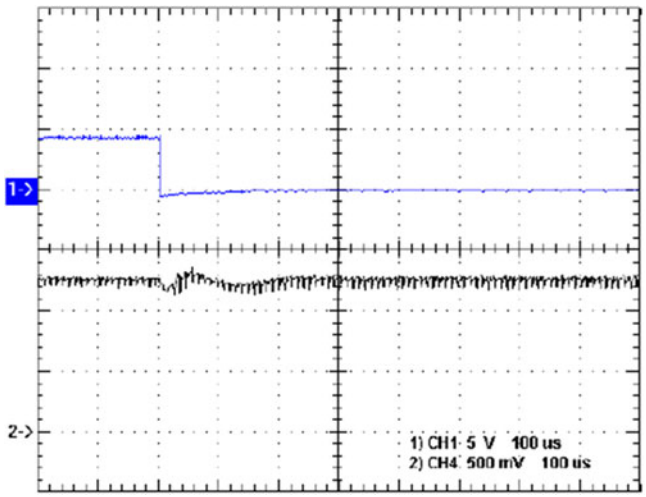

Fig. 47. Mode exchange transient response from low step-down gain to high step-down gain at the input voltage of 36 V and output current of 5 A: (1) Enable (5 V/div) and (2) v_o (500 mV/div).

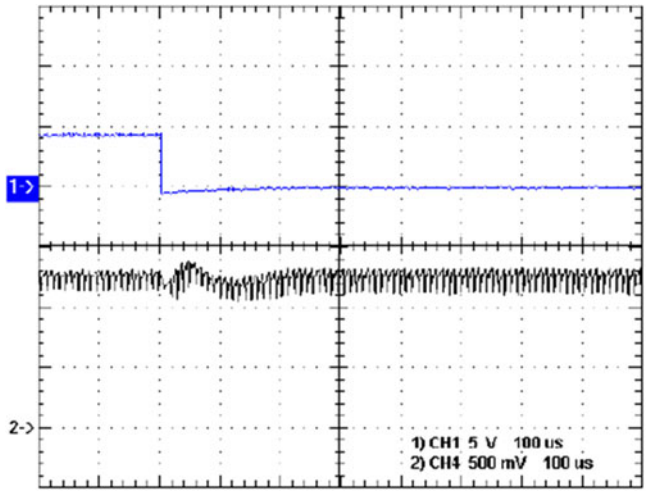

Fig. 48. Mode exchange transient response from low step-down gain to high step-down gain at the input voltage of 36 V and output current of 10 A: (1) Enable (5 V/div) and (2) v_o (500 mV/div).

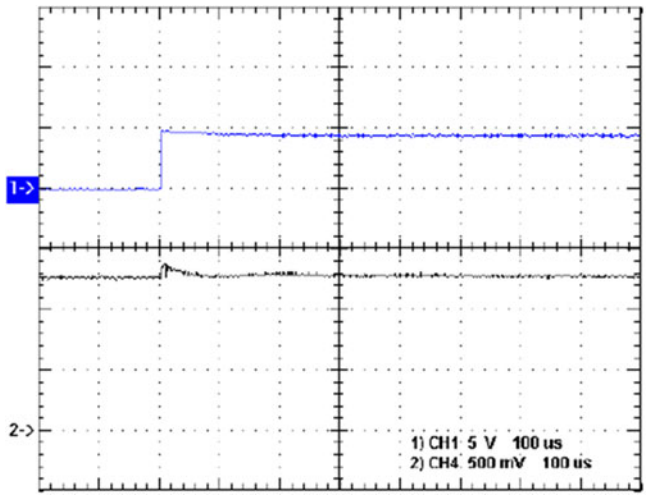

Fig. 49. Mode exchange transient response from high step-down gain to low step-down gain at the input voltage of 36 V and output current of 1 A: (1) Enable (5 V/div) and (2) v_o (500 mV/div).

The aforesaid equation can be rewritten as follows:

$$I_{\mathrm{LT}} = \frac{N_3}{N_1 + N_2} \cdot I_{N3} \tag{21}$$

where $\langle i_{\mathrm{LT}} \rangle$ or I_{LT} is the average values of i_{LT}.

Since I_{N3} is equal to I_o, (21) can be expressed by

$$I_{\mathrm{LT}} = \frac{N_3}{N_1 + N_2} \cdot I_o. \tag{22}$$

Replacing I_o with V_o/R_o yields the following equation:

$$I_{\mathrm{LT}} = \frac{N_3}{N_1 + N_2} \cdot \frac{V_o}{R_o}. \tag{23}$$

Also, Δi_{LT} can be expressed in the following:

$$\Delta i_{\mathrm{LT}} = \frac{v_{\mathrm{LT}} \Delta t}{L_T} = \frac{\frac{N_1+N_2}{N_3} \cdot V_o \cdot (1-D) T_s}{L_T}. \tag{24}$$

Therefore, the condition for L_{T} operating in the positive current region is shown below:

$$\begin{aligned} & 2I_{\mathrm{LT}} \geq \Delta i_{\mathrm{LT}} \\ & \Rightarrow 2 \cdot \left(\frac{N_3}{N_1 + N_2} \cdot \frac{V_o}{R_o} \right) \geq \frac{\frac{N_1+N_2}{N_3} \cdot V_o \cdot (1-D) T_s}{L_T} \\ & \Rightarrow \frac{2L_T}{R_o T_s} \geq \left(\frac{N_1 + N_2}{N_3} \right)^2 (1-D). \end{aligned} \tag{25}$$

Besides, L_T can be expressed by L_m as shown below:

$$\frac{2\left[\left(1 + \frac{N_2}{N_1} \right)^2 \cdot L_m \right]}{R_o T_s} \geq \left(\frac{N_1 + N_2}{N_3} \right)^2 (1-D). \tag{26}$$

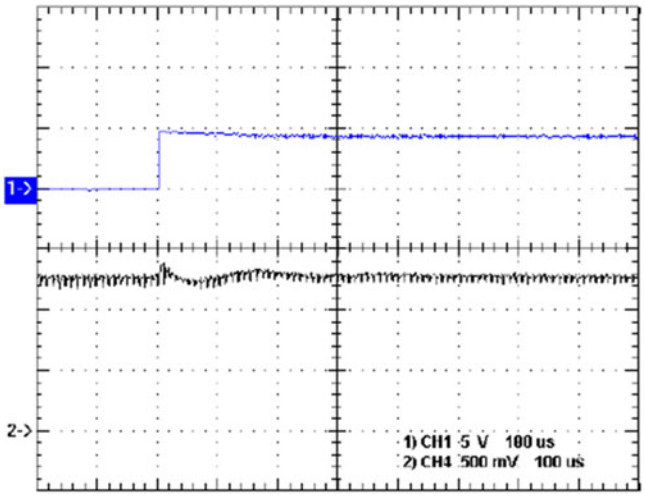

Fig. 50. Mode exchange transient response from high step-down gain to low step-down gain at the input voltage of 36 V and output current of 5 A: (1) Enable (5 V/div) and (2) v_o (500 mV/div).

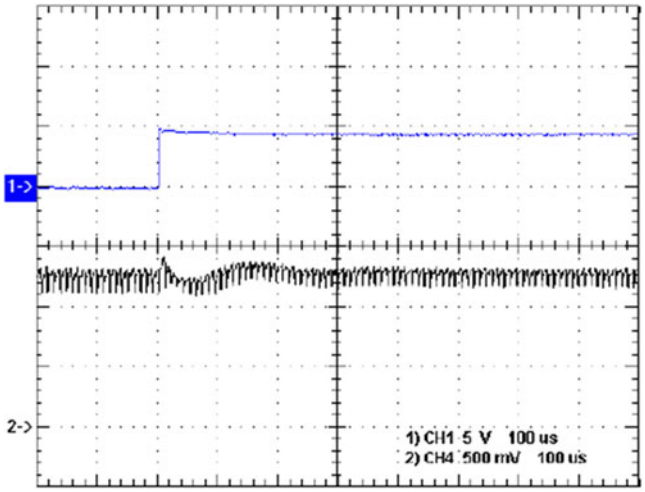

Fig. 51. Mode exchange transient response from high step-down gain to low step-down gain at the input voltage of 36 V and output current of 10 A: (1) Enable (5 V/div) and (2) v_o (500 mV/div).

Rearranging (26) yields the following equation:

$$\frac{2L_m}{R_o T_s} \geq \left(\frac{N_1}{N_3}\right)^2 (1-D) \Rightarrow K_2 \geq K_{\mathrm{crit2}}(D). \qquad (27)$$

That is to say, in (27), if K_2 is larger than $K_{\mathrm{crit2}}(D)$, L_m operates in the positive current region; otherwise, L_m works in the negative current region.

IV. Design Considerations

To verify the effectiveness of the proposed converter, a prototype has been built up and tested. Table I shows the specifications of the proposed converter, whereas Table II shows the components used in the proposed converter. Moreover, the design procedures of the mode switching point, the coupled inductor, and the active switches are shown as follows.

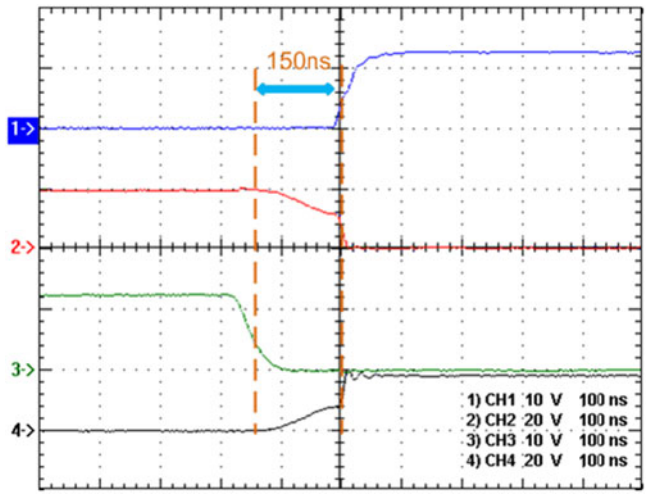

Fig. 52. Waveforms in the low step-down gain mode under the input voltage of 18 V and 10% of rated load: (1) v_{gs1} (10 V/ div); (2) v_{ds1} (20 V/ div); (3) v_{gs2} (10 V/ div); and (4) v_{ds2} (20 V/ div).

A. Determination of Mode Switching Point

Fig. 12 shows the experimental results of the proposed converter under a wide input voltage range and the output voltage of 1.2 V. From Fig. 12(a), it can be seen that at the input voltage of 54 V and the output current of 10A, the efficiency of the high step-down mode is higher than that of the low step-down mode by about 1.15%; at the input voltage of 54 V and the output current of 1 A, the efficiency of the high step-down mode is higher than that of the low step-down mode by about 8.6%. On the other hand, from Fig. 12(a), it can be seen that when the input voltage is decreased to 24 V, at the output current of 10 A, the efficiency of the low step-down mode is higher than that of the high step-down mode by about 5.4%.

Fig. 12(b) shows the actual duty cycle under different input voltages and output currents. In the low step-down gain mode, at the input voltage of 18 V, the duty cycle from 1 to 10 A locates between 20% and 35%. It is noted that for the proposed converter, the most energy is transferred to the output load during the off-state period. Hence, if the duty cycle is too large, the proposed converter would tend to be unstable.

From Fig. 12(a), it can be seen that a good mode switching point would be located at the input voltage of about 34 V. For design convenience, the mode switching point is set at 36 V. That is, if the input voltage is larger than 36 V, the proposed converter is operated in the high step-down gain mode; if the input voltage is lower than 36 V, the proposed converter is operated in the low step-down gain mode.

In this paper, two concerns are to be raised when the mode switching point is set at 36 V. First, the conventional brick converters have an input voltage range from 18 to 36 V or from 36 to 72 V, which is a typical requirement of the dc bus in the datacenter or telecom power system with input voltage range ratio of 2:1. Second, even though 36 V is not the best efficiency

point, using this voltage as mode switching point will make turns designed easily for the proposed converter with input voltage range from 18 to 54 V, namely input voltage range ratio of 3:1. This is because 36 V is a multiple of 3 or 2 and, hence, the turns ratio is integral.

B. Determination of Turns Ratio

In the proposed converter, the voltage gain contains the parameters of duty cycle and turns ratio. Therefore, in design, the tradeoff between turns ratio and duty cycle should be taken into consideration.

As seen in Table I, the input voltage is from 18 to 54 V. Also, from Section IV-A, if the input voltage is located between 18 and 36 V, the proposed converter is operated in the low step-down gain mode; if the input voltage is located between 36 and 54 V, the proposed converter is operated in the high step-down gain mode. In addition, the actual duty cycle of the proposed converter is desired to be higher than 10%. Therefore, in the low step-down gain mode, when the input voltage is 36 V, the proposed converter has the smallest duty cycle. Thus, the turns ratio can be obtained based on (5):

$$\frac{1.2}{36} = 0.1 \cdot \left(\frac{N_2 + N_3}{N_1 + N_2 + N_3} \right). \tag{28}$$

From (28), the turns ratio can be obtained:

$$N_1 : (N_2 + N_3) = 2 : 1. \tag{29}$$

In the high step-down gain mode, when the input voltage is 54 V, the proposed converter has the smallest duty cycle. Thus, the turns ratio can be obtained based on (10):

$$\frac{1.2}{54} = 0.1 \cdot \left(\frac{N_3}{N_1 + N_2 + N_3} \right). \tag{30}$$

From (30), the turns ratio can be obtained to be

$$(N_1 + N_2) : N_3 = 3.5 : 1. \tag{31}$$

According to (29) and (31), the following relationship can be obtained:

$$\begin{cases} N_1 = 2(N_2 + N_3) \\ N_1 + N_2 = 3.5 N_3 \end{cases}. \tag{32}$$

Based on (32), the turns ratio for the proposed converter can be obtained to be

$$N_1 : N_2 : N_3 = 6 : 1 : 2. \tag{33}$$

C. Design of Coupled Inductor

To make sure that the magnetizing current i_{Lm} is always located in the positive current region, the required magnetizing inductance L_m can be obtained as follows.

In the low step-down gain mode, the minimum value of L_m can be obtained:

$$\begin{aligned} L_m > \frac{v_{\mathrm{Lm}} \Delta t}{\Delta i_{\mathrm{Lm}}} &= \frac{\left(\frac{N_1}{N_2+N_3}\right) \cdot V_o \cdot (1-D) T_s}{2 \cdot I_{Lm,\min}} \\ &= \frac{\left(\frac{N_1}{N_2+N_3}\right) \cdot V_o \cdot (1-D) T_s}{2 \cdot \left[\left(\frac{N_2+N_3}{N_1}\right) \cdot I_{o,\min}\right]} \\ &= \frac{\left(\frac{N_1}{N_2+N_3}\right)^2 \cdot V_o \cdot (1-D) T_s}{2 \cdot I_{o,\min}} \\ &= \frac{\left(\frac{6}{3}\right)^2 \times 1.2 \times (1-0.1) \times 10\mu}{2 \times 1} \\ &= 21.6\,\mu\mathrm{H} \end{aligned} \tag{34}$$

Also, in the high step-down gain mode, the minimum value of L_m can be obtained:

$$\begin{aligned} L_m > \frac{v_{\mathrm{Lm}} \Delta t}{\Delta i_{\mathrm{Lm}}} &= \frac{\left(\frac{N_1}{N_3}\right) \cdot V_o \cdot (1-D) T_s}{2 \cdot I_{Lm,\min}} \\ &= \frac{\left(\frac{N_1}{N_3}\right) \cdot V_o \cdot (1-D) T_s}{2 \cdot \left[\left(\frac{N_3}{N_1}\right) \cdot I_{o,\min}\right]} \\ &= \frac{\left(\frac{N_1}{N_3}\right)^2 \cdot V_o \cdot (1-D) T_s}{2 \cdot I_{o,\min}} \\ &= \frac{\left(\frac{6}{2}\right)^2 \times 1.2 \times (1-0.1) \times 10\,\mu}{2 \times 1} \\ &= 48.6\,\mu\mathrm{H}. \end{aligned} \tag{35}$$

To make sure that i_{Lm} is always located in the positive current region, the value of L_m should be selected to be larger than 48.6 μH as shown in (35). Finally, the value of L_m in the proposed converter is designed and measured to be 60 μH. As for the value of the leakage inductance L_{lk}, it is obtained by measurement, and this can be seen in Appendix C.

D. Selection of Switches

In the high step-down gain mode, states 3 and 4 shown in Fig. 10(c) and (d), which are the turn-on period of Q_4, are redrawn in Fig. 13(a); states 5, 6 and 7 shown in Fig. 10(e), (f) and (g), which are the turn-on period of the body diode of Q_4, are redrawn in Fig. 13(b). In these states, the body diode of Q_3 must not be forward-biased to prevent the coupled inductor from being short-circuited. Accordingly, the voltage across Q_3, v_{ds3}, should be smaller than the forward voltage of the body diode of Q_3, V_{Df3}. Therefore, v_{ds3} in these two cases can be obtained as follows.

In Fig. 13(a), v_{ds3} can be expressed:

$$v_{\mathrm{ds3}} = -(v_{N2} + v_{\mathrm{ds4}}) = -\left[\frac{N_2}{N_3}(v_{\mathrm{ds4}} - V_o) + v_{\mathrm{ds4}}\right]. \tag{36}$$

In the turn-on state of Q_4, $v_{\rm ds4}$ can be expressed:

$$v_{\rm ds4} = -i_{\rm ds4} \cdot R_{\rm ds4} \tag{37}$$

where $R_{\rm ds4}$ is the turn-on resistance of Q_4.

Substituting (37) into (36) yields the following equation:

$$v_{\rm ds3} = -\left[\frac{N_2}{N_3}(-i_{\rm ds4} \cdot R_{\rm ds4} - V_o) + (-i_{\rm ds4} \cdot R_{\rm ds4})\right]. \tag{38}$$

By rearranging the aforesaid equation, the following equation can be obtained:

$$v_{\rm ds3} = (i_{\rm ds4} \cdot R_{\rm ds4})\left(1 + \frac{N_2}{N_3}\right) + \frac{N_2}{N_3} \cdot V_o. \tag{39}$$

To prevent the body diode from being forward biased, the following condition can be obtained:

$$v_{\rm ds3} \le V_{Df,3}. \tag{40}$$

Therefore, based on (39) and (40), the following criterion can be obtained:

$$(i_{\rm ds4} \cdot R_{\rm ds4})\left(1 + \frac{N_2}{N_3}\right) + \frac{N_2}{N_3} \cdot V_o \le V_{Df,3}. \tag{41}$$

Similarly, in states 5, 6, and 7 in the high step-down gain mode, the body diode of Q_4 is forward biased as shown in Fig. 13(b). Thus, the other inequality can be expressed to be

$$V_{Df,4} \cdot \left(1 + \frac{N_2}{N_3}\right) + \frac{N_2}{N_3} \cdot V_o \le V_{Df,3} \tag{42}$$

where $V_{Df,4}$ is the body diode forward voltage of Q_4.

From (41) and (42), it can be seen that one can choose a MOSFET with relatively small turn-on resistance of Q_4 and relatively low forward voltage of the body diode of Q_4, and a MOSFET with a relatively high forward voltage of the body diode of Q_3. It is noted that the selection conditions of Q_4 will be described from (44) to (47). Therefore, a MOSFET with turn-on resistance of 1.2 $m\Omega$ and body diode forward voltage of 0.56 V is chosen for Q_4. Since $V_{Df,4}$ is usually much larger than $i_{\rm ds4} \cdot R_{\rm ds4}$, (42) is used to choose the minimum forward voltage of the body diode of Q_3.

Based on (42), and the values of N_2/N_3, $V_{Df,4}$ and V_o, the following inequality can be obtained:

$$(0.56).\left(1 + \frac{1}{2}\right) + \frac{1}{2}.(1.2) = 1.44 \le V_{Df,3}. \tag{43}$$

Based on (43), two AON6512 MOSFETs, with body diode forward voltage of 0.87 V and turn-on resistance of 1.4 $m\Omega$, are serially connected for Q_3. Thus, the total forward voltage is 1.74 V, which is higher than 1.44 V as calculated in (43), and the total turn-on resistance is 2.8 mΩ. The body diode voltage usually possesses a negative temperature coefficient. Thus, a high forward voltage of Q_3 is necessary.

In the low step-down gain mode, state 2 is the dead time period, and v_{N2} and v_{N3} are negative values. The body diode of Q_4 must not be forward-biased. To prevent the body diode of Q_4 from being forward-biased, the required body diode voltage of Q_4 is calculated as follows:

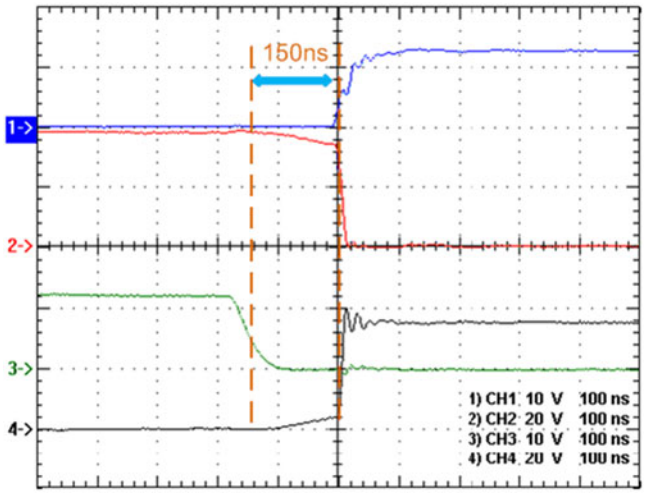

Fig. 53. Waveforms in the low step-down gain mode under the input voltage of 36 V and 10% of rated load: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm ds1}$ (20 V/ div); (3) $v_{\rm gs2}$ (10 V/ div); and (4) $v_{\rm ds2}$ (20 V/ div).

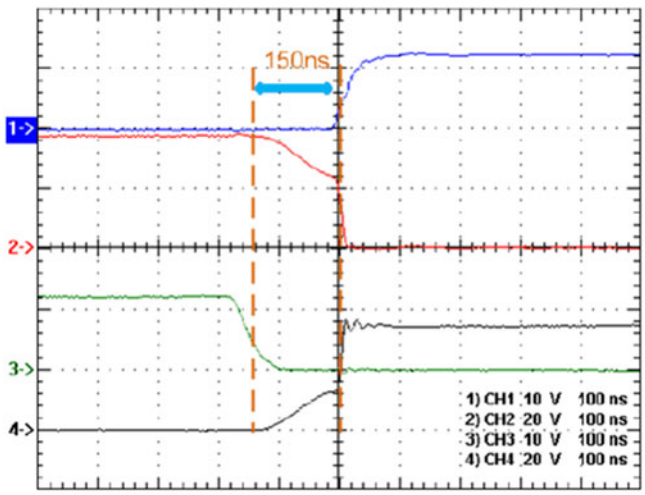

Fig. 54. Waveforms in the high step-down gain mode under the input voltage of 36 V and 10% of rated load: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm ds1}$ (20 V/ div); (3) $v_{\rm gs2}$ (10 V/ div); and (4) $v_{\rm ds2}$ (20 V/ div).

According to Fig. 8(b), the associated equations are

$$v_{N2} + v_{N3} = -(V_o + v_{\rm ds3}) = -(V_o + V_{Df,3}) \tag{44}$$

$$\begin{aligned} v_{\rm ds4} &= -(v_{N2} + v_{\rm ds3}) = -v_{N2} - V_{Df,3} \\ &= (V_o + V_{Df,3}) \times \frac{N_2}{N_2 + N_3} - V_{Df,3} \end{aligned} \tag{45}$$

where V_{Df3} is the forward voltage of the body diode of Q_3.

Therefore, by substituting the values of V_o and turns, and the specifications of Q_3 into (45), the voltage on Q_4, $v_{\rm ds4}$, can be obtained to be

$$\begin{aligned} v_{\rm ds4} &= (V_o + V_{Df,3}) \times \frac{N_2}{N_2 + N_3} - V_{Df,3} \\ &= (1.2 + 1.44) \times \frac{1}{3} - 1.44 = -0.56V. \end{aligned} \tag{46}$$

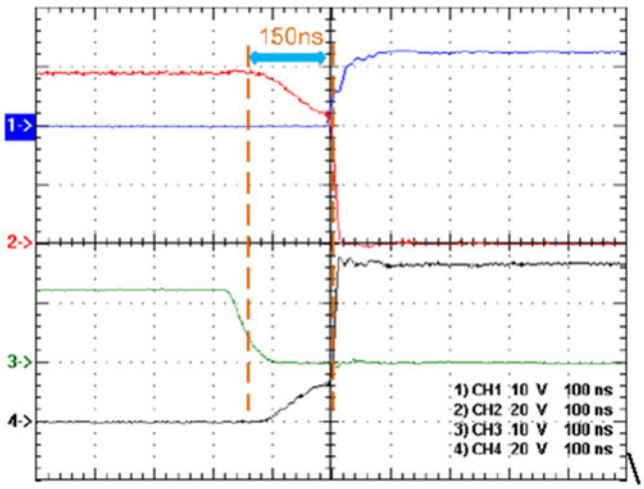

Fig. 55. Waveforms in the high step-down gain mode under the input voltage of 54 V and 10% of rated load: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm ds1}$ (20 V/ div); (3) $v_{\rm gs2}$ (10 V/ div); and (4) $v_{\rm ds2}$ (20 V/ div).

If the body diode of Q_4 is not conducted, then based on the specifications of Q_4, the following criterion must be hold:

$$v_{\rm ds4} \geq -V_{Df,4} = -0.56V \tag{47}$$

where V_{Df4} is the forward voltage of the body diode of Q_4.

In the low step-down gain mode, the voltages across the four switches Q_1, Q_2, Q_3, and Q_4 are calculated as follows:

$$V_{\rm ds1} = V_{\rm ds2} = V_{\rm in} = 36 \text{ V} \tag{48}$$

$$\begin{aligned} V_{\rm ds3} &= V_o + (V_{\rm in} - V_{\rm CB} - V_o) \cdot \left(\frac{N_2+N_3}{N_1+N_2+N_3}\right) \\ &= V_o + \left[V_{\rm in} - V_o \cdot \left(\frac{N_1}{N_2+N_3}\right) - V_o\right] \cdot \left(\frac{N_2+N_3}{N_1+N_2+N_3}\right) \\ &= 1.2 + \left[36 - 1.2 \cdot \left(\frac{6}{1+2}\right) - 1.2\right] \cdot \left(\frac{1+2}{6+1+2}\right) \\ &= 12 \text{ V} \end{aligned} \tag{49}$$

$$\begin{aligned} V_{\rm ds4} &= V_o + (V_{\rm in} - V_{\rm CB} - V_o) \cdot \left(\frac{N_3}{N_1+N_2+N_3}\right) \\ &= V_o + \left[V_{\rm in} - V_o \cdot \left(\frac{N_1}{N_2+N_3}\right) - V_o\right] \cdot \left(\frac{N_3}{N_1+N_2+N_3}\right) \\ &= 1.2 + \left[36 - 1.2 \cdot \left(\frac{6}{1+2}\right) - 1.2\right] \cdot \left(\frac{2}{6+1+2}\right) \\ &= 8.4 \text{ V}. \end{aligned} \tag{50}$$

In the high step-down gain mode, the voltages across the four switches Q_1, Q_2, Q_3, and Q_4 are calculated as following:

$$V_{\rm ds1} = V_{\rm ds2} = V_{\rm in} = 54 \text{ V} \tag{51}$$

$$\begin{aligned} V_{\rm ds3} &= V_o + (V_{\rm in} - V_{\rm CB} - V_o) \cdot \left(\frac{N_2+N_3}{N_1+N_2+N_3}\right) \\ &= V_o + \left[V_{\rm in} - V_o \cdot \left(\frac{N_1+N_2}{N_3}\right) - V_o\right] \cdot \left(\frac{N_2+N_3}{N_1+N_2+N_3}\right) \\ &= 1.2 + \left[54 - 1.2 \cdot \left(\frac{6+1}{2}\right) - 1.2\right] \cdot \left(\frac{1+2}{6+1+2}\right) \\ &= 17.4 \text{ V} \end{aligned} \tag{52}$$

$$\begin{aligned} V_{\rm ds4} &= V_o + (V_{\rm in} - V_{\rm CB} - V_o) \cdot \left(\frac{N_3}{N_1+N_2+N_3}\right) \\ &= V_o + \left[V_{\rm in} - V_o \cdot \left(\frac{N_1+N_2}{N_3}\right) - V_o\right] \cdot \left(\frac{N_3}{N_1+N_2+N_3}\right) \\ &= 1.2 + \left[54 - 1.2 \cdot \left(\frac{6+1}{2}\right) - 1.2\right] \cdot \left(\frac{2}{6+1+2}\right) \\ &= 12 \text{ V}. \end{aligned} \tag{53}$$

From (48) to (53), it can be seen that the voltage ratings of the MOSFETs should be determined based on the calculated values in the high step-down gain mode as shown in (51) to (53). Accordingly, two AON6248 MOSFETs with drain-source voltage rating of 60 V are selected for Q_1 and Q_2. Obviously, the switches Q_3 and Q_4 will be affected by the voltage spikes. Therefore, based on the previous discussion and the voltage stress calculation in (52), two AON6512 MOSFETs with drain-source voltage rating of 30 V are selected for Q_3. Thus, Q_3 has a voltage rating of 60 V ($= 30 \text{ V} \times 2$). Also, based on the voltage stress calculation in (53), one BSC014NE2LSI MOSFET with drain-source voltage rating of 25 V is selected for Q_4. The forward voltages of the body diodes of Q_1 and Q_2 should be as small as possible. However, the selection of the body diodes of Q_3 and Q_4 should be based on (43) and (47), respectively. With a high body diode forward voltage, the current passing through the body diode will lead to a high loss. Thus, the dead time should be well controlled. The dead time should be minimized as short as possible to reduce the currents passing through body diode.

V. Experimental Results

In this section, the associated waveforms are measured to verify the effectiveness of the proposed converter.

A. Measurements in Low Step-Down Gain Mode

Figs. 14–29 show the waveforms in the low step-down gain mode. Figs. 14 and 15 show the gate driving signals $v_{\rm gs1}$, $v_{\rm gs2}$, $v_{\rm gs3}$ and $v_{\rm gs4}$ at the input voltage of 18 V under the output currents of 1 and 10 A, respectively. Figs. 16 and 17 show the gate driving signals $v_{\rm gs1}$, $v_{\rm gs2}$, $v_{\rm gs3}$ and $v_{\rm gs4}$ at the input voltage of 36 V under the output currents of 1 and 10 A, respectively. Figs. 18–20 show the winding currents

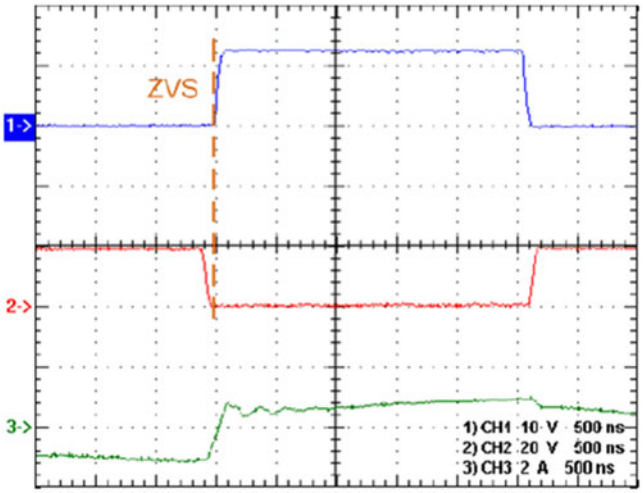

Fig. 56. Waveforms related to Q_1 in the low step-down gain mode under the input voltage of 18 V and 26% of rated load: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm ds1}$ (20 V/ div); and (3) $i_{\rm lk}$ (2 A/ div).

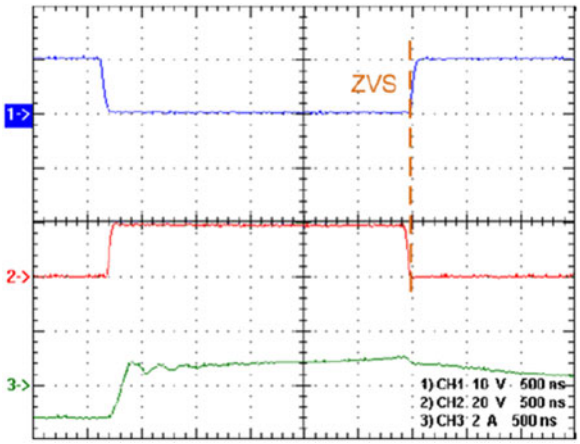

Fig. 57. Waveforms related to Q_2 in the low step-down gain mode under the input voltage of 18 V and 28% of rated load: (1) $v_{\rm gs2}$ (10 V/ div); (2) $v_{\rm ds2}$ (20 V/ div); (3) $i_{\rm lk}$ (2 A/ div).

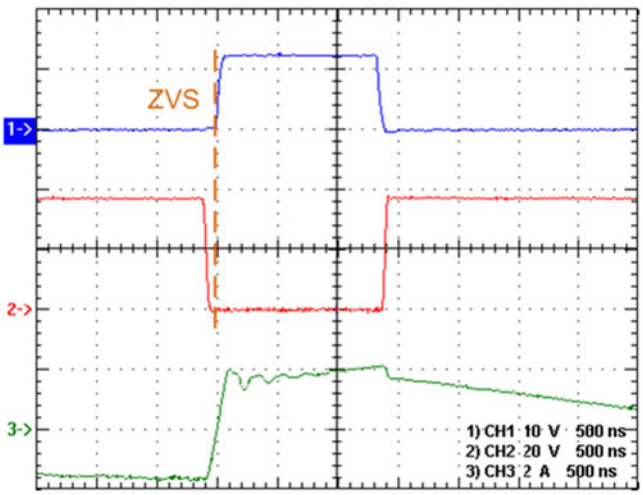

Fig. 58. Waveforms related to Q_1 in the low step-down gain mode under the input voltage of 36 V and 60% of rated load: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm ds1}$ (20 V/ div); and (3) $i_{\rm lk}$ (2 A/ div).

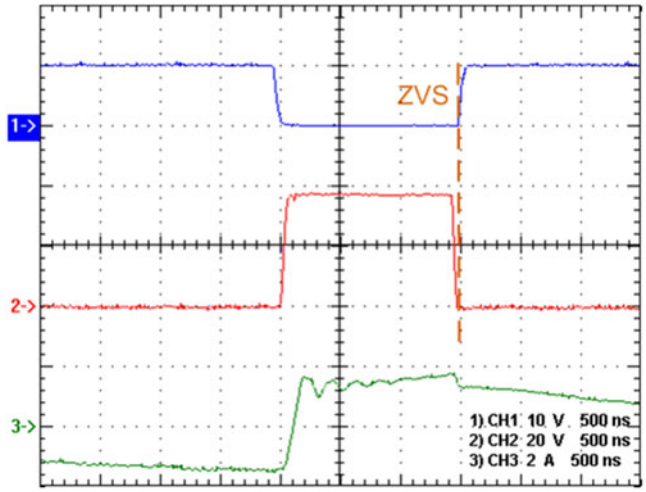

Fig. 59. Waveforms related to Q_2 in the low step-down gain mode under the input voltage of 36 V and 50% of rated load: (1) $v_{\rm gs2}$ (10 V/ div); (2) $v_{\rm ds2}$ (20 V/ div); and (3) $i_{\rm lk}$ (2 A/ div).

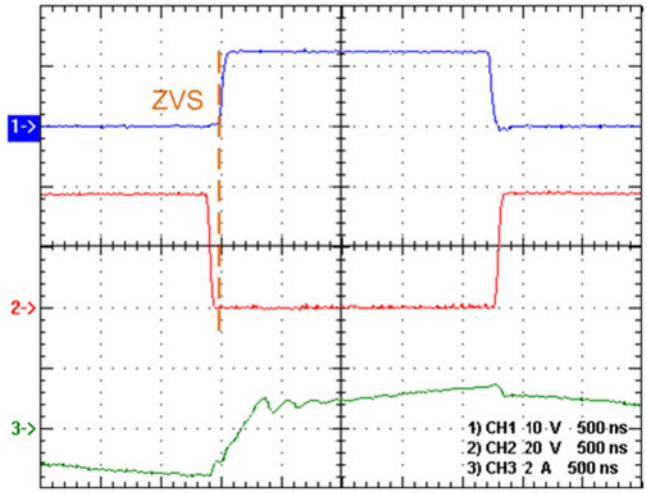

Fig. 60. Waveforms related to Q_1 in the high step-down gain mode under the input voltage of 36 V and 50% of rated load: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm ds1}$ (20 V/ div); and (3) $i_{\rm lk}$ (2 A/ div).

$i_{\rm lk}$, i_{N2} and i_{N3} at the input voltage of 18 V under the output currents of 1, 5, and 10 A, respectively. Figs. 21–23 show the winding currents $i_{\rm lk}$, i_{N2} and i_{N3} at the input voltage of 36 V under the output currents of 1, 5, and 10 A, respectively. Figs. 24–26 show the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$ at the input voltage of 18 V under the output currents of 1, 5, and 10 A, respectively. Figs. 27–29 show the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$ at the input voltage of 36 V under the output currents of 1, 5, and 10 A, respectively. From Figs. 14 and 15, it can be seen that the actual duty cycles for Q_1 under the output currents of 1 and 10 A are 0.22 and 0.33, respectively. The ideal duty cycle for Q_1 is 0.2 so the higher the load current is, the more the actual duty cycle deviates from the ideal duty cycle due to the output voltage being controlled at 1.2 V. From Figs. 16 and 17, it can be seen that the actual duty cycles for Q_1 under the output currents of 1 and 10 A are 0.12 and 0.14, respectively. The ideal duty

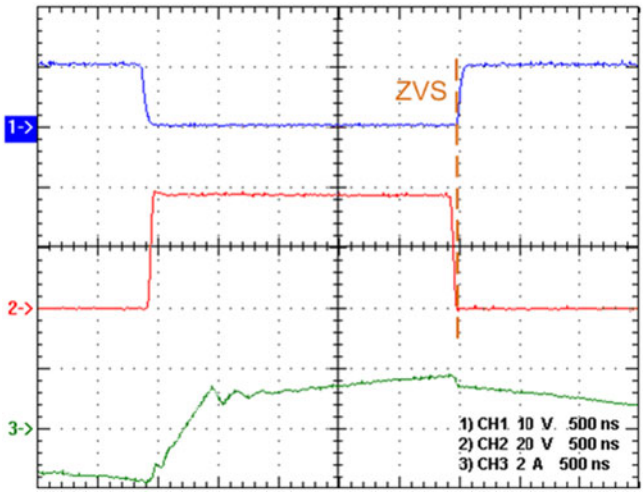

Fig. 61. Waveforms related to Q_2 in the high step-down gain mode under the input voltage of 36 V and 60% of rated load: (1) $v_{\rm gs2}$ (10 V/ div); (2) $v_{\rm ds2}$ (20 V/ div); and (3) $i_{\rm lk}$ (2 A/ div).

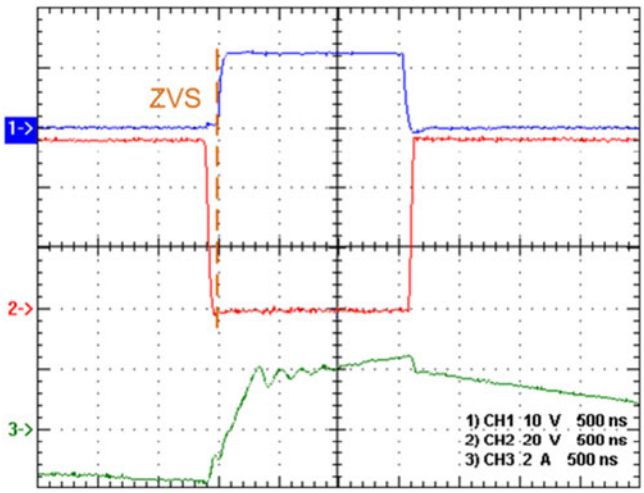

Fig. 62. Waveforms related to Q_1 in the high step-down gain mode under the input voltage of 54 V and 85% of rated load: (1) $v_{\rm gs1}$ (10 V/ div); (2) $v_{\rm ds1}$ (20 V/ div); and (3) $i_{\rm lk}$ (2 A/ div).

cycle for Q_1 is 0.1. From Figs. 18 to 23, it can be seen that when Q_1 is turned ON, the currents $i_{\rm lk}$, i_{N2} and i_{N3} increase slowly because the three windings N_1, N_2, and N_3 are serially connected, which can be regarded as a single inductor with a value of $\{[(N_2+N_3)/N_1]+1\}^2 \cdot L_m + L_{\rm lk}$. Moreover, when Q_1 is turned OFF, Q_2 and Q_3 are turned ON, and $L_{\rm lk}$ and C_B resonate together. In addition, without considering current spikes and ringing, i_{N2} is equal to i_{N3} in the low step-down gain mode. From Figs. 24 to 26, one can see that the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$, at the input voltage of 18 V under the output currents of 1, 5, and 10 A, are about 6 and 4 V without considering voltage spikes and ringing. Similarly, From Figs. 27 to 29, one can see that the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$, at the input voltage of 36 V under the output currents of 1, 5, and 10 A, are about 12 and 8 V without considering voltage spikes and ringing. It should be noted that when the output current increases, the voltage stresses

Fig. 63. Waveforms related to Q_2 in the high step-down gain mode under the input voltage of 54 V and 85% of rated load: (1) $v_{\rm gs2}$ (10 V/ div); (2) $v_{\rm ds2}$ (20 V/ div); and (3) $i_{\rm lk}$ (2 A/ div).

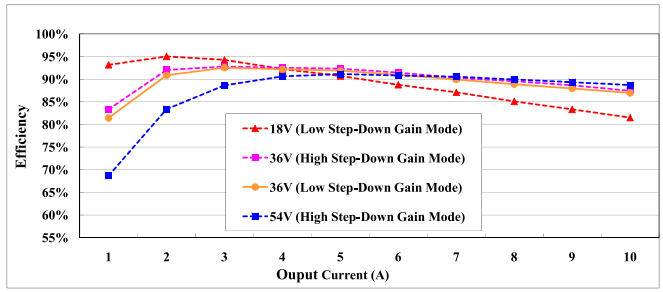

Fig. 64. Curves of efficiency versus output current.

will decrease a little. This is because when the output current increases, the voltage across C_B will increase a little. From Figs. 24 to 29, it can be seen that Q_3 and Q_4 possess ZVS or near ZVS turn-ON.

B. Measurements in High Step-Down Gain Mode

Figs. 30–45 show the waveforms in the high step-down gain mode. Figs. 30 and 31 show the gate driving signals $v_{\rm gs1}$, $v_{\rm gs2}$, $v_{\rm gs3}$, and $v_{\rm gs4}$ at the input voltage of 36 V under the output currents of 1 and 10 A, respectively. Figs. 32 and 33 show the gate driving signals $v_{\rm gs1}$, $v_{\rm gs2}$, $v_{\rm gs3}$, and $v_{\rm gs4}$ at the input voltage of 54 V under the output currents of 1 and 10 A, respectively. Figs. 34 to 36 show the winding currents $i_{\rm lk}$, i_{N2}, and i_{N3} at the input voltage of 36 V under the output currents of 1, 5, and 10 A, respectively. Figs. 37 to 39 show the winding currents $i_{\rm lk}$, i_{N2}, and i_{N3} at the input voltage of 54 V under the output currents of 1, 5, and 10 A, respectively.

Figs. 40 to 42 show the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$ at the input voltage of 36 V under the output currents of 1, 5, and 10 A, respectively. Figs. 43 to 45 show the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$ at the input voltage of 54 V under the output currents of 1, 5, and 10 A, respectively. From Figs. 30 and 31, it can be seen

that the actual duty cycles for Q_1 under the output currents of 1 and 10 A are 0.18 and 0.21, respectively. The ideal duty cycle for Q_1 is 0.15. From Figs. 32 and 33, it can be seen that the actual duty cycles for Q_1 at 1 and 10 A are 0.11 and 0.13, respectively. The ideal duty cycle for Q_1 is 0.1. From Figs. 34 to 39, it can be seen that when Q_1 is turned ON, the currents $i_{\rm lk}$, i_{N2}, and i_{N3} increase slowly because the three windings N_1, N_2 and N_3 are serially connected, which can be regarded as a single inductor with a value of $\{[(N_2+N_3)/N_1]+1\}^2 \cdot L_m + L_{\rm lk}$. Moreover, when Q_1 is turned OFF, the body diode of Q_3 is forward biased, which can be seen in Fig. 10(b). Thus, there is a small current spike occurring in i_{N2} and i_{N3} when the body diode of Q_3 is forward biased because $i_{N2} = i_{N3} = i_{\rm lk} + (-i_{\rm ds3})$. After that, Q_2 and Q_4 are turned ON, and $L_{\rm lk}$ and C_B resonate together. In addition, without considering current spikes and ringing, $i_{\rm lk}$ is equal to i_{N2} in the high step-down gain mode. From Figs. 40 to 42, one can see that the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$, at the input voltage of 36 V under the output currents of 1, 5, and 10 A, are about 11.6 and 8 V without considering voltage spikes and ringing. Similarly, From Figs. 43 to 45, one can see that the voltage stresses $v_{\rm ds3}$ and $v_{\rm ds4}$, at the input voltage of 54 V under the output currents of 1, 5, and 10 A, are about 17.5 and 10 V without considering voltage spikes and ringing. It should be noted that when the output current increases, the voltage stresses will decrease a little. This is because when the output current increases, the voltage across C_B will increase a little. From Figs. 40 to 45, it can be seen that Q_3 and Q_4 possess ZVS or near ZVS turn-ON.

C. Mode Exchange Transient Responses

Figs. 46–48 show the mode exchange transient responses from the low step-down gain mode to the high step-down gain mode at the input voltage of 36 V under the output currents of 1, 5, and 10 A, respectively. Figs. 49–51 show the mode exchange transient responses from the high step-down gain mode to the low step-down gain mode at the input voltage of 36 V under the output currents of 1, 5, and 10 A, respectively.

From Figs. 46 to 51, it can be seen that the overshoots/undershoots and recovery times of the output voltage are all within 200 mV and 300 μs, respectively.

D. Turn-On Features of Q_1, Q_2, Q_3, and Q_4

In the proposed converter, the switches Q_3 and Q_4 function as SR switches to do freewheeling. This behavior is similar to the low-side switch of the SR buck converter, which inherently possesses ZVS or near ZVS turn-ON. This has been verified in Figs. 24–29 and Figs. 40–45.

On the other hand, the ZVS turn-ON of Q_1 and Q_2 will be discussed in the following. Since the components have been chosen, the leakage inductance of the coupled inductor and the output capacitance of the switch are fixed. In this paper, an additional inductor and an additional capacitor are not used to compensate the leakage inductance and the switch output capacitance. Accordingly, at 10% of rated load, the dead times between $v_{\rm gs1}$ and $v_{\rm gs2}$ are set to be 150 ns, so as to make sure that the switches are turned on at the valley of the resonant period and hence to obtain relatively optimal efficiency on this condition. By doing so, the dead time is determined only by the leakage inductance and switch output capacitance, independent of input voltage and load current. This can be seen from Figs. 52 to 55, and each figure shows the gate driving signal for Q_1, $v_{\rm gs1}$, the gate driving signal for Q_2, $v_{\rm gs2}$, the voltage across Q_1, $v_{\rm ds1}$, and the voltage across Q_2, $v_{\rm ds2}$. Afterward, as the load current is increased, one can find the entry points of ZVS turn-ON of Q_1 and Q_2 under the input voltage of 18 V in the low step-down gain mode in Figs. 56 and 57, respectively, 36 V in the low step-down gain mode in Figs. 58 and 59, respectively, 36 V in the high step-down gain mode in Figs. 60 and 61, respectively, and 54 V in the high step-down gain mode in Figs. 62 and 63, respectively. It should be noticed that in Figs. 53 and 54, under the same input voltage of 36 V and output current of 1 A, the voltage $v_{\rm ds1}$ in the low step-down gain mode decreases faster than that in the high step-down gain mode. This is because the current used to discharge the output capacitance of Q_1 in the low step-down gain mode is larger than the current used to discharge the output capacitance of Q_1 in the high step-down gain mode. The currents $(i_{\rm lk})$ used to discharge the output capacitance of Q_1 in the low step-down gain mode and the high step-down gain mode can be observed in Figs. 21 and 34, respectively. This is because in the high step-down gain mode, the equivalent primary side is composed of N_1 and N_2, but in the low step-down gain mode, the equivalent primary side is N_1. From Figs. 56 to 63, it can be seen that the ZVS turn-ON of Q_1 and Q_2 is related to the input voltage and output current.

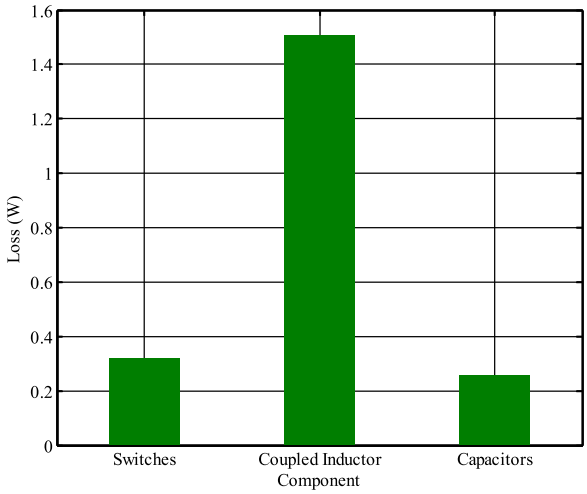

Fig. 65. Loss breakdown under the input voltage of 18 V and the load current of 10 A.

E. Efficiency and Loss Breakdown

In this paper, at the input voltage below 36 V, the converter operates in the low step-down gain mode, whereas at the input voltage above 36 V, the converter operates in the high step-down gain mode. Therefore, the efficiency curves related to the input voltages of 18, 36, and 54 V under

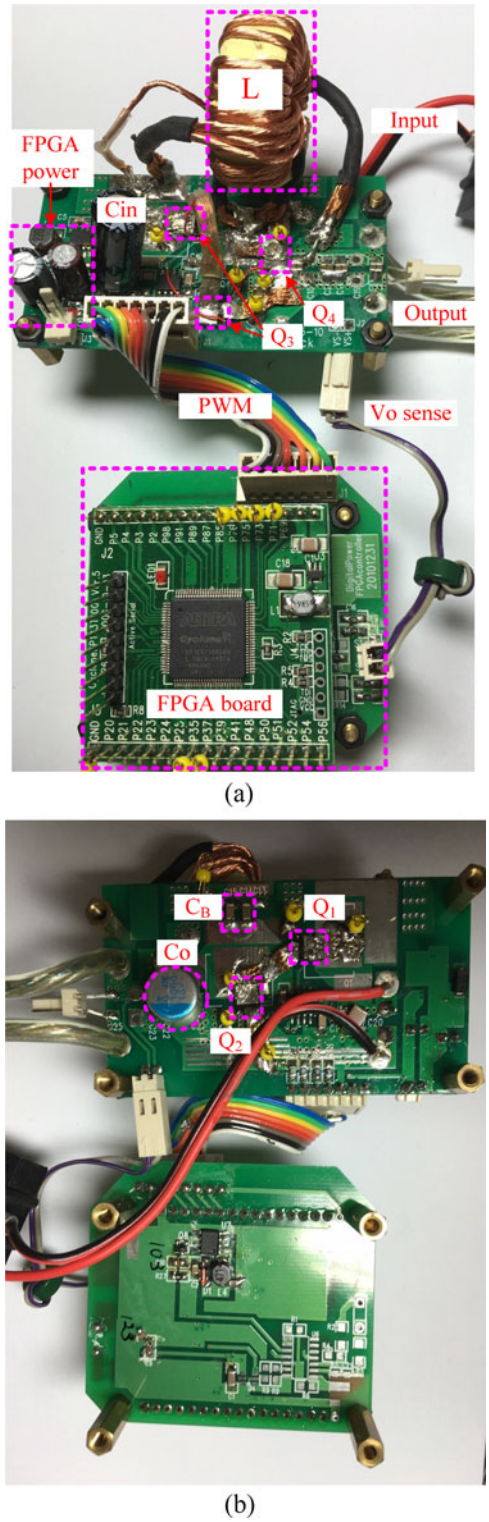

Fig. 66. Photo of the experimental setup: (a) top view and (b) bottom view.

different output current levels are shown in Fig. 64. From this figure, it can be seen that during the light load, the lower the input voltage is, the higher the efficiency, whereas during the heavy load, the higher the input voltage is, the higher the efficiency.

Since the proposed converter, operated under the input voltage of 18 V and the load current of 10 A, has lowest efficiency all over the input voltage and current range, only the loss breakdown in this case is given. From Fig. 65, it can be seen that the major power loss comes from the coupled inductor. The loss of the coupled inductor contains the copper loss and core loss. To further improve the efficiency, cores with lower core loss can be used, and the wires should be carefully designed.

F. Photo of Experimental Setup

Fig. 66 shows the photo of the experimental setup.

VI. Conclusion

In the telecommunication applications, the DPSs containing three stages have been widely used. In general, the nominal high DC bus voltage is 48 V, which is generated from the ac–dc converter. Next, the second stage is an isolated converter, which converts 48V to 12V. After that, the third stage is a nonisolated dc–dc converter, called POL, steps down 12 V to the low voltage the load requires. However, to improve the efficiency, a high step-down converter, named ultrahigh step-down converter which can converts 48 V to the low voltage required by the load, is presented [11]. Furthermore, in actual applications, the high dc bus voltage has a wide range, and the bus voltage range is usually 2:1. The experimental results show that when the input voltage increases, the efficiency of the ultrahigh step-down converter decreases. Particularly, the experimental results show the efficiency of the ultrahigh step-down converter decreases to 60% when it operates at the input voltage of 54 V and output current of 1 A.

Therefore, in this paper, the major objective focuses on the efficiency improvement of the ultrahigh step-down converter [11], with a wide input voltage range from 18 to 54 V and an output voltage of 1.2 V. When the input voltage of the proposed converter varies, the voltage gain can be changed to a suitable one to make this converter operate at higher efficiency. As compared with the ultrahigh step-down converter [11], the efficiencies of the proposed converter operating at the input voltage of 54 V and output current of 5 and 10 A are improved by about 1%. Moreover, the efficiency of the proposed converter operating at the input voltage of 54 V and output current of 1 A is improved by about 8%.

It is noted that a great difference between the proposed circuit and the tapped inductor buck converter [9] is that using C_B and Q_2 in the proposed circuit. These two components provide the winding N_1 a current path so as to achieve ZVS turn-on operation of high-voltage-side switches Q_1 and Q_2. In addition, the capacitor C_B functions as a voltage source so as to reduce the divided voltages across the windings N_2 and N_3. By doing so, the voltage across Q_3 and Q_4 can be decreased. Accordingly, although the switches Q_3 and Q_4 have turn-off rings, the corresponding voltage spikes are lower than the voltage ratings of the used MOSFETs.

APPENDIX A

Table III shows the pros and cons of the existing POLs and the proposed converter.

TABLE III
PROS AND CONS OF THE EXISTING POLS AND THE PROPOSED CONVERTER

	Pros	Cons
Single stage buck	• Low cost • Small size • 1 inductor • Main switch voltage rating = input voltage • 1 half bridge driver • 2 switches	• Small duty cycle • High switching loss • High-side switch failure risk
[6]-[8]	• No high-side switch failure risk • Main switch voltage rating = input voltage	• Low efficiency • High cost • Large size • More components: 3 bulk capacitors, 2 inductors, 2 controllers, 2 half-bridge drivers, 4 switches
[9]-[10]	• Less components • 1 coupled inductor • 2 switches • 2 bulk capacitors	• High switch voltage rating • Floating high-side driver • Hard switching on all switches • 1 floating driver+ 1 channel low-side driver
[11]	• 1 controller • 1 half-bridge driver • 3 switches • 2 bulk capacitors • ZVS turn-on • No high voltage appearing in the output	• Narrow input range
[4],[12],	• Isolated DC-DC converter plus buck converter • Very low main switch failure risk from electrical insulation • Easy for multi-output	• High cost • Large size • More than 3 bulk capacitors • More than 4 switches
Proposed converter	• Main switch voltage rating = input voltage • ZVS or near ZVS turn-on for all switches • 1 coupled inductor	• Coupled inductor with 3 windings • 1 half-bridge driver plus dual channel channel low-side driver • 4 switches

the proposed converter.

APPENDIX B

As for the controller shown in Fig. 67, it is implemented by one-comparator sampling [13], [14], which is basically built up by one voltage divider constructed by two resistors R_1 and R_2, one constant current source of 1.5 mA, one comparator, and one saw-toothed wave generator established by one small-power MOSFET switch S_1, two capacitors $C_{\rm ramp}$ and C_b, and one diode D_1. It is noted that the ac component of the saw-toothed wave is obtained by the ac coupled capacitor C_b via one operational amplifier (abbreviated as OP) used as a buffer. Afterward, this saw-toothed wave $v'_{\rm ramp}$ is summed with the sensed voltage v'_o, and the resultant signal is compared with the voltage reference $V_{\rm ref}$, so as to generate the signal VFB, which is sent to the field programmable gate array to create suitable gate driving signals after the feedback counter, PID controller and PWM generator.

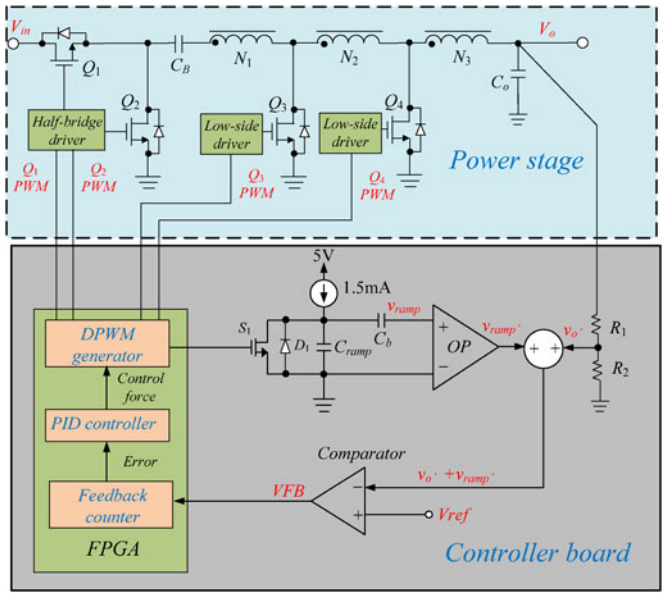

Fig. 67. Control scheme for the proposed converter.

APPENDIX C

The leakage inductance of the coupled inductor is calculated based on the measurement values shown in Table IV, which is referred to the literature [15], under the operating frequency of 100 kHz using an LCR meter.

TABLE IV
MEASUREMENTS OF THE COUPLED INDUCTOR

Inductance measured from N_1 with N_2 and N_3 opened: $L_{N1-\rm open}$	38.57 μH
Inductance measured from N_1 with N_2 and N_3 shorted: $L_{N1-\rm short}$	2.678 μH
Inductance measured from N_2 with N_3 and N_1 opened: $L_{N2-\rm open}$	2.251 μH
Inductance measured from N_2 with N_3 and N_1 shorted: $L_{N2-\rm short}$	1.565 μH
Inductance measured from N_3 with N_1 and N_2 opened: $L_{N3-\rm open}$	4.515 μH
Inductance measured from N_3 with N_1 and N_2 shorted: $L_{N3-\rm short}$	1.451 μH

According to Table IV, the coupling coefficient k_1 of N_1 with respect to N_2 and N_3 is

$$k_1 = \sqrt{1 - \frac{L_{N1-\rm short}}{L_{N1-\rm open}}} = \sqrt{1 - \frac{2.678\mu}{38.57\mu}} = 0.9647. \quad (54)$$

Also, the coupling coefficient k_2 of N_2 with respect to N_3 and N_1 is

$$k_2 = \sqrt{1 - \frac{L_{N2-\rm short}}{L_{N2-\rm open}}} = \sqrt{1 - \frac{1.565\mu}{2.251\mu}} = 0.5447. \quad (55)$$

And, the coupling coefficient k_3 of N_3 with respect to N_1 and N_2 is

$$k_3 = \sqrt{1 - \frac{L_{N3-\text{short}}}{L_{N3-\text{open}}}} = \sqrt{1 - \frac{1.451\mu}{4.515\mu}} = 0.8241. \quad (56)$$

Therefore, the coupling coefficient k is

$$\begin{aligned} k &= \sqrt{k_1 k_2 k_3} \\ &= \sqrt{0.9647 \times 0.5447 \times 0.8241} = 0.7565 \quad (57) \\ L_{\text{lk}} &= (1-k) L_{N1-\text{open}} \\ &= (1 - 0.7565) \times 38.57\mu = 9.39\mu\text{H}. \quad (58) \end{aligned}$$

Therefore, the leakage inductance L_{lk} is 9.39 μH.

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