# Study of a Current Control Strategy Based on Multisampling for High-Power Grid-Connected Inverters With an *LCL* filter

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***Abstract*—The high-power grid-connected inverters with *LCL* filters have been widely used. Current control plays a key role in the grid-connected inverter control system. To cope with the inherent resonance of the *LCL* filter, active damping (AD) methods are usually employed. However, the AD performance is impaired by control delays which are introduced in the digital control implementation process. Besides, the lag phase due to control delays limits the system bandwidth and stability margin. The effects of control delays are more noteworthy in the high-power grid-connected inverter due to its low switching frequency. This paper investigates the current control strategy based on multisampling for the high-power grid-connected inverter with the *LCL* filter. First, the multisampled AD scheme is studied, which can reduce control delays effectively and improve AD performance. Besides, the multisampled control without additional damping whether passive or active is researched. Through the inverter-side current feedback, the system can realize single-current-loop control based on multisampling. Thus, the control system is simplified and it can be stable, and achieve better dynamic performance. Finally, experimental results show that the proposed control schemes are effective.**

***Index Terms*—Active damping, control without additional damping (CWAD), inverter, *LCL* filter, multisample.**

## I. Introduction

As an interface between distributed power generation systems and the power grid, a grid-connected inverter is important in power conversion and guaranteeing to inject high-quality power into the grid [1]. With the grid-connected inverter power increasing, the *LCL* filter has been widely used. Current control plays a vital role in the grid-connected inverter control system [2].

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However, the inherent resonance of the *LCL* filter is easy to cause inverter system unstable. In order to stabilize the system, some solutions have been proposed, including passive damping (PD) methods, active damping (AD) methods, and control without additional damping (CWAD) whether passive or active. The PD method usually adds a resistor in the *LCL* filter, which is easy to implement but at the expense of increased losses [3], [4]. The power loss is unacceptable especially in a high-power system. The AD methods are adopted to damp the resonance through the modification of the control algorithm, including virtual resistance method [5], notch filter method [6], double current loop control [7], state feedback [8], etc. AD methods are realized flexibly while need extra sensors generally. The CWAD can be realized through single-current-loop control [9], [10]. This scheme avoids additional power loss and sensors, reducing system cost and simplifying the control algorithm.

However, the computation delay and pulse width modulation (PWM) delay are introduced in the digital control implementation process [11], [12]. These control delays have a significat influence on the AD method, leading to poor performance [13]. Moreover, the lag phase caused by delays can limit system bandwidth and stability margin [12]. In order to reduce control delays for improving AD control performance, several solutions have been addressed in many publications [13]–[15]. Wu and Lehn [14] present a control method combining deadbeat current control with optimal state-feedback pole assignment. The scheme can be considered as the way of predictive control. This control scheme usually depends on a plant model to predict the needed control signal, thus it may introduce additional estimation errors due to inaccurate plant parameters. The other type of method to reduce control delays is to shift the sampling instant toward the PWM reference update instant [13] or modify the PWM modulation such as dual sampling modes [15]. This kind scheme can reduce the computation delay but not the PWM delay. The PWM delay cannot be neglected especially at low switching frequency in a high-power grid-connected inverter. In fact, multisampling is a promising approach to reduce the computation delay and the PWM delay. Such sampling scheme has been studied in [16] and [17], where the filter is the *L* filter without considering resonance peak. However, the multisampling approach has been rarely studied in the high-power inverter with an *LCL* filter. In this paper, it is extend to the AD control for the *LCL*-filter inverter.

The study of CWAD also has been discussed in recent literatures [10], [18]–[20]. It has been demonstrated that single-current-loop control can be made stable. Simple but effective single-current-loop control strategies with traditional proportional-integral (PI) controller are promising control strategies, and these control strategies are popular in industrial applications [20]. In [10], it is shown that both inverter-side current feedback (ICF) and grid-side current feedback (GCF) can be employed to realize single-current-loop control, and the delay time significantly affects system stability. For a GCF loop, a time delay addition method is needed. However, additional delay causing phase lag will limit system bandwidth and stability margin. Moreover, in an industrial converter, the current sensors are integrated on the converter side as they are used for protection [21]. Then, it needs extra sensors to measure grid current when applying the GCF loop, thus it may be an unsatisfactory choice. Alternatively, for the ICF loop, the delay time needs to be reduced to stabilize the system. This scheme just requires one set of current sensors on the converter side, and it is chosen in this paper. As for the ICF loop control, to reduce control delays, a linear predictor-based time delay reduction method is proposed in [10]. However, the predictor largely depends on system parameters and may have poor performances because of the low switching frequency in a high-power inverter [22]. Since the multisampling approach can reduce control delays effectively, it should be able to realize ICF single-current-loop control, which so far has not yet been extensively studied in the literature.

This paper investigates the multisampled AD method based on capacitor voltage feedback. Compared with conventional sampling AD, it reduces the control delays and improves the AD performance. Then the CWAD based on multisampling is researched in this paper. It is stable to realize ICF single-current-loop control. With this scheme, it avoids using extra sensors, reducing system cost and control algorithm complexity, and the current dynamic response performance and the system stability margin are greatly improved. Furthermore, the experimental comparison of these two control strategies are carried out by a small-scale experiment. The remainder of this paper is organized as follows. In Section II, the current control of inverter with the *LCL* filter is introduced. In Section III, the active damping control based on multisampling is presented. In Section IV, the current CWAD based on multisampling is presented. Section V shows some experimental results and Section VI summarizes the conclusions.

## II. Current Control of the Grid-Connected Inverter With the *LCL* Filter

### A. System Description

The configuration of a three phase grid-connected inverter with an *LCL* filter is shown in Fig. 1(a), where $V_{\rm dc}$ is DC voltage. $L_1$ is the inverter-side inductor, $L_2$ is the grid-side inductor, and $C$ is the filter capacitor. Its equivalent single-phase circuit is shown in Fig. 1(b), where $v_{\rm inv}$ is the output voltage of the inverter and $e$ is the grid voltage. $i_1$ is the inverter-side current sensed for feedback, and $i_2$ is the grid-side current injected to the grid.

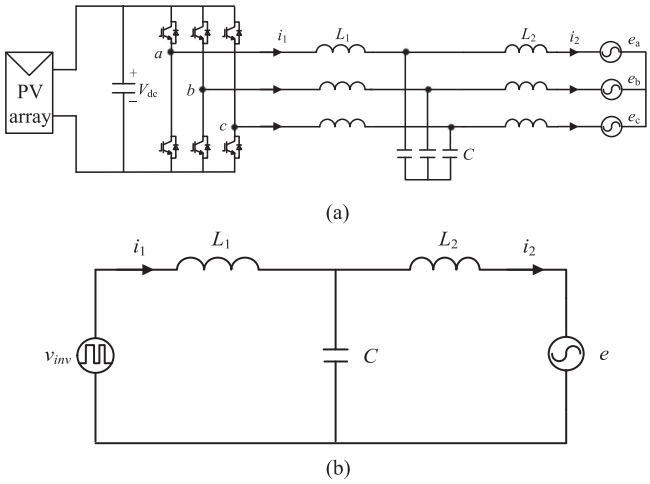



Fig. 1. A three phase grid-connected inverter with the *LCL* filter. (a) System circuit. (b) Equivalent single-phase circuit.

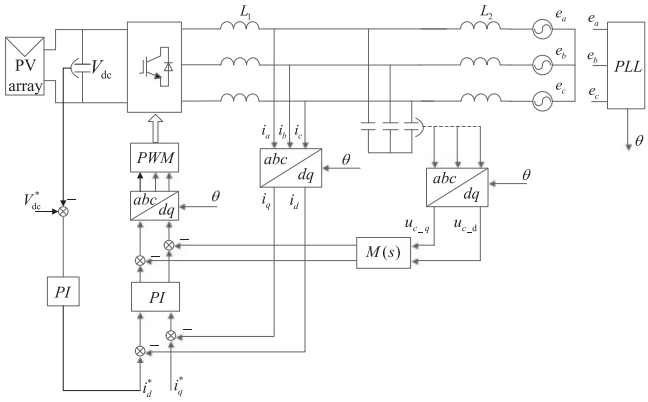



Fig. 2. Control structure of active damping.

The transfer function related to the inverter output voltage $v_{\rm inv}$ and the inverter-side current $i_1$, and the resonant frequency are expressed, respectively, as follows:

$$G_{\rm p}(s) = \frac{i_1}{v_{\rm inv}} = \frac{L_2Cs^2+1}{L_1L_2Cs^3+(L_1+L_2)s}, \tag{1}$$

$$\omega_{\rm res} = 2\pi f_{\rm res} = \sqrt{\frac{L_1+L_2}{L_1L_2C}}. \tag{2}$$

In the high-power grid-connected inverter, the switching frequency is low. In order to filter out the harmonic of the switching frequency, the resonant frequency of the *LCL* filter is usually only a few hundred hertz [23], which limits the system bandwidth and affects the stability.

### B. Active Damping Control Based on Capacitor Voltage Feedback

The capacitor voltage feedback active damping is one of the first studied methods and continues being in use [21], [24], [25]. It has turned out that the feedback of capacitor voltage through lead-lag network is a kind of effective method to damp resonance [21]. The control structure is shown in Fig. 2. The current control uses the synchronous rotating dq-frame, and the phase angle of

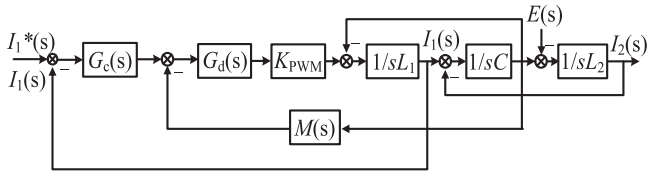



Fig. 3. Control block of current loop control with active damping.

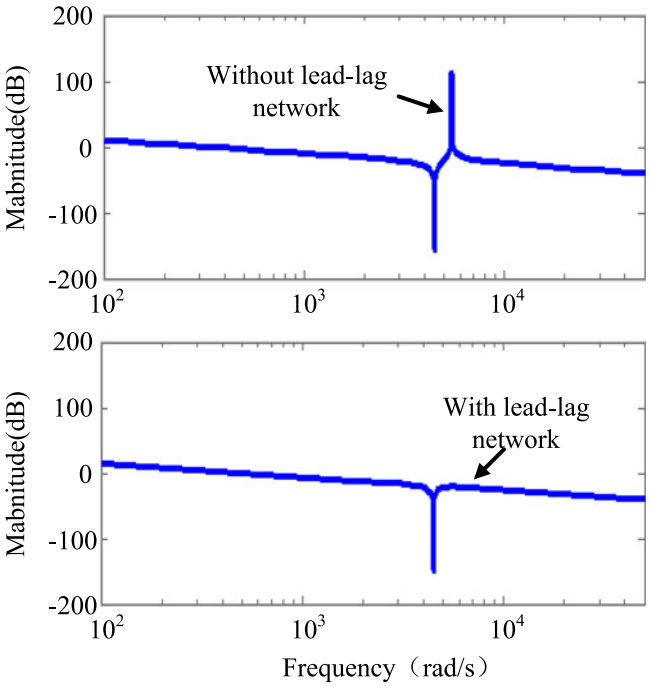



Fig. 4. Bode diagram of the *LCL* filter with the lead-lag network.

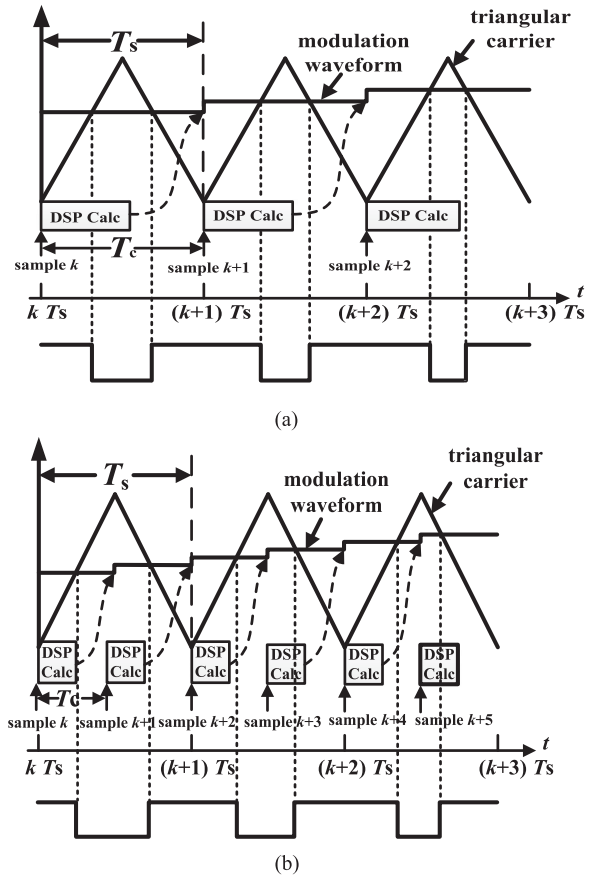



Fig. 5. Conventional sampling digital control for the PWM diagram. (a) Single-update mode. (b) Double-update mode.

grid is obtained through a phase-locked loop (PLL). The active current reference $i_{\mathrm{d}}^{*}$ is generated by the outer voltage loop, and the reactive current reference $i_{\mathrm{q}}^{*}$ is given according to the needed reactive power. The inverter-side currents are sensed and compared to the current reference. Then the current error is sent to the current controller, which is the PI controller here. The capacitor voltage is fed back through lead-lag network *M*(s) to damp the *LCL* filter resonance actively.

Because the dynamics of the voltage loop is much slower than that of the current loop and the dc-link can be assumed to be constant [26], the current loop can be analyzed independently. Therefore, the following analysis considers the characteristics of the current loop only. The current loop control block diagram is shown in Fig. 3. $G_c(s)$ is the PI controller and $G_d(\mathrm{s})$ is the control delays. $K_{\mathrm{pwm}}$ represents the gain of the PWM.

The lead-lag network *M*(s) is expressed as [27]

$$M(s) = k_d \frac{T_d s + 1}{\alpha T_d s + 1} \tag{3}$$

where $k_d$, $T_d$ and $\alpha$ are the parameters of the lead-lag network.

If not considering control delays, the bode diagram of the *LCL* filter with a lead-lag network is shown in Fig. 4. As seen, this AD method has good inhibition effect on the resonant peak.

As aforementioned, Fig. 4 is obtained without considering control delays. It works in the situation that the delays can be ignored in a high switching frequency inverter. However, the switching frequency is usually low to reduce the switching loss in the high-power grid-connected inverter, thus the control delays could not be ignored and affect AD performance.

### C. Control Delays in the Current Control Loop

Commonly, the grid-connected inverter is controlled based on digital signal processor (DSP). Conventional sampling digital control for PWM include single-update mode and double-update mode [28], [29], shown in Fig. 5, where $T_c$ is sampling period and $T_s$ is switching period.

As seen in Fig. 5, the signal sampling and update are operated at the valley or the peak of the triangular carrier. With the digital control, there is computation and PWM delays. The computation delay is the time duration between the sampling instant and the modulation waveform update instant, which is used for sampling and calculation [15]. The computation delay time is one sampling period $T_c$, thus it is equal to the switching period $T_s$ for single-update mode [see Fig. 5(a)] or half of the switching period $T_{\mathrm{s}}/2$ for double-update mode [see Fig. 5(b)].

The PWM delay is often considered as definitely half of the sampling period [11], [15]. The modulation waveform is constant after it has been updated until the next update instant, which forms a sinusoidal step waveform, while the output of the inverter is a PWM square waveform. The PWM delay is generated

in the transport process from the sinusoidal step waveform to the PWM square waveform.

The PWM model is built through a small-signal Laplace-domain analysis in [28]. According to the conclusion in [28], the single-update PWM model and the double-update PWM model are expressed, respectively, as follows:

$$G_{\mathrm{PWM\_1}}(s) = \frac{1}{2}\left(e^{-s\frac{DT_c}{2}} + e^{-s\frac{(2-D)T_c}{2}}\right), \tag{4}$$

$$G_{\mathrm{PWM\_2}}(s) = \frac{1}{2}\left(e^{-s(1-D)T_c} + e^{-sDT_c}\right) \tag{5}$$

where $D$ is duty cycle.

Frequency-domain models of (4) and (5) are denoted as

$$G_{\mathrm{PWM\_1}}(j\omega) = \cos\left(\frac{\omega(1-D)T_c}{2}\right)e^{-j\omega\frac{T_c}{2}}, \tag{6}$$

$$G_{\mathrm{PWM\_2}}(j\omega) = \cos\left(\omega\left(D-\frac{1}{2}\right)T_c\right)e^{-j\omega\frac{T_c}{2}} \tag{7}$$

where $\omega$ is the angular frequency.

As can be seen, the delay of PWM modulation is the half sampling period $T_c/2$.

In a word, the control delays are introduced in the digital control for inverter based on DSP, including the computation delay and the PWM delay. The total delay time $t_d$ is $3T_c/2$. For the single-update mode, $T_s = T_c$, the delay time is $3T_s/2$. For the double-update mode, $T_s = 2T_c$, the delay time is $3T_s/4$.

### D. Analysis of Stability Impacted by Control Delays

According to Fig. 3, the transfer function of the control loop is given by

$$G_{AD}(s) = \frac{I_2(s)}{I_1^*(s)} = \frac{G_c(s)G_d(s)K_{\mathrm{PWM}}}{\begin{array}{l}(s^3L_1L_2C + s^2L_2CG_c(s)G_d(s)K_{\mathrm{PWM}} + sL_2 \\ +sL_1 + sL_2M(s)G_d(s)K_{\mathrm{PWM}} + G_c(s)G_d(s)K_{\mathrm{PWM}})\end{array}}. \tag{8}$$

The transfer function of the PI controller can be expressed as

$$G_c(s) = K_{\mathrm{p}} + \frac{K_{\mathrm{i}}}{s} \tag{9}$$

where $K_p$ is the proportional coefficient and $K_i$ is the integral coefficient.

Since the integral coefficient has little effect at the amplitude–frequency characteristics of high frequency, the proportional coefficient $K_p$ determines the cutoff frequency of the system. Therefore, a larger $K_p$ means a faster dynamic response and a larger loop gain at low frequencies [30]. The integral term can be designed to have a negligible influence on system stability, so in the analysis and experiment it is kept at the same value and small relatively in different sampling control schemes. The $K_p$ is adjusted to reflect the system bandwidth and stable margin at different control schemes. For the conventional sampling PWM control, the control delays will limit the range of $K_p$ to ensure system stability. Taking the single-update mode as an example, the system stability at different $K_p$ is analyzed with and without time delay. The related parameters are given in Table I.

TABLE I
PARAMETERS OF GRID-CONNECTED INVERTER WITH LCL FILTER

| Parameters | Values |
|---|---|
| Rated power $P$ | 5 kW |
| Grid voltage $e_{\mathrm{AB}}$ | 110 V |
| Fundamental frequency $f$ | 50 Hz |
| DC-link voltage $V_{\mathrm{dc}}$ | 210 V |
| Switching frequency $f_s$ | 2 kHz |
| Inverter-side inductor $L_1$ | 2 mH |
| Grid-side inductor $L_2$ | 1 mH |
| Filter capacitor $C$ | 50 $\mu$F |

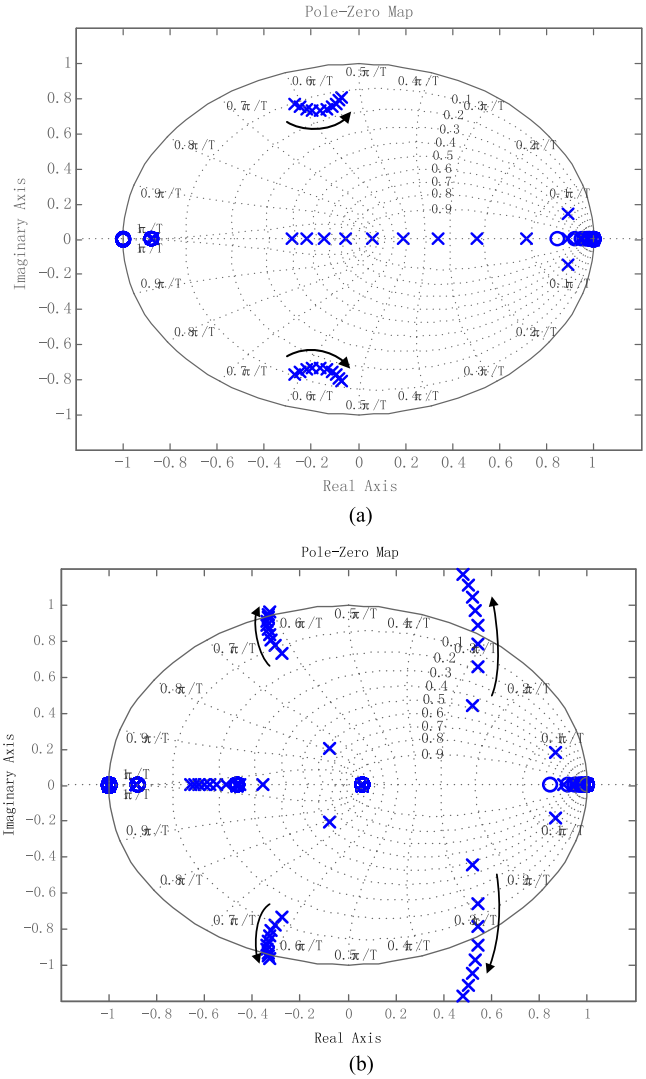



Fig. 6. Pole-zero map by varying $K_p$ from small to large. (a) Without control delays. (b) With control delays.

Fig. 6 shows the pole-zero map according to (8) by varying $K_p$. Without considering control delays, the pole-zero map according to $K_p$ from small to large in a certain range is shown in Fig. 6(a). It can be seen that poles are located in the unit

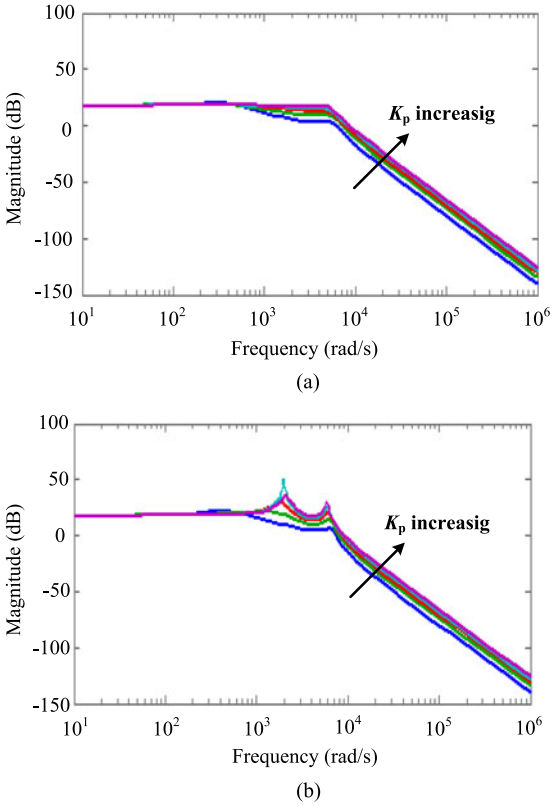



Fig. 7. Bode diagrams by varying $K_{\mathrm{p}}$ from small to large. (a) Without control delays. (b) With control delays.

circle, so the system can be stable. While considering control delays, the pole-zero map according to $K_p$ from small to large in a certain range is shown in Fig. 6(b). It shows that when $K_p$ increases to some value, poles moving outside of the unit circle, the system becomes unstable from stable.

Fig. 7 shows the bode diagram according to (8) by varying $K_p$. Without considering control delays, the bode diagram according to $K_p$ from small to large in a certain range is shown in Fig. 7(a). It can be seen that the resonant peak is inhibited around the resonant frequency. While considering control delays, the bode diagram according to $K_p$ from small to large in a same range as Fig. 7(a) is shown in Fig. 7(b). It shows that when $K_p$ is small, the resonant peak can be inhibited. While $K_p$ increases to some value, the resonant peak exists, which impairs the system stability.

As analyzed above, the delay affects system stability even if the AD method has been used. When delay is large, in order to ensure system stability, the value of $K_p$ cannot be too large, which limits bandwidth and stability margin.

## III. Active Damping Control Based on Multisampling

### A. PWM Modulation Based on Multisampling

In order to reduce the computation delay and the PWM delay, the multisampling approach can be used. The multisampled PWM digital implementation is shown in Fig. 8(a). With this approach, signals such as voltage and current are sampled and the modulation waveforms signal are updated *N* times per

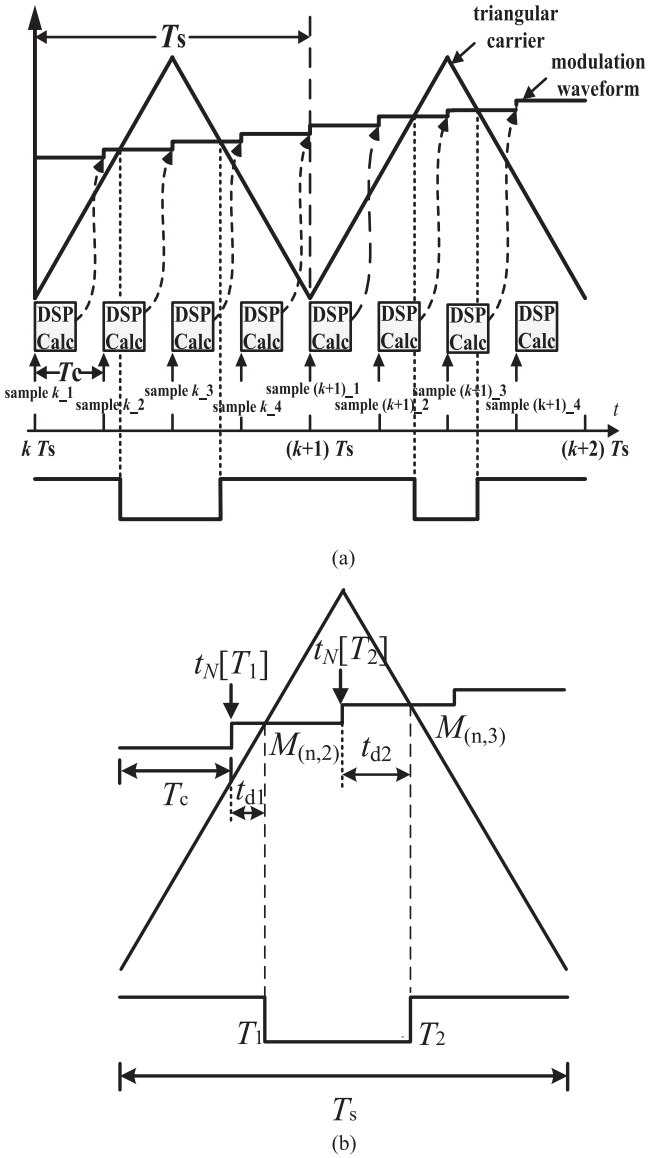



Fig. 8. PWM with multisampling. (a) Multisampled PWM digital implementation. (b) Diagram of multisampling for PWM in one switching period.

switching period, where *N* is multisampling coefficient, that is, $f_c = N \cdot f_s$ ($f_c$ is sampling frequency and $f_s$ is switching frequency). As shown in Fig. 8(a), the computation delay is one sampling period $T_c$, that is, $T_s/N$.

As for the PWM transport process, it is different with single-update and double-update modes. In the condition of multisampling, not every modulation signal interacts with carrier to generate PWM pulses. The PWM delay is a half sampling period, which can be analyzed with the small-signal method [28], [31]. It is shown in Fig. 8(b) in detail. $M_{(\mathrm{n,k})}$ represents the *k*th update modulation signal of the *N*th switching period. For example, $M_{(\mathrm{n},2)}$ and $M_{(\mathrm{n},3)}$ represent the second and the third update modulation signal in the *n*th switching period, which interact with the rise and fall ramp of the triangle carrier, respectively. $t_N[t_k]$ denotes the update instant preceding $t_k$. As shown in Fig. 8(b), $T_1$ and $T_2$ denote the time of PWM falling edge and the rising edge, respectively, then $t_N[T_1]$ is the

update instant preceding $T_1$, so as $t_N[T_2]$. $t_{d1}$ is the time between $t_N[T_1]$ and $T_1$, and $t_{d2}$ is the time between $t_N[T_2]$ and $T_2$. According to the small-signal analysis method used in [28] and [31], PWM model can be given by

$$G_{\mathrm{PWM\_N}}(s) = \frac{1}{2}\left(e^{-st_{d1}} + e^{-st_{d2}}\right). \tag{10}$$

The modulation waveform in a switching period can be considered approximately as a constant value because the switching period is relatively small to the fundamental wave period. Then $t_{d1}$ and $t_{d2}$ are expressed as

$$\begin{cases} t_{d1} = T_1 - t_N[T_1] \approx \frac{1}{2}(1-D)T_s - t_N\left[\frac{1}{2}(1-D)T_s\right] \\ t_{d2} = T_2 - t_N[T_2] \approx \frac{1}{2}(1+D)T_s - t_N\left[\frac{1}{2}(1+D)T_s\right] \end{cases}. \tag{11}$$

The frequency domain of (10) is given by

$$\begin{aligned} &G_{\mathrm{PWM\_N}}(j\omega) \\ &= \cos\frac{\omega(t_{d1}-t_{d2})}{2}\left(\cos\frac{\omega(t_{d1}+t_{d2})}{2} - j\sin\frac{\omega(t_{d1}+t_{d2})}{2}\right). \end{aligned} \tag{12}$$

The signals are sampled at equal time interval in a switching period, so

$$\begin{aligned} &\frac{1}{2}(t_{d1}+t_{d2}) \\ &= \frac{1}{2}\left(T_s - \left(t_N\left[\frac{1}{2}(1+D)T_s\right] + t_N\left[\frac{1}{2}(1-D)T_s\right]\right)\right) \\ &= \frac{1}{2}\frac{T_s}{N}. \end{aligned} \tag{13}$$

From (10) and (13), the PWM model can be given by

$$G_{\mathrm{PWM\_N}}(j\omega) = \cos\frac{\omega(t_{d1}-t_{d2})}{2}e^{-j\omega\frac{T_s}{2N}}. \tag{14}$$

Since $t_{d1} - t_{d2}$ is small, (14) shows that PWM can be considered as a pure delay link under the condition of multisampling, and the delay time is $T_s/2N$.

Through the above analysis, it can be seen that the total delay time is $t_d = T_s/N + T_s/2N = 3T_s/2N$ for multisampling PWM digital control, and the delay time is related to multisampling coefficient *N*. Compared with single-update and double-update modes, the delay time is reduced by increasing the value of *N*. However, the value of *N* should not be too large, because the modulation signal needs enough time to be calculated out before the next sampling instant. If the value of *N* is too large, the control chip is required to have high computational speed. Moreover, the improvement of system control performance is not obvious [17].

In a word, it can be found that the control delay of conventional sampling and multisampling PWM digital control can be expressed as $t_d = 3T_s/2N$, so it is given as (15) in a uniform way to represent the control delays in different sampling approaches. It denotes single-update when $N = 1$, double-update when $N = 2$ and natural sampling when $N \to \infty$. The delay time in natural sampling is zero [32]

$$G_d(s) = e^{-s\frac{3T_s}{2N}}. \tag{15}$$

### *B. Active Damping With Capacitor Voltage Feedback Based on Multisampling*

The expression of lead-lag network *M*(s) has been given in (3). The design method of *M*(s) is important, which is analyzed in detail in [21] and used here. From (3), the maximum phase shift $\varphi$ is obtained as

$$\varphi = \arcsin\frac{1-\alpha}{1+\alpha}. \tag{16}$$

In order to damp the resonance peak actively, the lead-lag network has better behave as a differentiator at frequencies around the resonance frequency, where damping is necessary, by selecting $\varphi$ close to 90° and frequency of $\varphi$ equal to resonance frequency [21], that is

$$\begin{aligned} 90^\circ &= \varphi - \omega_{\mathrm{res}}\frac{1.5T_s}{N}\frac{360}{2\pi} \\ \omega_m &= \frac{1}{T_d\sqrt{\alpha}} = \sqrt{\frac{L_1+L_2}{L_1L_2C}}. \end{aligned} \tag{17}$$

$T_d$ and $\alpha$ are confirmed according to the above conditions. $k_d$ is selected by pole-zero map, which is obtained according (8) by varying $k_d$ from small to large, as shown in Fig. 9. To show the advantage of multisampled AD, the double-update AD and the multisampled ($N = 8$) AD are analyzed comparatively, and it can be seen that to achieve the optimal active damping performance, for double-update, $k_d = -0.6$, for multisampling, $k_d = 0.1$.

The pole-zero map according to $K_p$ varying from small to large is shown in Fig. 10. It shows that the range of $K_p$ increases for multisampling, which denotes that system can obtain higher bandwidth and stable margin compared with double-update.

## IV. Current CWAD Based on Multisampling

From above analysis, compared with conventional sampling AD, multisampled AD improves the system control performance. However, for the active damping method, it usually needs additional sensors, leading to increase cost. What's more, the control algorithm is complex, so it requires to be repeated debugging based on the actual situation in order to get the best control performance when it is employed. To address this issue, the CWAD is a promising scheme. Fig. 11 shows the control block of ICF single-current-loop control. This method does not require additional damping methods and control algorithm is simple, resulting in a cost-effective solution.

In [10], the relationship between control delays and stability of single-loop controlled grid-connected inverters with *LCL* filters has been fully studied. It shows that delay is the key factor to affect stability for ICF single-loop control and analyzes the range of control delay for system stability. Through the analysis in [10], there are many available ranges for the control delay. While considering achieving the highest bandwidth, the range

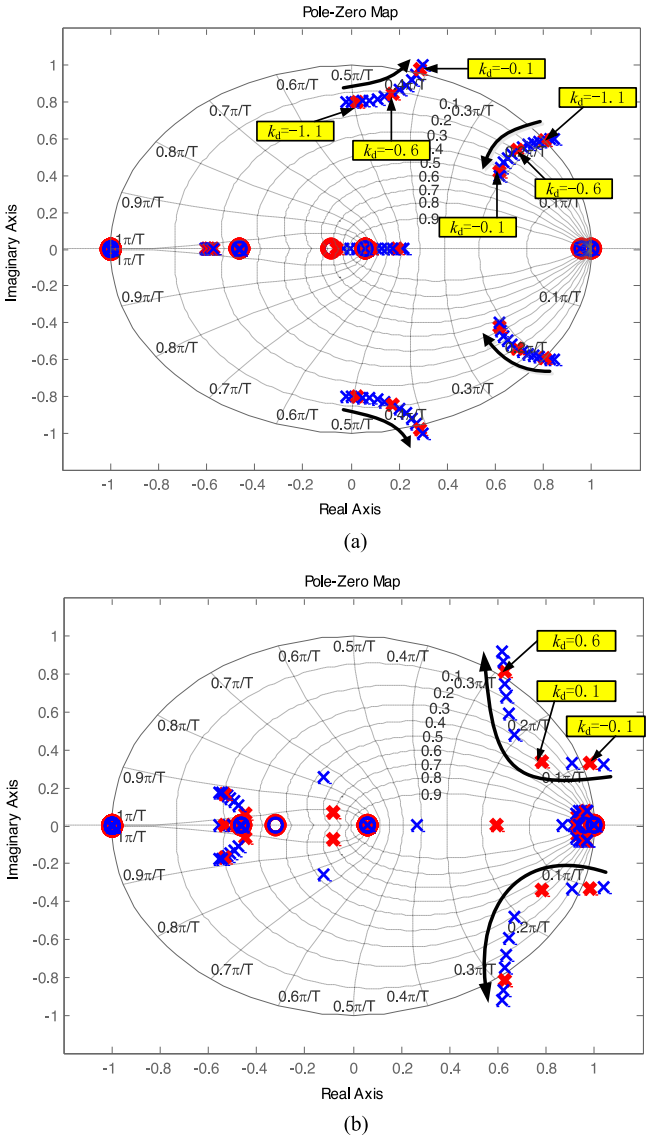



Fig. 9. Pole-zero map by varying $k_{\mathrm{d}}$ from small to large. (a) Double-update. (b) Multisample ($N = 8$).

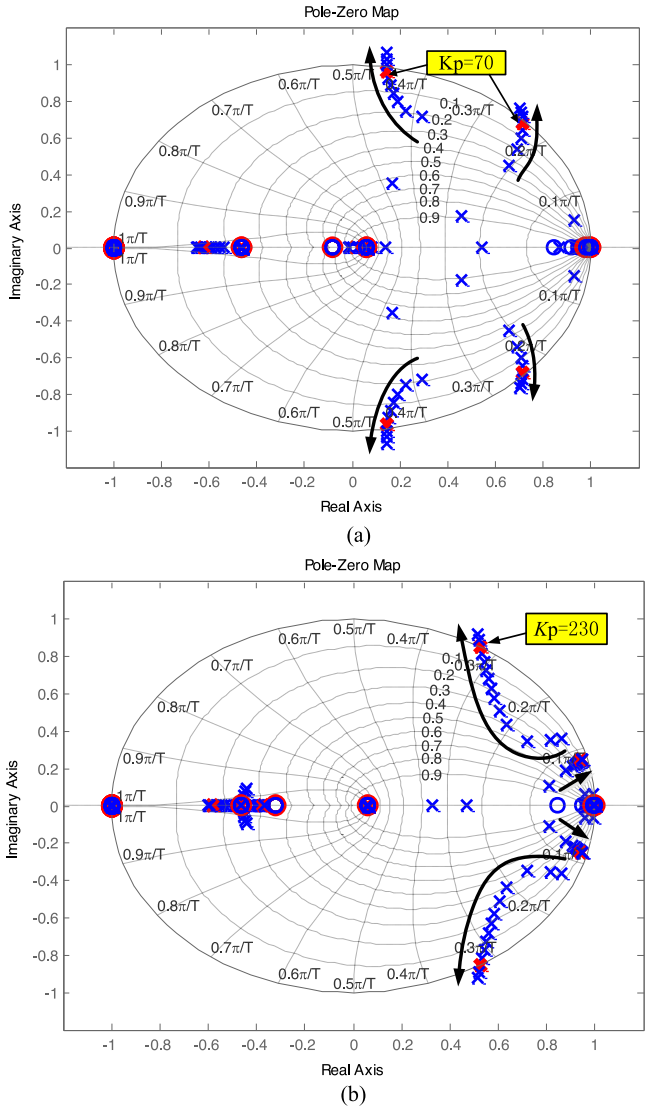



Fig. 10. Pole-zero map by varying $K_{\mathrm{p}}$ from small to large. (a) Double-update. (b) Multisample ($N = 8$).

of time delay can be expressed as

$$t_d < \frac{\pi}{2\omega_{\mathrm{res}}}. \tag{18}$$

In this paper, $t_d$ is $3T_c/2$ and $\omega_{\mathrm{res}}$ is $2\pi f_{\mathrm{res}}$. So according to (18), the stable range can be derived as

$$f_c > 6f_{\mathrm{res}}. \tag{19}$$

It shows that the stable range for ICF single-loop control is $f_c > 6f_{\mathrm{res}}$. Here, one-sixth of the sampling frequency ($f_c/6$) can be regarded as the critical frequency ($f_{\mathrm{crit}}$). When $f_{\mathrm{res}} < f_{\mathrm{crit}}$, system can be stable.

Usually, in order to better filter out the switching frequency harmonics, $f_{\mathrm{res}}$ is usually set to $f_s/4 \sim f_s/2$ [30]. In this condition, because of different control delays, different sampling schemes affect system stability. It is analyzed as follows.

For the single-update, $f_{\mathrm{crit}} = f_s/6, f_{\mathrm{res}} > f_{\mathrm{crit}}$, the system is unstable. For double-update, $f_{\mathrm{crit}} = f_s/3$, if $f_{\mathrm{res}}$ is

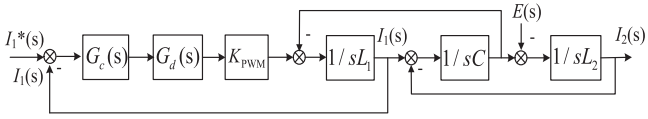
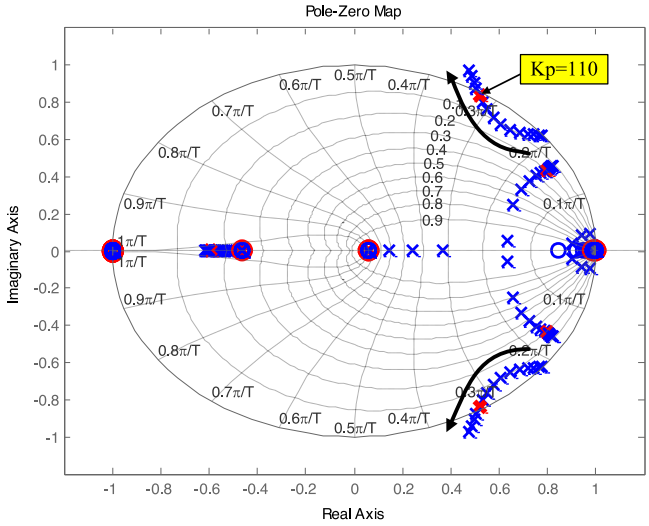


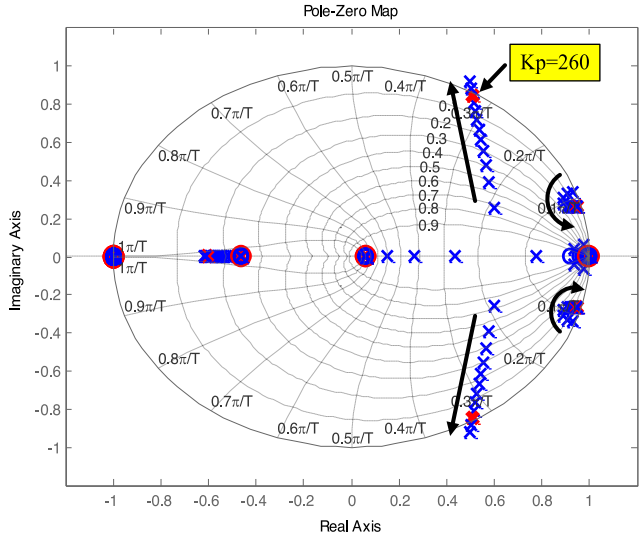

Fig. 11. Control block of the ICF single-current-loop.

$f_s/4 \sim f_s/3$, then the system is stable. If $f_{\mathrm{res}}$ is $f_s/3 \sim f_s/2$, according to the conclusion above, it seems that the system is unstable. However, the conclusion about $f_{\mathrm{crit}} = f_{\mathrm{c}}/6$ is drawn from ignoring some uncertain factors such as parasitic damping and dead zone effect. If these factors are considered, even when $f_{\mathrm{res}}$ is $f_{\mathrm{s}}/3 \sim f_s/2$, system maybe stable for double-update, but the stable margin is uncertain. Therefore, under the condition of double-update, the system stability is uncertain and it obviously can not be adopted directly.

To ensure sufficient stability margin, the control delays need to be further reduced. The multisampling approach is used to reduce control delays and analyzed as follows.




(a)




(b)

Fig. 12. Pole-zero map by varying $K_p/2$ for ICF sing-current-loop control. (a) Multisample ($N = 4$). (b) Multisample ($N = 8$).

The transfer function from Fig. 11 is expressed as

$$G_{\mathrm{CWAD}}(s) = \frac{I_2(s)}{I_1^*(s)} = \frac{G_c(s)\,G_d(s)\,K_{\mathrm{PWM}}}{\left(s^3 L_1 L_2 C + s^2 L_2 C G_c(s)\,G_d(s)\,K_{\mathrm{PWM}} + sL_1 + sL_2 + G_c(s)\,G_d(s)\,K_{\mathrm{PWM}}\right)}. \quad (20)$$

From (20), the pole-zero map according to $K_p$ varying from small to large is shown in Fig. 12. It shows that the range of $K_p$ increases with multisampling coefficient increasing. So we can obtain the conclusion that it does not need additional sensors to get better control performance by using ICF under the condition of multisampling.

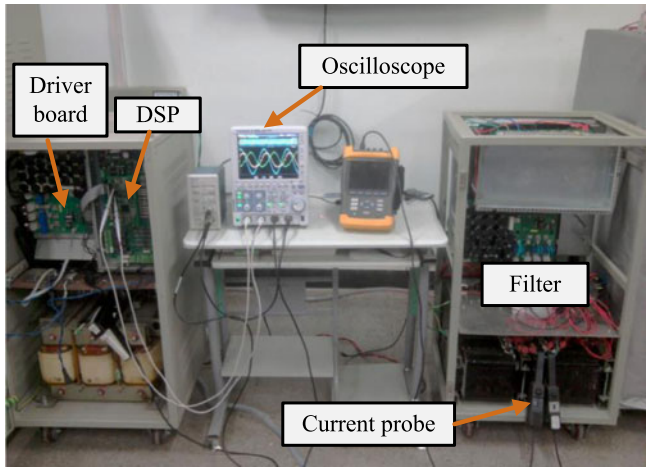



Fig. 13. Photograph of the experimental prototype.

## V. Experimental Verification

### A. Description of the Prototype

Experiments are carried out on a small-scale prototype system of a three-phase grid-connected inverter with an *LCL* filter, which is shown in Fig. 13. The control circuit is implemented on a DSP chip TMS320F28335. The parameters of the prototype are shown in Table I where the grid (line-voltage rms value is 400 V) is connected to the inverter via a transformer (transformation ratio is 380/105).

### B. Experimental Results

Fig. 14 gives the steady-state current waveforms under control with CWAD and AD for double-update. Without the AD control algorithm, the system can be stable but $K_p$ is small [see Fig. 14(a)]. Thus system bandwidth is low. If $K_p$ increases, currents oscillate even in the steady state as shown in Fig. 14(b). In this case, the AD method based on capacitor voltage feedback is adopted to increase system damping and currents are stable, as shown in Fig. 14(c).

Fig. 14 shows that conventional sampling AD can damp resonance and improve bandwidth to a certain extent. However, the AD could not reduce the control delays and the bandwidth and stability margin is still limited due to control delays. If $K_p$ is tuned larger, currents oscillate as shown in Fig. 15(a) and the spectrum of $i_{2a}$ is shown in Fig. 15(b). In this case, a multisampled AD scheme is used to make currents stable as shown in Fig. 15(c) and the spectrum is shown in Fig. 15(d). It shows that using a multisampling approach can improve the stability margin of AD control. As to the harmonic components around the switching frequency, they are attenuated owing to the effect of the *LCL* filter, which is shown as the partial enlarged view in Fig. 15(b) and (d). They are small and have little influence on control performance and output current spectra.

Fig. 16 gives the current dynamic performance in the *d* axis of the rotating *dq*-frame under the condition of different sampling AD schemes. In order to observe the dynamic response clearly, current data are obtained from the DSP serial communication interface and stored. Then the dynamic response waveforms are

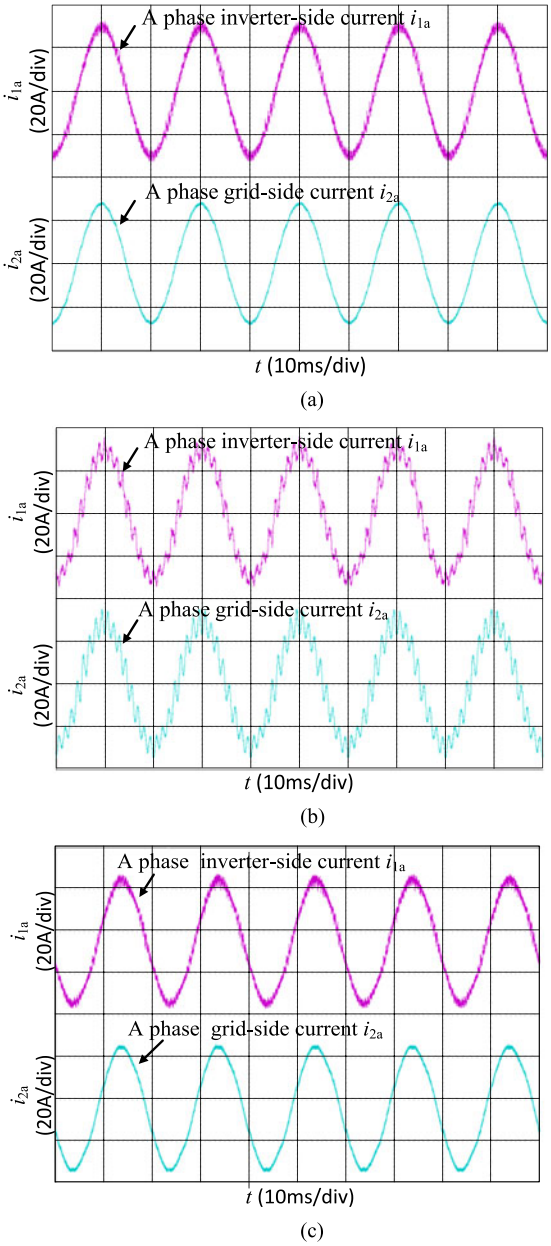



Fig. 14. Steady state current waveforms for double-update. (a) CWAD scheme ($K_p = 15$). (b) CWAD scheme ($K_p = 30$). (c) AD scheme ($K_p = 30$).

obtained according to the stored data by using MATLAB. $i_{\mathrm{d}}^{*}$ is the given current reference, $i_d$ is the actual current feedback, and $\Delta i_{\mathrm{d}}$ is the current error between $i_{\mathrm{d}}^{*}$ and $i_d$. For the AD scheme of double-update PWM digital control, when $K_p = 30$, current recovers in the steady state again after about 57 ms, as shown in Fig. 16(a). If $K_p$ is tuned to 80, currents oscillate [see Fig. 15(a)], so its dynamic response waveforms are not shown. In this case, multisampled AD is used, and current becomes stable. In the dynamic experiment, current recovers in the steady state after about 32 ms, as shown in Fig. 16(b). It shows that using the multisampling approach can improve dynamic response of AD control.

Fig. 17 gives the current waveforms when the CWAD scheme is adopted. It is achieved through ICF single-current-loop

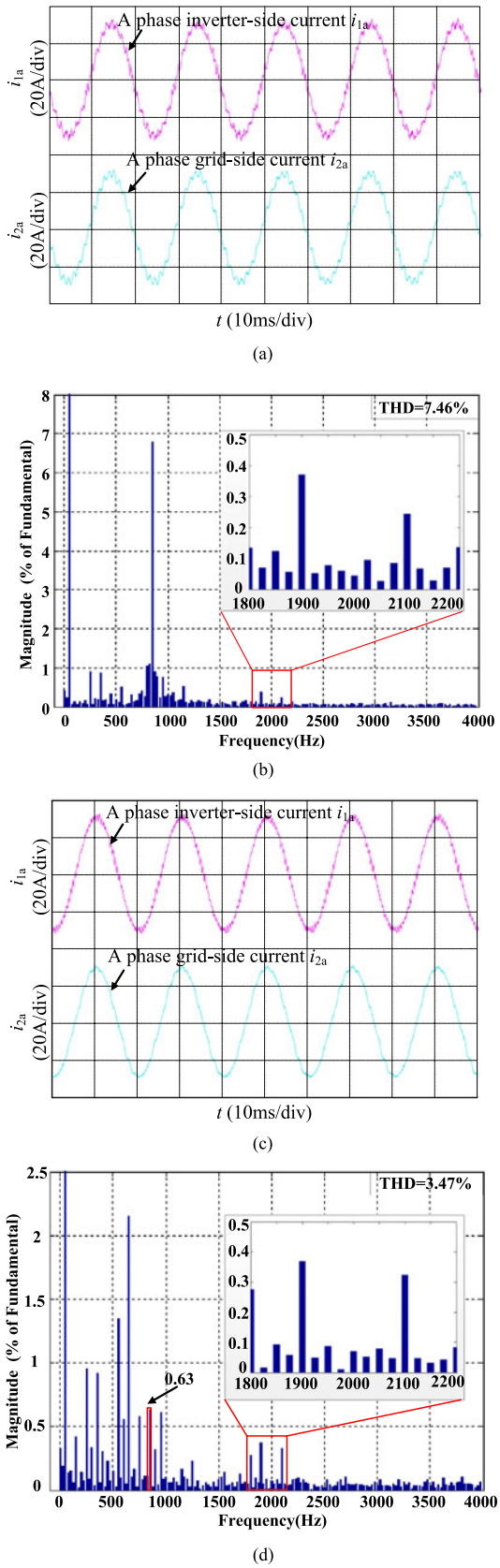



Fig. 15. Steady state current waveforms for different sampling AD schemes when $K_{\mathrm{p}} = 80$. (a) double-update AD scheme. (b) Current spectrum of $i_{2\mathrm{a}}$ for the double-update AD scheme. (c) Multisampled AD scheme ($N = 8$). (d) Current spectrum of $i_{2\mathrm{a}}$ for multisampled AD scheme ($N = 8$).

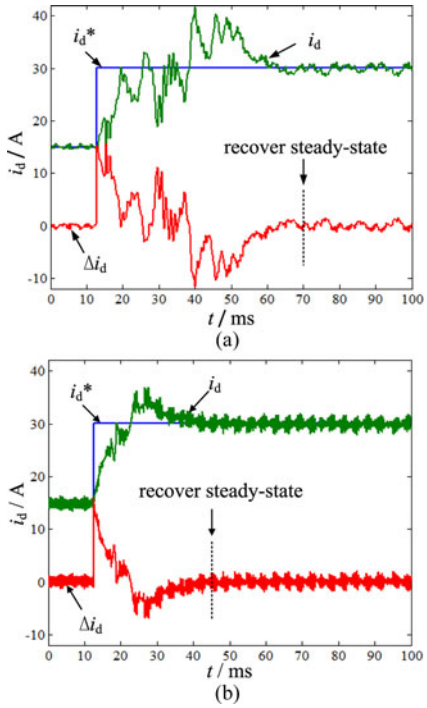



Fig. 16. Dynamic response current waveforms in $d$ axis for different sampling AD schemes. (a) Double-update AD scheme ($K_{\rm p} = 30$). (b) MultiMultisampled AD scheme ($N = 8$, $K_{\rm p} = 80$).

control based on multisampling. Due to delay reduced further, the stability margin is improved, thus current can be stable when $K_p = 80$ even without additional damping, as shown in Fig. 17(a). The spectrum of $i_{2\rm a}$ is shown in Fig. 17(b). The harmonic components around the switching frequency are attenuated by the *LCL* filter and have little influence on output current spectra in this experiment. Compared with AD, CWAD avoids using extra sensors and simplifies control algorithm. However, the total harmonic distortion (THD) of $i_{2\rm a}$ with CWAD is larger slightly than that with AD. The resonance peak is inhibited with AD while it is not with CWAD, thus the harmonic around resonance frequency with CWAD is also slightly larger than that with AD [see Figs. 15(d) and 17(b)]. On the other hand, the CWAD system has a better dynamic performance. Fig. 17(c) shows that current recovers in the steady state after about 25 ms.

## VI. Conclusion

As for the high-power grid-connected inverter with the *LCL* filter, the control delays can affect AD control and limit system bandwidth and stability margin, leading to poor control performance. In this paper, on the basis of conventional sampling AD control, multisampled AD control is studied to improve AD performance. On the other hand, AD scheme usually requires additional sensors. Based on the analysis, the multisampled CWAD scheme through ICF single-current-loop control is further researched that reduces the system cost and control algorithm complexity, meanwhile improving system bandwidth and stability margin.

In order to validate the proposed control scheme, an experimental prototype is built and tested. The experimental results

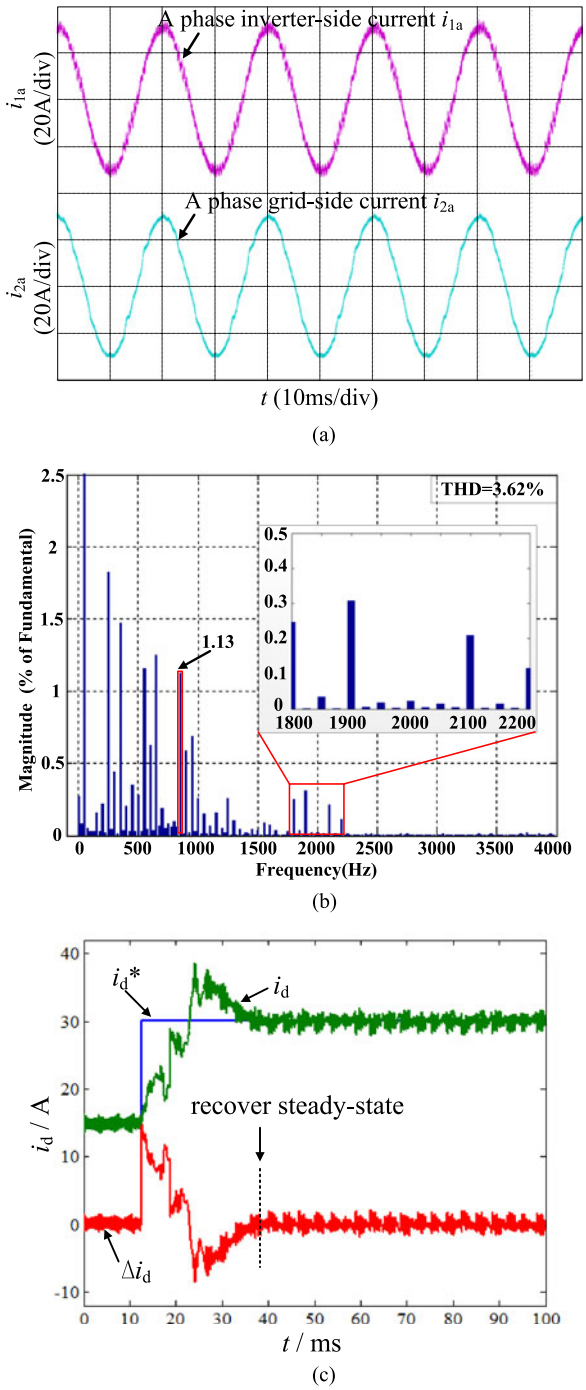



Fig. 17. Current waveforms using the CWAD scheme based on multisampling ($N = 8$) when $K_p = 80$. (a) Steady-state current waveforms. (b) Current spectrum of $i_{2\rm a}$ for steady-state current waveforms. (c) Dynamic response current waveforms.

verified the effectiveness of the control scheme investigated in this paper. Except for system bandwidth and stability margin, current harmonic control is also important for the high-power grid-connected inverter. Because of the sampling frequency increasing, some harmonic will be injected into the control loop. It is a complex problem for multisampling and may be related to multisampling coefficient, sampling location, and other factors, which will be analyzed in future work.

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