Small-Signal Model of the Five-Level Unidirectional T-Rectifier

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***Abstract*—In this paper, a small signal model is proposed for the new unidirectional three-phase T-type rectifier topology known as five-level T-Rectifier (5L T-RECT). The proposed model is obtained starting from the large signal analytical representation of the 5L T-RECT configuration. The derived equations have been simplified using the synchronous reference frame transformation; to this purpose, the average values over the fundamental period T_0 are considered for the input phase voltages. After that, the converter steady-state and dynamic models are derived by means of the local linearization around the desired operating point. The transfer functions related to the inputs and outputs of the system are, therefore, obtained and depicted. The achieved 5L T-RECT model has been first verified using the linear analysis tool in the MATLAB/Simulink environment starting from the detailed switching model. Theoretical results exhibit a very good accuracy between the small-signal, the large-signal, and the switching models. Then, experimental activity is depicted to further validate the proposed small-signal model.**

***Index Terms*—AC–DC power conversion, modeling, multilevel power electronic converters, power electronics, state-space methods.**

I. Introduction

SWITCHING converter topologies are highly nonlinear systems because they contain transistors and diodes that are operated as switches with only two states, open and closed. The ac–dc topologies normally require control circuits to ensure the line current wave shaping and to regulate the dc output voltage against the variations of the loads and the fluctuations of the line voltage [1]. The linearization of the power converter behavior is at the basis of a more predictable tuning procedure of the related control loops. It can be achieved by applying the well-known stability criteria of the linear systems [2], [3]. Hence, converters control loop design requires achieving the system dynamic model (i.e., analytical description). Due to the nonlinear time-varying nature of the switching converters such as ac–dc topologies, it is difficult to predict their dynamic characteristics. The aim of the power electronic converters modeling is to provide a mathematical expression that contains the information on the steady state and the dynamic behavior of the system. A low-frequency state-space model of the converter can result by applying the state-space averaging (SSA) method [4]. Consequently, from the large signal average system description, it is very important to develop reliable small-signal models that allow designers to obtain the converter dynamic behaviors reducing the prototyping cost and the design cycle time [5], [6]. The provided small-signal model is at the basis of control loops design, starting from linear control strategies such as proportional-integral (PI)-based vector control or when even more complex model-based control structures are used. Especially for the latter topologies, the control action performance is directly related to the model representation. Without the small-signal analytical description, except for some specific controllers that do not require any tuning (i.e., hysteretic controllers), the designer cannot take advantage of the well-known control system theory and is forced to use the so-called trial-and-error approach, which yields unsatisfactory dynamic performance. Moreover, the availability of the linearized system equations results in the possibility to use nonlinear and adaptive control structures to strongly improve the complete dynamic response, as it is described in [7].

Among the ac–dc topologies, power factor correction (PFC) circuits are widely required in energy conversion systems that use power electronic devices. Their main role is to compensate the nonlinearity of the ac–dc systems and, thus, to reduce or even eliminate the resulting voltage and current harmonics injected into the distribution network [8]–[10]. In fact, in several applications, $\mathrm{THD}_i < 5\%$ at rated power is often required. In other, for instance aircraft on-board power supplies, relatively high inner mains impedances exist, and thus even stricter limits, i.e., $\mathrm{THD}_i < 3\%$, have to be satisfied. In order to make the industrial and scientific community more sensitive to the power quality topic, international standards (IEEE 519, IEC 555, IEC 1000-3-2, IEC 61000 series etc.) have become increasingly strict in this field [11]. Three-phase PFC rectifier topologies are ever more used in various applications as input power stage, such as variable speed drives, uninterruptible power system (UPS), data centers and telecom power supplies, dc motor drives, battery charging, power conversion, etc., [12]. In the last decades, new interface topologies have evolved from unidirectional two-level to three-level rectifiers [13], [14]. The utilization of multilevel converters can lead to designs with higher power

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ratings and improved power quality. However, the large number of power switches significantly increases cost and control complexity [15]. Anyway, applications such as variable speed drives, UPS, and telecom power supplies, where both power density and specific weight are of the greatest importance, have become potential users of unidirectional three-level rectifiers [16], [17]. In particular, the Vienna-type is often used as the multilevel rectifier stage. The control of the Vienna rectifier is relatively problematical because it features a three-level structure. Midpoint voltage balancing is a well-known issue in application of three-level converters. Therefore, dc-link neutral-point voltage regulation is required. In the recent years, a lot of research has been done on this aspect, including the averaged model derivation and the control scheme development [18]–[21]. The methodology used to derive the averaged model is often based on SSA technique. Subsequently, the small-signal model based on the large-signal model is proposed for the Vienna rectifier [22]–[26].

Among the multilevel topologies for ac–dc conversion, the 5L T-RECT configuration is attracting the interest of researchers [26], [27]. The 5L T-RECT exhibits a good conduction path for high modulation index compared to either the five-level neutral-point-clamped (NPC) topology or the flying-capacitors (FC). In both NPC and FC topologies, for high-modulation index, the current path includes four power devices, whereas, in the 5L T-RECT, the current path is through the series of an insulated-gate bipolar transistor (IGBT) and a diode in all the operating conditions. In general terms, the lower the current path is, the lower will be the switching and conduction losses. Today, the general trend is to increase the presence of Si/SiC/GaN in order to limit the quantity of iron and copper. Following this tendency, the investigated configuration is able to provide a five-level line-to-line voltage with four switches and six diodes for each phase leg when ac–dc unidirectional power flow is assured. However, the total power of Si required for the investigate five-level topology is similar to that one of standard three-level or two-level solutions. The benefits of a higher number of levels, such as significant reduction of current ripple, are therefore almost for free.

Some configurations mainly based on Vienna topology were presented in the literature [27], [28], where the detailed mode of operation is illustrated. In [29], a new multilevel converter structure with stacked cells is depicted. However, when a bidirectional power flow is provided, the number of active devices usually increases. In the proposed 5L T-RECT configuration, the number of switches is reduced, thanks to its inherent unidirectional power flow, which is very common in some applications, such as generating units, UPS ac–dc input stage, etc.

An example of a unidirectional switching cells multilevel converter can be found in [30] with reference to single-phase applications. Also in [30], the proposed converter configuration is extended to a five-level three-phase system, where each phase leg is composed by six power switches and six diodes, then the one-phase topology is replicated three times to achieve the three-phase configuration.

In this paper, a new small-signal model is developed for the 5L T-RECT. The 5L T-RECT small-signal model can be seen as a basic step toward the control design and to understand the dynamic behavior of the proposed converter topology. Initially,

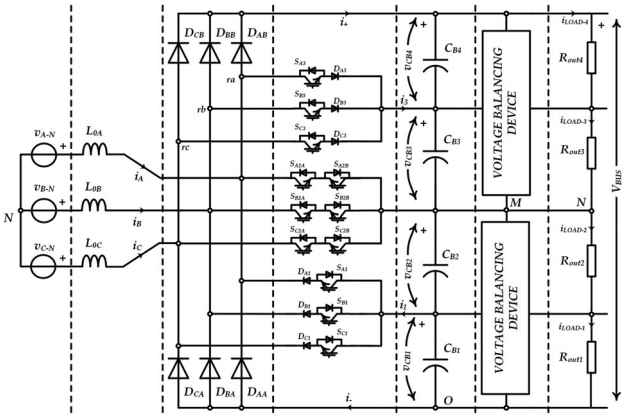

Fig. 1. Complete scheme of the 5L T-RECT topology with the dedicated balancing circuit.

the equivalent averaged model of the 5L T-RECT converter in the stationary frame, considering both ac and dc-side effects, has been elaborated. A deepened analysis and the validation of the large signal model of 5L T-RECT have been previously discussed in [31]. Performing the local linearization around the nominal operating point, from the state-space averaged model, the converter steady-state and dynamic models are derived in this paper. A set of transfer functions, relating the inputs to the outputs of the system, are obtained. The analytical model has been validated by comparing the obtained transfer functions and the system's responses with the averaged and switching models and some experimental results.

II. 5L T-RECT State-Space Average Model

As illustrated in Fig. 1, the rectifier consists of five functional blocks: input filter inductors $L_{0\mathrm{A}}$, $L_{0\mathrm{B}}$ and $L_{0\mathrm{C}}$; three-phase diode bridge; a set of IGBT connected between the diode bridge, and the dc-bus capacitors; a set of four series connected dc-bus capacitors C_{B1}, C_{B2}, C_{B3}, C_{B4}; two voltage balancing devices. Four load resistors are considered in order to achieve the most general possible model; in fact, the configuration with the dc-bus load being modeled through only one resistor can be derived as the particular solution of the proposed study. The IGBTs are controlled in order to ensure a sinusoidal waveform of the input current and a regulated dc-link voltage at the output. Due to converter no-idealities, the injected average current may cause deviation of the voltage distribution among the series connected capacitors, as described in detail in [32]. For this reason, a balancing circuit is used in order to obtain the desired condition $v_{\mathrm{CB1}} + v_{\mathrm{CB2}} = v_{\mathrm{CB3}} + v_{\mathrm{CB4}}$.

Hence, the dc-bus partial voltages v_{CB1}, v_{CB2}, v_{CB3}, v_{CB4}, are assumed to be equal, $v_{\mathrm{CB1}} = v_{\mathrm{CB2}} = \frac{v_{\mathrm{BUS}}}{4} - \frac{\Delta v_{\mathrm{BUS}}}{4}$, $v_{\mathrm{CB3}} = v_{\mathrm{CB4}} = \frac{v_{\mathrm{BUS}}}{4} + \frac{\Delta v_{\mathrm{BUS}}}{4}$ with $\Delta v_{\mathrm{BUS}} = v_{\mathrm{CB3}} + v_{\mathrm{CB4}} - (v_{\mathrm{CB1}+} v_{\mathrm{CB2}})$, intended as the unbalance between the two partial output dc-buses (i.e., top and bottom with respect to the midpoint). As illustrated in Fig. 1, the bottom-side switch is voltage bidirectional and current unidirectional. Accordingly, it is realized as a series connected IGBT, $\mathrm{S_{p1}}$ and diode $\mathrm{D_{p1}}$ (with p: A, B, C). The middle switch is voltage and current bidirectional and it is composed by two IGBTs in common emitter

configuration, $\mathrm{S}_{p2\mathrm{A}}$ and $\mathrm{S}_{p2\mathrm{B}}$. The top-side switch is realized as a series connected IGBT and diode, S_{p3} and D_{p3}. Therefore, it is a voltage bidirectional and current unidirectional equivalent switch. The modeling approach applied to the converter shown in Fig. 1 is based on the SSA technique. In this method, all the variables are averaged across one pulse width modulation (PWM) sampling period T_S. A comprehensive description of the SSA method and the 5L T-RECT large-signal model has been presented in [31]. It represents the starting point of the analysis related to the small-signal circuit description, where main steps are summarized hereafter.

A. State-Space Equations

State-space equations related to the input ac side and the output dc side are at the basis of the analytical model of the converter. The complete set of equations are summarized in (1), shown at the bottom of the page, where

$$\Gamma = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix},$$

$$\mathrm{SGN}_1 = \begin{bmatrix} \mathrm{sgn}\,(i_A) & 0 & 0 \\ 0 & \mathrm{sgn}\,(i_B) & 0 \\ 0 & 0 & \mathrm{sgn}\,(i_C) \end{bmatrix}$$

$$\mathbf{I} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix},\ \mathrm{SGN}_2 = \frac{1+\mathrm{SGN}_1}{2},$$

$$\mathrm{SGN}_3 = \frac{1-\mathrm{SGN}_1}{2}$$

$\theta(i_p)$ is a threshold function defined as $\theta(i_p) = \begin{cases} 1 & i_p \geq 0 \\ 0 & i_p < 0 \end{cases}$ and $\overline{\theta}(i_p) = \begin{cases} 0 & i_p \geq 0 \\ 1 & i_p < 0 \end{cases}$ is its logic complement.

The switching function $\mathrm{S}_{p(1,2,3)}$ is defined as $S_{p(1,2,3)} = \begin{cases} 0 & \text{switch off} \\ 1 & \text{switch on} \end{cases}$ where $p \in A,\ B,\ C$.

B. State Space Averaging

Considering (1), the equivalent average model of the 5L T-RECT topology in the stationary reference frame has been obtained as in [31]. System state equations are as follows:

$$\left.\begin{cases} L\dfrac{d\mathbf{i_p}}{dt} = \mathbf{v_p} - \dfrac{v_{\mathrm{BUS}}}{4}\boldsymbol{\Gamma}\mathbf{d'_p} \\ C\dfrac{d}{dt}\begin{bmatrix} v_{\mathrm{BUS}} \\ \Delta v_{\mathrm{BUS}} \end{bmatrix} = \begin{pmatrix} \mathbf{d'^{T}_p}\left[\mathbf{I} - \dfrac{\Delta v_{\mathrm{BUS}}}{v_{\mathrm{BUS}}}\mathrm{SGN}_1\right]\mathbf{i_p} \\ \mathbf{d'^{T}_p}\left[\mathrm{SGN}_1 - \dfrac{\Delta v_{\mathrm{BUS}}}{v_{\mathrm{BUS}}}\mathbf{I}\right]\mathbf{i_p} \end{pmatrix} + \\ \qquad -\begin{pmatrix} 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \end{pmatrix}\begin{pmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \end{pmatrix} \end{cases}\right\rangle \begin{matrix} \mathrm{ac\ -\ side} \\ \\ \\ \mathrm{dc\text{-}side.} \end{matrix} \tag{2}$$

In (2), the term $\boldsymbol{d'}_p = [d'_A, d'_B, d'_C]$ is the new control vector related to the complete three-phase system representation defined as

$$d'_p = \begin{cases} (1-d_{p2})\left(2 - d_{p1}\bar{\theta}(i_p) - d_{p3}\theta(i_p)\right) \\ \qquad 0.5 < m \leq 1 \quad \text{five-level} \\ \left(\mathrm{sgn}(i_p) + \dfrac{\Delta v_{\mathrm{BUS}}}{v_{\mathrm{BUS}}}\right) \\ (1-d_{p2})\left(\mathrm{sgn}(i_p) + \dfrac{\Delta v_{\mathrm{BUS}}}{v_{\mathrm{BUS}}}\right) \\ \qquad 0 \leq m \leq 0.5 \quad \text{three-level} \end{cases}. \tag{3}$$

In (3), $d_{p1},\ d_{p2}$ and d_{p3} are respectively the duty-cycle related to the switches 1, 2, and 3 of the phase p, $p \in A,\ B,\ C$, and m is the modulation index. In general, the modulation index can be regulated between 0 and 1 if the linear region is considered, even when the third-harmonic injection strategy is used. When the modulation index is between 0 and 0.5, the converter degenerates into the three-level topology being S_{p3} and S_{p1} always 1 (switches closed). When the modulation index is above 0.5, the rectifier exhibits the proper four and five voltage levels.

$$\begin{cases} \begin{bmatrix} v_{A-N} \\ v_{B-N} \\ v_{C-N} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} + \boldsymbol{\Gamma}\frac{v_{\mathrm{BUS}}}{2}\left(\mathrm{SGN}_1 + \frac{\Delta v_{\mathrm{BUS}}}{v_{\mathrm{BUS}}}\mathbf{I} - \frac{1}{2}\left(1 + \frac{\Delta v_{\mathrm{BUS}}}{v_{\mathrm{BUS}}}\right)\right. \\ \qquad \left.\cdot\mathrm{SGN}_2\begin{bmatrix} S_{A3} \\ S_{B3} \\ S_{C3} \end{bmatrix} + \frac{1}{2}\left(1 - \frac{\Delta v_{\mathrm{BUS}}}{v_{\mathrm{BUS}}}\right)\mathrm{SGN}_3\begin{bmatrix} S_{A1} \\ S_{B1} \\ S_{C1} \end{bmatrix}\right)\begin{bmatrix} 1-S_{A2} \\ 1-S_{B2} \\ 1-S_{C2} \end{bmatrix} \\ C\dfrac{dv_{\mathrm{BUS}}}{dt} = \displaystyle\sum_{p=A,B,C}(1-S_{p2})\,|i_p|\left[2 - S_{p3}\theta(i_p) - S_{p1}\bar{\theta}(i_p)\right]\mathrm{sgn}(i_p) - (i_{L1}+i_{L2}+i_{L3}+i_{L4}) \\ C\dfrac{d\Delta v_{\mathrm{BUS}}}{dt} = \displaystyle\sum_{p=A,B,C}(1-S_{p2})\,|i_p|\left[2 - S_{p3}\theta(i_p) - S_{p1}\bar{\theta}(i_p)\right] + (i_{L1}+i_{L2}-i_{L3}-i_{L4}) \end{cases} \tag{1}$$

C. Reference Frame Transformation

The ac-side equation in (2) is time invariant, whereas the dc-side expression is still linked to the time-varying model that depends on the sign of the input line currents. Hence, the averaged model is obtained as in (4) by applying the *abc*-to-*dq0* transformation [33]. In detail, the new vectors $[v_d\ v_q\ v_0]^T = \mathbf{K}[v_A\ v_B\ v_C]^T, [i_d\ i_q\ i_0]^T = \mathbf{K}[i_A\ i_B\ i_C]^T, [d'_d\ d'_q\ d'_0]^T = \mathbf{K}[d'_A\ d'_B\ d'_C]^T$ are replaced into (4), where *K* is the well-known Park's transformation defined as in [31] and reported below. Performing the required dot products, results shown in (4) are directly obtained

$$\mathbf{K} = \frac{2}{3}\begin{bmatrix} \sin(\omega_0 t) & \sin(\omega_0 t - 2\pi/3) & \sin(\omega_0 t - 4\pi/3) \\ \cos(\omega_0 t) & \cos(\omega_0 t - 2\pi/3) & \cos(\omega_0 t - 4\pi/3) \\ 3/2 & 3/2 & 3/2 \end{bmatrix}$$

$$\begin{cases} L\dfrac{di_d}{dt} = v_d + L\omega_0 i_q - \dfrac{v_{\rm BUS}}{4}d'_d \\ L\dfrac{di_q}{dt} = v_q - L\omega_0 i_d - \dfrac{v_{\rm BUS}}{4}d'_q \\ C\dfrac{dv_{\rm BUS}}{dt} = \dfrac{3}{2}\left(d'_d \cdot i_d + d'_q \cdot i_q\right) - \alpha\dfrac{\Delta v_{\rm BUS}}{v_{\rm BUS}}d'_0 \\ \qquad\qquad \cdot i_d - (i_{L1} - i_{L2} - i_{L3} - i_{L4}) \\ C\dfrac{d\Delta v_{\rm BUS}}{dt} = -\dfrac{3}{2}\dfrac{\Delta v_{\rm BUS}}{v_{\rm BUS}}\left(d'_d \cdot i_d + d'_q \cdot i_q\right) + \alpha d'_0 \\ \qquad\qquad \cdot i_d + (i_{L1} + i_{L2} - i_{L3} - i_{L4}) \end{cases} . \tag{4}$$

As it is shown in (4), the converter in Fig. 1 may be represented in low-frequency domain by a fourth-order nonlinear dynamic system, having i_d, i_q, $v_{\rm BUS}$, $\Delta v_{\rm BUS}$ as state variables; d'_d, d'_q and d'_0 as control inputs; and finally v_d and v_q as disturbances. Since the three-phase input voltages are assumed to be balanced and the *d-q* reference frame rotates with the same angular speed ω_0 of the sinusoidal inputs, the homopolar components v_0 and i_0 are equal to zero. In (4), α is a theoretical constant parameter estimated at $2/\pi$ [18]. The corresponding equivalent circuit is shown in Fig. 2 for the *d* and *q* axes, where

$$i_1 = \frac{3}{2}d'_d \cdot i_d, \quad i_2 = \frac{3}{2}d'_q \cdot i_q, \quad i_3 = \alpha\frac{\Delta v_{\rm BUS}}{v_{\rm BUS}}d'_0 \cdot i_d,$$
$$i'_1 = \alpha d'_0 \cdot i_d, i'_2 = \frac{3}{2}\frac{\Delta v_{\rm BUS}}{v_{\rm BUS}}d'_d \cdot i_d, i'_3 = \frac{3}{2}\frac{\Delta v_{\rm BUS}}{v_{\rm BUS}}d'_q \cdot i_q.$$

III. 5L T-RECT Proposed Small-Signal Model

In the *dq0* synchronous reference frame, each state variable can be related to a steady-state value. Hence, the calculation of the steady-state point of operation is carried out by setting to zero all the time derivatives in (4).

Furthermore, it is assumed that the dc-link capacitors voltage is balanced and the converter operates with unity power factor. Hence, the steady-state space-vector of the line currents is considered proportional to the space-vector of the mains line-to-neutral voltages. These considerations provide the operating steady-state condition which is as follows:

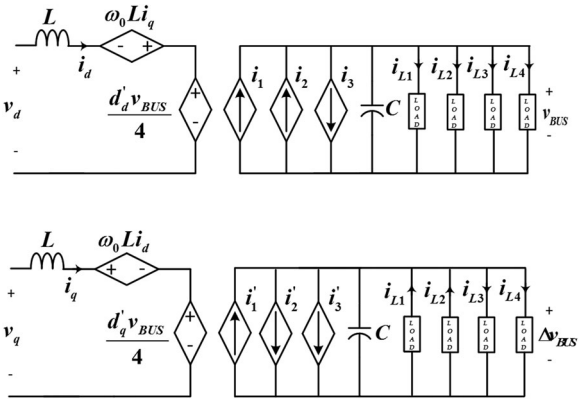

Fig. 2. Complete *dq-axes* state-space average model for the 5L T-RECT.

$$v_d^* = \sqrt{2}V_s, i_d^* = \sqrt{2}I_s^*, v_{\rm BUS}^* = V_{\rm BUS}^*, v_q^* = i_q^* = 0$$
$$d'^*_d = \frac{4\sqrt{2}V_s}{V_{\rm BUS}^*}, d'^*_q = -\frac{4L\omega_0\sqrt{2}I_s^*}{V_{\rm BUS}^*}$$
$$d'^*_0 = \frac{\left(i^*_{\rm LOAD-4} + i^*_{\rm LOAD-3}\right) - \left(i^*_{\rm LOAD-1} + i^*_{\rm LOAD-2}\right)}{\alpha\sqrt{2}I_s^*} \tag{5}$$

where V_s is the rms value of the input voltage, I_s^* is the rms ac line current and $V_{\rm BUS}^*$ is the total dc output voltage. In addition, with reference to Fig. 1, by assuming a balanced purely resistive dc load, it can be written as

$$i_{\rm LOAD-1} = \frac{v_{\rm BUS} - \Delta v_{\rm BUS}}{4R};\ i_{\rm LOAD-2} = \frac{v_{\rm BUS} - \Delta v_{\rm BUS}}{4R};$$
$$i_{\rm LOAD-3} = \frac{v_{\rm BUS} + \Delta v_{\rm BUS}}{4R};\ \ i_{\rm LOAD-4} = \frac{v_{\rm BUS} + \Delta v_{\rm BUS}}{4R}$$

with $R_{\rm out1} = R_{\rm out2} = R_{\rm out3} = R_{\rm out4} = R$. The considered load resistors can be achieved by $R = v_{\rm BUS}^2/4P_{\rm nom}$, being $P_{\rm nom}$ the whole dc-bus load power.

The system small-signal linearization consists of representing each time variable as the sum of two terms, its desired steady-state value (dc) and a first order time-varying signal (ac), neglecting higher order variations. The ac signal represents the assumed small variation of the variable in nearness of its steady-state dc value. In order to establish the small-signal dynamic model, the equations (4) are analytically linearized around the dc operating point defined in (5). Accordingly, the linear state equations can be written in a compact matrix form as depicted

$$\dot{\tilde{x}}(t) = \mathbf{A}\tilde{x}(t) + \mathbf{B}\tilde{d}(t) + \mathbf{E}\tilde{v}(t) \tag{6}$$

where $\tilde{x}(t) = [\tilde{i}_d(t), \tilde{i}_q(t), \tilde{v}_{\rm BUS}(t), \Delta\tilde{v}_{\rm BUS}(t)]^T$ is the state vector, $\tilde{d}(t) = [\tilde{d}'_d(t)\ \tilde{d}'_q(t)\ \tilde{d}'_0(t)]^T$ is the control or input vector, and $\tilde{v}(t) = [\tilde{v}_d(t)\ \tilde{v}_q(t)]^T$ is the disturbance vector. The state matrix *A*, the control matrix *B*, the disturbance matrix *E* are defined as

$$A = \left.\frac{\partial f}{\partial x_\sim}\right|_{x=x_0} \quad B = \left.\frac{\partial f}{\partial d_\sim}\right|_{x=x_0} \quad C = \left.\frac{\partial f}{\partial v_\sim}\right|_{x=x_0} \tag{7}$$

where the nonlinear function *f* describes the system as in (4) and x_0 is the selected operating point. The application to (4) of the partial differentiation, as defined in (7), leads to the following expressions:

$$A = \begin{pmatrix} 0 & \omega_0 & -\dfrac{\sqrt{2}V_s}{LV^*_{\rm BUS}} & 0 \\ -\omega_0 & 0 & \dfrac{\omega_0\sqrt{2}I^*_s}{V^*_{\rm BUS}} & 0 \\ \dfrac{6\sqrt{2}V_s}{CV^*_{\rm BUS}} & -\dfrac{6L\omega_0\sqrt{2}I^*_s}{CV^*_{\rm BUS}} & -\dfrac{1}{RC} & 0 \\ 0 & 0 & 0 & -\dfrac{12V_sI^*_s}{CV^{*2}_{\rm BUS}} - \dfrac{1}{RC} \end{pmatrix}$$

$$B = \begin{pmatrix} -\dfrac{V^*_{\rm BUS}}{4L} & 0 & 0 \\ 0 & -\dfrac{V^*_{\rm BUS}}{4L} & 0 \\ \dfrac{3\sqrt{2}I^*_s}{2C} & 0 & 0 \\ 0 & 0 & \dfrac{\alpha\sqrt{2}I^*_s}{C} \end{pmatrix}, E = \begin{pmatrix} \dfrac{1}{L} & 0 \\ 0 & 0 \\ 0 & \dfrac{1}{L} \\ 0 & 0 \end{pmatrix}. \quad (8)$$

Applying the Laplace's transform to the state equations (6), the well-known frequency-domain representation of the converter is obtained as

$$\tilde{X}(s) = (sI - \mathbf{A})^{-1}\mathbf{B}\tilde{D}(s) + (sI - \mathbf{A})^{-1}\mathbf{E}\tilde{V}(s) \quad (9)$$

I denotes the 4×4 identity matrix and $\tilde{X}(s), \tilde{D}(s), \tilde{V}(s)$ are respectively the Laplace' transforms of vectors $\tilde{x}(t), \tilde{d}(t), \tilde{v}(t)$. Substituting (8) into (9) and performing some algebraic manipulations, a compact matrix representation can be written as

$$\begin{bmatrix} \tilde{i}_d(s) \\ \tilde{i}_q(s) \\ \tilde{v}_{\rm BUS}(s) \\ \Delta\tilde{v}_{\rm BUS}(s) \end{bmatrix} = \begin{pmatrix} G_{id11} & G_{id21} & G_{vd11} \\ G_{\Delta vd11} & G_{id12} & G_{id22} \\ G_{vd12} & G_{\Delta vd12} & G_{id13} \\ G_{id23} & G_{vd13} & G_{\Delta vd13} \end{pmatrix} \begin{bmatrix} \tilde{d}'_d(s) \\ \tilde{d}'_q(s) \\ \tilde{d}'_0(s) \end{bmatrix} + \begin{pmatrix} G_{iv11} & G_{iv21} \\ G_{vv11} & G_{\Delta vv11} \\ G_{iv12} & G_{iv22} \\ G_{vv12} & G_{\Delta vv12} \end{pmatrix} \begin{bmatrix} \tilde{v}_d(s) \\ \tilde{v}_q(s) \end{bmatrix}. \quad (10)$$

Result of (10) represents the small-signal model of the 5L T-RECT. It can be noticed that the system is described by 20 transfer functions, relating the five inputs $\{\tilde{d}'_d\ \tilde{d}'_q\ \tilde{d}'_0\ \tilde{v}_d\ \tilde{v}_q\}$ to the four outputs $\{\tilde{i}_d\ \tilde{i}_q\ \tilde{v}_{\rm BUS}\ \Delta\tilde{v}_{\rm BUS}\}$. The used notation is in the form $G_{\rm xyzt}(s)$, where *x* is an output coming from the vector $\tilde{X}(s)$, *y* is an input being an element of either $\tilde{D}(s)$ or $\tilde{V}(s)$, *z* is the rank of the output *x* in the vector $\tilde{X}(s)$ and *t* is the rank of the input *y* in the vector $\tilde{D}(s)$ or $\tilde{V}(s)$. The corresponding equivalent block diagram which is obtained considering the achieved transfer functions is shown in Fig. 3.

The expressions of the transfer functions are summarized in Table I. It can be noticed that some of them are equal to zero and do not participate to the equivalent block diagram shown in Fig. 3.

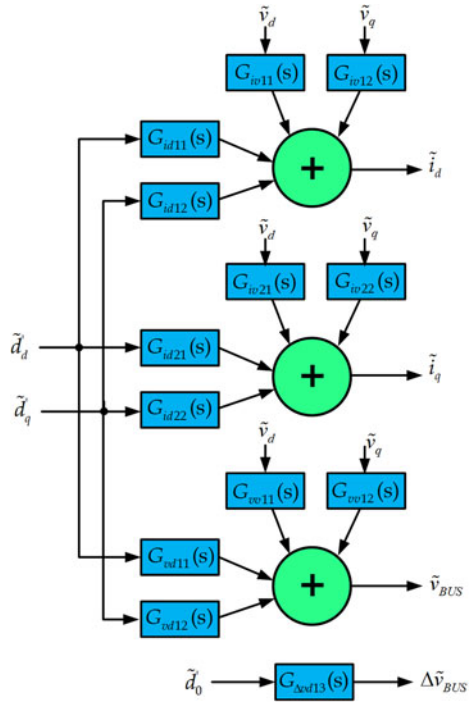

Fig. 3. Block diagram of the converter in small-signal model.

IV. Results

Previously depicted results achieved by the analytical investigation, are compared with the 5L T-RECT average and switching model. Simulations have been performed with reference to a system being composed of a permanent magnet synchronous machine (PMSG) feeding the ac–dc rectifier having the operating specifications as in Table II.

The electric generator mechanical speed is set to 3500 r/min, resulting in a rectifier modulation index around 0.95. In such conditions, the steady-state values of the rms supply voltage, the rms ac line current and the dc-bus output voltage are respectively equal to 250 V, 21 A, and 700 V. Almost unity displacement power factor and phase disposition PWM modulation with sinusoidal third-harmonic injection [34] is considered. Carrier-based PWM used to control 5L T-RECT switches is based on four different carriers, $\rm c_3$, $\rm c_{2A}$, $\rm c_{2B}$, and $\rm c_1$, each one linked to a different power device, S_{x3}, $S_{\rm x2A}$, $S_{\rm x2B}$ and S_{x1}, where *x* stands for A, B, or C phase. Modulation scheme is summarized in Fig. 4 with reference to three-phase sinusoidal modulating signals $m_{\rm A}$, $m_{\rm B}$, and $m_{\rm C}$.

A. Simulation Results

In order to validate the 5L T-RECT small-signal model, a full digital-switching converter description has been developed within the MATLAB/Simulink environment. The obtained model has been analyzed using the provided linear analysis tool. Moreover, in order to better prove the validity of the proposed

TABLE I
5L T-RECT TRANSFER FUNCTIONS

$G_{id11} = \frac{\tilde{i}_d}{\tilde{d}'_d}$	$-\frac{V^*_{\rm BUS}}{4L}\frac{s^2+\beta_{11}s}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{id12} = \frac{\tilde{i}_d}{\tilde{d}'_q}$	$-\frac{V^*_{\rm BUS}\omega_0}{4L}\frac{s+\beta_{11}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{id13} = \frac{\tilde{i}_d}{\tilde{d}'_0}$	0
$G_{id21} = \frac{\tilde{i}_q}{\tilde{d}'_d}$	$\frac{V^*_{\rm BUS}\omega_0}{4L}\frac{\beta_{12}s+\tau}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{id22} = \frac{\tilde{i}_q}{\tilde{d}'_q}$	$-\frac{V^*_{\rm BUS}}{4L}\frac{s^2+\tau s+\beta_{13}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{id23} = \frac{\tilde{i}_q}{\tilde{d}'_0}$	0
$G_{vd11} = \frac{\tilde{v}_{\rm BUS}}{\tilde{d}'_d}$	$\frac{3\sqrt{2}I^*_s}{2C}\frac{s^2+\beta_{14}s}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{vd12} = \frac{\tilde{v}_{\rm BUS}}{\tilde{d}'_q}$	$\frac{3\sqrt{2}I^*_s\omega_0}{2C}\frac{s+\beta_{14}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{vd13} = \frac{\tilde{v}_{\rm BUS}}{\tilde{d}'_0}$	0
$G_{\Delta vd11} = \frac{\Delta\tilde{v}_{\rm BUS}}{\tilde{d}'_d}$	0
$G_{\Delta vd12} = \frac{\Delta\tilde{v}_{\rm BUS}}{\tilde{d}'_q}$	0
$G_{\Delta vd13} = \frac{\Delta\tilde{v}_{\rm BUS}}{\tilde{d}'_0}$	$\frac{\sqrt{2}I^*_s\alpha}{C}\frac{1}{s+\beta_{15}}$
$G_{iv11} = \frac{\tilde{i}_d}{\tilde{v}_d}$	$\frac{1}{L}\frac{s^2+\tau s+\beta_{16}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{iv12} = \frac{\tilde{i}_d}{\tilde{v}_q}$	$\frac{\omega_0}{L}\frac{s+\beta_{11}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{iv21} = \frac{\tilde{i}_q}{\tilde{v}_d}$	$-\frac{\omega_0}{L}\frac{s+\beta_{17}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{iv22} = \frac{\tilde{i}_q}{\tilde{v}_q}$	$\frac{1}{L}\frac{s^2+\tau s+\beta_{13}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{vv11} = \frac{\tilde{v}_{\rm BUS}}{\tilde{v}_d}$	$\frac{6\sqrt{2}V_s}{CLV^*_{\rm BUS}}\frac{s+\beta_{18}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{vv12} = \frac{\tilde{v}_{\rm BUS}}{\tilde{v}_q}$	$-\frac{6\sqrt{2}I^*_s\omega_0}{CV^*_{\rm BUS}}\frac{s+\beta_{14}}{s^3+\tau s^2+(\omega_0^2\beta_{12}+\beta_{13})s+\tau\omega_0^2}$
$G_{\Delta vv11} = \frac{\Delta\tilde{v}_{\rm BUS}}{\tilde{v}_d}$	0
$G_{\Delta vv12} = \frac{\Delta\tilde{v}_{\rm BUS}}{\tilde{v}_q}$	0

where $\tau = \frac{1}{RC}, \beta_{11} = \tau + \frac{12{\rm V}_s I^*_s}{CV^{*2}_{\rm BUS}}, \beta_{12} = 1 + \frac{12{\rm L}I^{*2}_s}{CV^{*2}_{\rm BUS}}, \beta_{13} = \frac{12{\rm V}^2_s}{CLV^{*2}_{\rm BUS}}$,
$\beta_{14} = -\frac{V_s}{LI^*_s}, \beta_{15} = \tau - \frac{6{\rm V}_s I^*_s}{CV^{*2}_{\rm BUS}}, \beta_{16} = \frac{12{\rm L}\omega_0^2 I^{*2}_s}{CV^{*2}_{\rm BUS}}$,
$\beta_{17} = \tau - \frac{12{\rm V}_s I^*_s}{CV^{*2}_{\rm BUS}}, \beta_{18} = \frac{L\omega_0^2 I^*_s}{V_s}$

TABLE II
5L T-RECT AND PMSG MAIN PARAMETERS

Mechanical input power [W]	17 000
PM machine rated speed [r/min]	3500
PM machine rated phase EMF [$V_{\rm rms}$]	250
Rated phase current [$A_{\rm rms}$]	22
PM machine pole-pairs	5
PM machine inductance [μH]	500
Rated dc-bus voltage [V]	700
Switching frequency [kHz]	12
DC-bus capacitors, each one [μF]	152

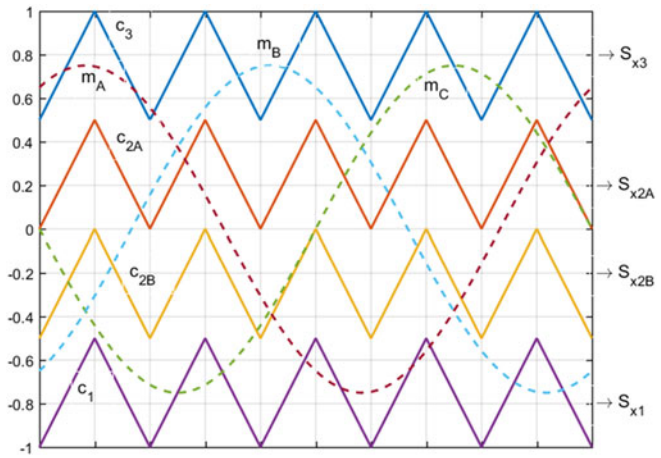

Fig. 4. Modulating scheme for the 5L T-RECT converter.

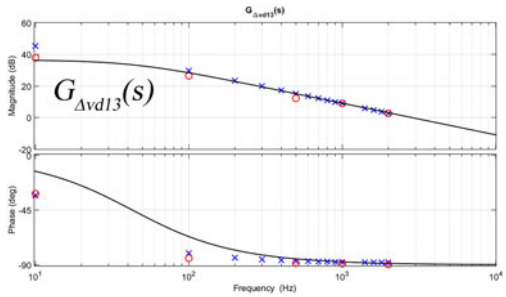

Fig. 5. Bode diagrams related to the transfer function control input $\tilde{d}'_0$ to output $\Delta\tilde{v}_{\rm BUS}$: small signal model (solid trace), average model (blue cross), and linearized switching model (red circle).

small-signal model, the average large-signal model presented in [31] has been also considered in the comparison, by performing a software-based direct linear analysis.

A disturbance signal is added to each steady-state input variable, while the remaining inputs are kept constant. The magnitude of the disturbance signal is selected around 1% of the corresponding static input. This is enough to generate a reasonable oscillation of the outputs around their steady-state values, without affecting the model accuracy.

The Bode diagram between the control inputs $\tilde{d}'_0$ and the output $\Delta\tilde{v}_{\rm BUS}$ is depicted in Fig. 5, where it exhibits a first order system behavior. It can be recognized the good agreement between the proposed linear system analytical representation and the linearized models. Fig. 6 shows the results of the group of transfer functions (TFs) between the disturbance inputs $\tilde{v}_d, \tilde{v}_q$ and the outputs $\tilde{i}_d$, $\tilde{i}_q$, $\tilde{v}_{\rm BUS}$ and $\Delta\tilde{v}_{\rm BUS}$. The TFs in this group have in common to be third order systems due to inductance and capacitors degeneration as highlighted in Fig. 2. It can be noticed that the three completely different analytical descriptions exhibit a good matching for all the nonzero transfer functions.

B. Experimental Results

Furthermore, experimental tests have been performed, where possible, to finally support the presented mathematical system

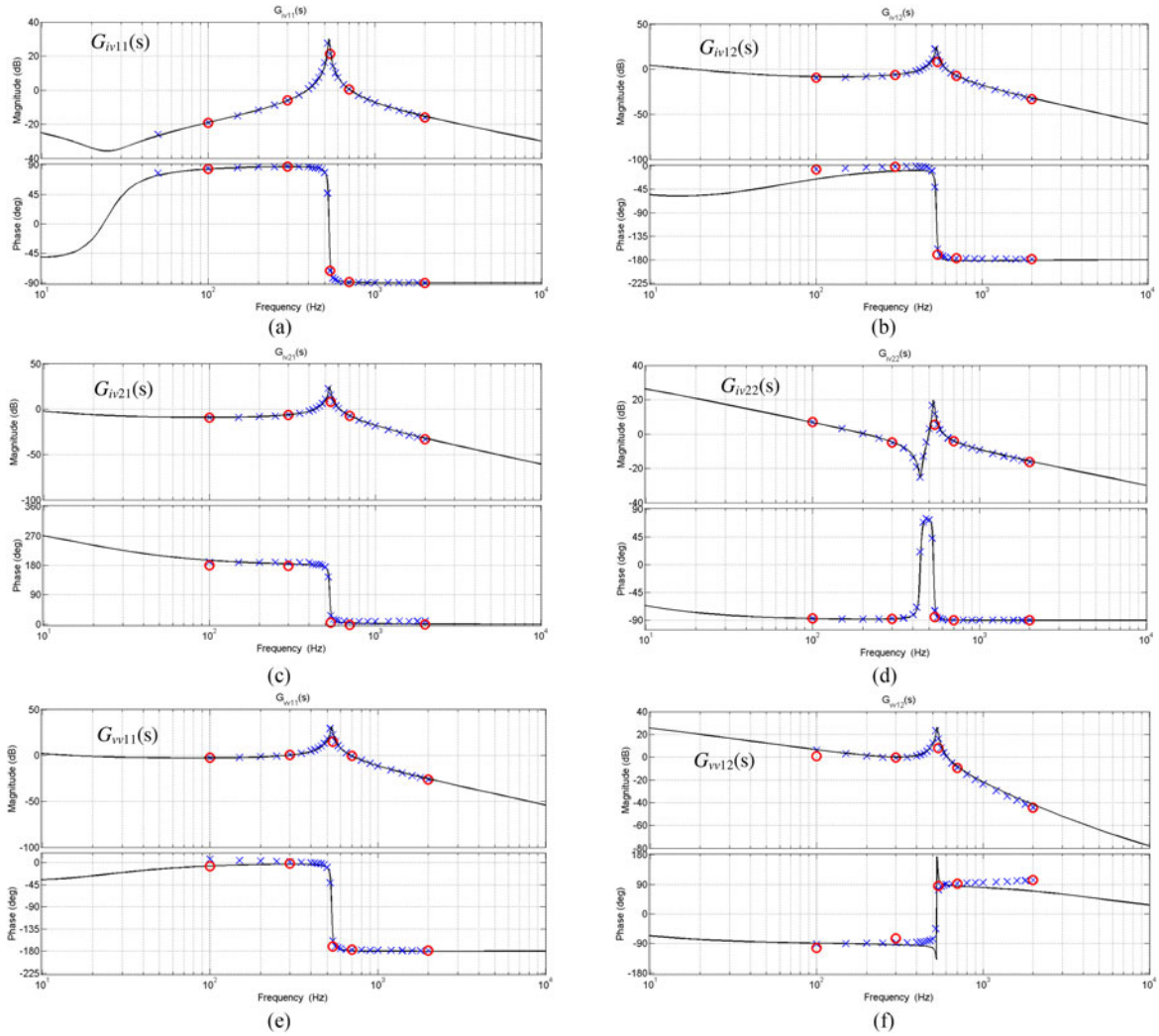

Fig. 6. Bode diagrams related to the transfer functions inputs $\tilde{v}_d$, $\tilde{v}_q$ to outputs $\tilde{i}_d$, $\tilde{i}_q$, and $\tilde{v}_{\mathrm{BUS}}$: small signal model (solid trace), average model (blue cross), and linearized switching model (red circle). (a) $G_{iv11}(\mathrm{s})$, (b) $G_{iv12}(\mathrm{s})$, (c) $G_{iv21}(\mathrm{s})$, (d) $G_{iv22}(\mathrm{s})$, (e) $G_{vv11}(\mathrm{s})$, and (f) $G_{vv12}(\mathrm{s})$.

description. With reference to the experimental tests performed to carry out the system TFs, different methods have been proposed so far to be implemented for the experimental verification [35], [36]. Due to the very high complexity of the system and the measurements to be done, the following procedure was used. In order to stimulate the system, the sinusoidal perturbation has been generated internally to the digital signal processor used to control the system. Each perturbation was characterized by a proper amplitude, frequency, and zero reference phase. After that, the output measure to be considered for each TF has been analyzed by a Yokogawa WT3000 precision analyzer setup in harmonic mode. In this manner, the related output harmonic can be obtained with respect to magnitude and phase. However, phase synchronization is a hard issue when TFs have to be carried out. In order to overcome this issue, the input stimulus and the output measurement have been synchronized by a dedicated trigger signal which was internally generated by the digital signal processor and acquired by the WT3000 as zero-phase reference. Fig. 7 depicts the block scheme of the 5L T-RECT and its related control structure.

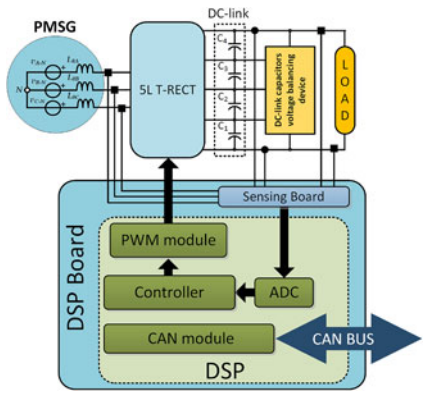

Fig. 7. Block scheme of the 5L T-RECT and related controller.

Finally, Fig. 8 shows the simulation results and the experimental results of the transfer functions group that relates the control inputs $\tilde{d}'_d$ and $\tilde{d}'_q$ to the outputs $\tilde{i}_d$, $\tilde{i}_q$, and $\tilde{v}_{\mathrm{BUS}}$. As the previously shown group, reported TFs are still related to

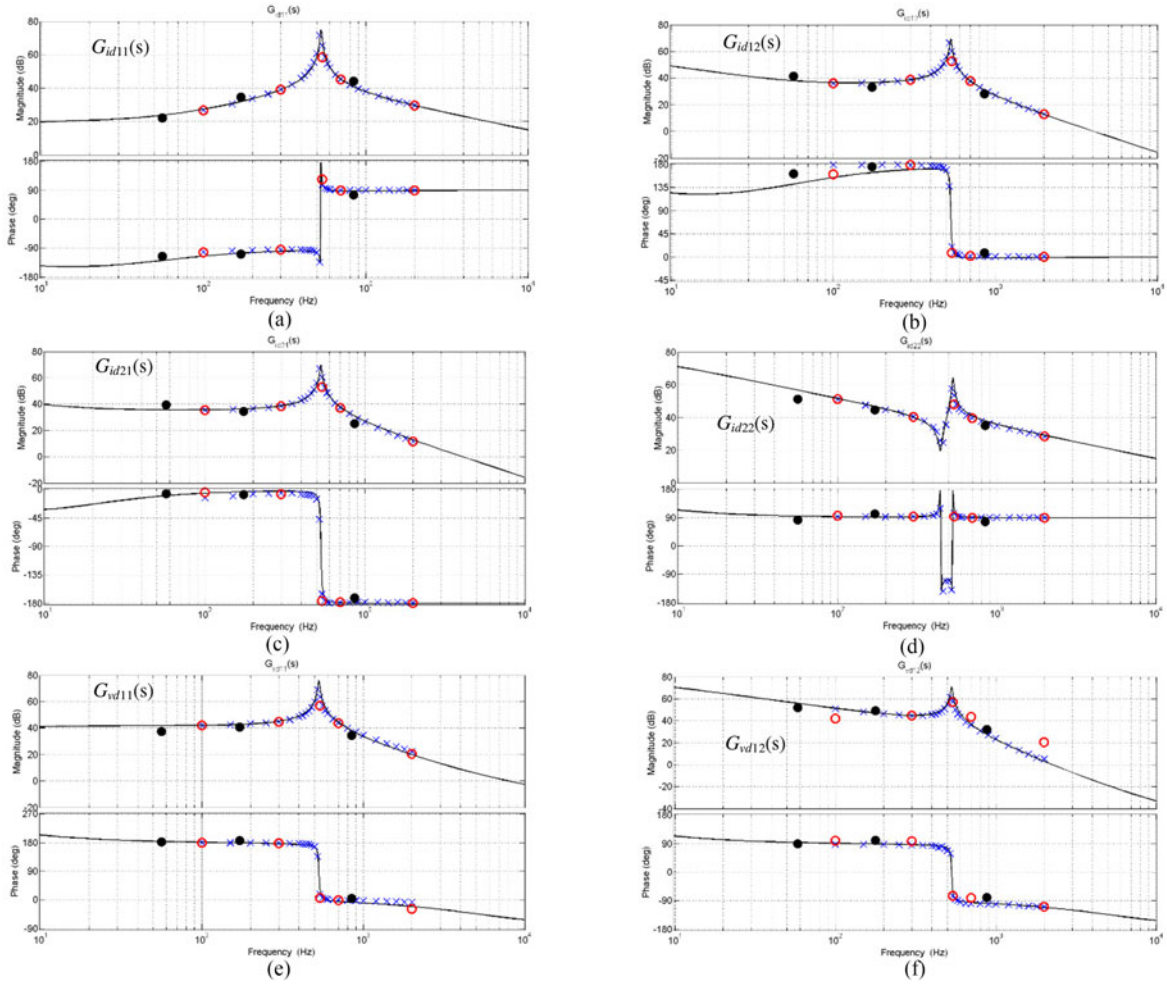

Fig. 8. Bode diagrams related to the transfer functions control inputs $\tilde{d}'_d$ and $\tilde{d}'_q$ to outputs $\tilde{i}_d$, $\tilde{i}_q$, and $\tilde{v}_{\mathrm{BUS}}$: small signal model (solid trace), average model (blue cross), linearized switching model (red circle), and experimental results (black dot). (a) $G_{id11}(\mathrm{s})$, (b) $G_{id12}(\mathrm{s})$, (c) $G_{id21}(\mathrm{s})$, (d) $G_{id22}(\mathrm{s})$, (e) $G_{vd11}(\mathrm{s})$, and (f) $G_{vd12}(\mathrm{s})$.

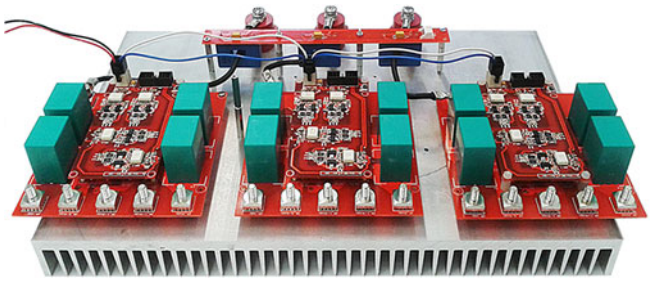

Fig. 9. 5L T-RECT prototype.

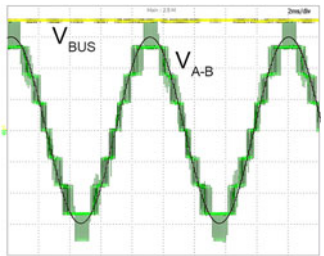

Fig. 10. Experimental line-to-line voltage with superimposed line-to-line voltage from the average model.

third-order systems having the same pole locations but different zeros. Solid line is related to the small-signal model, whereas, cross, circle, and black dot are the results achieved respectively from the large-signal average model, the linearized switching model, and the experimental results. The experimental validation, in actual operating conditions, has been performed on the 5L T-RECT inverter prototype shown in Fig. 9.

The 5L T-RECT control unit is based on the TMS320F28335 digital signal controller from Texas Instruments having a dedicated scheduler operating at 12 kHz and synchronously with the rectifier switching frequency. Fig. 10 shows the rectifier input line-to-line voltage $(V_{\mathrm{A-B}})$ with superimposed the line-to-line voltage achieved from the average model. It can be noticed a good matching between the experimental result and the analytical equations simulation model.

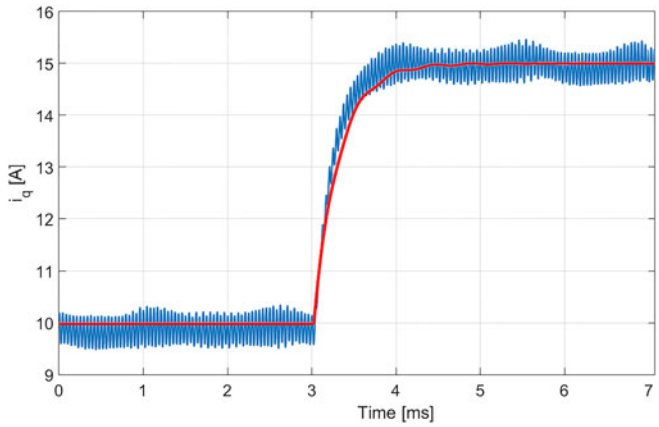

Fig. 11. System dynamic response to a step change of the q-axis current: experimental result (blue trace), small signal model (red trace).

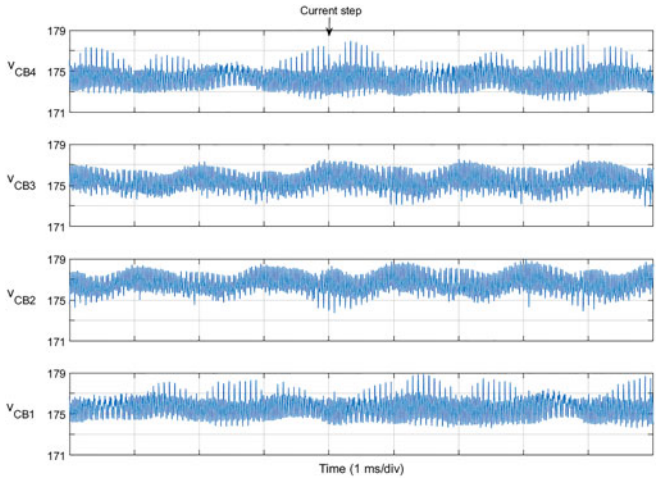

Fig. 12. DC-link capacitors voltage under q-axis current step variation.

Finally, the q-axis current step is performed to further verify the depicted small-signal model. This test was performed in order to provide information on the accuracy of the illustrated analytical representation; the more the step response obtained from the small-signal model is similar to the step response of the real setup, the more the achieved small-signal model is consistent.

The experimental test has been carried out according to the following procedure. The same control algorithm is used in both the average model, the small-signal model and in the actual system. In the performed test, the current regulation has been obtained using the well-known PI-based field oriented control strategy and feeding the 5L T-RECT with a permanent magnet generator. The gains of the proportional-integral controllers have been tuned using the previously obtained and described transfer functions to provide 750 Hz bandwidth on both d and q axes. Moreover, the control parameters have been implemented as they have been calculated, without any adjustment passing from the simulation model to the experimental setup. In this case, the result from the transfer function evaluation is superimposed to the acquired q-axis current waveform which is provided by the control board digital-to-analog converter. It can be noticed how the two behaviors are very similar, as it is depicted in Fig. 11, thus proving the effectiveness on the proposed converter mathematical representation.

In order to demonstrate that the balancing circuit dynamic response is much faster that the control bandwidth, a specific test has been performed. In this case, the dc link is controlled by the external active load, whereas the 5L T-RECT converter is fully regulated through current control, which represents the highest control bandwidth available in such a system (i.e., 750 Hz). In fact, if the uncontrolled balancing converter would exhibit a slower time constant with respect to the current controller, an unbalance transient should be recognized across the dc-link capacitor voltage distribution. As illustrated in Fig. 12, at the highlighted time instant, the current reference is increased from 80% of the rated current to full load. To better depict this effect, data have been saved in a .txt file by the scope at a high-sampling rate (10 MS/s) and plotted offline. It can be seen that the current perturbation does not affect the voltage distribution among the dc-link capacitor. Moreover, it can be also recognized, that the balancing circuit performs with a voltage regulation accuracy below 1% with no feedback and additional sensors.

V. Conclusion

The small-signal model for the 5L T-RECT power converter has been derived and analyzed. The proposed model has been presented in both time-domain and frequency-domain, and the corresponding transfer functions have been evaluated. Results of the small-signal model, established for such a complex structure, closely resemble the ones obtained from a software-based linear analysis applied to the average and switching models. For better utilization of the dc-link voltage, the proposed analysis can also be used to predict, and then to overcome, the well-known issues related to the midpoint voltage unbalancing. Moreover, illustrated transfer functions are at the basis of control loop design, avoiding any trial-and-error tuning procedure.

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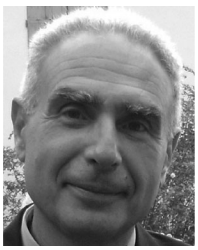

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